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# FOD073L

## LVTT/LVCMOS Compatible Low Input Current High Gain Split Darlington Optocoupler

### Features

- Low power consumption
- Low input current: 0.5mA
- Dual channel 8-pin SOIC package
- High CTR: 400% minimum
- High CMR: 10kV/μs
- Guaranteed performance over temperature 0°C to 70°C
- U.L. recognized (File # E90700)
- LVTT/LVCMOS Compatible output

### Applications

- Digital logic ground isolation – LVTT/LVCMOS
- Telephone ring detector
- EIA-RS-232C line receiver
- High common mode noise line receiver
- μP bus isolation
- Current loop receiver

### Description

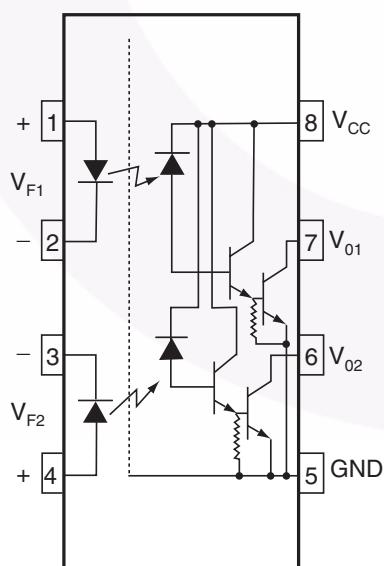
The FOD073L optocoupler consists of an AlGaAs LED optically coupled to a high gain split darlington photodetector. This device is specified to operate at a 3.3V supply voltage.

An integrated emitter – base resistor provides superior stability over temperature.

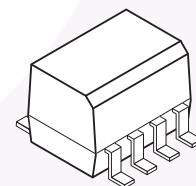
The combination of a very low input current of 0.5mA and a high current transfer ratio of 2000% (typical) makes this device particularly useful for input interface to MOS, CMOS, LSTTL and EIA RS232C, while output compatibility is ensured to LVCMOS as well as high fan-out LVTT requirements.

An internal noise shield provides exceptional common mode rejection of 10kV/μs.

### Schematic



### Package Outline



### Truth Table

LED	V <sub>O</sub>
ON	LOW
OFF	HIGH

**Absolute Maximum Ratings** (No derating required up to 85°C)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Value	Units	
$T_{STG}$	Storage Temperature	-40 to +125	°C	
$T_{OPR}$	Operating Temperature	-40 to +85	°C	
$T_{SOL}$	Lead Solder Temperature (Wave solder only. See reflow profile for surface mount devices)	260 for 10 sec	°C	
<b>EMITTER</b>				
$I_F$ (avg)	DC/Average Forward Input Current	Each Channel	20	mA
$I_F$ (pk)	Peak Forward Input Current (50% duty cycle, 1ms P.W.)	Each Channel	40	mA
$I_F$ (trans)	Peak Transient Input Current ( $\leq 1\mu s$ P.W., 300 pps)	Each Channel	1.0	A
$V_R$	Reverse Input Voltage	Each Channel	5	V
$P_D$	Input Power Dissipation	Each Channel	35	mW
<b>DETECTOR</b>				
$I_O$ (avg)	Average Output Current	Each Channel	60	mA
$V_{EB}$	Emitter-Base Reverse Voltage (FOD070L, FOD270L)	Each Channel	0.5	V
$V_{CC}, V_O$	Supply Voltage, Output Voltage	Each Channel	-0.5 to 7	V
$P_D$	Output power dissipation	Each Channel	100	mW

**Electrical Characteristics** ( $T_A = 0$  to  $70^\circ\text{C}$  unless otherwise specified)**Individual Component Characteristics**

Symbol	Parameter	Test Conditions	Min.	Typ.*	Max.	Unit
<b>EMITTER</b>						
$V_F$	Input Forward Voltage	$T_A = 25^\circ\text{C}$ $I_F = 1.6\text{mA}$ (Each Channel)		1.35	1.7	V
$BV_R$	Input Reverse Breakdown Voltage	$T_A = 25^\circ\text{C}$ , $I_R = 10\mu\text{A}$ (Each Channel)	5.0			V
<b>DETECTOR</b>						
$I_{OH}$	Logic High Output Current	$I_F = 0\text{ mA}$ , $V_O = V_{CC} = 3.3\text{V}$ (Each Channel)		0.05	25	$\mu\text{A}$
$I_{CCL}$	Logic Low Supply Current	$I_{F1} = I_{F2} = 1.6\text{mA}$ , $V_{O1} = V_{O2} = \text{Open}$ , $V_{CC} = 3.3\text{V}$		0.8	3	mA
$I_{CCH}$	Logic High Supply Current	$I_{F1} = I_{F2} = 0\text{mA}$ , $V_{O1} = V_{O2} = \text{Open}$ , $V_{CC} = 3.3\text{V}$		0.01	2	$\mu\text{A}$

**Transfer Characteristics**

Symbol	Parameter	Test Conditions	Min.	Typ.*	Max.	Unit
CTR	COUPLED Current Transfer Ratio (Note 1)	$I_F = 0.5\text{mA}$ , $V_O = 0.4\text{V}$ , $V_{CC} = 3.3\text{V}$	400		7000	%
$V_{OL}$	Logic Low Output Voltage	$I_F = 1.6\text{mA}$ , $I_O = 8\text{mA}$ , $V_{CC} = 3.3\text{V}$ $I_F = 5\text{mA}$ , $I_O = 15\text{mA}$ , $V_{CC} = 3.3\text{V}$		0.07	0.3	V
				0.07	0.4	

**Switching Characteristics** ( $V_{CC} = 3.3\text{ V}$ )

Symbol	Parameter	Test Conditions	Min.	Typ.*	Max.	Unit
$T_{PHL}$	Propagation Delay Time to Logic LOW	$R_L = 4.7\text{k}\Omega$ , $I_F = 0.5\text{mA}$ (Fig. 9)		5	30	$\mu\text{s}$
$T_{PLH}$	Propagation Delay Time to Logic HIGH	$R_L = 4.7\text{k}\Omega$ , $I_F = 0.5\text{mA}$ (Fig. 9)		25	90	$\mu\text{s}$
$ ICM_H $	Common Mode Transient Immunity at Logic HIGH	$I_F = 0\text{ mA}$ , $ V_{CMI}  = 10\text{ V}_{\text{P-P}}$ , $T_A = 25^\circ\text{C}$ , $R_L = 2.2\text{k}\Omega$ (Note 2) (Fig. 10)	1,000	10,000		$\text{V}/\mu\text{s}$
$ ICM_L $	Common Mode Transient Immunity at Logic LOW	$I_F = 1.6\text{mA}$ , $ V_{CMI}  = 10\text{ V}_{\text{P-P}}$ , $R_L = 2.2\text{k}\Omega$ , $T_A = 25^\circ\text{C}$ (Note 2) (Fig. 10)	1,000	10,000		$\text{V}/\mu\text{s}$

\*All typicals at  $T_A = 25^\circ\text{C}$

**Electrical Characteristics** (Continued) ( $T_A = 0$  to  $70^\circ\text{C}$  unless otherwise specified)**Isolation Characteristics**

Symbol	Characteristics	Test Conditions	Min.	Typ.*	Max.	Unit
$I_{I-O}$	Input-Output Insulation Leakage Current	Relative humidity = 45%, $T_A = 25^\circ\text{C}$ , $t = 5$ s, $V_{I-O} = 3000$ VDC (Note 3)			1.0	$\mu\text{A}$
$V_{ISO}$	Withstand Insulation Test Voltage	$R_H \leq 50\%$ , $T_A = 25^\circ\text{C}$ , $I_{I-O} \leq 2\mu\text{A}$ , $t = 1$ min. (Note 3)	2500			$V_{\text{RMS}}$
$R_{I-O}$	Resistance (Input to Output)	$V_{I-O} = 500$ VDC (Note 3)		$10^{12}$		$\Omega$
$C_{I-O}$	Capacitance (Input to Output)	$f = 1$ MHz (Notes 3, 4)		0.7		$\text{pF}$
$I_{I-I}$	Input-Input Insulation Leakage Current	$RH \leq 45\%$ , $V_{I-I} = 500$ VDC (Note 5)	0.005			$\mu\text{A}$
$R_{I-I}$	Input-Input Resistance	$V_{I-I} = 500$ VDC (Note 5)		$10^{11}$		$\Omega$
$C_{I-I}$	Input-Input Capacitance	$f = 1$ MHz (Note 5)		0.03		$\text{pF}$

\*All typicals at  $T_A = 25^\circ\text{C}$

**Notes:**

1. Current Transfer Ratio is defined as a ratio of output collector current,  $I_O$ , to the forward LED input current,  $I_F$ , times 100%.
2. Common mode transient immunity in logic high level is the maximum tolerable (positive)  $dV_{CM}/dt$  on the leading edge of the common mode pulse signal,  $V_{CM}$ , to assure that the output will remain in a logic high state (i.e.,  $V_O > 2.0$  V). Common mode transient immunity in logic low level is the maximum tolerable (negative)  $dV_{CM}/dt$  on the trailing edge of the common mode pulse signal,  $V_{CM}$ , to assure that the output will remain in a logic low state (i.e.,  $V_O < 0.8$  V).
3. Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.
4.  $C_{I-O}$  is measured by shorting pins 1 and 2 or pins 3 and 4 together and pins 5 through 8 shorted together.
5. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.

## Typical Performance Curves

Fig. 1 Input Forward Current vs Forward Voltage

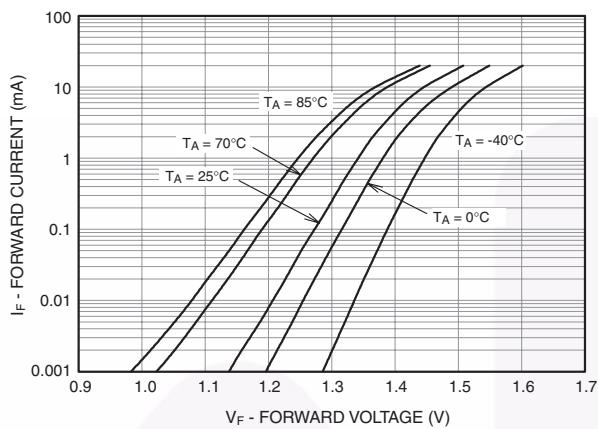


Fig. 2 Current Transfer Ratio vs. Input Forward Current

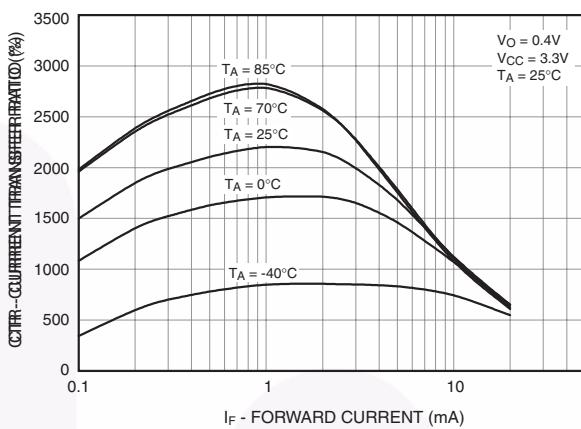


Fig. 3 DC Transfer Characteristics

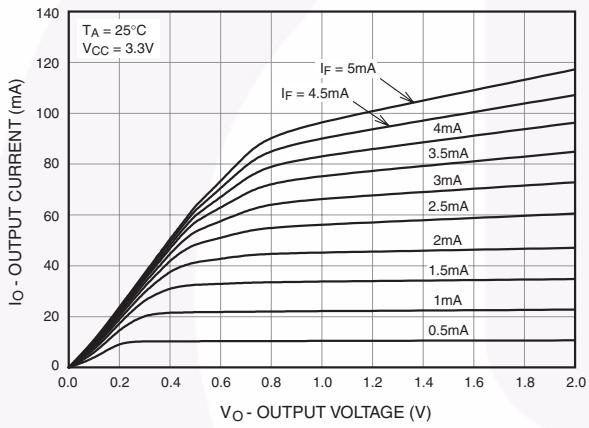


Fig. 4 Supply Current vs Input Forward Current

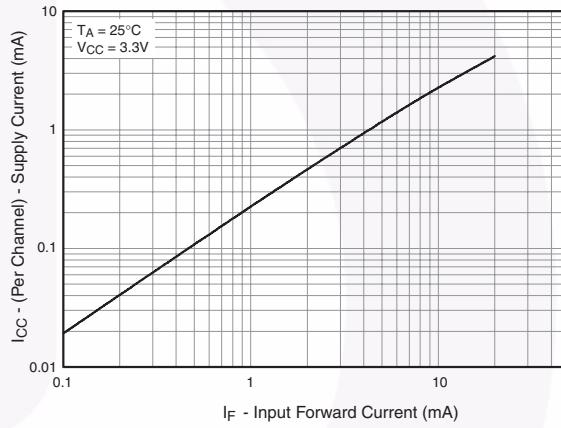


Fig. 5 Output Current vs Input Forward Current

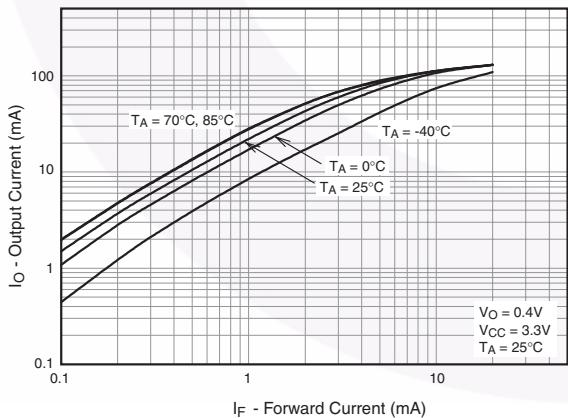
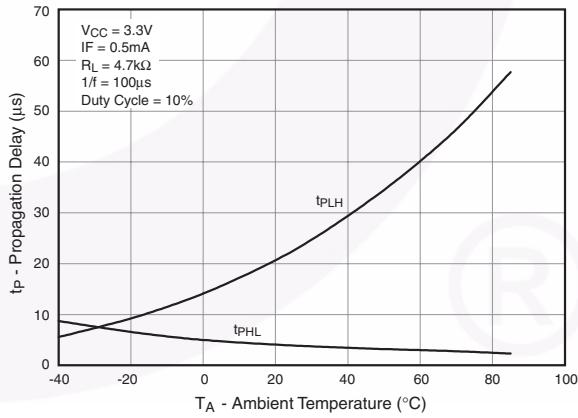


Fig. 6 Propagation Delay vs. Ambient Temperature



## Typical Performance Curves (Continued)

Fig. 7 Propagation Delay To Logic Low vs Pulse Period

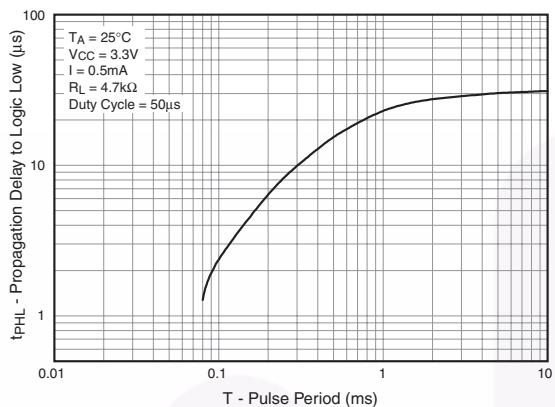
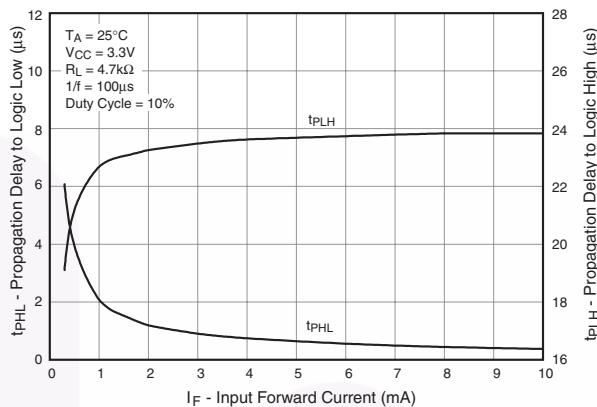


Fig. 8 Propagation Delay vs. Input Forward Current



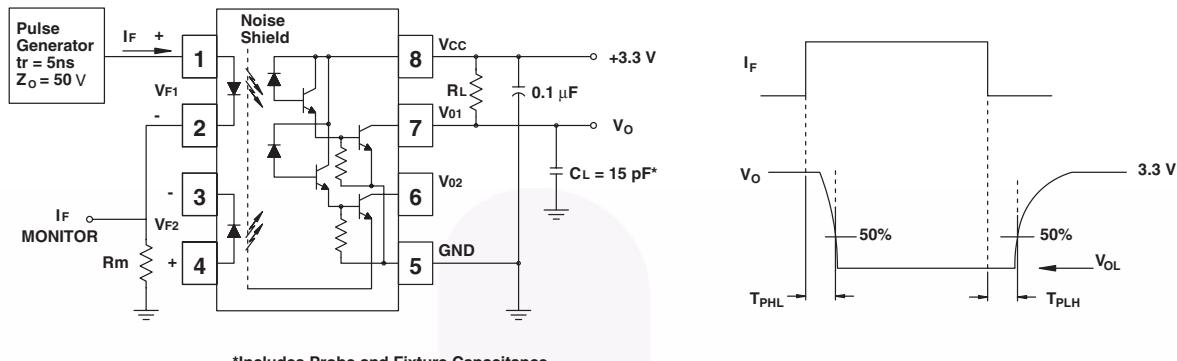


Fig. 9 Switching Time Test Circuit

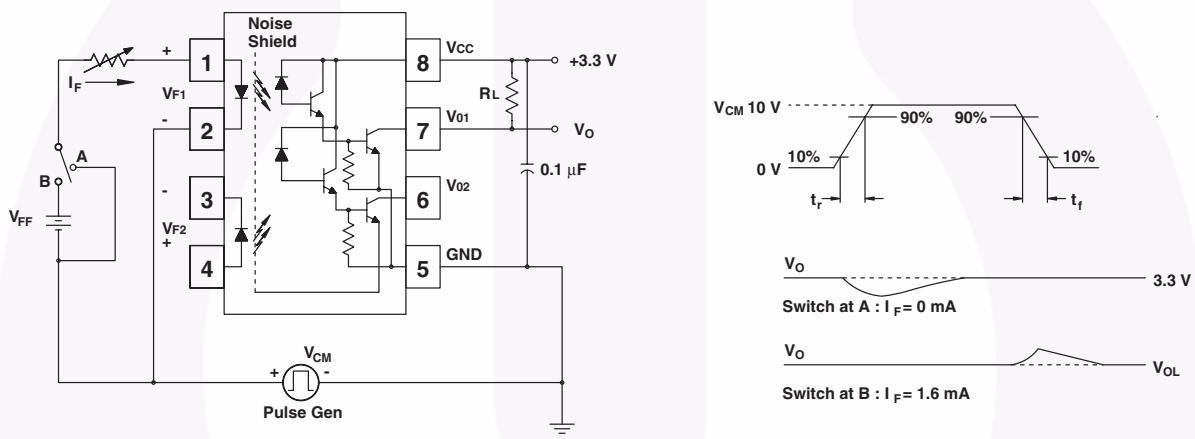
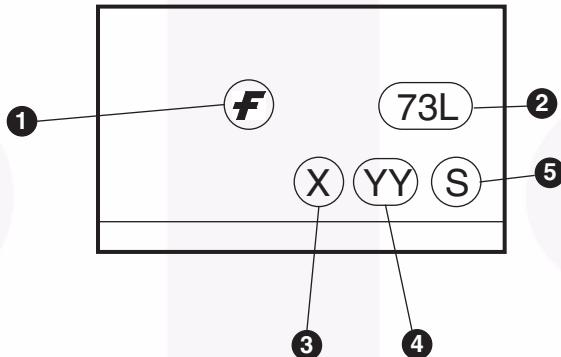


Fig. 10 Common Mode Immunity Test Circuit

## Ordering Information

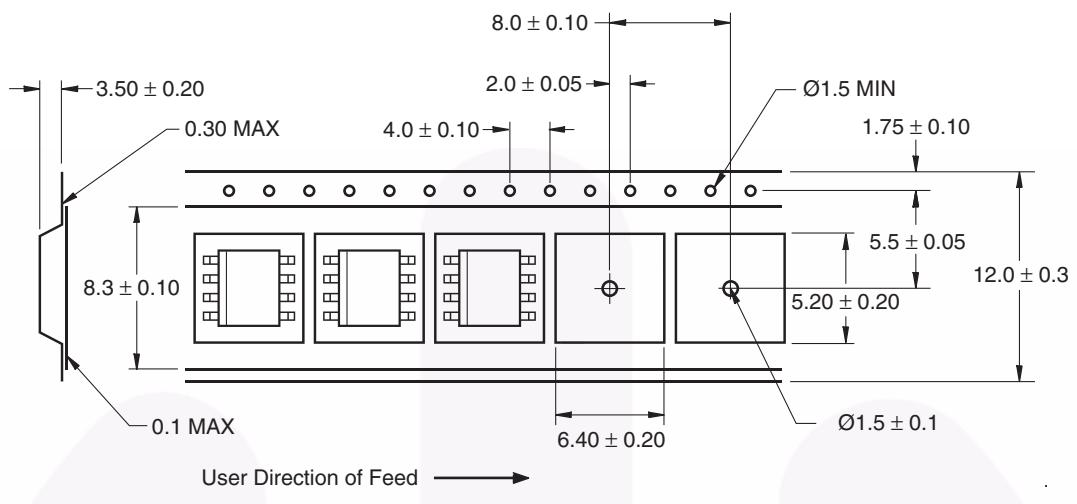
Option	Order Entry Identifier	Description
No Suffix	FOD073L	Shipped in tubes (50 units per tube)
R2	FOD073LR2	Tape and reel (2,500 units per reel)

## Marking Information

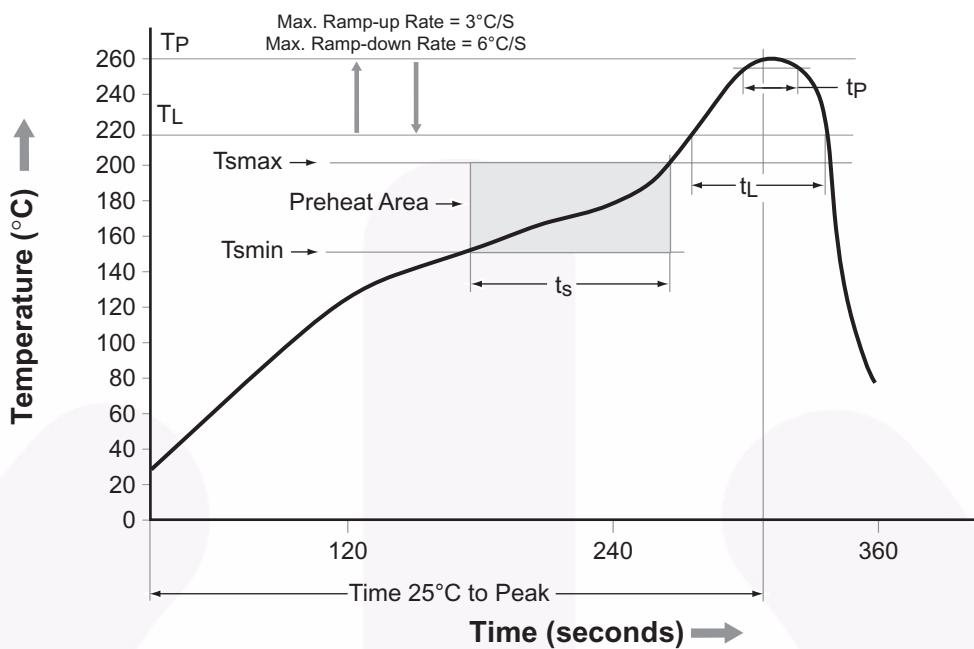


Definitions	
1	Fairchild logo
2	Device number
3	One digit year code, e.g., '3'
4	Two digit work week ranging from '01' to '53'
5	Assembly package code

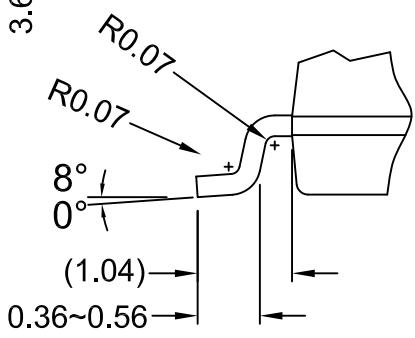
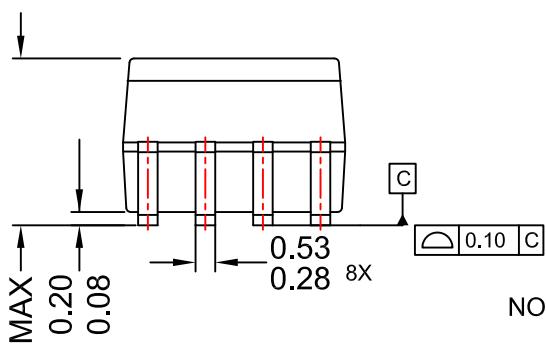
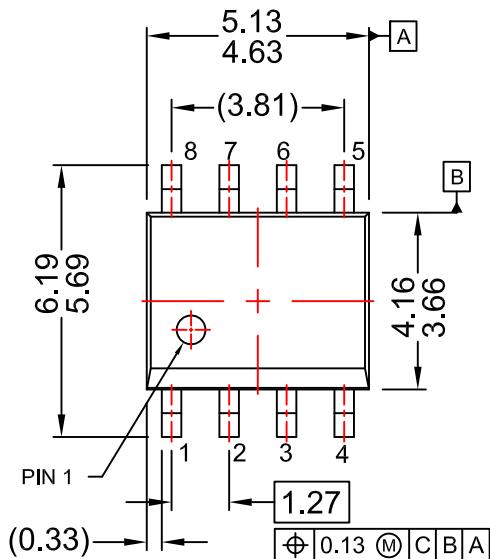
## Carrier Tape Specifications



## Reflow Profile

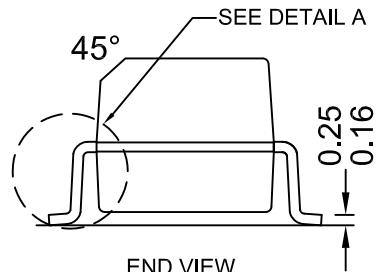


Profile Feature	Pb-Free Assembly Profile
Temperature Min. (Tsmin)	150°C
Temperature Max. (Tsmax)	200°C
Time (t <sub>S</sub> ) from (Tsmin to Tsmax)	60–120 seconds
Ramp-up Rate (t <sub>L</sub> to t <sub>P</sub> )	3°C/second max.
Liquidous Temperature (T <sub>L</sub> )	217°C
Time (t <sub>L</sub> ) Maintained Above (T <sub>L</sub> )	60–150 seconds
Peak Body Package Temperature	260°C +0°C / -5°C
Time (t <sub>P</sub> ) within 5°C of 260°C	30 seconds
Ramp-down Rate (T <sub>P</sub> to T <sub>L</sub> )	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.



DETAIL A

## LAND PATTERN RECOMMENDATION



## NOTES:

- A) NO STANDARD APPLIES TO THIS PACKAGE
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M.
- E) DRAWING FILENAME: MKT-M08Erev5

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