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FPF1205 / FPF1206 IntelliMAX™ Advanced Load Switch

Features

- 1.2 V to 4.0 V Input Voltage Operating Range
- Typical R_{ON} : 75 m Ω at $V_{IN}=3.3$ V
110 m Ω at $V_{IN}=1.8$ V
240 m Ω at $V_{IN}=1.2$ V
- Slew Rate Control with t_R : 110 μ s
- Output Discharge Function on FPF1206
- Low <1.5 μ A Quiescent Current
- Extra Low <100 nA Off Supply Current
- ESD Protected: Above 7000 V HBM, 2000 V CDM
- GPIO/CMOS-Compatible Enable Circuitry
- 4-Bump WLCSP, 0.76 mm x 0.76 mm, 0.4 mm Pitch

Applications

- Mobile Devices and Smart Phones
- Portable Media Devices
- Ultra-Portable / Mobile Computing
- Advanced Notebook, UMPC, MID
- Portable Medical Devices
- GPS and Navigation Equipment

Description

The FPF1205/06 is an ultra-small IntelliMAX™ load switch with integrated P-channel switch and analog control features. Internal slew-rate control prevents inrush current and the resulting excessive voltage drop on power rail. The input voltage range operates from 1.2 V to 4.0 V to provide power-disconnect capability for post-regulated power rails in portable and consumer products. The low shut-off current of 1 μ A (maximum) allows power designs to meet standby and off-power drain specifications.

The FPF1205/06 is controlled by an active-HIGH logic input (ON pin) compatible with standard CMOS GPIO circuitry found on Field Programmable Gate Array (FPGA) and embedded processors. The FPF1205/06 is available in a 0.76 mm x 0.76 mm 4-bump Wafer-Level Chip-Scale Package (WLCSP).

Ordering Information

Part Number	Top Marking	Switch (Typical) at 3.3 V_{IN}	Output Discharge	ON Pin Activity	t_R	Package
FPF1205UCX	QJ	75 m Ω	NA	Active HIGH	110 μ s	4-Ball WLCSP, 0.76 mm x 0.76 mm, 0.4 mm Pitch
FPF1206UCX	QK	75 m Ω	6 5 Ω	Active HIGH	110 μ s	

Application Diagram

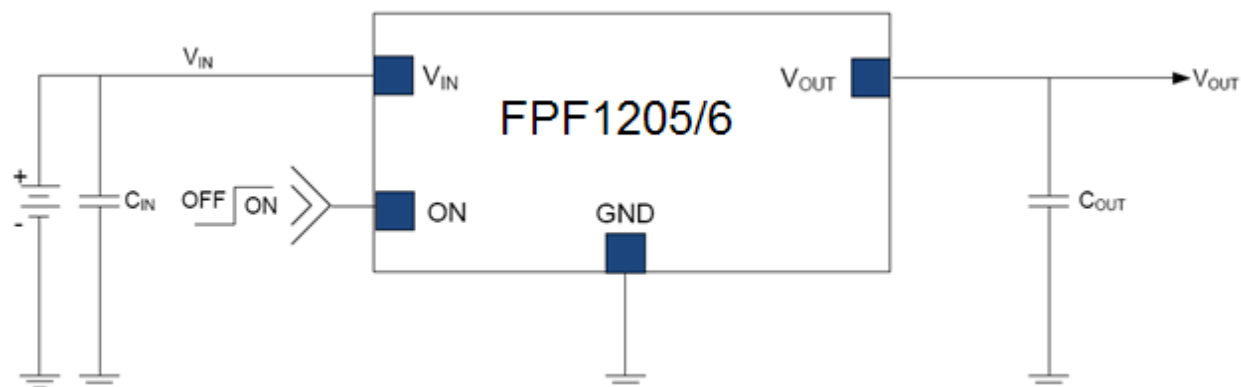


Figure 1. Typical Application

Notes:

1. $C_{IN}=1\ \mu\text{F}$, X5R, 0603 (for example, Murata GRM185R60J105KE26).
2. $C_{OUT}=0.1\ \mu\text{F}$, X5R, 0805 (for example, Murata GRM216R61A105KA01).

Functional Block Diagram

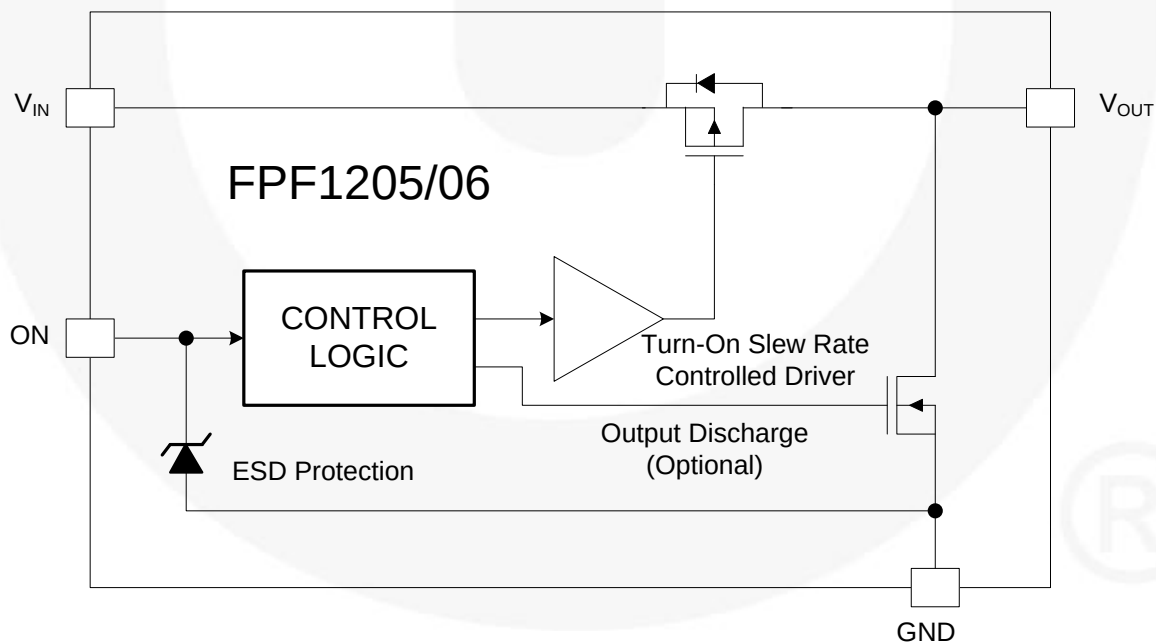


Figure 2. Functional Block Diagram (Output Discharge for FPF1206 Only)

Pin Configurations

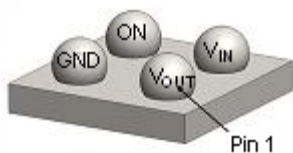


Figure 3. WLCSP Bumps Facing Up (Top View)

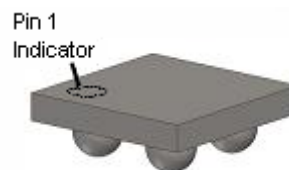


Figure 4. WLCSP Bumps Facing Down (Bottom View)

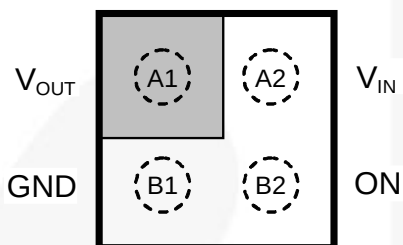


Figure 5. Pin Assignments (Top View)

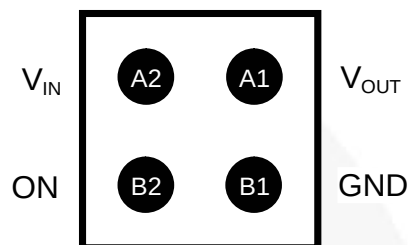


Figure 6. Pin Assignments (Bottom View)

Pin Definitions

Pin #	Name	Description
A1	V _{OUT}	Switch Output
A2	V _{IN}	Supply Input, Input to the power switch
B1	GND	Ground
B2	ON	ON/OFF control, active HIGH

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN}	V_{IN} , V_{OUT} , V_{ON} to GND		-0.3	4.2	V
I_{SW}	Maximum Continuous Switch Current			1.2	A
P_D	Power Dissipation at $T_A=25^{\circ}\text{C}$			1.0	W
T_{STG}	Storage Junction Temperature		-65	+150	$^{\circ}\text{C}$
T_A	Operating Temperature Range		-40	+85	$^{\circ}\text{C}$
Θ_{JA}	Thermal Resistance, Junction-to-Ambient	1S2P with One Thermal Via		110	$^{\circ}\text{C/W}$
		1S2P without Thermal Via		95	
ESD	Electrostatic Discharge Capability ^(3,4)	Human Body Model, JESD22-A114	7		kV
		Charged Device Model, JESD22-C101	2		

Notes:

3. Measured using 2S2P JEDEC std. PCB.
4. Measured using 2S2P JEDEC PCB COLD PLATE Method.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Supply Voltage	1.2	4.0	V
T_A	Ambient Operating Temperature	-40	+85	$^{\circ}\text{C}$

Electrical Characteristics

Unless otherwise noted, $V_{IN}=1.2$ to 4.0 V and $T_A=-40$ to $+85^\circ\text{C}$. Typical values are at $V_{IN}=3.3$ V and $T_A=25^\circ\text{C}$.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Basic Operation						
V_{IN}	Supply Voltage		1.2		4.0	V
$I_{Q(OFF)}$	Off Supply Current	$V_{ON}=GND$, $V_{OUT}=Open$, $V_{IN}=4$ V			100	nA
I_{SD}	Shutdown Current	$V_{ON}=GND$, $V_{OUT}=GND$			1	μA
I_Q	Quiescent Current	$I_{OUT}=0$ mA			1.5	μA
R_{ON}	On Resistance	$V_{IN}=3.3$ V, $I_{OUT}=200$ mA, $T_A=25^\circ\text{C}$		75	100	m Ω
		$V_{IN}=1.8$ V, $I_{OUT}=200$ mA, $T_A=25^\circ\text{C}$		110	150	
		$V_{IN}=1.2$ V, $I_{OUT}=200$ mA, $T_A=25^\circ\text{C}$		240	300	
		$V_{IN}=1.8$ V, $I_{OUT}=200$ mA, $T_A=85^\circ\text{C}$		160	200	
R_{PD}	Output Discharge $R_{PULL\ DOWN}$	$V_{IN}=3.3$ V, $V_{ON}=0$ V, $I_{FORCE}=20$ mA, $T_A=25^\circ\text{C}$, FPF1206		65	110	Ω
V_{IH}	On Input Logic HIGH Voltage	$V_{IN} < 1.5$ V	0.9			V
		$V_{IN}=1.5$ V to 4.0 V	1.1			
V_{IL}	On Input Logic LOW Voltage	$V_{IN}=1.2$ V to 4.0 V			0.75	V
I_{ON}	On Input Leakage	$V_{ON}=V_{IN}$ or GND			1	μA
Dynamic Characteristics⁽⁵⁾						
t_{DON}	Turn-On Delay ⁽⁶⁾	$V_{IN}=3.3$ V, $R_L=10$ Ω , $C_L=0.1$ μF , $T_A=25^\circ\text{C}$		110		μs
t_R	V_{OUT} Rise Time ⁽⁶⁾			110		
t_{ON}	Turn-On Time ⁽⁶⁾			220		
t_{DOFF}	Turn-Off Delay ⁽⁶⁾	$V_{IN}=3.3$ V, $R_L=10$ Ω , $C_L=0.1$ μF , $T_A=25^\circ\text{C}$, FPF1205		7		μs
t_F	V_{OUT} Fall Time ⁽⁶⁾			2		
t_{OFF}	Turn-Off Time ⁽⁶⁾			9		
t_{DOFF}	Turn-Off Delay	$V_{IN}=3.3$ V, $R_L=500$ Ω , $C_L=0.1$ μF , $T_A=25^\circ\text{C}$, FPF1205		10		μs
t_F	V_{OUT} Fall Time			95		
t_{OFF}	Turn-Off Time ⁽⁶⁾			105		
t_{DOFF}	Turn-Off Delay	$V_{IN}=3.3$ V, $R_L=500$ Ω , $C_L=0.1$ μF , $T_A=25^\circ\text{C}$, FPF1206 ⁽⁷⁾		7.0		μs
t_F	V_{OUT} Fall Time			10.5		
t_{OFF}	Turn-Off Time ⁽⁶⁾			17.5		

Notes:

- These parameters are guaranteed by design and characterization; not production tested.
- $t_{DON}/t_{DOFF}/t_R/t_F$ are defined in Figure 24.
- Output discharge path is enabled during device off.

Typical Performance Characteristics

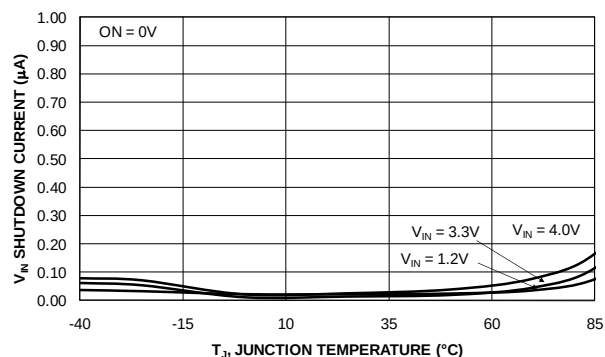


Figure 7. Shutdown Current vs. Temperature

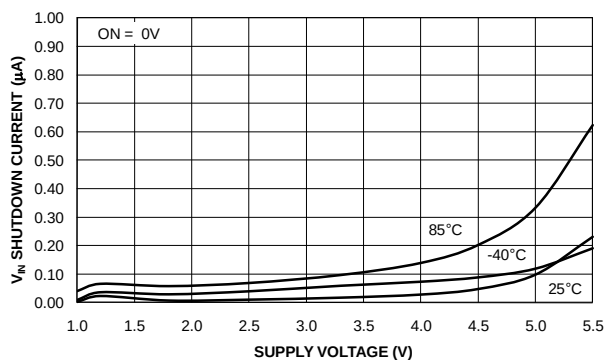


Figure 8. Shutdown Current vs. Supply Voltage

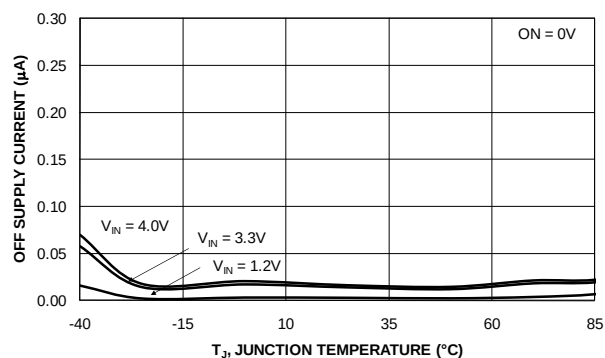


Figure 9. Off Supply Current vs. Temperature
(FPF1205, V_{OUT} Floating)

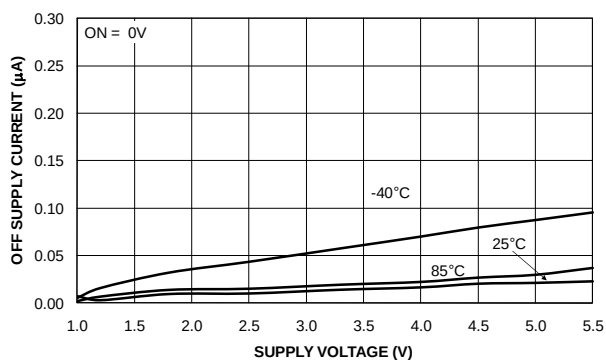


Figure 10. Off Supply Current vs. Supply Voltage
(FPF1205, V_{OUT} Floating)

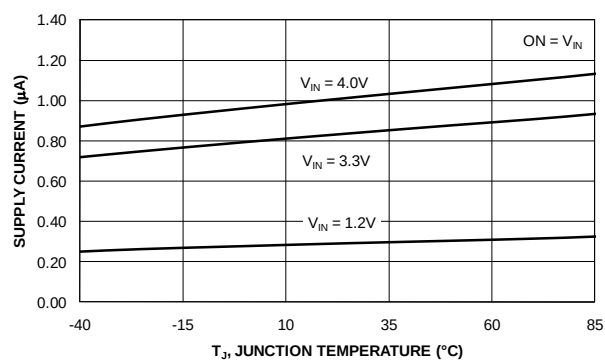


Figure 11. Quiescent Current vs. Temperature

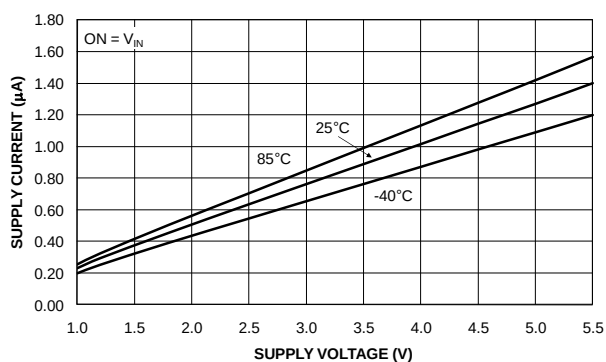


Figure 12. Quiescent Current vs. Supply Voltage

Typical Performance Characteristics

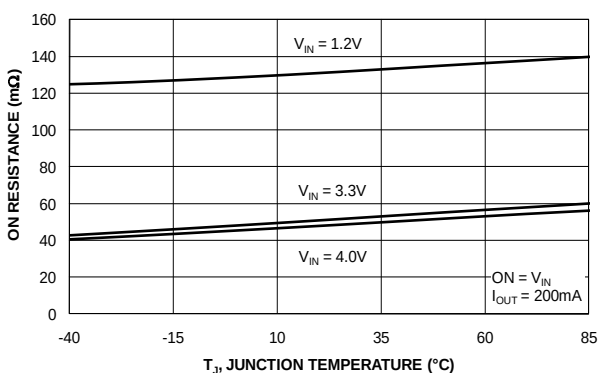


Figure 13. R_{ON} vs. Temperature

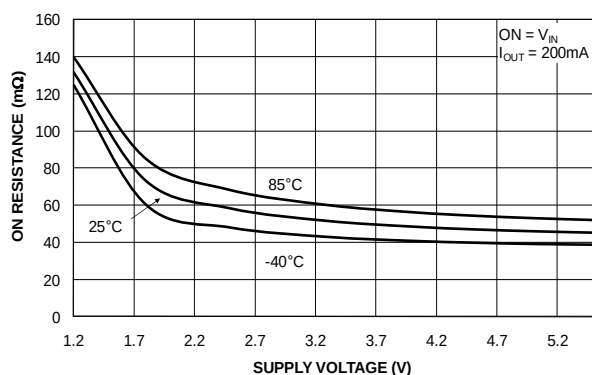


Figure 14. R_{ON} vs. Supply Voltage

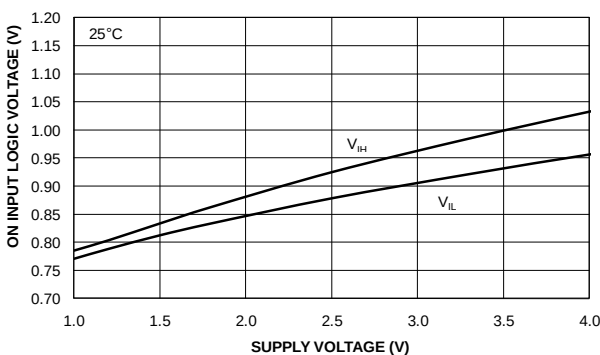


Figure 15. ON-Pin Threshold vs. V_{IN}

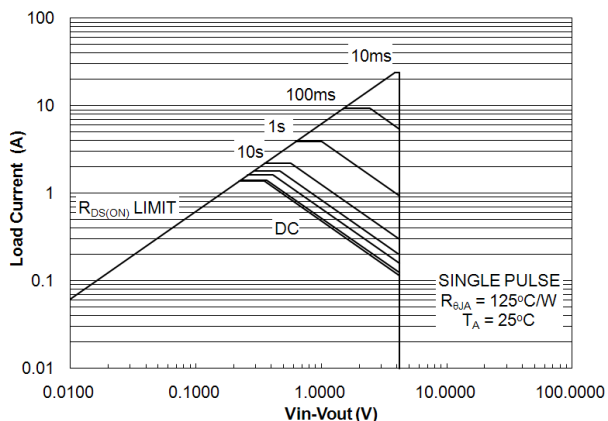


Figure 16. Load Current vs. $V_{IN}-V_{OUT}$

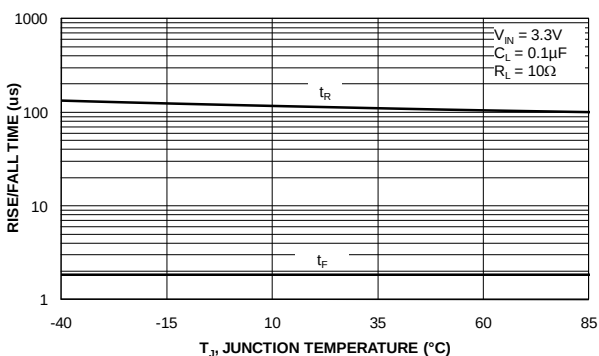


Figure 17. V_{OUT} Rise and Fall Time vs. Temperature at $R_L=10\ \Omega$

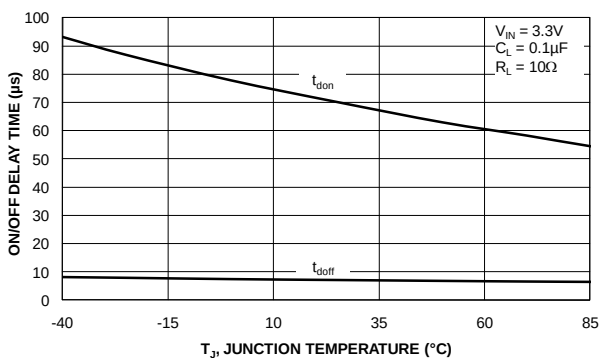


Figure 18. V_{OUT} Turn-On and Turn-Off Delay vs. Temperature at $R_L=10\ \Omega$

Typical Performance Characteristics

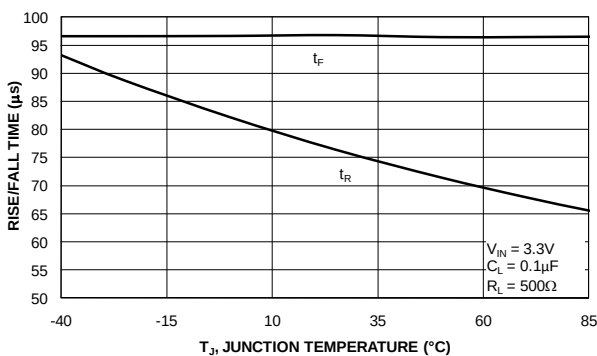


Figure 19. V_{OUT} Rise and Fall Time vs. Temperature at $R_L=500\ \Omega$

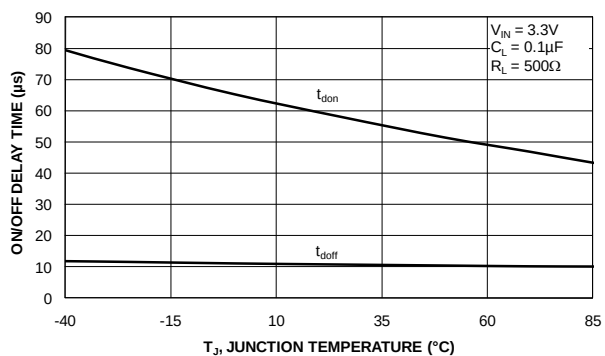


Figure 20. V_{OUT} Turn-On and Turn-Off Delay vs. Temperature at $R_L=500\ \Omega$

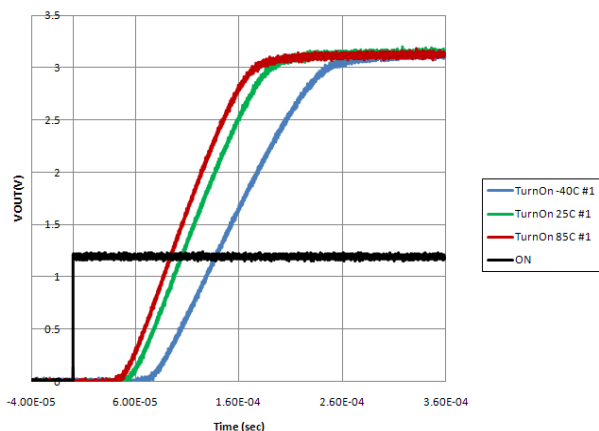


Figure 21. Turn-On Response ($V_{IN}=3.3\text{ V}$, $C_{IN}=1\ \mu\text{F}$, $C_{OUT}=0.1\ \mu\text{F}$, $R_L=10\ \Omega$)

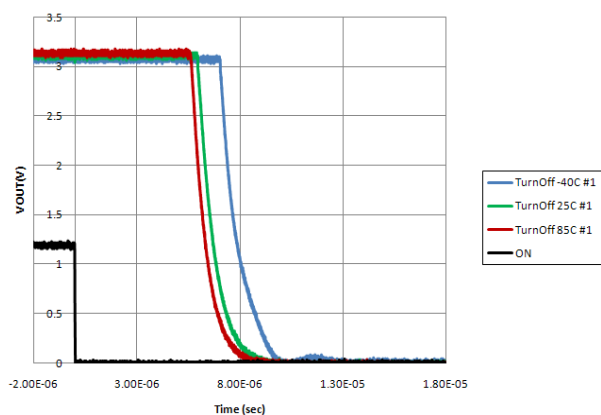


Figure 22. Turn-Off Response ($V_{IN}=3.3\text{ V}$, $C_{IN}=1\ \mu\text{F}$, $C_{OUT}=0.1\ \mu\text{F}$, $R_L=10\ \Omega$)

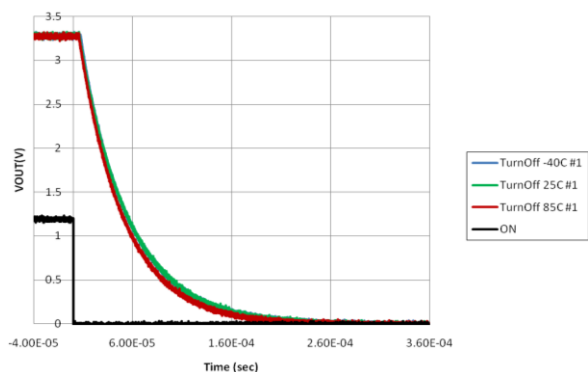


Figure 23. Turn-Off Response (FPF1205 = No Output Pull-Down Resistor) ($V_{IN}=3.3\text{ V}$, $C_{IN}=1\ \mu\text{F}$, $C_{OUT}=0.1\ \mu\text{F}$, $R_L=500\ \Omega$)

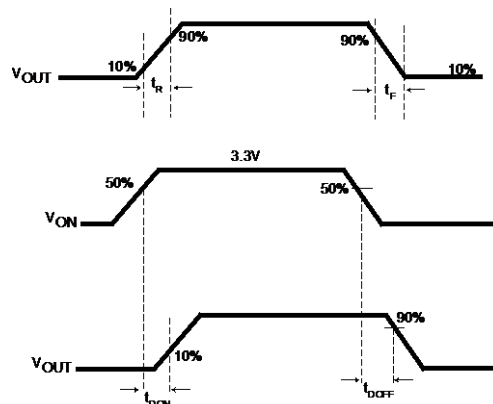


Figure 24. Timing Diagram

Notes:

8. $t_{ON}=t_R + t_{DON}$.
9. $t_{OFF}=t_F + t_{DOFF}$.

Operation and Application Description

The FPF1205 and FPF1206 are low- R_{ON} P-channel load switches with controlled turn-on. The core of each device is a 50 m Ω P-channel MOSFET and controller capable of functioning over a wide input operating range of 1.2 - 4.0 V. The ON pin, an active HIGH GIOP / CMOS-compatible input, controls the state of the switch.

The FPF1206 contains a 65 Ω on-chip load resistor for quick output discharge when the switch is turned off.

Input Capacitor

To limit the voltage drop on the input supply caused by transient inrush current when the switch turns on into a discharged load capacitor or short-circuit, a capacitor must be placed between the V_{IN} and GND pins. A 1 μ F ceramic capacitor, C_{IN} , placed close to the pins is usually sufficient. Higher-value C_{IN} can be used to reduce the voltage drop in higher-current applications.

Output Capacitor

A 0.1 μ F capacitor, C_{OUT} , should be placed between the V_{OUT} and GND pins. This capacitor prevents parasitic

board inductance from forcing V_{OUT} below GND when the switch is on. C_{IN} greater than C_{OUT} is highly recommended. C_{OUT} greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN} .

Board Layout

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effect that parasitic trace inductance may have on normal and short-circuit operation. Using wide traces or large copper planes for all pins (V_{IN} , V_{OUT} , ON, and GND) helps minimize the parasitic electrical effects along with minimizing the case ambient thermal impedance. However, the V_{OUT} pin of FPF1206 should not connect directly the battery source due to the discharge mechanism of the load switch.

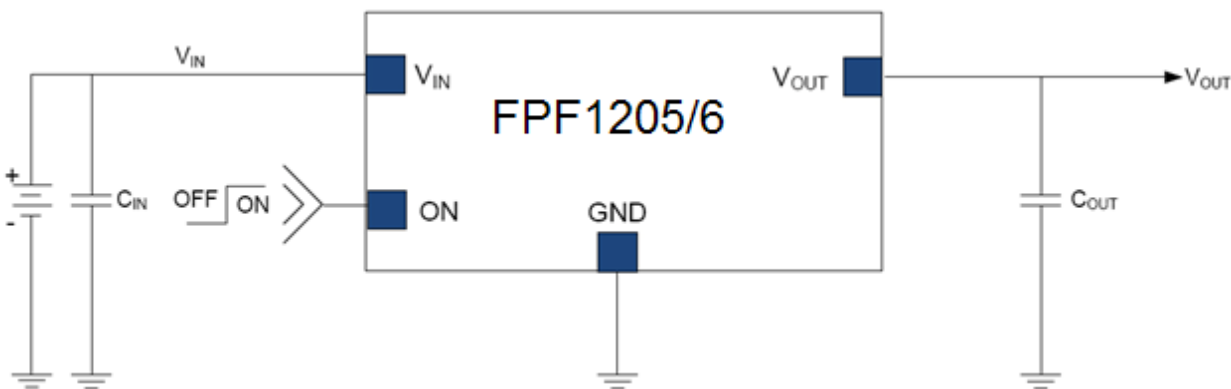
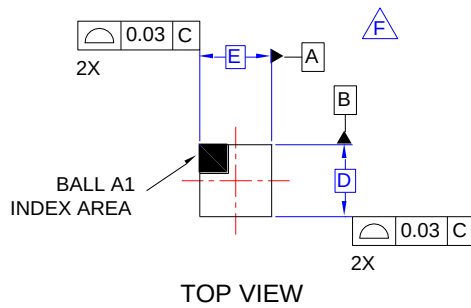
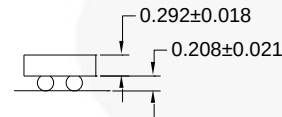
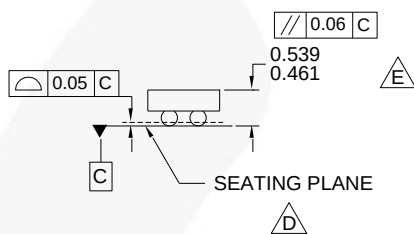
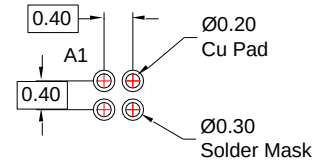


Figure 25. Typical Application

Physical Dimensions



RECOMMENDED LAND PATTERN (NSMD PAD TYPE)



NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCE PER ASME Y14.5M, 1994.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 500 MICRONS ± 39 MICRONS (461-539 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILNAME: MKT-UC004AFrev1.

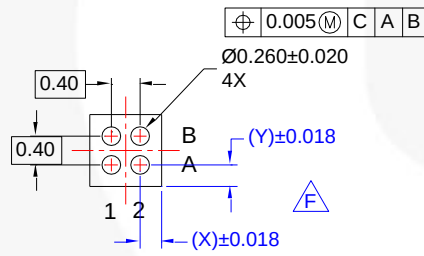


Figure 26. 4 Ball, 0.76 x 0.76 mm Wafer-Level Chip-Scale WLCSP Packaging

Product-Specific Dimensions

Product	D	E	X	Y
FPF1205UCX	760 μm ± 30 μm	760 μm ± 30 μm	0.180 mm ± 0.018 μm	0.180 mm ± 0.018 μm
FPF1206UCX	760 μm ± 30 μm	760 μm ± 30 μm	0.180 mm ± 0.018 μm	0.180 mm ± 0.018 μm

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