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May 2014

# FQA13N50CF

## N-Channel QFET® FRFET® MOSFET

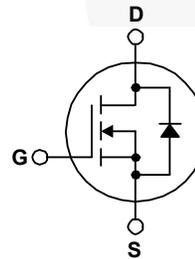
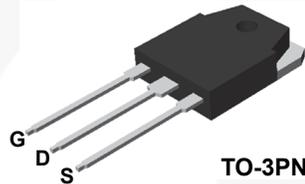
500 V, 15 A, 480 mΩ

### Features

- 15 A, 500 V,  $R_{DS(on)} = 480 \text{ m}\Omega$  (Max.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 7.5 \text{ A}$
- Low Gate Charge (Typ. 43 nC)
- Low  $C_{RSS}$  (Typ. 20 pF)
- 100% Avalanche Tested
- Fast Recovery Body Diode (Typ. 100 ns)

### Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FQA13N50CF	Unit
$V_{DSS}$	Drain-Source Voltage	500	V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	15
		- Continuous ( $T_C = 100^\circ\text{C}$ )	9.5
$I_{DM}$	Drain Current - Pulsed (Note 1)	60	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	860	mJ
$I_{AR}$	Avalanche Current (Note 1)	15	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	21.8	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ (Note 3)	4.5	V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ )		218
		- Derate above $25^\circ\text{C}$	1.56
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FQA13N50CF	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.58	$^\circ\text{C}/\text{W}$
$R_{\theta JS}$	Thermal Resistance, Case-to-Sink, Typ.	0.24	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	40	$^\circ\text{C}/\text{W}$

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQA13N50CF	FQA13N50CF	TO-3PN	Tube	N/A	N/A	30 units

## Electrical Characteristics T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit	
<b>Off Characteristics</b>							
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	500	--	--	V	
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	--	0.5	--	V/°C	
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 500 V, V <sub>GS</sub> = 0 V	--	--	1	μA	
		V <sub>DS</sub> = 400 V, T <sub>C</sub> = 125°C	--	--	10	μA	
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V	--	--	100	nA	
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V	--	--	-100	nA	
<b>On Characteristics</b>							
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0	--	4.0	V	
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 7.5 A	--	0.43	0.48	Ω	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40 V, I <sub>D</sub> = 7.5 A	--	15	--	S	
<b>Dynamic Characteristics</b>							
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	--	1580	2055	pF	
C <sub>oss</sub>	Output Capacitance		--	180	235	pF	
C <sub>rss</sub>	Reverse Transfer Capacitance		--	20	25	pF	
<b>Switching Characteristics</b>							
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 250 V, I <sub>D</sub> = 15 A, R <sub>G</sub> = 25 Ω	--	25	60	ns	
t <sub>r</sub>	Turn-On Rise Time		--	100	210	ns	
t <sub>d(off)</sub>	Turn-Off Delay Time		(Note 4)	--	130	270	ns
t <sub>f</sub>	Turn-Off Fall Time		(Note 4)	--	100	210	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 400 V, I <sub>D</sub> = 15 A, V <sub>GS</sub> = 10 V	--	43	56	nC	
Q <sub>gs</sub>	Gate-Source Charge		(Note 4)	--	7.5	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		(Note 4)	--	18.5	--	nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>							
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	15	A	
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	60	A	
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 15 A	--	--	1.4	V	
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 15 A, dI <sub>F</sub> / dt = 100 A/μs	--	100	--	ns	
Q <sub>rr</sub>	Reverse Recovery Charge		--	0.4	--	μC	

### NOTES:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. L = 5.6 mH, I<sub>AS</sub> = 15 A, V<sub>DD</sub> = 50 V, R<sub>G</sub> = 25 Ω, starting T<sub>J</sub> = 25°C.
3. I<sub>SD</sub> ≤ 15 A, di/dt ≤ 200 A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, starting T<sub>J</sub> = 25°C.
4. Essentially independent of operating temperature typical characteristics.

## Typical Performance Characteristics

Figure 1. On-Region Characteristics

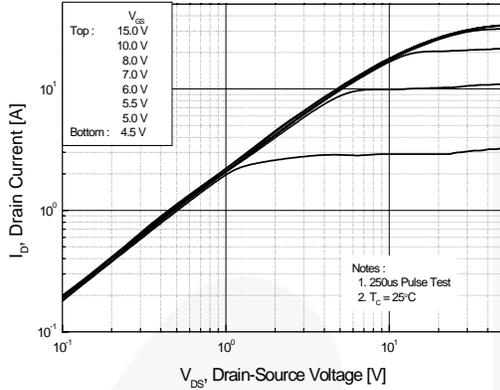


Figure 2. Transfer Characteristics

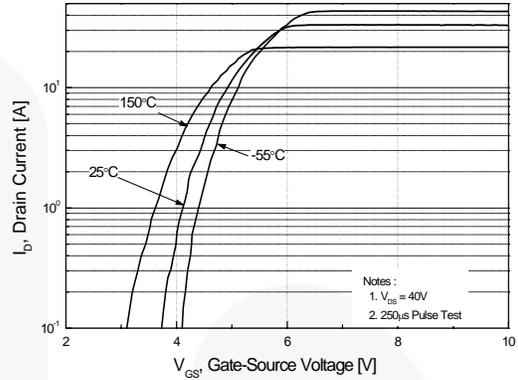


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

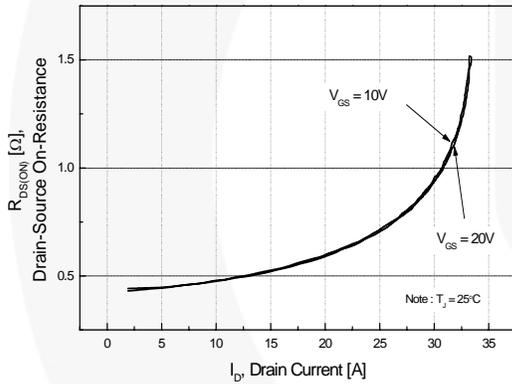


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

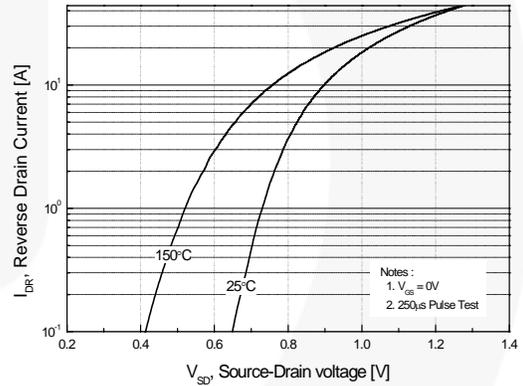


Figure 5. Capacitance Characteristics

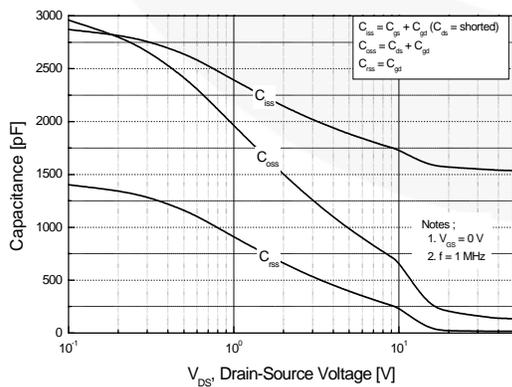
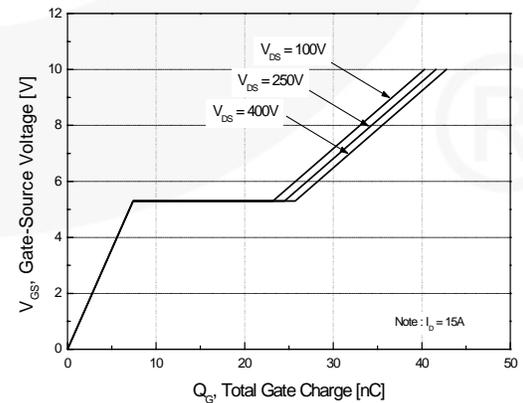
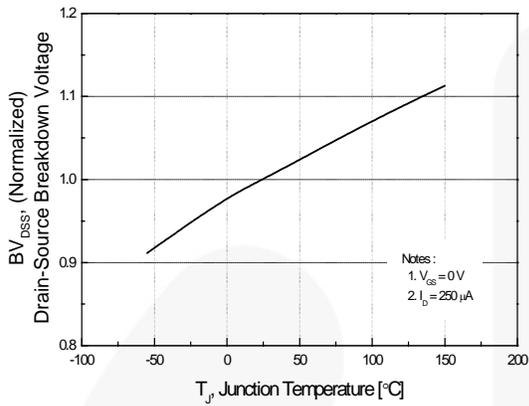


Figure 6. Gate Charge Characteristics

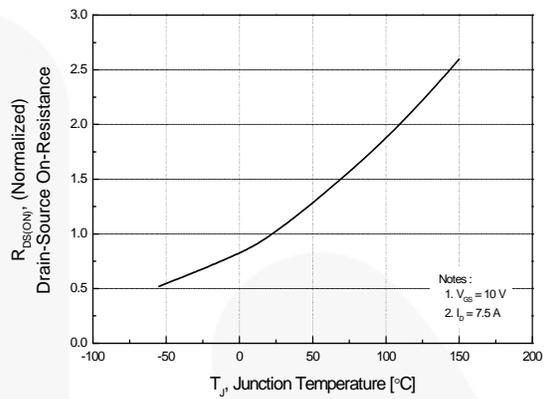


**Typical Performance Characteristics** (Continued)

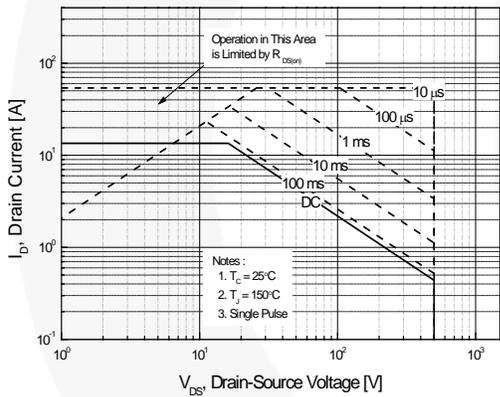
**Figure 7. Breakdown Voltage Variation vs. Temperature**



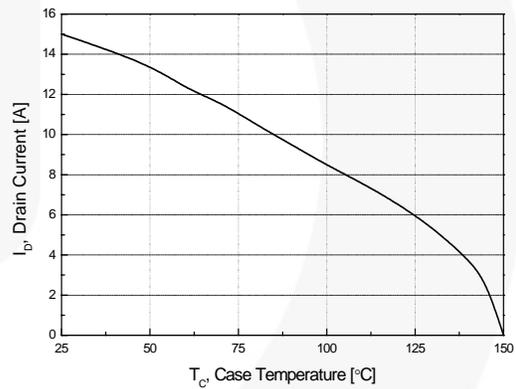
**Figure 8. On-Resistance Variation vs. Temperature**



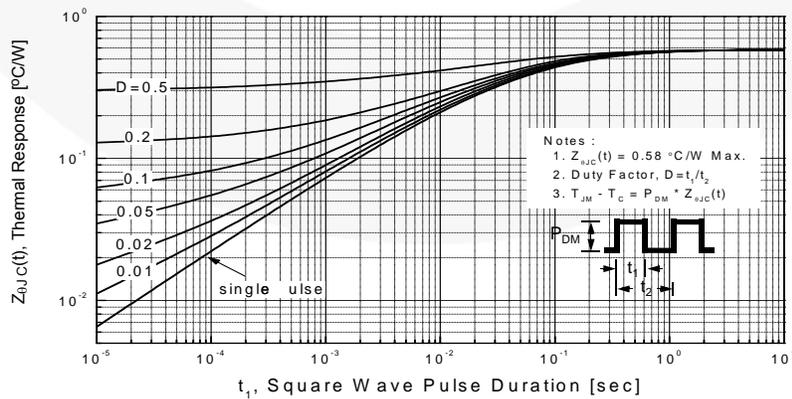
**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Transient Thermal Response Curve**



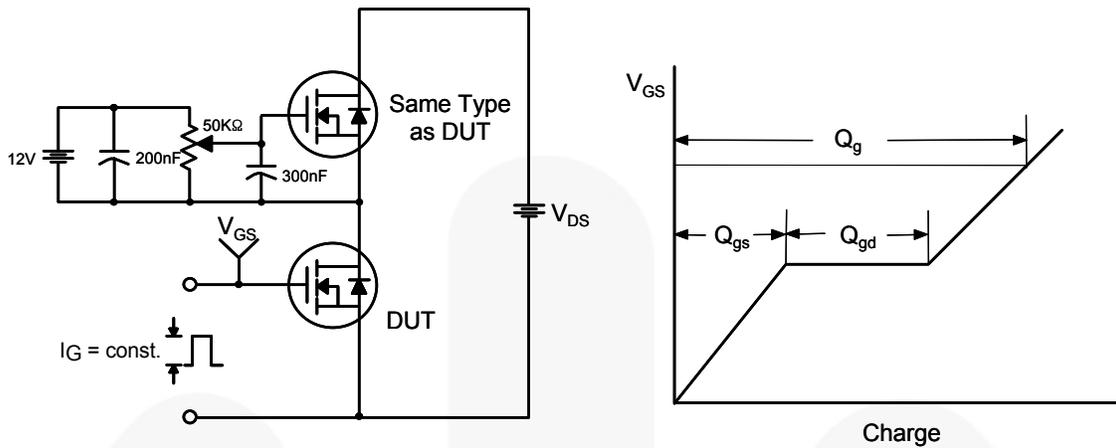


Figure 12. Gate Charge Test Circuit & Waveform

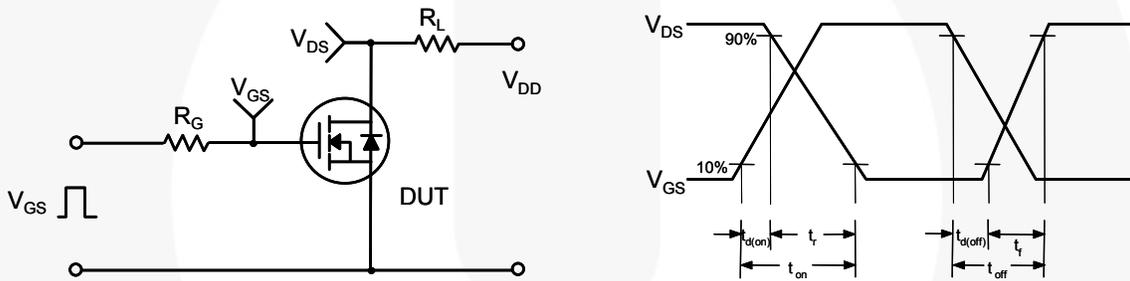


Figure 13. Resistive Switching Test Circuit & Waveforms

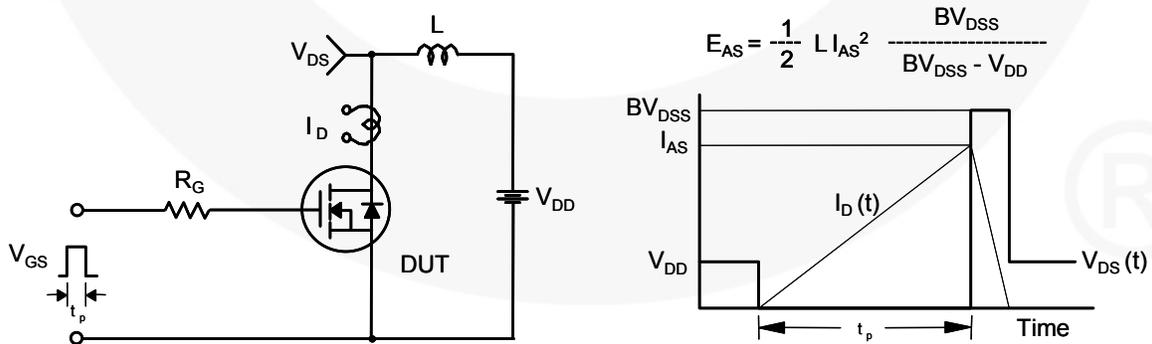


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

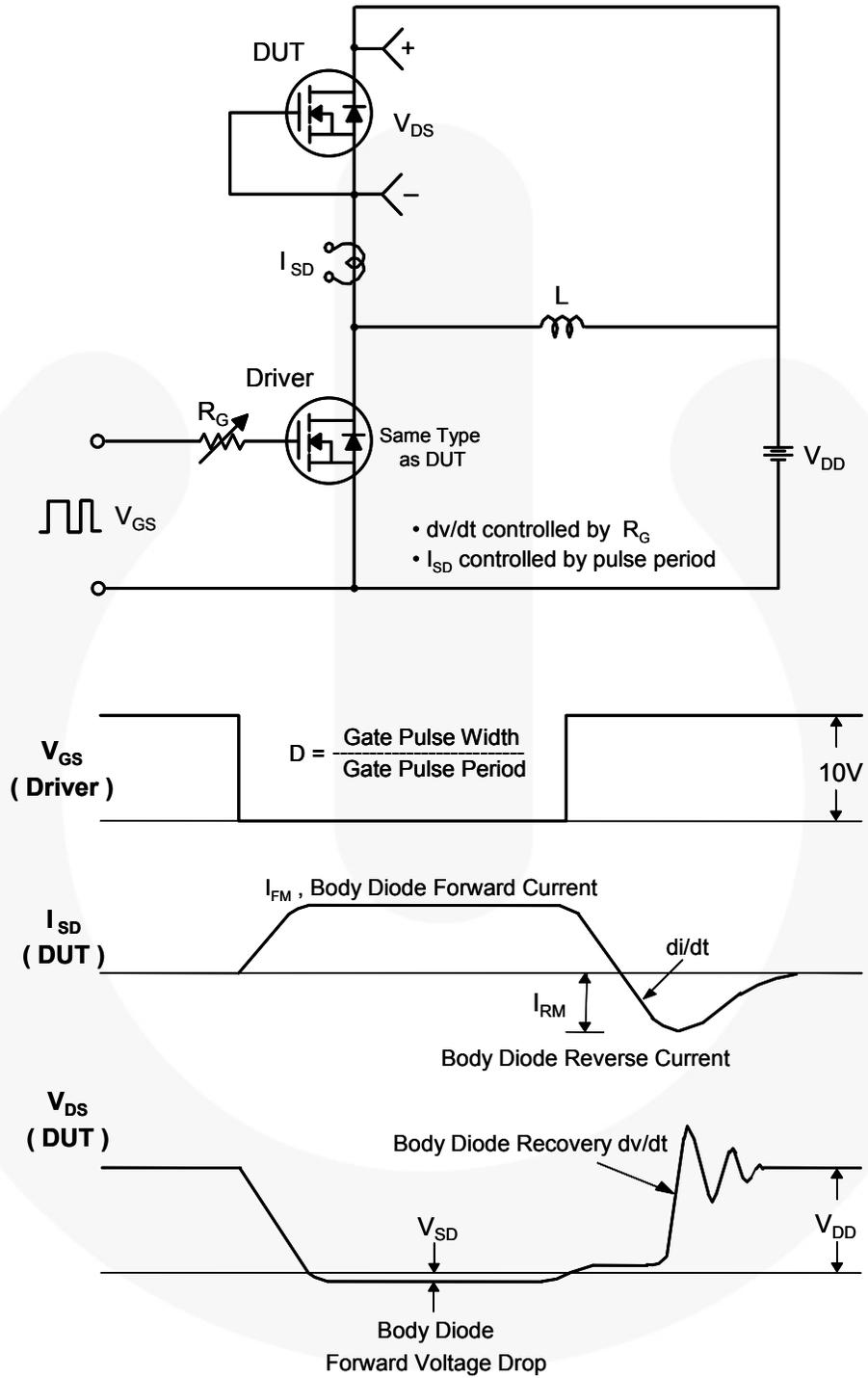


Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms





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