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FQAF16N50

N-Channel QFET® MOSFET

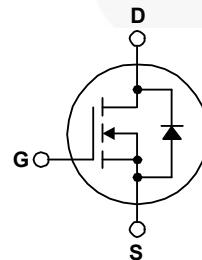
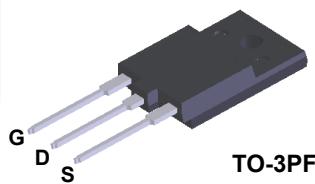
500 V, 11.3 A, 320 mΩ

Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 11.3 A, 500 V, $R_{DS(on)}$ = 320 mΩ (Max.) @ $V_{GS} = 10$ V, $I_D = 5.65$ A
- Low Gate Charge (Typ. 60 nC)
- Low C_{rss} (Typ. 35 pF)
- 100% Avalanche Tested



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FQAF16N50	Unit
V_{DSS}	Drain-Source Voltage	500	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	11.3	A
	- Continuous ($T_C = 100^\circ\text{C}$)	7.15	A
I_{DM}	Drain Current - Pulsed	(Note 1)	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	mJ
I_{AR}	Avalanche Current	(Note 1)	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	110	W
	- Derate above 25°C	0.88	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FQAF16N50	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	1.14	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	40	$^\circ\text{C}/\text{W}$

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQAF16N50	FQAF16N50	TO-3PF	Tube	N/A	N/A	30 units

Electrical Characteristics $T_c = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$\text{V}_{\text{GS}} = 0 \text{ V}$, $\text{I}_D = 250 \mu\text{A}$	500	--	--	V
$\Delta \text{BV}_{\text{DSS}} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$\text{I}_D = 250 \mu\text{A}$, Referenced to 25°C	--	0.53	--	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$\text{V}_{\text{DS}} = 500 \text{ V}$, $\text{V}_{\text{GS}} = 0 \text{ V}$	--	--	1	μA
		$\text{V}_{\text{DS}} = 400 \text{ V}$, $T_c = 125^\circ\text{C}$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$\text{V}_{\text{GS}} = 30 \text{ V}$, $\text{V}_{\text{DS}} = 0 \text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$\text{V}_{\text{GS}} = -30 \text{ V}$, $\text{V}_{\text{DS}} = 0 \text{ V}$	--	--	-100	nA

On Characteristics

$\text{V}_{\text{GS(th)}}$	Gate Threshold Voltage	$\text{V}_{\text{DS}} = \text{V}_{\text{GS}}$, $\text{I}_D = 250 \mu\text{A}$	3.0	--	5.0	V
$\text{R}_{\text{DS(on)}}$	Static Drain-Source On-Resistance	$\text{V}_{\text{GS}} = 10 \text{ V}$, $\text{I}_D = 5.65 \text{ A}$	--	0.25	0.32	Ω
g_{FS}	Forward Transconductance	$\text{V}_{\text{DS}} = 50 \text{ V}$, $\text{I}_D = 5.65 \text{ A}$	--	11	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$\text{V}_{\text{DS}} = 25 \text{ V}$, $\text{V}_{\text{GS}} = 0 \text{ V}$, $f = 1.0 \text{ MHz}$	--	2300	3000	pF
C_{oss}	Output Capacitance		--	325	420	pF
C_{rss}	Reverse Transfer Capacitance		--	35	45	pF

Switching Characteristics

$t_{\text{d(on)}}$	Turn-On Delay Time	$\text{V}_{\text{DD}} = 250 \text{ V}$, $\text{I}_D = 16 \text{ A}$, $\text{R}_G = 25 \Omega$	--	45	100	ns
t_r	Turn-On Rise Time		--	180	370	ns
$t_{\text{d(off)}}$	Turn-Off Delay Time		--	130	270	ns
t_f	Turn-Off Fall Time		--	100	210	ns
Q_g	Total Gate Charge	$\text{V}_{\text{DS}} = 400 \text{ V}$, $\text{I}_D = 16 \text{ A}$, $\text{V}_{\text{GS}} = 10 \text{ V}$	--	60	75	nC
Q_{gs}	Gate-Source Charge		--	14	--	nC
Q_{gd}	Gate-Drain Charge		--	28	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current	--	--	11.3	A	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	45.2	A	
V_{SD}	Drain-Source Diode Forward Voltage	$\text{V}_{\text{GS}} = 0 \text{ V}$, $\text{I}_S = 11.3 \text{ A}$	--	--	1.4	V
t_{rr}	Reverse Recovery Time	$\text{V}_{\text{GS}} = 0 \text{ V}$, $\text{I}_S = 16 \text{ A}$, $d\text{I}_F / dt = 100 \text{ A}/\mu\text{s}$	--	340	--	ns
Q_{rr}	Reverse Recovery Charge		--	3.2	--	μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 13.8 \text{ mH}$, $\text{I}_{\text{AS}} = 11.3 \text{ A}$, $\text{V}_{\text{DD}} = 50 \text{ V}$, $\text{R}_G = 25 \Omega$, Starting $T_J = 25^\circ\text{C}$
3. $\text{I}_{\text{SD}} \leq 16 \text{ A}$, $\text{dI}/\text{dt} \leq 200 \text{ A}/\mu\text{s}$, $\text{V}_{\text{DD}} \leq \text{BV}_{\text{DSS}}$, Starting $T_J = 25^\circ\text{C}$
4. Essentially independent of operating temperature

Typical Characteristics

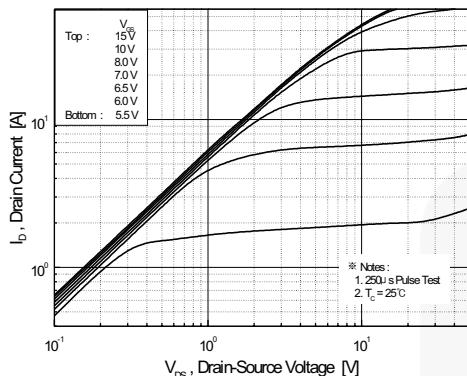


Figure 1. On-Region Characteristics

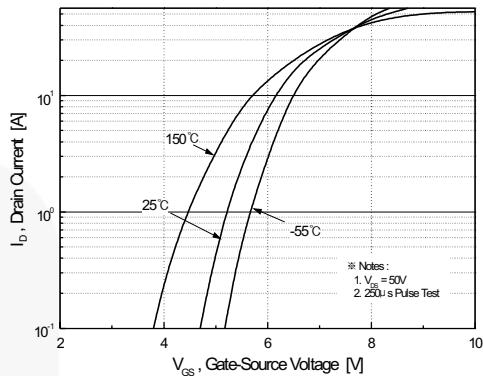


Figure 2. Transfer Characteristics

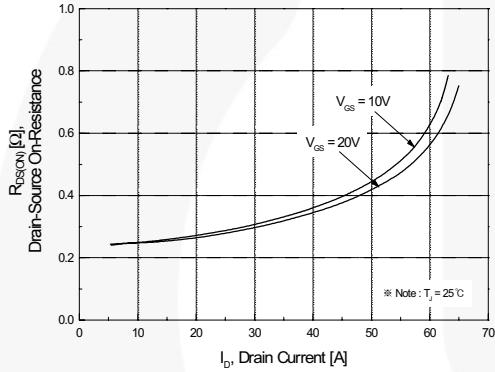


Figure 3. On-Resistance Variation vs.
Drain Current and Gate Voltage

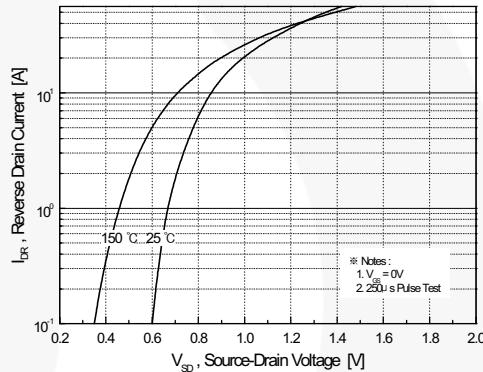


Figure 4. Body Diode Forward Voltage
Variation vs. Source Current
and Temperature

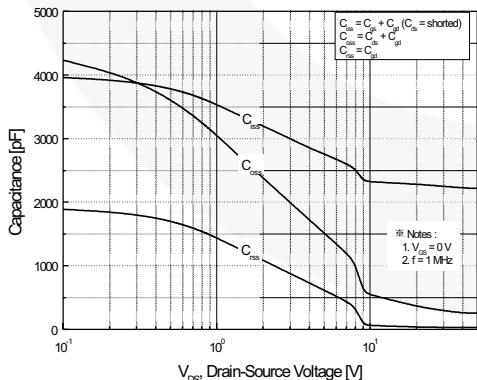


Figure 5. Capacitance Characteristics

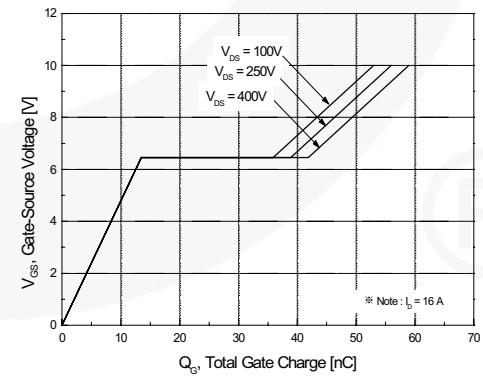


Figure 6. Gate Charge Characteristics

Typical Characteristics (continued)

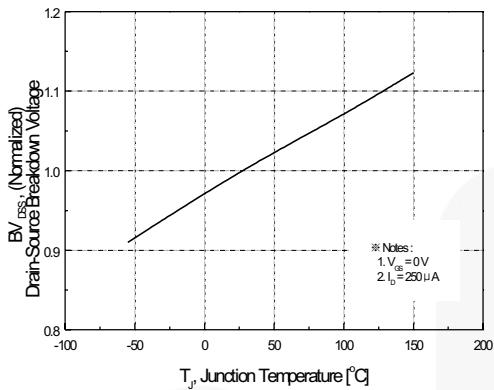


Figure 7. Breakdown Voltage Variation vs. Temperature

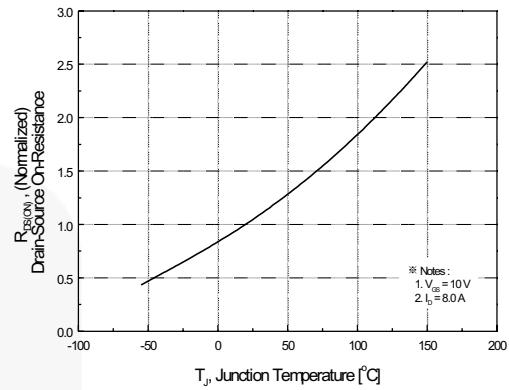


Figure 8. On-Resistance Variation vs. Temperature

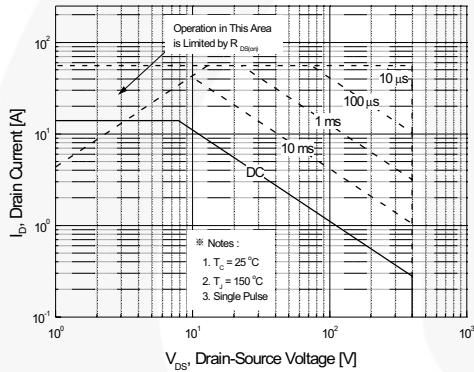


Figure 9. Maximum Safe Operating Area

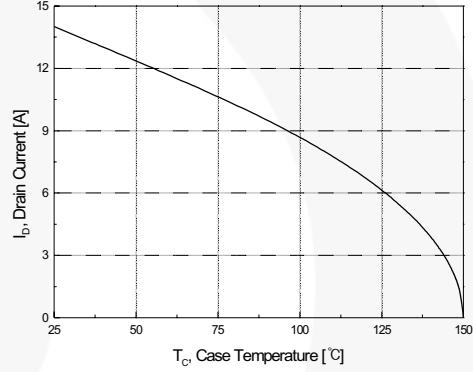


Figure 10. Maximum Drain Current vs. Case Temperature

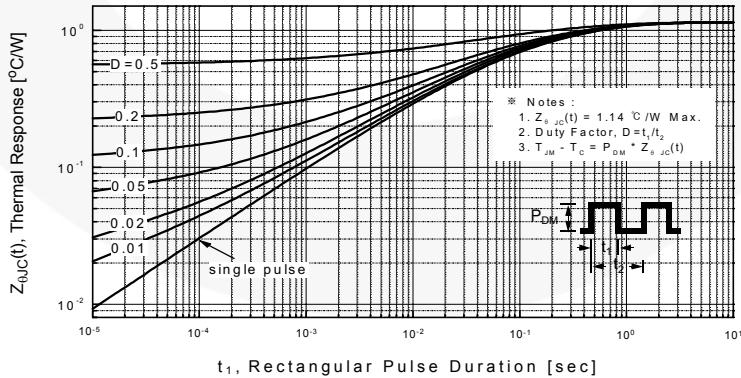


Figure 11. Transient Thermal Response Curve

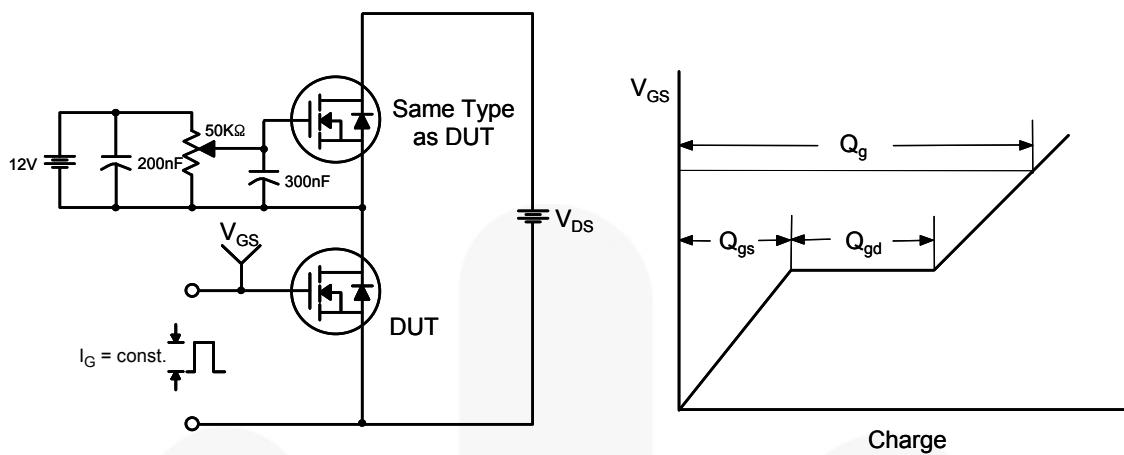


Figure 12. Gate Charge Test Circuit & Waveform

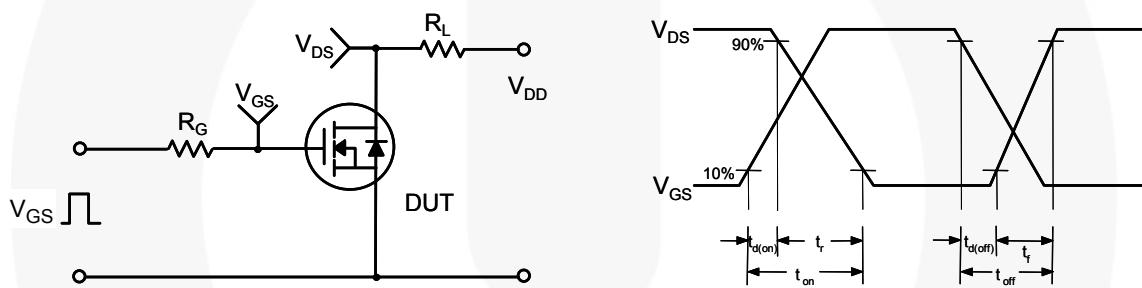


Figure 13. Resistive Switching Test Circuit & Waveforms

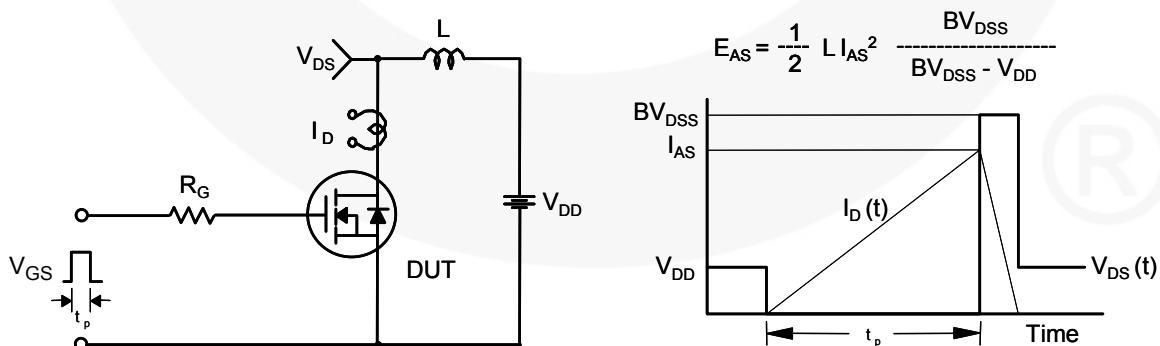


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

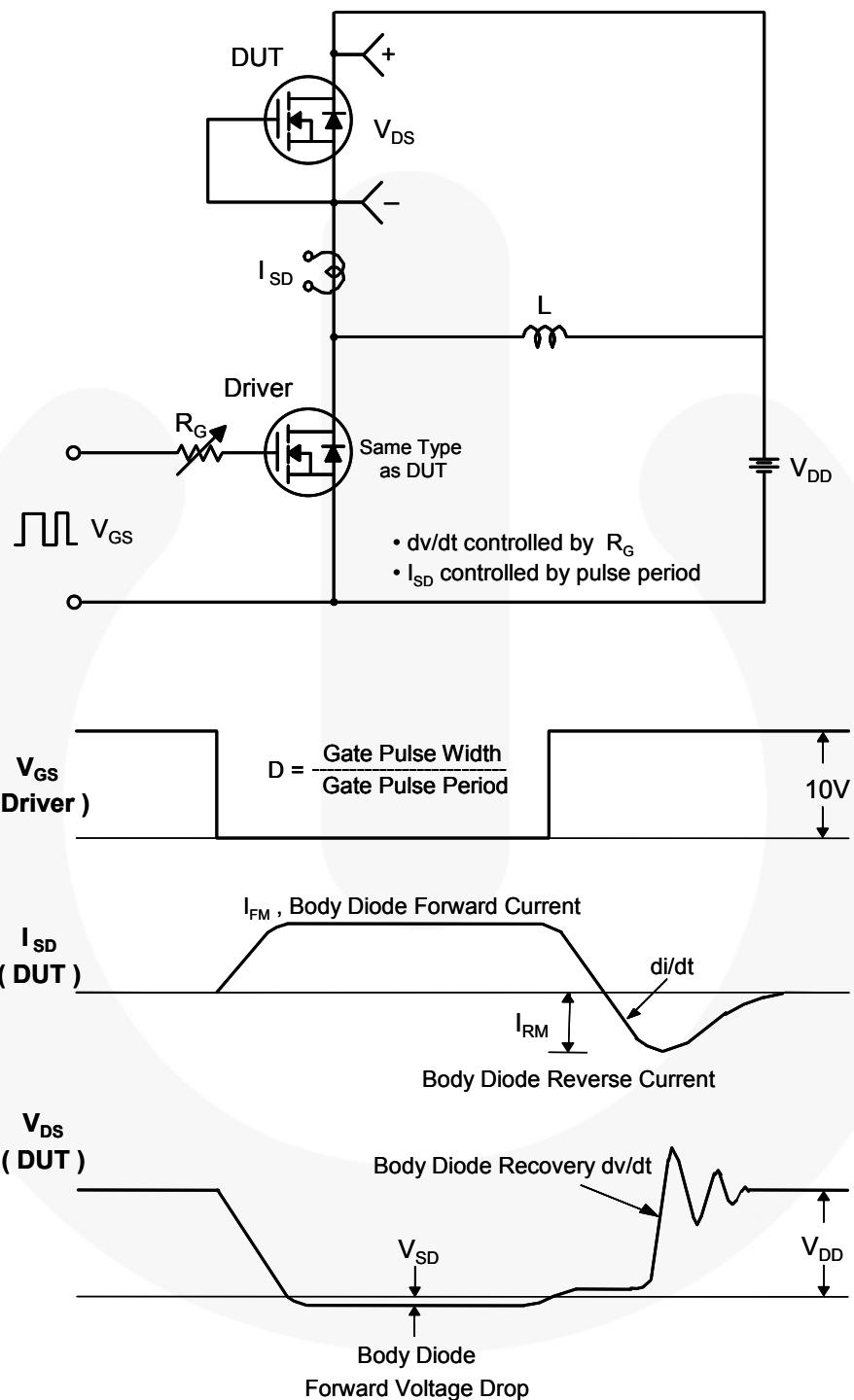
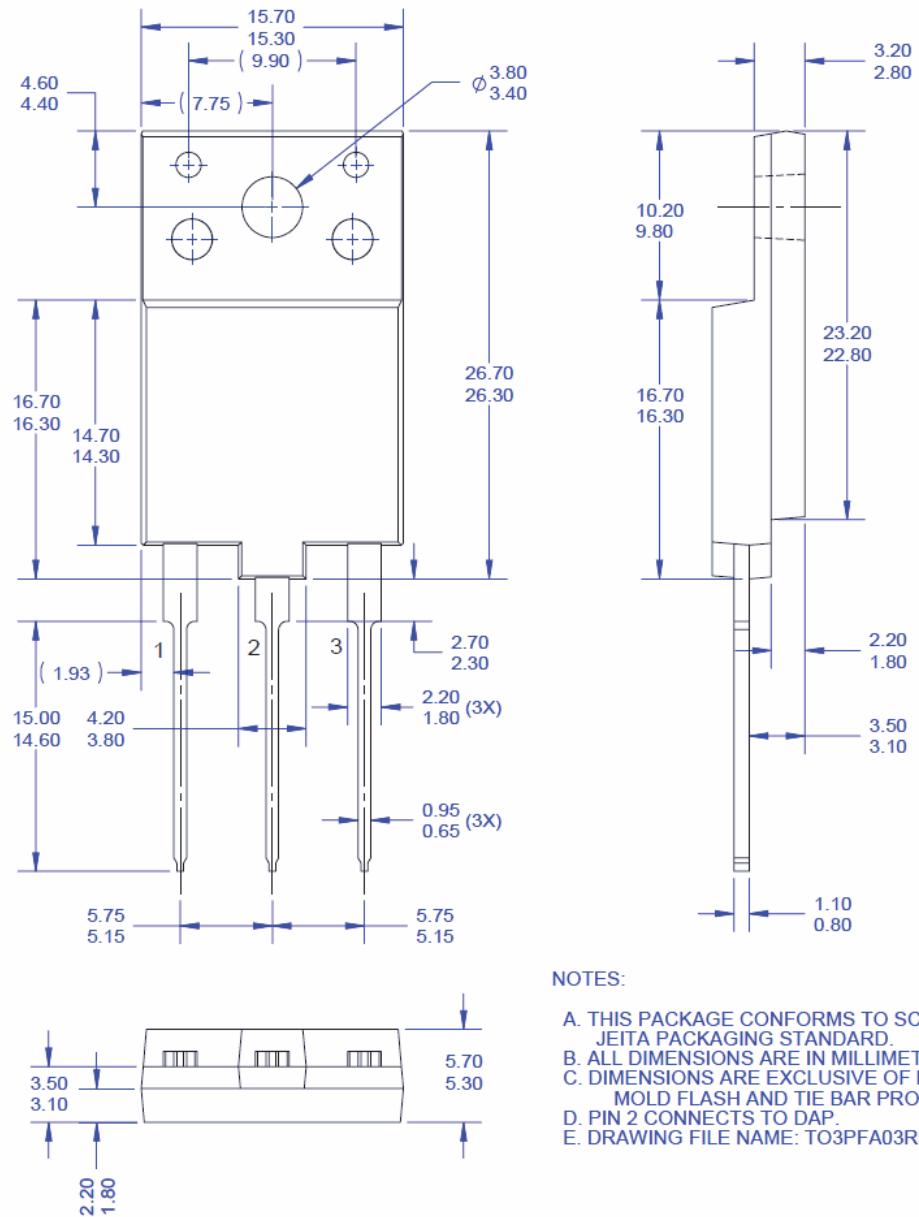


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions



NOTES:

- A. THIS PACKAGE CONFORMS TO SC94 JEITA PACKAGING STANDARD.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- D. PIN 2 CONNECTS TO DAP.
- E. DRAWING FILE NAME: TO3PFA03REV1

Figure 16. TO3PF, Molded, 3-Lead, Full Pack (AG)

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