

## FQH44N10

### N-Channel QFET® MOSFET

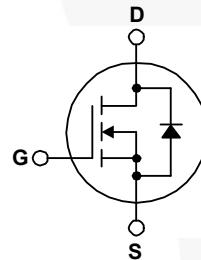
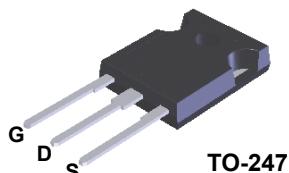
100 V, 48 A, 39 mΩ

#### Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

#### Features

- 48 A, 100 V,  $R_{DS(on)} = 39 \text{ mΩ}$  (Max.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 24 \text{ A}$
- Low Gate Charge (Typ. 48 nC)
- Low  $C_{rss}$  (Typ. 85 pF)
- 100% Avalanche Tested
- 175°C Maximum Junction Temperature Rating



#### Absolute Maximum Ratings

$T_c = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter		FQH44N10_F133	Unit
$V_{DSS}$	Drain-Source Voltage		100	V
$I_D$	Drain Current	- Continuous ( $T_c = 25^\circ\text{C}$ )	48	A
		- Continuous ( $T_c = 100^\circ\text{C}$ )	34	A
$I_{DM}$	Drain Current	- Pulsed	(Note 1)	A
$V_{GSS}$	Gate-Source Voltage		$\pm 25$	V
$E_{AS}$	Single Pulsed Avalanche Energy		530	mJ
$I_{AR}$	Avalanche Current		48	A
$E_{AR}$	Repetitive Avalanche Energy		18	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$		6.0	V/ns
$P_D$	Power Dissipation ( $T_c = 25^\circ\text{C}$ )		180	W
	- Derate above 25°C		1.2	W/°C
$T_J, T_{STG}$	Operating and Storage Temperature Range		-55 to +175	°C
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

#### Thermal Characteristics

Symbol	Parameter	FQH44N10_F133	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.83	°C/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink, Typ.	0.24	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	40	°C/W

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQH44N10_F133	FQH44N10	TO-247	Tube	N/A	N/A	30 units

## Electrical Characteristics $T_c = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
$\text{BV}_{\text{DSS}}$	Drain-Source Breakdown Voltage	$\text{V}_{\text{GS}} = 0 \text{ V}$ , $\text{I}_D = 250 \mu\text{A}$	100	--	--	V
$\Delta \text{BV}_{\text{DSS}} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$\text{I}_D = 250 \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.1	--	$\text{V}/^\circ\text{C}$
$\text{I}_{\text{DSS}}$	Zero Gate Voltage Drain Current	$\text{V}_{\text{DS}} = 100 \text{ V}$ , $\text{V}_{\text{GS}} = 0 \text{ V}$	--	--	1	$\mu\text{A}$
		$\text{V}_{\text{DS}} = 80 \text{ V}$ , $T_c = 150^\circ\text{C}$	--	--	10	$\mu\text{A}$
$\text{I}_{\text{GSSF}}$	Gate-Body Leakage Current, Forward	$\text{V}_{\text{GS}} = 25 \text{ V}$ , $\text{V}_{\text{DS}} = 0 \text{ V}$	--	--	100	nA
$\text{I}_{\text{GSSR}}$	Gate-Body Leakage Current, Reverse	$\text{V}_{\text{GS}} = -25 \text{ V}$ , $\text{V}_{\text{DS}} = 0 \text{ V}$	--	--	-100	nA
<b>On Characteristics</b>						
$\text{V}_{\text{GS(th)}}$	Gate Threshold Voltage	$\text{V}_{\text{DS}} = \text{V}_{\text{GS}}$ , $\text{I}_D = 250 \mu\text{A}$	2.0	--	4.0	V
$\text{R}_{\text{DS(on)}}$	Static Drain-Source On-Resistance	$\text{V}_{\text{GS}} = 10 \text{ V}$ , $\text{I}_D = 24 \text{ A}$	--	0.03	0.039	$\Omega$
$\text{g}_{\text{FS}}$	Forward Transconductance	$\text{V}_{\text{DS}} = 40 \text{ V}$ , $\text{I}_D = 24 \text{ A}$	--	31	--	S
<b>Dynamic Characteristics</b>						
$\text{C}_{\text{iss}}$	Input Capacitance	$\text{V}_{\text{DS}} = 25 \text{ V}$ , $\text{V}_{\text{GS}} = 0 \text{ V}$ , $f = 1.0 \text{ MHz}$	--	1400	1800	pF
$\text{C}_{\text{oss}}$	Output Capacitance		--	425	550	pF
$\text{C}_{\text{rss}}$	Reverse Transfer Capacitance		--	85	110	pF
<b>Switching Characteristics</b>						
$t_{\text{d(on)}}$	Turn-On Delay Time	$\text{V}_{\text{DD}} = 50 \text{ V}$ , $\text{I}_D = 43.5 \text{ A}$ , $\text{R}_G = 25 \Omega$	--	19	45	ns
$t_r$	Turn-On Rise Time		--	190	390	ns
$t_{\text{d(off)}}$	Turn-Off Delay Time		--	90	190	ns
$t_f$	Turn-Off Fall Time		--	100	210	ns
$Q_g$	Total Gate Charge	$\text{V}_{\text{DS}} = 80 \text{ V}$ , $\text{I}_D = 43.5 \text{ A}$ , $\text{V}_{\text{GS}} = 10 \text{ V}$	--	48	62	nC
$Q_{\text{gs}}$	Gate-Source Charge		--	9.0	--	nC
$Q_{\text{gd}}$	Gate-Drain Charge		--	24	--	nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
$\text{I}_S$	Maximum Continuous Drain-Source Diode Forward Current	--	--	48	--	A
$\text{I}_{\text{SM}}$	Maximum Pulsed Drain-Source Diode Forward Current	--	--	192	--	A
$\text{V}_{\text{SD}}$	Drain-Source Diode Forward Voltage	$\text{V}_{\text{GS}} = 0 \text{ V}$ , $\text{I}_S = 48 \text{ A}$	--	--	1.5	V
$t_{\text{rr}}$	Reverse Recovery Time	$\text{V}_{\text{GS}} = 0 \text{ V}$ , $\text{I}_S = 43.5 \text{ A}$ , $d\text{I}_F / dt = 100 \text{ A}/\mu\text{s}$	--	98	--	ns
$Q_{\text{rr}}$	Reverse Recovery Charge		--	360	--	nC

### Notes:

1. Repetitive rating : pulse-width limited by maximum junction temperature.
2.  $L = 0.345 \text{ mH}$ ,  $\text{I}_{\text{AS}} = 48 \text{ A}$ ,  $\text{V}_{\text{DD}} = 25 \text{ V}$ ,  $\text{R}_G = 25 \Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $\text{I}_{\text{SD}} \leq 43.5 \text{ A}$ ,  $d\text{I}/dt \leq 300 \text{ A}/\mu\text{s}$ ,  $\text{V}_{\text{DD}} \leq \text{BV}_{\text{DSS}}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature.

## Typical Characteristics

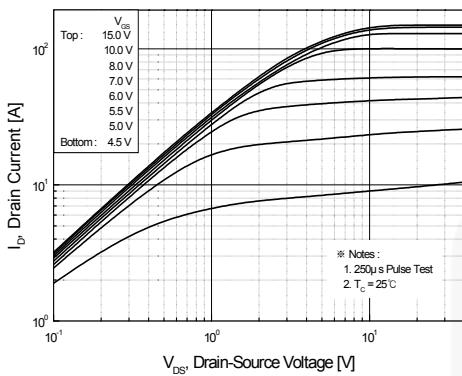


Figure 1. On-Region Characteristics

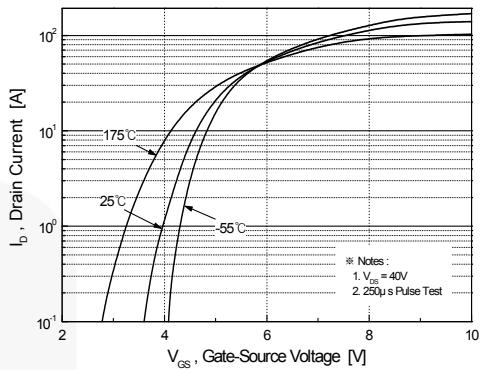


Figure 2. Transfer Characteristics

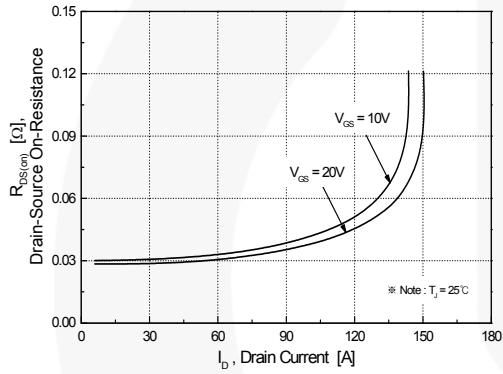


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

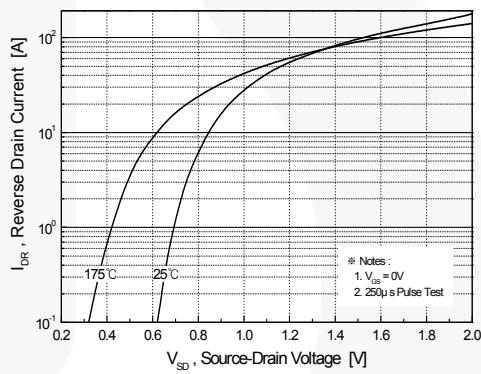


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

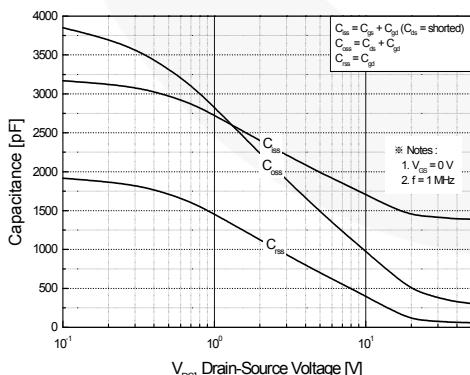


Figure 5. Capacitance Characteristics

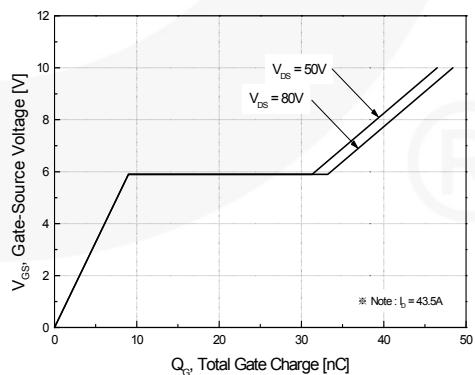
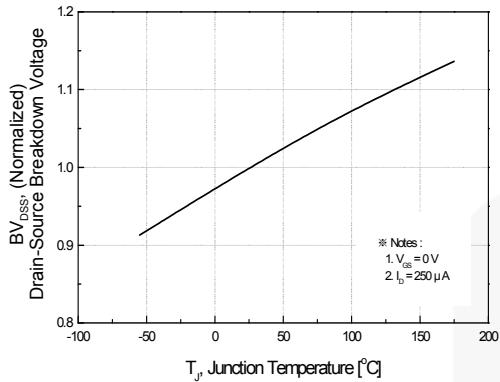
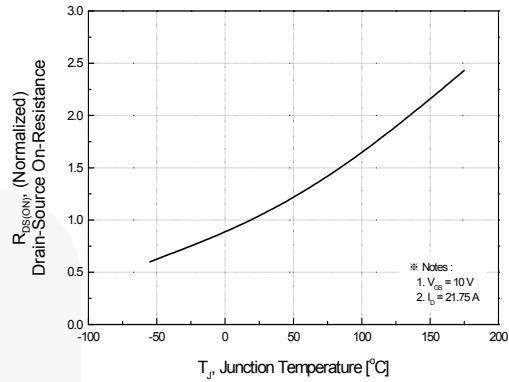


Figure 6. Gate Charge Characteristics

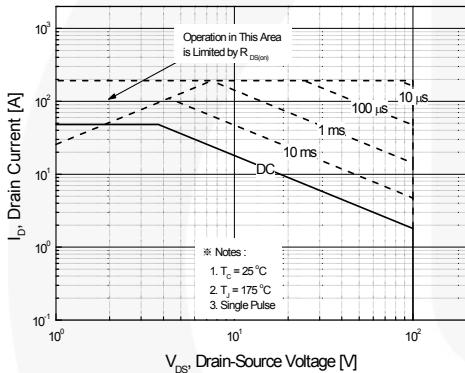
## Typical Characteristics (Continued)



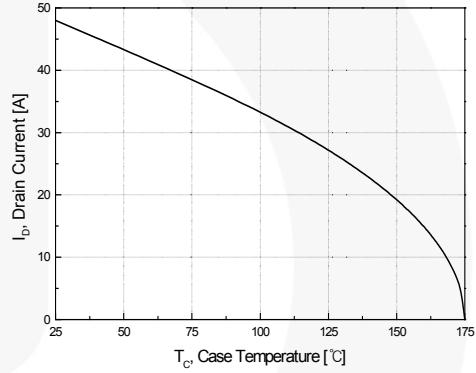
**Figure 7. Breakdown Voltage Variation vs. Temperature**



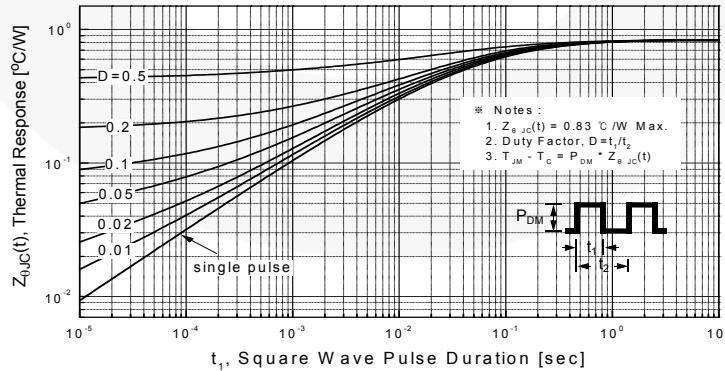
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Transient Thermal Response Curve**

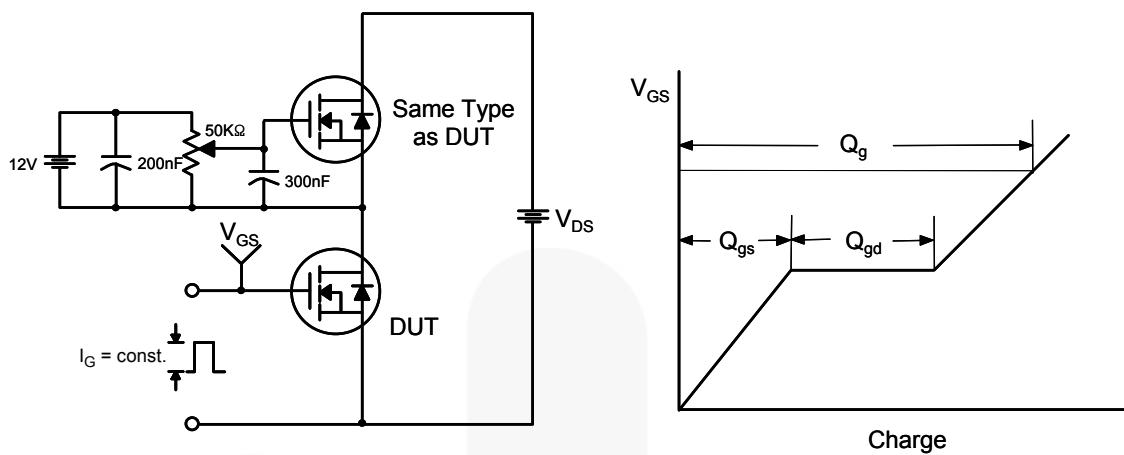


Figure 12. Gate Charge Test Circuit & Waveform

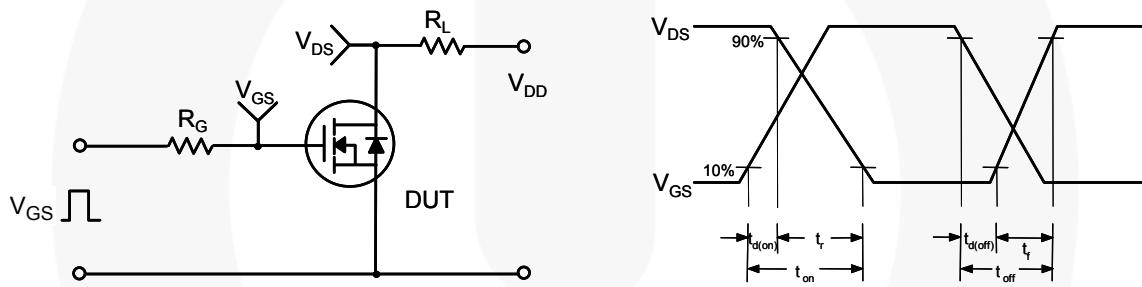


Figure 13. Resistive Switching Test Circuit & Waveforms

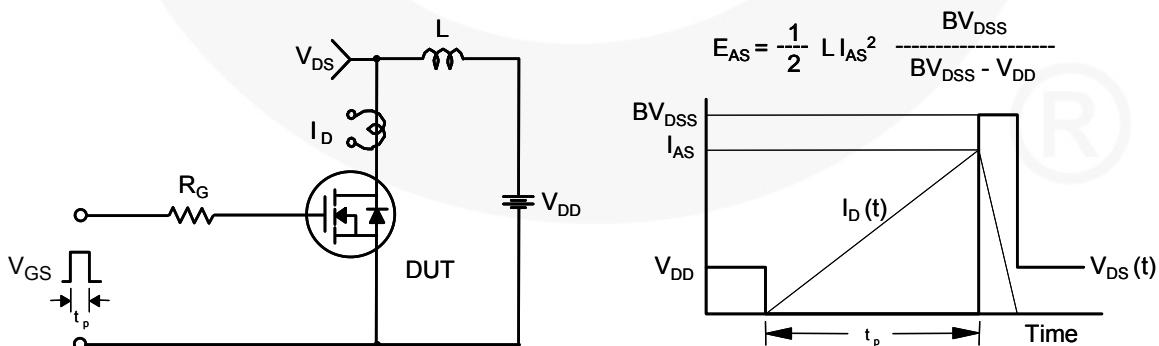


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

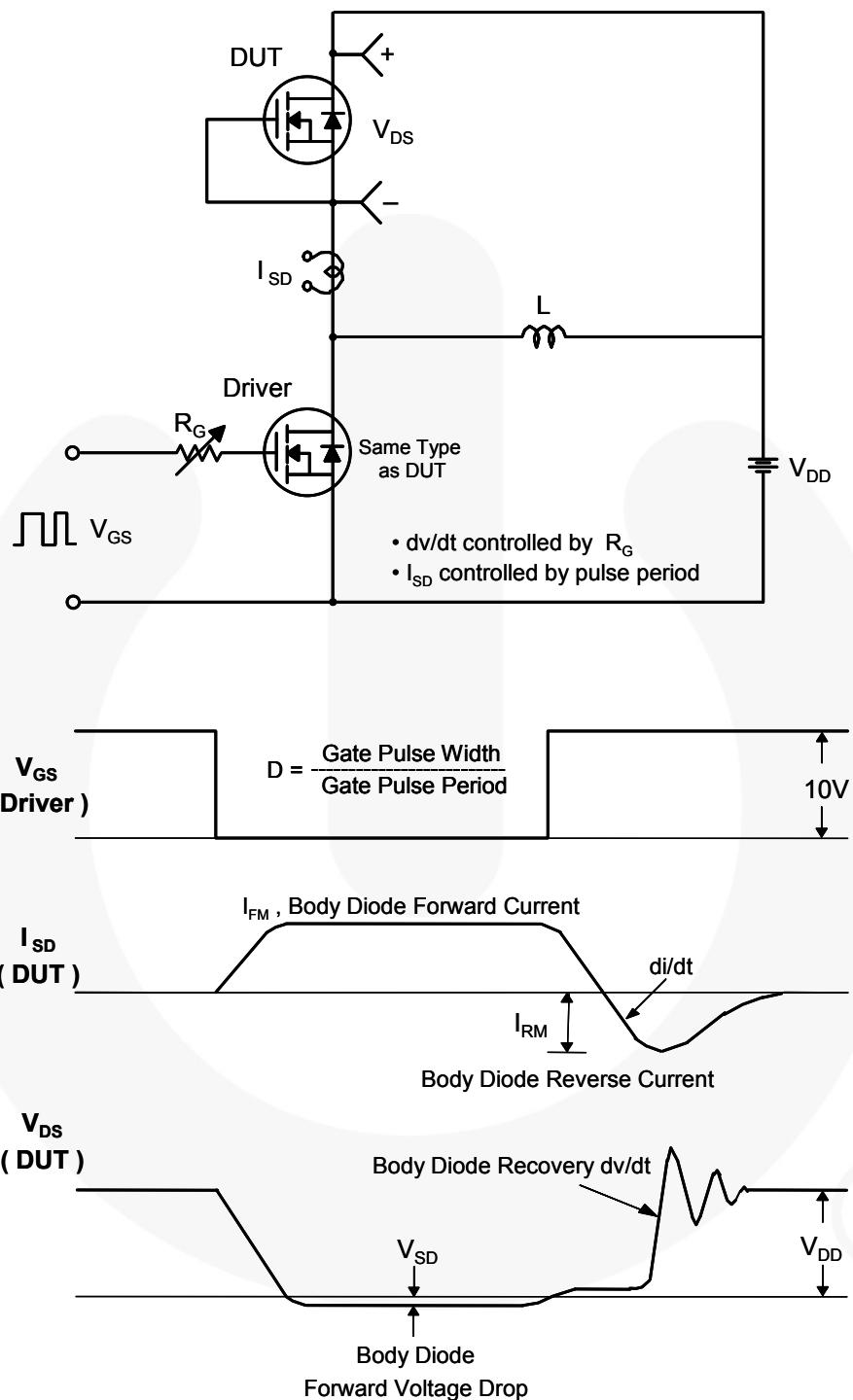
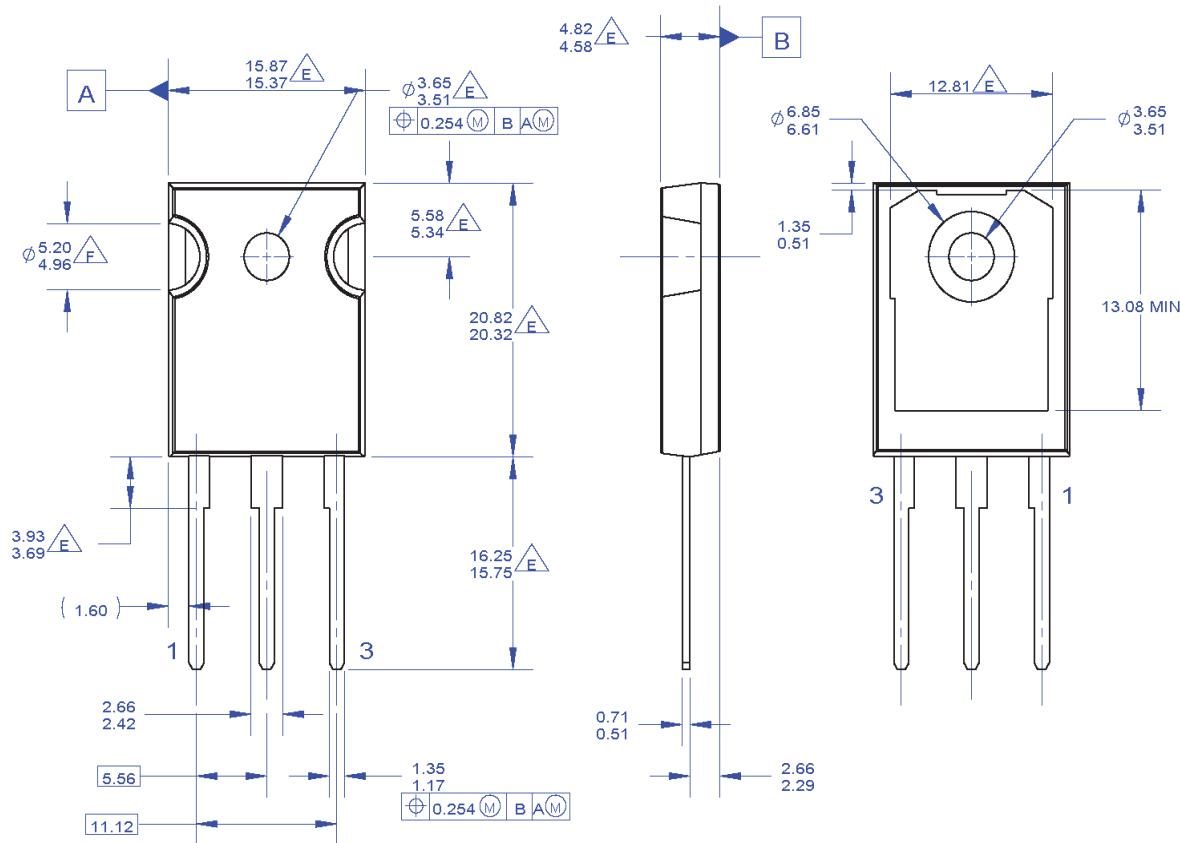


Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

## Mechanical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. PACKAGE REFERENCE: JEDEC TO-247, ISSUE E, VARIATION AB, DATED JUNE, 2004.
- B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DRAWING CONFORMS TO ASME Y14.5 - 1994

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**Figure 16. TO-247, Molded, 3-Lead, Jedec Variation AB**

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