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FSL206MR

Green Mode Fairchild Power Switch (FPS™)

Features

- Internal Avalanche-Rugged SenseFET: 650V
- Precision Fixed Operating Frequency: 67kHz
- No-Load <150mW at 265V_{AC} without Bias Winding; <25mW with Bias Winding for FSL206MR, <30mW with Bias Winding for FSL206MRBN
- No Need for Auxiliary Bias Winding
- Frequency Modulation for Attenuating EMI
- Line Under-Voltage Protection (LUVF)
- Pulse-by-Pulse Current Limiting
- Low Under-Voltage Lockout (UVLO)
- Ultra-Low Operating Current: 300μA
- Built-In Soft-Start and Startup Circuit
- Various Protections: Overload Protection (OLP), Over-Voltage Protection (OVP), Thermal Shutdown (TSD), Abnormal Over-Current Protection (AOCP) Auto-Restart Mode for All Protections

Applications

- SMPS for STB, DVD, and DVCD Player
- SMPS for Auxiliary Power

Related Resources

- [Fairchild Power Supply WebDesigner – Flyback Design and Simulation – In Minutes at No Expense](#)
- [AN-4137 — Design Guidelines for Offline Flyback Converters Using FPS™](#)
- [AN-4141 — Troubleshooting and Design Tips for Fairchild Power Switch \(FPS™\) Flyback Applications](#)
- [AN-4147 — Design Guidelines for RCD Snubber of Flyback](#)
- [AN-4150 — Design Guidelines for Flyback Converters Using FSQ-Series Fairchild Power Switch \(FPS™\)](#)

Description

The FSL206MR integrated Pulse-Width Modulator (PWM) and SenseFET is specifically designed for high-performance offline Switched-Mode Power Supplies (SMPS) while minimizing external components. This device integrates high-voltage power regulators that combine an avalanche-rugged SenseFET with a Current-Mode PWM control block.

The integrated PWM controller includes: a 7.8V regulator, eliminating the need for auxiliary bias winding; Under-Voltage Lockout (UVLO) protection; Leading-Edge Blanking (LEB); an optimized gate turn-on/turn-off driver; EMI attenuator; Thermal Shutdown (TSD) protection; temperature-compensated precision current sources for loop compensation; soft-start during startup; and fault-protection circuitry such as Overload Protection (OLP), Over-Voltage Protection (OVP), Abnormal Over-Current Protection (AOCP), and Line Under-Voltage Protection (LUVF).

The internal high-voltage startup switch and the Burst-Mode operation with very low operating current reduce the power loss in Standby Mode. As a result, it is possible to reach a power loss of 150mW with no bias winding and 25mW (for FSL206MR) or 30mW (for FSL206MRBN) with a bias winding under no-load conditions when the input voltage is 265V_{AC}.

Pin Configuration

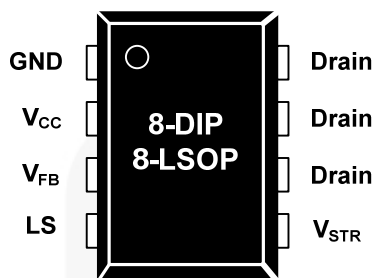


Figure 3. Pin Configuration

Pin Definitions

Pin #	Name	Description
1	GND	Ground. SenseFET source terminal on primary side and internal control ground.
2	V _{CC}	Positive Supply Voltage Input. Although connected to an auxiliary transformer winding, current is supplied from pin 5 (V _{STR}) via an internal switch during startup (see <i>Internal Block Diagram</i> section). It is not until V _{CC} reaches the UVLO upper threshold (8V) that the internal startup switch opens and device power is supplied via the auxiliary transformer winding.
3	V _{FB}	Feedback Voltage. Non-inverting input to the PWM comparator, with a 0.11mA current source connected internally and a capacitor and opto-coupler typically connected externally. There is a delay while charging external capacitor C _{FB} from 2.4V to 5V using an internal 2.7μA current source. This delay prevents false triggering under transient conditions, but allows the protection mechanism to operate under true overload conditions.
4	LS	Line Sense Pin. This pin is used to protect the device when the input voltage is lower than the rated input voltage range. If this pin is not used, connect to ground.
5	V _{STR}	Startup. Connected to the rectified AC line voltage source. At startup, the internal switch supplies internal bias and charges an external storage capacitor placed between the V _{CC} pin and ground. Once V _{CC} reaches 8V, all internal blocks are activated. After that, the internal high-voltage regulator (HV REG) turns on and off irregularly to maintain V _{CC} at 7.8V.
6, 7, 8	Drain	Drain. Designed to connect directly to the primary lead of the transformer and capable of switching a maximum of 650V. Minimizing the length of the trace connecting these pins to the transformer decreases leakage inductance.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. $T_A = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
V_{STR}	V_{STR} Pin Voltage	-0.3	650.0	V
V_{DS}	Drain Pin Voltage	-0.3	650.0	V
V_{CC}	Supply Voltage		26	V
V_{LS}	LS Pin Voltage	-0.3	Internally Clamped Voltage ⁽⁴⁾	V
V_{FB}	Feedback Voltage Range	-0.3	Internally Clamped Voltage ⁽⁴⁾	V
I_{DM}	Drain Current Pulsed ⁽⁵⁾		1.5	A
E_{AS}	Single-Pulsed Avalanche Energy ⁽⁶⁾		11	mJ
P_D	Total Power Dissipation		1.3	W
T_J	Operating Junction Temperature	-40	+150	$^\circ\text{C}$
T_A	Operating Ambient Temperature	-40	+125	$^\circ\text{C}$
T_{STG}	Storage Temperature	-55	+150	$^\circ\text{C}$
ESD	Human Body Model, JESD22-A114		4	KV
	Charged Device Model, JESD22-C101		2	

Notes:

- V_{FB} is clamped by internal clamping diode ($13\text{V } I_{CLAMP_MAX} < 100\mu\text{A}$). After shutdown, before V_{CC} reaching V_{STOP} , $V_{SD} < V_{FB} < V_{CC}$.
- Repetitive rating; pulse-width limited by maximum junction temperature.
- $L=21\text{mH}$, starting $T_J=25^\circ\text{C}$.

Thermal Impedance

$T_A=25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Value	Unit
θ_{JA}	Junction-to-Ambient Thermal Impedance ⁽⁷⁾	93	$^\circ\text{C/W}$

Notes:

- JEDEC recommended environment, JESD51-2 and test board, JESD51-10 with minimum land pattern for 8DIP and JESD51-3 with minimum land pattern for 8LSOP.

Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit	
SenseFET Section							
BV _{DSS}	Drain-Source Breakdown Voltage	V _{CC} = 0V, I _D = 250μA	650			V	
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 650V, V _{GS} = 0V			50	μA	
		V _{DS} = 520V, V _{GS} = 0V, T _A = 125°C ⁽⁸⁾			250	μA	
R _{DS(ON)}	Drain-Source On-State Resistance ⁽⁹⁾	V _{GS} = 10V, I _D = 0.3A		14	19	Ω	
C _{iSS}	Input Capacitances	V _{GS} = 0V, V _{DS} = 25V, f = 1MHz		162		pF	
C _{oSS}	Output Capacitance	V _{GS} = 0V, V _{DS} = 25V, f = 1MHz		14.9		pF	
C _{rSS}	Reverse Transfer Capacitance	V _{GS} = 0V, V _{DS} = 25V, f = 1MHz		2.7		pF	
t _r	Rise Time	V _{DS} = 325V, I _D = 0.5A, R _G = 25Ω		6.1		ns	
t _f	Fall Time	V _{DS} = 325V, I _D = 0.5A, R _G = 25Ω		43.6		ns	
Control Section							
f _{OSC}	Switching Frequency	V _{FB} = 4V, V _{CC} = 10V	61	67	73	KHz	
Δf _{OSC}	Switching Frequency Variation	-25°C < T _J < 85°C		±5	±10	%	
f _M	Frequency Modulation ⁽⁸⁾			±3		KHz	
D _{MAX}	Maximum Duty Cycle	V _{FB} = 4V, V _{CC} = 10V	66	72	78	%	
D _{MIN}	Minimum Duty Cycle	V _{FB} = 0V, V _{CC} = 10V	0	0	0	%	
V _{START}	UVLO Threshold Voltage	V _{FB} = 0V, V _{CC} Sweep	7	8	9	V	
V _{STOP}		After Turn On	6	7	8	V	
I _{FB}	Feedback Source Current	V _{FB} = 0V, V _{CC} = 10V	90	110	130	μA	
t _{S/S}	Internal Soft-Start Time	V _{FB} = 4V, V _{CC} = 10V	10	15	20	ms	
Burst Mode Section							
V _{BURH}	Burst-Mode HIGH Threshold Voltage	V _{CC} = 10V, V _{FB} Increase	FSL206MR	0.66	0.83	1.00	V
			FSL206MRB	0.40	0.50	0.60	V
V _{BURL}	Burst-Mode LOW Threshold Voltage	V _{CC} = 10V, V _{FB} Decrease	FSL206MR	0.59	0.74	0.89	V
			FSL206MRB	0.28	0.35	0.42	V
HYS _{BUR}	Burst-Mode Hysteresis		FSL206MR		90		mV
			FSL206MRB		150		mV
Protection Section							
I _{LIM}	Peak Current Limit	V _{FB} = 4V, di/dt = 300mA/μs, V _{CC} = 10V	0.54	0.60	0.66	A	
t _{CLD}	Current Limit Delay ⁽⁸⁾			100		ns	
V _{SD}	Shutdown Feedback Voltage	V _{CC} = 10V	4.5	5.0	5.5	V	
I _{DELAY}	Shutdown Delay Current	V _{FB} = 4V	2.1	2.7	3.3	μA	
t _{LEB}	Leading-Edge Blanking Time ⁽⁸⁾		250			ns	
V _{AOCP}	Abnormal Over-Current Protection ⁽⁸⁾			0.7		V	
V _{OVP}	Over-Voltage Protection	V _{FB} = 4V, V _{CC} Increase	23.0	24.5	26.0	V	
V _{LS_OFF}	Line-Sense Protection On to Off	V _{FB} = 3V, V _{CC} = 10V, V _{LS} Decrease	1.9	2.0	2.1	V	
V _{LS_ON}	Line-Sense Protection Off to On	V _{FB} = 3V, V _{CC} = 10V, V _{LS} Increase	1.4	1.5	1.6	V	
TSD	Thermal Shutdown Temperature ⁽⁸⁾		125	135	150	°C	
HYS _{TSD}	TSD Hysteresis Temperature ⁽⁸⁾			60		°C	

Continued on the following page...

Electrical Characteristics (Continued) $T_A = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
High Voltage Regulator Section						
V_{HVR}	HV Regulator Voltage	$V_{FB} = 0V, V_{STR} = 40V$		7.8		V
Total Device Section						
I_{OP1}	Operating Supply Current (Control Part Only, without Switching)	$V_{CC} = 15V, 0V < V_{FB} < V_{BURL}$		0.3	0.5	mA
I_{OP2}	Operating Supply Current (Control Part Only, without Switching)	$V_{CC} = 8V, 0V < V_{FB} < V_{BURL}$		0.25	0.45	mA
I_{OP3}	Operating Supply Current ⁽⁸⁾ (While Switching)	$V_{CC} = 15V, V_{BURL} < V_{FB} < V_{SD}$			1.3	mA
I_{CH}	Startup Charging Current	$V_{CC} = 0V, V_{STR} > 40V$	1.6	1.9	2.2	mA
I_{START}	Startup Current	$V_{CC} = \text{Before } V_{START}, V_{FB} = 0V$		100	150	μA
V_{STR}	Minimum V_{STR} Supply Voltage	$V_{CC} = V_{FB} = 0V, V_{STR}$ Increase		26		V

Notes:

8. Though guaranteed by design, not 100% tested in production.
 9. Pulse test: pulse width=300ms, duty cycle=2%.

Typical Performance Characteristics

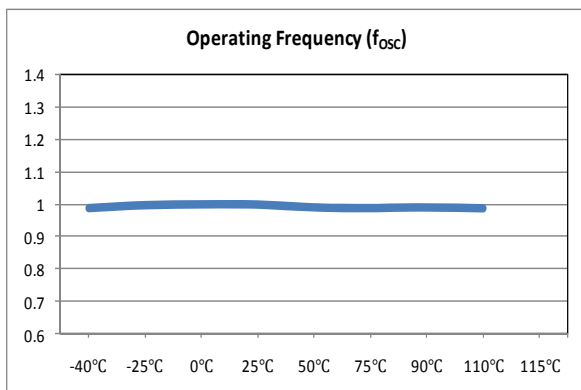


Figure 4. Operating Frequency vs. Temperature

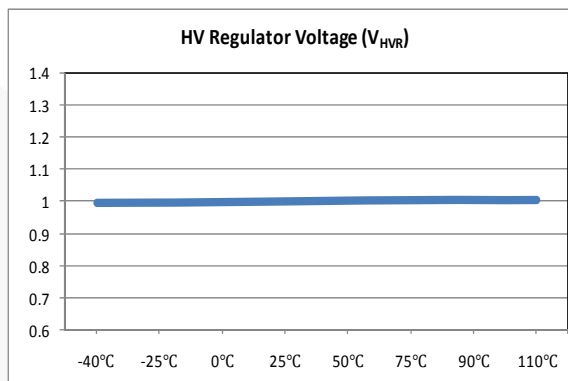


Figure 5. HV Regulator Voltage vs. Temperature

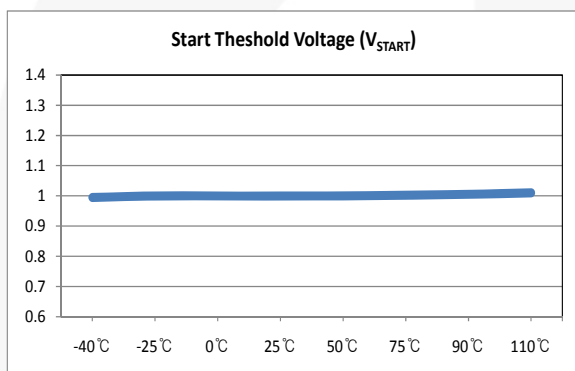


Figure 6. Start Threshold Voltage vs. Temperature

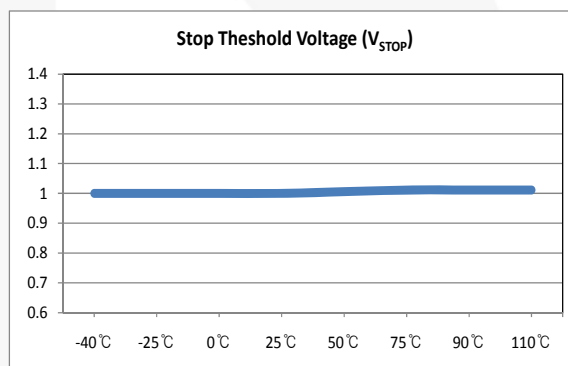


Figure 7. Stop Threshold Voltage vs. Temperature

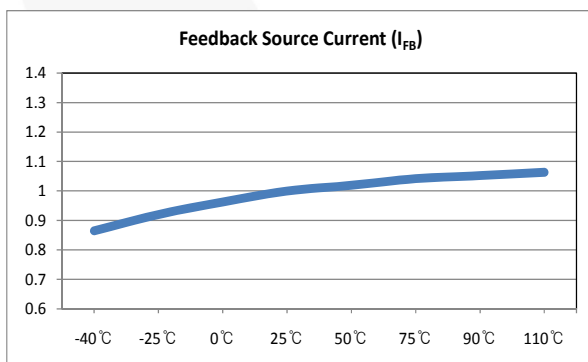


Figure 8. Feedback Source Current vs. Temperature

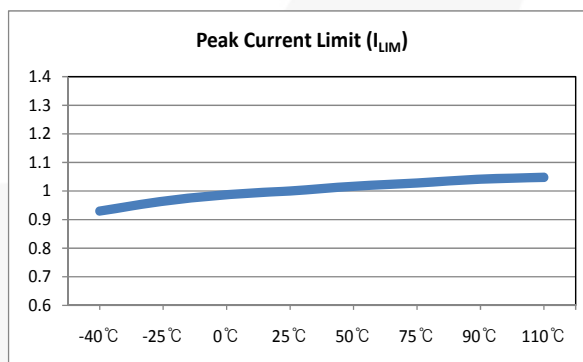


Figure 9. Peak Current Limit vs. Temperature

Typical Performance Characteristics (Continued)

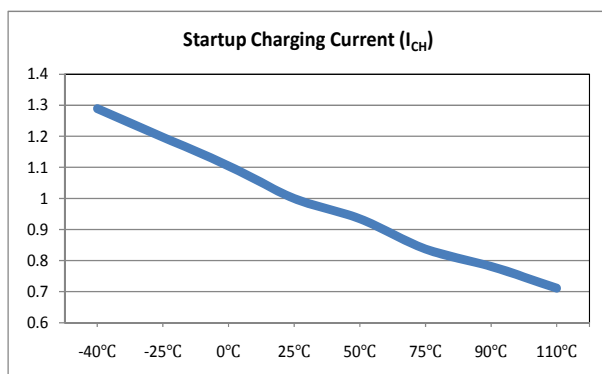


Figure 10. Startup Charging Current vs. Temperature

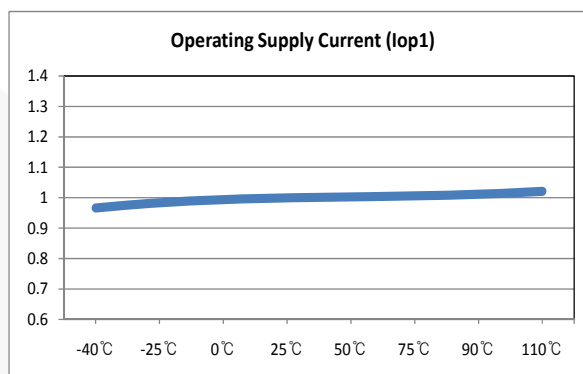


Figure 11. Operating Supply Current 1 vs. Temperature

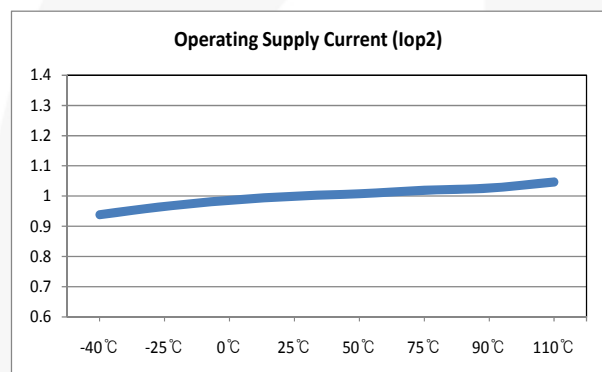


Figure 12. Operating Supply Current 2 vs. Temperature

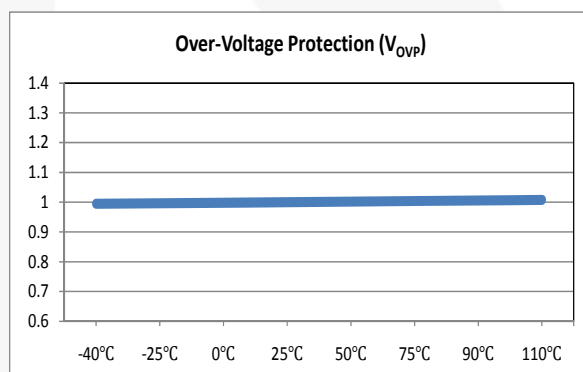


Figure 13. Over-Voltage Protection Voltage vs. Temperature

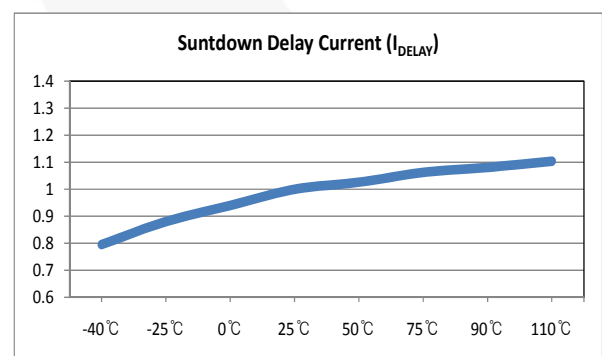


Figure 14. Shutdown Delay Current vs. Temperature

Functional Description

Startup

At startup, an internal high-voltage current source supplies the internal bias and charges the external capacitor (C_A) connected to the V_{CC} pin, as illustrated in Figure 15. An internal high-voltage regulator (HV REG) located between the V_{STR} and V_{CC} pins regulates the V_{CC} to 7.8V and supplies operating current. Therefore, FSL206MR needs no auxiliary bias winding.

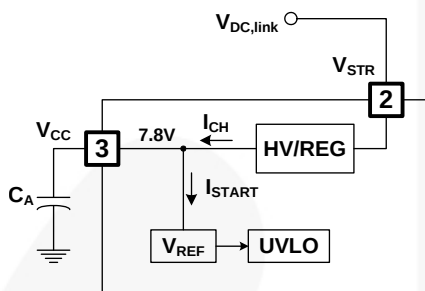


Figure 15. Startup Block

Oscillator Block

The oscillator frequency is set internally and the FPS™ has a random frequency fluctuation function.

Fluctuation of the switching frequency can reduce EMI by spreading the energy over a wider frequency range than the bandwidth measured by the EMI test equipment. The amount of EMI reduction is directly related to the range of the frequency variation. The range of frequency variation is fixed internally; however, its selection is randomly chosen by the combination of an external feedback voltage and internal free-running oscillator. This randomly chosen switching frequency effectively spreads the EMI noise near switching frequency and allows the use of a cost-effective inductor instead of an AC input line filter to satisfy world-wide EMI requirements.

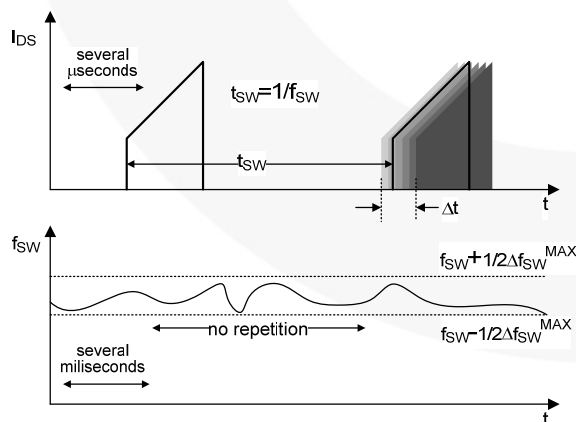


Figure 16. Frequency Fluctuation Waveform

Feedback Control

FSL206MR employs Current-Mode control, as shown in Figure 17. An opto-coupler (such as the FOD817A) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the R_{SENSE} resistor makes it possible to control the switching duty cycle. When the shunt regulator reference pin voltage exceeds the internal reference voltage of 2.5V; the opto-coupler LED current increases, feedback voltage V_{FB} is pulled down, and the duty cycle is reduced. This typically occurs when input voltage is increased or output load is decreased.

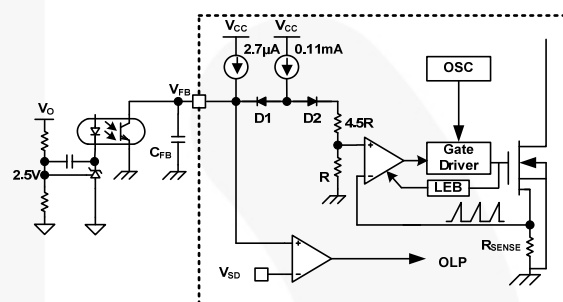


Figure 17. Pulse-Width-Modulation (PWM) Circuit

Leading-Edge Blanking (LEB)

At the instant the internal SenseFET is turned on, the primary-side capacitance and secondary-side rectifier diode reverse recovery typically cause a high-current spike through the SenseFET. Excessive voltage across the R_{SENSE} resistor leads to incorrect feedback operation in the Current-Mode PWM control. To counter this effect, the FPS employs a leading-edge blanking (LEB) circuit (see Figure 17). This circuit inhibits the PWM comparator for a short time (t_{LEB}) after the SenseFET is turned on.

Protection Circuits

The protective functions include Overload Protection (OLP), Over-Voltage Protection (OVP), Under-Voltage Lockout (UVLO), Line Under-Voltage Protection (LUV), Abnormal Over-Current Protection (AOCP), and thermal shutdown (TSD). Because these protection circuits are fully integrated inside the IC without external components, reliability is improved without increasing cost. Once a fault condition occurs, switching is terminated and the SenseFET remains off. This causes V_{CC} to fall. When V_{CC} reaches the UVLO stop voltage V_{STOP} (7V), the protection is reset and the internal high-voltage current source charges the V_{CC} capacitor via the V_{STR} pin. When V_{CC} reaches the UVLO start voltage V_{START} (8V), the FPS resumes normal operation. In this manner, auto-restart can alternately enable and disable the switching of the power SenseFET until the fault condition is eliminated.

Line Under-Voltage Protection (LUVP)

If the input voltage of the converter is lower than the minimum operating voltage, the converter input current increases too much, causing components failure. If the input voltage is low, the converter should be protected. In the FSL206MR, the LUVP circuit senses the input voltage using the LS pin and, if this voltage is lower than 1.5V, the LUVP signal is generated. The comparator has 0.5V hysteresis. If the LUVP signal is generated, the output drive block is shut down and the output voltage feedback loop is saturated.

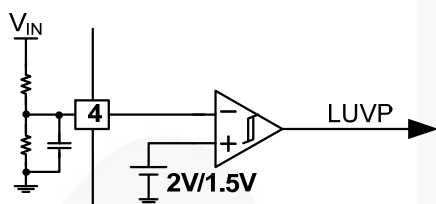


Figure 21. Line UVP Circuit

Soft-Start

The FSL206MR has an internal soft-start circuit that slowly increases the feedback voltage, together with the SenseFET current, after it starts. The typical soft-start time is 15ms, as shown in Figure 22, where progressive increments of the SenseFET current are allowed during the startup phase. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. It also helps prevent transformer saturation and reduce the stress on the secondary diode.

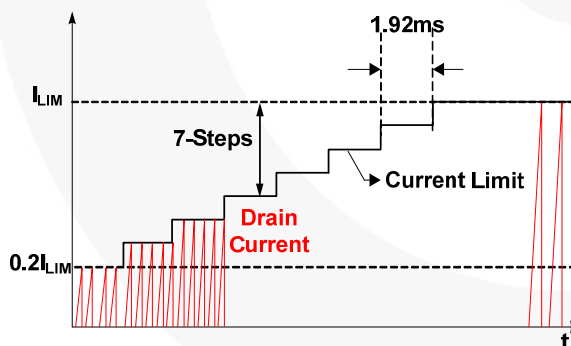


Figure 22. Internal Soft-Start

Burst Operation

To minimize power dissipation in Standby Mode, the FPS enters Burst Mode. As the load decreases, the feedback voltage decreases. As shown in Figure 23, the device automatically enters Burst Mode when the feedback voltage drops below V_{BURH} . Switching continues until the feedback voltage drops below V_{BURL} . At this point, switching stops and the output voltages start to drop at a rate dependent on the standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH} , switching resumes. The feedback voltage then falls and the process repeats. Burst Mode alternately enables and disables switching of the SenseFET and reduces switching loss in Standby Mode.

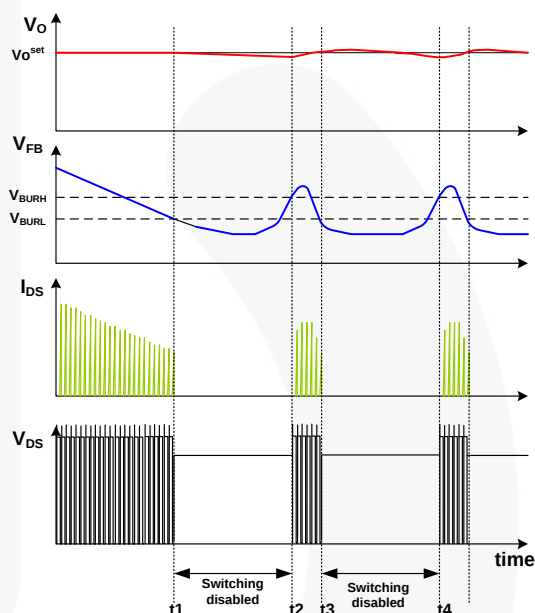
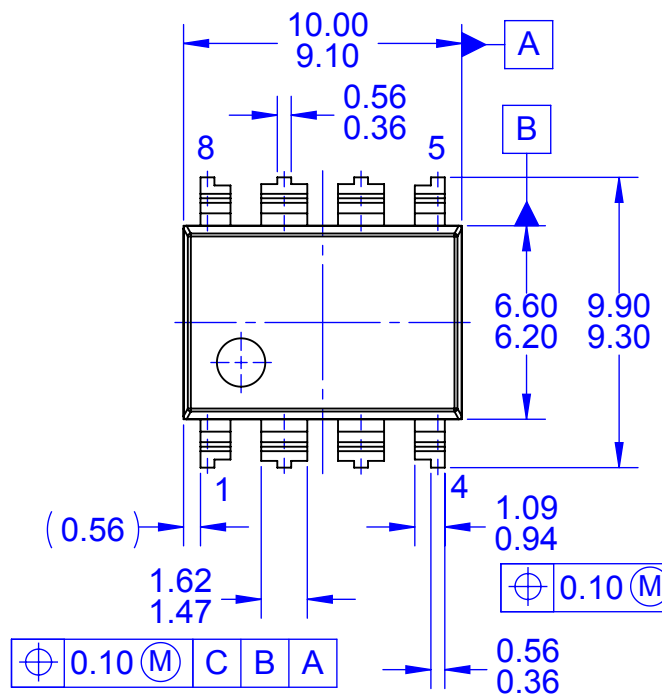
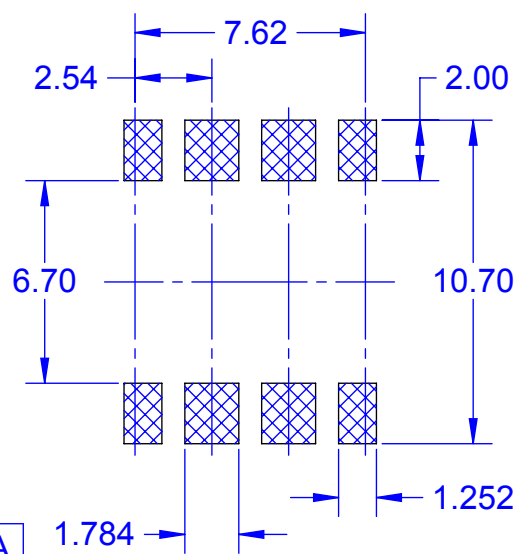


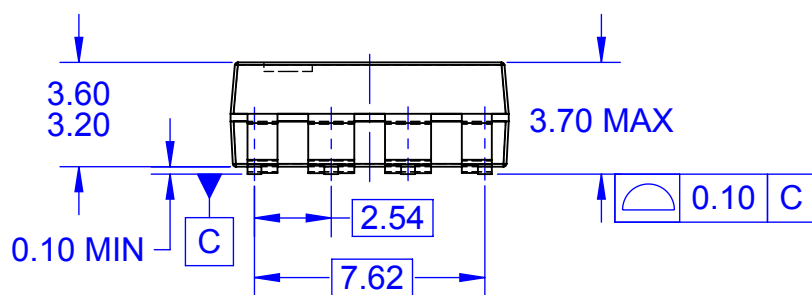
Figure 23. Burst-Mode Operation



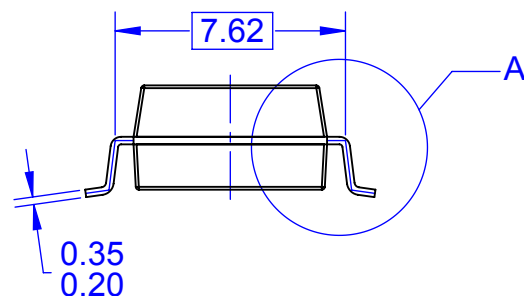
TOP VIEW



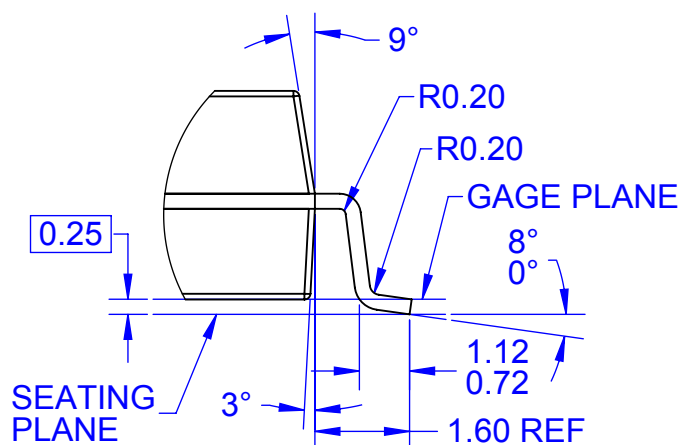
LAND PATTERN RECOMMENDATION



FRONT VIEW



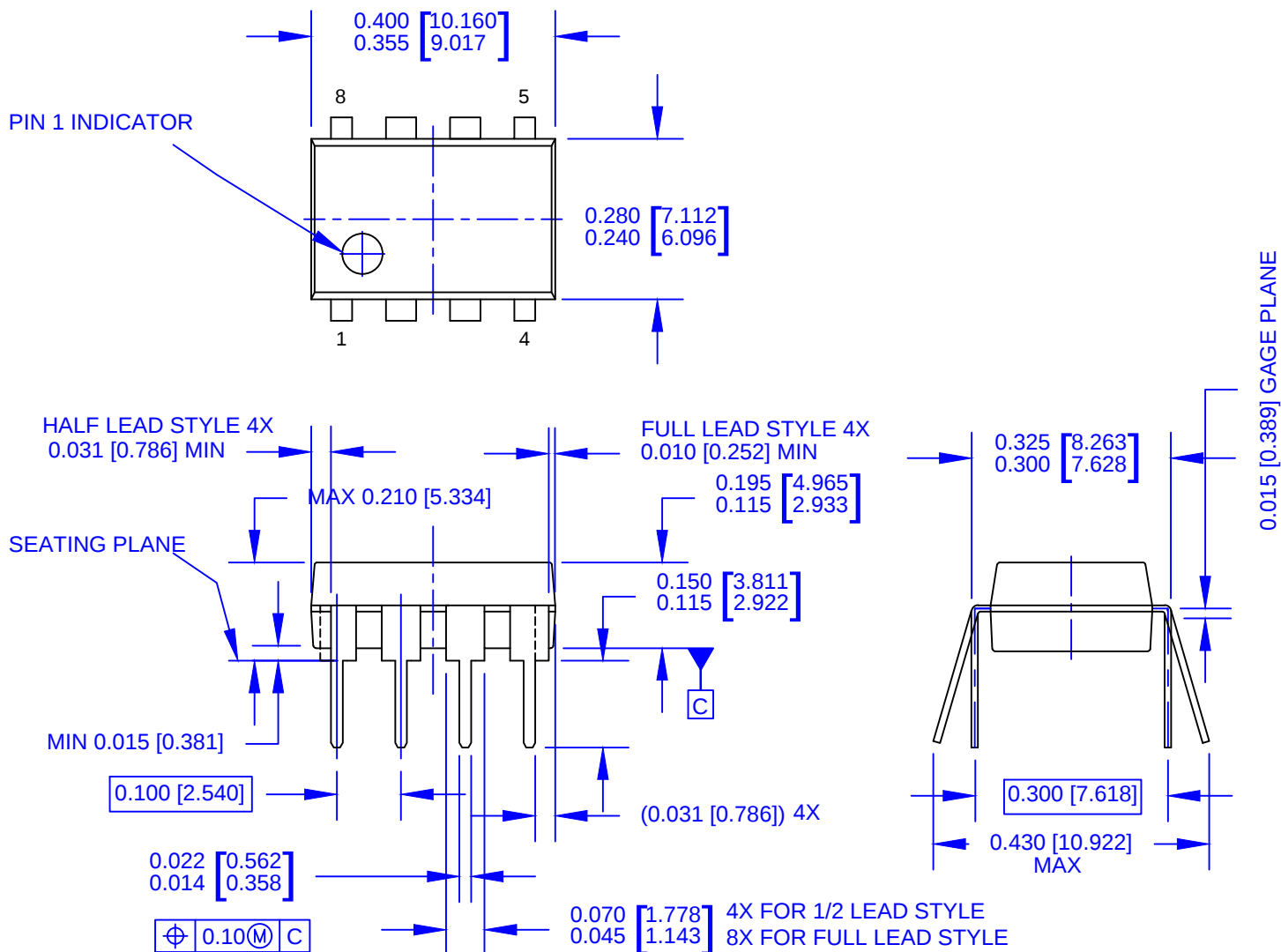
SIDE VIEW



DETAIL A
SCALE 2:1

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 - B. ALL DIMENSIONS ARE IN MILLIMETERS
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
 - D. DIMENSIONS AND TOLERANCES PER ASME Y14.5M-2009
 - E. DRAWING FILENAME: MKT-MLSOP08Arev2

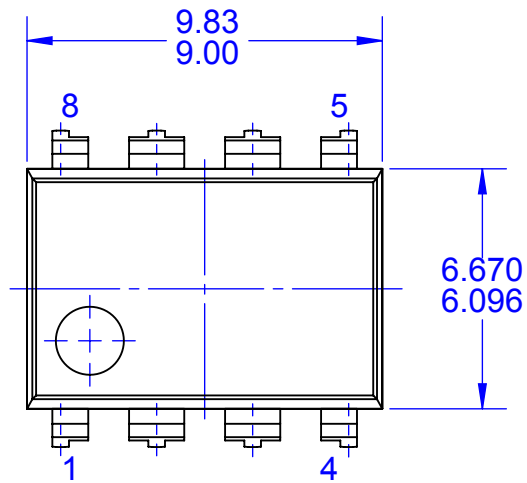




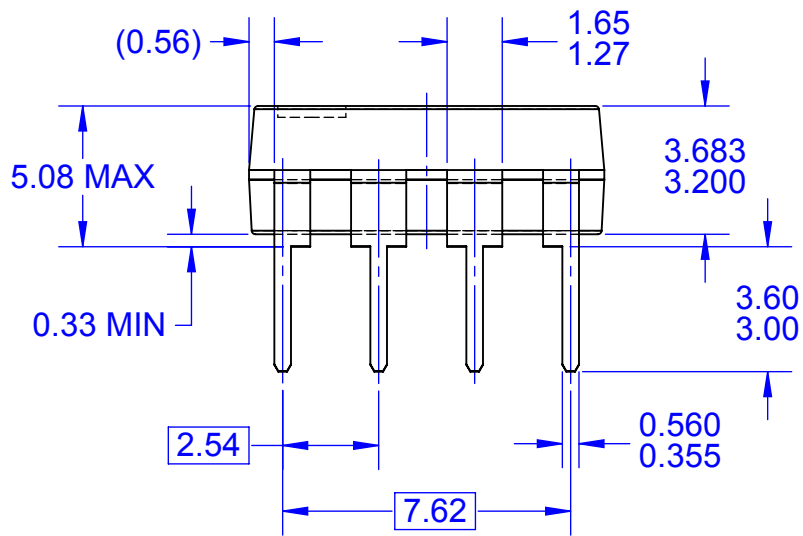
NOTES:

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- DIMENSIONS AND TOLERANCES PER ASME Y14.5M-2009
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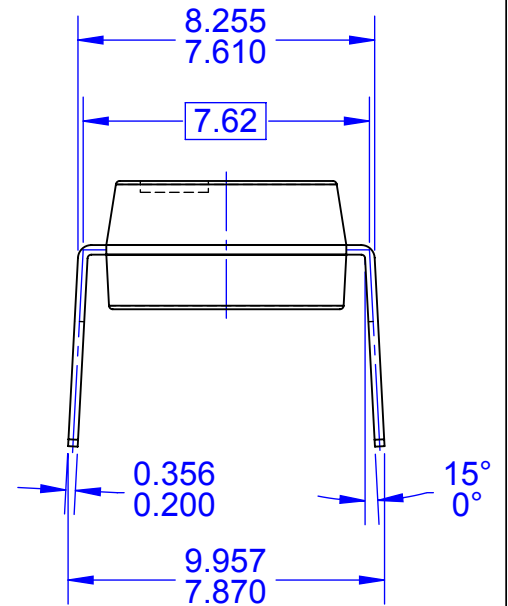




TOP VIEW



FRONT VIEW



SIDE VIEW

NOTES:

- CONFORMS TO JEDEC MS-001, VARIATION BA
- ALL DIMENSIONS ARE IN MILLIMETERS
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- DIMENSIONS AND TOLERANCES PER ASME Y14.5M-2009
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