CHAPTER 14
ELECTRICAL SPECIFICATIONS

14.1. ABSOLUTE MAXIMUM RATINGS

Table 14-1 provides environmental stress ratings for the chip set components. Functional operation at the absolute maximum and minimum is not implied or guaranteed. Extended exposure to maximum ratings may affect device reliability. Further, precautions should be taken to avoid high static voltages and electric fields to prevent static electric discharge.

Table 14-1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
	Storage Temperature	-65	150	°C	
	Case Temperature Under Bias	-65	110	°C	
V_{CC3}	3 V Supply Voltage with respect to V_{SS}	-0.5	4.6	V	
V_{CC5}	5 V Supply Voltage with respect to V_{SS}	-0.5	6.5	V	
V_{IN5}	5V Buffer DC Input Voltage	-0.5	$V_{CC}5$+0.5 not to exceed $V_{CC}5$-MAX	V	(1) (4)
V_{IN3}	3V Only Buffer DC Input Voltage	-0.5	$V_{CC}3$+0.5 not to exceed V_{CC3}-MAX	V	(2) (4)
V_{INSB}	5V Safe Buffer DC Input Voltage	-0.5	$V_{CC}5$+0.3 not to exceed 5.55	V	(3) (4)

NOTES:

1. Applies to 82497 Cache Controller and 82492 Cache SRAM inputs.
2. Applies to Pentium® processor (735\90, 815\100, 1000\120, 1110\133) inputs associated with Table 14-2.
3. Applies to Pentium processor (735\90, 815\100, 1000\120, 1110\133) CLK and PICCLK inputs.
4. See overshoot/undershoot transient spec.

14.2. DC SPECIFICATIONS

The DC specifications that follow refer only to the external interface. The external interface connects to 5V buffers (all 82497 Cache Controller and 82492 Cache SRAM signals), 5VT buffers (Pentium processor (735\90, 815\100, 1000\120, 1110\133) CLK and PICCLK inputs), and 3.3V buffers (all other Pentium processor (735\90, 815\100, 1000\120, 1110\133) signals).

Both the 82497 Cache Controller and 82492 Cache SRAM require a 3.3V and 5V supply. The 82497 Cache Controller and 82492 Cache SRAM are 5V components and require 3.3V supplies to bias their address and data bus buffers to the Pentium processor (735\90, 815\100, 1000\120, 1110\133).

The 82497 Cache Controller and 82492 Cache SRAM are 5V parts internally, with some 3.3V I/O signals. The Pentium processor (735\90, 815\100, 1000\120, 1110\133) is a 3.3V part internally, with 3.3V I/O. However, the Pentium processor (735\90, 815\100, 1000\120, 1110\133) CLK and PICCLK inputs are 5V-tolerant. Since the 3.3V (5V-tolerant) input levels defined in Table 14-2 are the same as the 5V TTL levels, the CLK and PICCLK inputs are compatible with existing clock drivers.

Table 14-2. 3.3V DC Specifications

T_{CASE} = 0 to 85°C $V_{CC}3$ = 3.135-3.6V					
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Notes**
V_{IL3}	Input Low Voltage	-0.3	0.8	V	TTL Level (3)
V_{IH3}	Input High Voltage	2.0	$V_{CC}3$+0.3	V	TTL Level (3)
V_{OL3}	Output Low Voltage		0.4 0.2	V	TTL Level (1) (3) CMOS Level (4)
V_{OH3}	Output High Voltage	2.4 $V_{CC}3$-0.2		V	TTL Level (2) (3) CMOS Level (4)
$I_{CC}3$	Power Supply Current		80 40		82497 3.3 V I/O only 82492 3.3 V I/O only

NOTES:

1. Parameter measured at 4 mA.
2. Parameter measured at 2 mA.
3. 3.3V TTL levels apply to the signals between the Pentium® processor and the Memory Bus Controller or Memory Bus, with the exception of CLK and PICCLK.
4. Parameter guaranteed by design at 100 uA. 3.3V CMOS output levels apply to all signals included in Note 3.

Table 14-3. 3.3V (5-V Tolerant) DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
$V_{IL}3$	Input Low Voltage	-0.3	0.8	V	TTL Level (1)
$V_{IH}3$	Input High Voltage	2.0	$V_{CC}5$+0.3	V	TTL Level (1)

NOTES:

1. 3.3V (5V-tolerant) TTL levels apply to the Pentium® processor (735\90, 815\100, 1000\120, 1110\133) signals CLK and PICCLK.

Table 14-4. 5V DC Specifications

T_{CASE} = 0 to 85°C V_{CC} = 4.75V – 5.25V					
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Notes**
$V_{IL}5$	Input Low Voltage	-0.3	0.8	V	TTL Level (3)
$V_{IH}5$	Input High Voltage	2.0	V_{CC5}+0.3	V	TTL Level (3)
$V_{OL}5$	Output Low Voltage		0.45	V	TTL Level (1) (3)
$V_{OH}5$	Output High Voltage	2.4		V	TTL Level (2) (3)
$I_{CC}5$	Power Supply Current		900 400	mA	82497 @ 66 MHz (5) 82492 @ 66 MHz (6)

NOTES:

1. Parameter measured at 4 mA load. For MCFA[6-0], MSET[10-0], MTAG[11-0] this parameter is measured at 12 mA load.
2. Parameter measured at 1 mA load. For MCFA[6-0], MSET[10-0], MTAG[11-0] this parameter is measured at 2 mA load.
3. 5V TTL levels apply to the signals between the 82497/82492 and the Memory Bus Controller or Memory Bus.
4. This parameter may be lower.
5. Typical 82497 $I_{CC}5$ is 800 mA. 800mA is the worst case $I_{CC}5$ value which corresponds to a mixture of test patterns.
6. 82492 $I_{CC}5$ may be considerably less depending on cycle mix. For example idle clocks only require approximately 75 mA. Typical 82492 $I_{CC}5$ is 250 mA, assuming a typical cycle mix of: 50% Read Hit - MRU Hit Burst = 4, 20% Write Hit Burst, 30% idle.

Table 14-5. Input and Output Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
C_{IN}	Input Capacitance		15	pF	(4)
C_O	Output Capacitance		20	pF	(4)
$C_{I/O}$	I/O Capacitance		25	pF	(4)
C_{CLK}	CLK Input Capacitance		15	pF	(4)
C_{TIN}	Test Input Capacitance		15	pF	(4)
C_{TOUT}	Test Output Capacitance		20	pF	(4)
C_{TCK}	Test Clock Capacitance		15	pF	(4)
I_{LI}	Input Leakage Current		±15	uA	$0 < V_{IN} < V_{CC}$ (1)
I_{LO}	Output Leakage Current		±15	uA	$0 < V_{IN} < V_{CC}$ (1)
I_{IL}	Input Leakage Current		200 –400	uA uA	V_{IN} = 0.4V (2) V_{IN} = 2.4V (3)

NOTES:

1. This parameter is for input without pull-up or pull-down.
2. This parameter is for input with pull-up.
3. This parameter is for input with pull-down.
4. Guaranteed by design.

14.3. AC SPECIFICATIONS

The AC specifications consist of two sections, Optimized and External Interface specifications.

14.3.1. Optimized Interface

The optimized interface is the high-performance interconnect between the Pentium processor (735\90, 815\100, 1000\120, 1110\133), 82497 cache controller and 82492 Cache SRAM. This interface is tuned for the known configuration options of the chip set and includes specially designed (non-standard) input and output buffers optimized for the electrical environment of each signal path. To access these buffers you must assert specific configuration pins during reset, namely **BUSCHK#** (Pentium processor (735\90, 815\100, 1000\120, 1110\133)) and **CLDRV** (82497 Cache Controller).

The layout of a Chip Set system should be very similar to the layout of a Pentium processor/82496 Cache Controller/82491 Cache SRAM layout. The 3.3V buffers of the Pentium processor (735\90, 815\100, 1000\120, 1110\133) chip set behave almost identically to the 5V buffers of the Pentium processor. Note, however, that the byte enable (BE0#-BE3#) pins of a Pentium processor (735\90, 815\100, 1000\120, 1110\133) layout must

accommodate a larger load because the byte enable pins are used to sample the Pentium processor's (735\90, 815\100, 1000\120, 1110\133) APIC ID at reset.

The specification of this interface is also non-standard, and includes specifications for:

- Flight Times, and
- Signal Quality

The specifications that follow define the requirements of each path in the optimized interface. As outlined in Table 14-6, there are three classes of specifications: flight time to guarantee signal timing; signal quality to guarantee reliable operation; and, buffer models to simulate flight time and signal quality.

Table 14-6. Three Specification Classes

Specification Class	Purpose	Parameters
Flight Time	Guarantee Timing	Maximum Flight Time Minimum Flight Time Maximum Settling Time Recommendation
Signal Quality	Guarantee Reliable Operation	Absolute Maximum Signal Overshoot (Undershoot) Maximum Group Average Overshoot (Undershoot) Maximum Time Beyond the Supply Maximum Signal Ring-back
Buffer Models	Completely Specify Flight Time and Signal Quality	Cin - Input Capacitance Lp - Package Inductance Cp - Package Capacitance dV/dt - Voltage source rate of change Ro - Output impedance Co - Output Capacitance

14.3.1.1. FLIGHT TIME SPECIFICATION

The chip set uses two V_{CC} supplies: $V_{CC}3$ and $V_{CC}5$. When measuring flight times, use the following V_{CC} references:

Drivers	Vcc Reference	Receivers	Vcc Reference
CPU-CRAM CPU-CACHE CPU-CCTL	$V_{CC}3$	CPU-CRAM CPU-CACHE CPU-CCTL	$V_{CC}3$
CPU-CCTL5T	$V_{CC}5$	CPU-CCTL5T	$V_{CC}3$
CCTL-CRAM	$V_{CC}5$	CCTL-CRAM	$V_{CC}5$

Table 14-7 describes the maximum flight time and clock skew specifications. Tables 14-8 to 14-17 list the flight time and maximum clock skew specifications for each driver-receiver network in the optimized interface. For each net, the driver first order output buffer model type and receiver input buffer model type are also listed. Some signals have **two buffer types** listed in the "Driver Buffer Type" column. These are the signals whose buffer type is

selected using **BUSCHK#** (Pentium processor (735\90, 815\100, 1000\120, 1110\133)) and **CLDRV** (82497 Cache Controller). The first entry corresponds to driving these configuration signals HIGH during reset and the second to driving them LOW. The largest buffers available are not always the best selection since you must look at both flight time and signal quality when doing high speed timing analysis.

Table 14-7. Flight Time and Clock Skew Descriptions

Parameter	Description
Flight Time	Time delay for a signal to reach the receiving component referenced from the driving component's pin, when the driver is unloaded. It includes the time to traverse the PC board trace and any added output delay on the output buffer due to the trace and receiving component loading and is dependent on rise time at the receiving component. Must meet maximum and minimum specifications.
Maximum Clock Skew	Maximum clock skew is the difference in time of the clock signal arriving at different components. It is measured at 0.8V, 1.5V, and 2.0V.

14.3.1.1.1. 60-MHz Flight Times

Tables 14-8 to 14-12 list the flight time and clock skew specifications for the 60-MHz chip set.

These tables list both 256K chip set and 512K chip set connections. Where different connections are required, italicized print indicates 256K chip set connections.

Table 14-8. Signal Group: CPU to Cache RAM (CPU-CRAM)

Driver	Receiver	Max CLK Skew 60 MHz (ns)	Min Flight Time 60 MHz (ns)	Max Flight Time 60 MHz (ns)	Driver Buffer Type	Receiver Buffer Type
PP D0-D63	82492 CDATA0-3 82492 CDATA0-7	0.8	0.7	2.7	ZD2	ZR10
PP DP0-7	82492 CDATA0-3	0.8	0.7	2.7	ZD2	ZR10
82492 CDATA0-3 82492 CDATA0-7	PP D0-D63	0.8	0.7	2.4	ZD10	ZR4
82492 CDATA0-3	PP DP0-7	0.8	0.7	2.4	ZD10	ZR4

NOTE:

PP = Pentium® processor (735\90, 815\100, 1000\120, 1110\133)

Table 14-9. Signal Group: CPU to Cache (CPU-Cache)

Driver	Receiver	Max CLK Skew 60 MHz (ns)	Min Flight Time 60 MHz (ns)	Max Flight Time 60 MHz (ns)	Driver Buffer Type	Receiver Buffer Type
PP A3-A4	82497 CFA0-1	0.3	0.4	3.5	ZD6/ZD6a	ZR8
PP A5-A6 PP A5	82497 CFA5-6 82497 CFA6	0.3	0.4	3.5	ZD6/ZD6a	ZR8
PP A7-A17 PP A6-A16	82497 SET0-10	0.3	0.4	3.5	ZD6/ZD6a	ZR8
PP A3-A17 PP A3-A16	82492 A1-A15 82492 A2-A15	0.8	0.4	3.5	ZD6/ZD6a	ZR9
82497 CFA0-1	PP A3-A4	0.3	0.4	12.5	ZD7	ZR6
82497 CFA5-6 82497 CFA6	PP A5-A6 PP A5	0.3	0.4	12.5	ZD7	ZR6
82497 SET0-10	PP A7-A17 PP A6-A16	0.3	0.4	12.5	ZD7	ZR6
82497 CFA0-1	82492 A1-A2 82492 A2-A3	0.8	0.4	12.5	ZD7	ZR9
82497 CFA5-6 82497 CFA6	82492 A3-A4 82492 A4	0.8	0.4	12.5	ZD7	ZR9
82497 SET0-10	82492 A5-A15	0.8	0.4	12.5	ZD7	ZR9
PP W/R#	82497 W/R#	0.3	0.4	3.9	ZD5/ZD5a	ZR7
PP W/R#	82492 W/R#	0.8	0.8	3.9	ZD5/ZD5a	ZR9
PP HITM#	82497 HITM#	0.3	0.4	3.9	ZD5/ZD5a	ZR7
PP HITM#	82492 HITM#	0.8	0.6	3.9	ZD5/ZD5a	ZR9
PP ADS#	82492 ADS#	0.8	0.8	3.5	ZD5/ZD5a	ZR9
PP BE0-7#	82492 BE#	0.8	0.45	3.1	ZD1	ZR9
PP BE0-7#	82492 CDATA4-7	0.8	0.45	3.1	ZD1	ZR10

NOTE:

PP = Pentium® processor (735\90, 815\100, 1000\120, 1110\133)

Table 14-10. Signal Group: CPU to Cache Controller (CPU-CCTL)

Driver	Receiver	Max CLK Skew 60 MHz (ns)	Min Flight Time 60 MHz (ns)	Max Flight Time 60 MHz (ns)	Driver Buffer Type	Receiver Buffer Type
PP A18-A21 PP A17-A20	82497 TAG0-3	0.3	0.4	2.2	ZD6/ZD6a	ZR8
PP A22-A29 PP A21-A28	82497 TAG4-11	0.3	0.4	2.2	ZD3	ZR8
PP A30-A31 PP A29-A31	82497 CFA2-3 82497 CFA2-4	0.3	0.4	2.2	ZD3	ZR8
82497 TAG0-3	PP A18-A21 PP A17-A20	0.3	0.4	3.7	ZD7	ZR6
82497 TAG4-11	PP A22-A29 PP A21-A28	0.3	0.4	3.7	ZD7	ZR5
82497 AP	PP AP	0.3	0.4	3.7	ZD7	ZR3
82497 CFA2-3 82497 CFA2-4	PP A30-A31 PP A29-A31	0.3	0.4	3.7	ZD7	ZR5
PP AP	82497 AP	0.3	0.4	2.1	ZD4	ZR8
PP SCYC	82497 SCYC	0.3	0.4	2.1	ZD1	ZR7
PP PWT	82497 PWT	0.3	0.4	2.1	ZD1	ZR7
PP PCD	82497 PCD	0.3	0.4	2.1	ZD1	ZR7
PP M/IO#	82497 M/IO#	0.3	0.4	2.1	ZD1	ZR7
PP D/C#	82497 D/C#	0.3	0.4	1.9	ZD1	ZR7
PP LOCK#	82497 LOCK#	0.3	0.4	2.1	ZD1	ZR7
PP CACHE#	82497 CACHE#	0.3	0.4	2.1	ZD1	ZR7
PP ADSC#	82497 ADS#	0.3	0.4	2.0	ZD1	ZR7a

NOTE:

PP = Pentium® processor (735\90, 815\100, 1000\120, 1110\133)

Table 14-11. Signal Group: CPU to Cache Controller 5V Tolerant (CPU-CCTL5T)

Driver	Receiver	Max CLK Skew 60 MHz (ns)	Min Flight Time 60 MHz (ns)	Max Flight Time 60 MHz (ns)	Driver Buffer Type	Receiver Buffer Type
82497 AHOLD	PP AHOLD	0.3	0.4	2.2	ZD8	ZR1
82497 EADS#	PP EADS#	0.3	0.4	2.2	ZD8	ZR1
82497 KEN#	PP KEN#	0.3	0.4	2.2	ZD8	ZR1
82497 BRDYC1#	PP BRDYC#	0.3	0.4	2.1	ZD8	ZR2
82497 WBWT#	PP WBWT#	0.3	0.4	2.2	ZD8a	ZR1
82497 INV	PP INV	0.3	0.4	2.8	ZD8	ZR1a
82497 NA#	PP NA#	0.3	0.4	2.2	ZD8a	ZR1
82497 EWBE#	PP EWBE#	0.3	0.4	2.2	ZD8	ZR1
82497 BOFF#	PP BOFF#	0.3	0.5	4.3	ZD9/ZD9a	ZR1

NOTE:
PP = Pentium® processor (735\90, 815\100, 1000\120, 1110\133)

Table 14-12. Signal Group: Cache Controller to Cache RAM (CCTL-CRAM)

Driver	Receiver	Max CLK Skew 60 MHz (ns)	Min Flight Time 60 MHz (ns)	Max Flight Time 60 MHz (ns)	Driver Buffer Type	Receiver Buffer Type
82497 BOFF#	82492 BOFF#	0.8	0.5	4.0	ZD9/ZD9a	ZR9
82497 BLAST#	82492 BLAST#	0.8	0.4	3.4	ZD9/ZD9a	ZR9
82497 WRARR#	82492 WRARR#	0.8	0.4	3.4	ZD9/ZD9a	ZR9
82497 WAY	82492 WAY	0.8	0.4	3.4	ZD9/ZD9a	ZR9
82497 MCYC#	82492 MCYC#	0.8	0.4	3.4	ZD9/ZD9a	ZR9
82497 MAWEA#	82492 MAWEA#	0.8	0.4	3.4	ZD9/ZD9a	ZR9
82497 BUS#	82492 BUS#	0.8	0.4	3.4	ZD9/ZD9a	ZR9
82497 WBA	82492 WBA	0.8	0.4	3.4	ZD9/ZD9a	ZR9
82497 WBWE#	82492 WBWE#	0.8	0.4	3.4	ZD9/ZD9a	ZR9
82497 WBTYP	82492 WBTYP	0.8	0.4	3.4	ZD9/ZD9a	ZR9
82497 BRDYC2#	82492 BRDYC#	0.8	0.4	3.4	ZD9/ZD9a	ZR9
82497 BLEC#	82492 BLEC#	0.8	0.4	3.0	ZD9/ZD9a	ZR9

14.3.1.1.2. 66-MHZ Flight Times

Tables 14-13 to 14-17 list the flight time and clock skew specifications for the 66-MHz chip set.

The 66-MHz timings are divided into 256K and 512K timings. Where different connections are required, italicized print indicates 256K chip set connections.

Table 14-13. Signal Group: CPU to Cache RAM (CPU-CRAM)

Driver	Receiver	Max CLK Skew (ns)	Min Flight Time 66 MHz 256K (ns)	Max Flight Time 66 MHz 256K (ns)	Max Flight Time 66 MHz 512K (ns)	Driver Buffer Type	Receiver Buffer Type
PP D0-D63	82492 CDATA0-3 82492 CDATA0-7	0.7	0.7	2.2	2.2	ZD2	ZR10
PP DP0-7	82492 CDATA0-3	0.7	0.7	2.2	2.2	ZD2	ZR10
82492 CDATA0-3 82492 CDATA0-7	PP D0-D63	0.7	0.7	2.2	2.4	ZD10	ZR4
82492 CDATA0-3	PP DP0-7	0.7	0.7	2.2	2.4	ZD10	ZR4

NOTE:

PP = Pentium® processor (735\90, 815\100, 1000\120, 1110\133)

Table 14-14. Signal Group: CPU to Cache (CPU-Cache)

Driver	Receiver	Max CLK Skew (ns)	Min Flight Time 66 MHz 256K (ns)	Max Flight Time 66 MHz 256K (ns)	Max Flight Time 66 MHz 512K (ns)	Driver Buffer Type	Receiver Buffer Type
PP A3-A4	82497 CFA0-1	0.2	0.4	3.0	3.4	ZD6/ZD6a	ZR8
PP A5-A6 PP A5	82497 CFA5-6 82497 CFA6	0.2	0.4	3.0	3.4	ZD6/ZD6a	ZR8
PP A7-A17 PP A6-A16	82497 SET0-10	0.2	0.4	3.0	3.4	ZD6/ZD6a	ZR8
PP A3-A17 PP A3-A16	82492 A1-A15 82492 A2-A15	0.7	0.4	2.8	3.5	ZD6/ZD6a	ZR9
82497 CFA0-1	PP A3-A4	0.2	0.4	10.6	12.5	ZD7	ZR6
82497 CFA5-6 82497 CFA6	PP A5-A6 PP A5	0.2	0.4	10.6	12.5	ZD7	ZR6
82497 SET0-10	PP A7-A17 PP A6-A16	0.2	0.4	10.6	12.5	ZD7	ZR6
82497 CFA0-1	82492 A1-A2 82492 A2-A3	0.7	0.4	10.6	12.5	ZD7	ZR9
82497 CFA5-6 82497 CFA6	82492 A3-A4 82492 A4	0.7	0.4	10.6	12.5	ZD7	ZR9
82497 SET0-10	82492 A5-A15	0.7	0.4	10.6	12.5	ZD7	ZR9
PP W/R#	82497 W/R#	0.2	0.4	3.4	3.8	ZD5/ZD5a	ZR7
PP W/R#	82492 W/R#	0.7	0.7	3.4	3.8	ZD5/ZD5a	ZR9
PP HITM#	82497 HITM#	0.2	0.4	3.4	3.8	ZD5/ZD5a	ZR7
PP HITM#	82492 HITM#	0.7	0.5	3.4	3.8	ZD5/ZD5a	ZR9
PP ADS#	82492 ADS#	0.7	0.7	3.0	3.7	ZD5/ZD5a	ZR9
PP BE0-7#	82492 BE#	0.7	0.4	2.6	2.8	ZD1	ZR9
PP BE0-7#	82492 CDATA4-7	0.7	0.4	2.6	2.8	ZD1	ZR10

NOTE:

PP = Pentium processor (735\90, 815\100)

Table 14-15. Signal Group: CPU to Cache Controller (CPU-CCTL)

Driver	Receiver	Max CLK Skew (ns)	Min Flight Time 66 MHz 256K (ns)	Max Flight Time 66 MHz 256K (ns)	Max Flight Time 66 MHz 512K (ns)	Driver Buffer Type	Receiver Buffer Type
PP A18-A21 PP A17-A20	82497 TAG0-3	0.2	0.4	1.7	1.8	ZD6/ZD6a	ZR8
PP A22-A29 PP A21-A28	82497 TAG4-11	0.2	0.4	1.7	1.8	ZD3	ZR8
PP A30-A31 PP A29-A31	82497 CFA2-3 82497 CFA2-4	0.2	0.4	1.7	1.8	ZD3	ZR8
82497 TAG0-3	PP A18-A21 PP A17-A20	0.2	0.4	3.2	3.2	ZD7	ZR6
82497 TAG4-11	PP A22-A29 PP A21-A28	0.2	0.4	3.2	3.2	ZD7	ZR5
82497 AP	PP AP	0.2	0.4	3.2	3.2	ZD7	ZR3
82497 CFA2-3 82497 CFA2-4	PP A30-A31 PP A29-A31	0.2	0.4	3.2	3.2	ZD7	ZR5
PP AP	82497 AP	0.2	0.4	1.6	1.7	ZD4	ZR8
PP SCYC	82497 SCYC	0.2	0.4	1.6	1.7	ZD1	ZR7
PP PWT	82497 PWT	0.2	0.4	1.6	1.7	ZD1	ZR7
PP PCD	82497 PCD	0.2	0.4	1.6	1.7	ZD1	ZR7
PP M/IO#	82497 M/IO#	0.2	0.4	1.6	1.7	ZD1	ZR7
PP D/C#	82497 D/C#	0.2	0.4	1.4	1.7	ZD1	ZR7
PP LOCK#	82497 LOCK#	0.2	0.4	1.6	1.7	ZD1	ZR7
PP CACHE#	82497 CACHE#	0.2	0.4	1.6	1.7	ZD1	ZR7
PP ADSC#	82497 ADS#	0.2	0.4	1.7	1.7	ZD1	ZR7a

NOTE:

PP = Pentium® processor (735\90, 815\100, 1000\120, 1110\133)

Table 14-16. Signal Group: CPU to Cache Controller 5V Tolerant (CPU-CCTL5T)

Driver	Receiver	Max CLK Skew (ns)	Min Flight Time 66 MHz 256K (ns)	Max Flight Time 66 MHz 256K (ns)	Max Flight Time 66 MHz 512K (ns)	Driver Buffer Type	Receiver Buffer Type
82497 AHOLD	PP AHOLD	0.2	0.4	1.7	1.7	ZD8	ZR1
82497 EADS#	PP EADS#	0.2	0.4	1.7	1.7	ZD8	ZR1
82497 KEN#	PP KEN#	0.2	0.4	1.7	1.7	ZD8	ZR1
82497 BRDYC1#	PP BRDYC#	0.2	0.4	1.7	1.7	ZD8	ZR2
82497 WBWT#	PP WBWT#	0.2	0.4	1.9	1.9	ZD8a	ZR1
82497 INV	PP INV	0.2	0.4	2.3	2.3	ZD8	ZR1a
82497 NA#	PP NA#	0.2	0.4	1.7	1.7	ZD8a	ZR1
82497 EWBE#	PP EWBE#	0.2	0.4	1.7	1.7	ZD8	ZR1
82497 BOFF#	PP BOFF#	0.2	0.4	3.4	3.5	ZD9/ZD9a	ZR1

NOTE:

PP = Pentium® processor (735\90, 815\100, 1000\120, 1110\133)

Table 14-17. Signal Group: Cache Controller to Cache RAM (CCTL-CRAM)

Driver	Receiver	Max CLK Skew (ns)	Min Flight Time (ns)	Max Flight Time 66 MHz 256K (ns)	Max Flight Time 66 MHz 512K (ns)	Driver Buffer Type	Receiver Buffer Type
82497 BOFF#	82492 BOFF#	0.7	0.4	3.5	3.9	ZD9/ZD9a	ZR9
82497 BLAST#	82492 BLAST#	0.7	0.4	2.7	3.08	ZD9/ZD9a	ZR9
82497 WRARR#	82492 WRARR#	0.7	0.4	2.7	3.0	ZD9/ZD9a	ZR9
82497 WAY	82492 WAY	0.7	0.4	2.8	3.0	ZD9/ZD9a	ZR9
82497 MCYC#	82492 MCYC#	0.7	0.4	2.7	2.9	ZD9/ZD9a	ZR9
82497 MAWEA#	82492 MAWEA#	0.7	0.4	2.9	3.0	ZD9/ZD9a	ZR9
82497 BUS#	82492 BUS#	0.7	0.4	2.9	3.0	ZD9/ZD9a	ZR9
82497 WBA	82492 WBA	0.7	0.4	2.9	3.0	ZD9/ZD9a	ZR9
82497 WBWE#	82492 WBWE#	0.7	0.4	2.9	3.0	ZD9/ZD9a	ZR9
82497 WBTYP	82492 WBTYP	0.7	0.4	2.9	3.0	ZD9/ZD9a	ZR9
82497 BRDYC2#	82492 BRDYC#	0.7	0.4	2.5	2.9	ZD9/ZD9a	ZR9
82497 BLEC#	82492 BLEC#	0.7	0.4	2.7	2.9	ZD9/ZD9a	ZR9

14.3.1.2. OPTIMIZED INTERFACE SIGNAL QUALITY SPECIFICATIONS

All signals in the optimized interface must meet signal quality specifications when the signal reaches the input of a chip. There are two signal quality specifications to meet when simulating a signal's behavior: ringback (or overshoot) and group average overshoot. There is also a settling time guideline to make sure the ringing of the signal does not impact the simulations. Figure 14-1 illustrates the parameters used to verify acceptable signal quality.

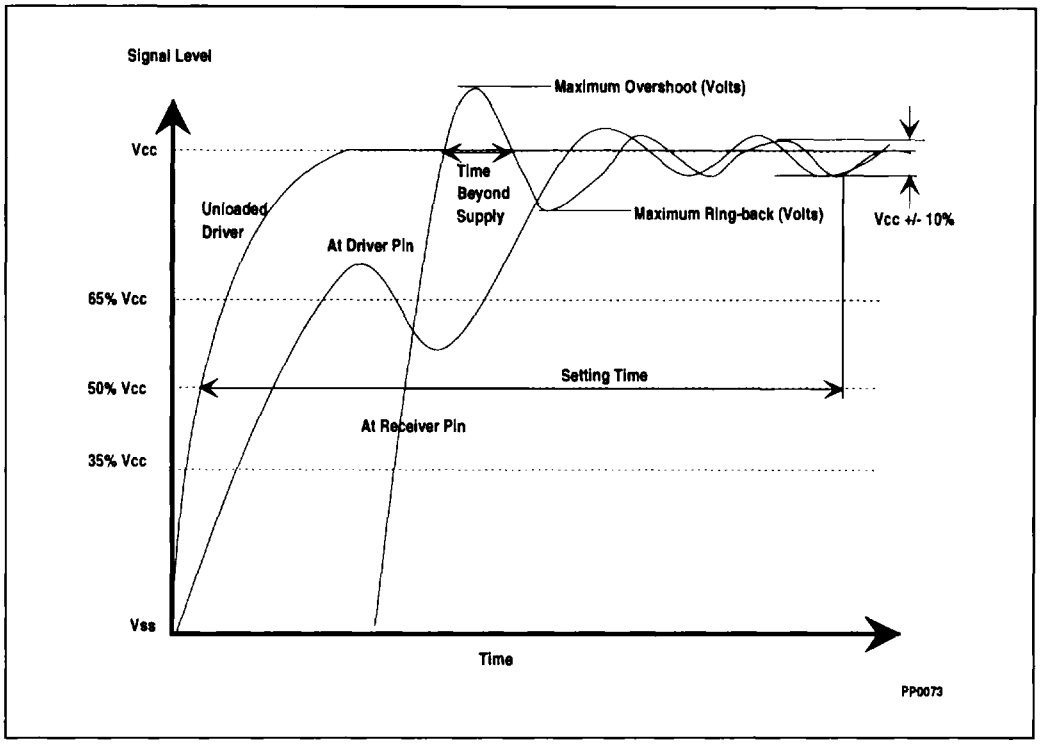


Figure 14-1. Driver and Receiver Signal Waveforms Showing Signal Quality Parameters

14.3.1.2.1. Ringback

Ringback is the result of the input overshooting V_{CC} (or undershooting V_{SS}).

Ringback specifications may be met with the diodes included or excluded from the input buffer model. If included, the ringback specification will be easier to meet. If the simulator cannot simulate ringback, the ringback specification may be guaranteed by meeting the overshoot specification.

The overshoot specification is used to guarantee ringback if ringback cannot be simulated. If ringback is simulated, the overshoot specification may be ignored. When simulating overshoot, the diodes (and Rs) must be removed from the input buffer model.

Notice that the ringback specification for the 5V-tolerant group of inputs is specified with respect to $V_{CC}3$. This makes ringback easier to meet for low-to-high transitioning signals.

14.3.1.2.2. Settling Time

The settling time is defined as the time a signal requires at the receiver to settle within 10% of V_{CC} or V_{SS}.

Most available simulation tools are unable to simulate settling time so that it accurately reflects silicon measurements. On a physical board, second order effects and other effects serve to dampen the signal at the receiver. Because of all these concerns, settling time is a recommendation or a tool for layout tuning and not a specification.

Settling time is simulated at the slow corner, the values to use to make simulation in the slow corner are in Table 14-18. This factor is simulated to make sure that there is no impact on the flight times of the signals if the waveform has not settled. Settling time may be simulated with the diodes included or excluded from the input buffer model. If diodes are included, settling time recommendation will be easier to meet.

Although simulated settling time has not shown good correlation with physical, measured settling time, settling time simulations can still be used as a tool to tune layouts.

Use the following procedure to verify board simulation and tuning with concerns for settling time.

Simulate settling time at the slow corner for a particular signal.

1. If settling time violations occur (signal requires more than 12.5 ns to settle to ±10% of its final value), simulate signal trace with DC diodes in place at the receiver pin.
2. If settling time violations still occur, simulate flight times for 5 consecutive cycles for that particular signal.
3. If flight time values are consistent over the 5 simulations, settling time should not be a concern. If however, flight times are not consistent over the 5 simulations, tuning of the layout is required.
4. Note that, for signals that are allocated 2 cycles for flight time, the recommended settling time is doubled.

NOTE

The signal quality specifications are different for certain signal groups and that they may reference different V_{CC} levels.

Table 14-18. Specifications for Signal Quality

Parameter	Description	CPU-CCTL5T (5VT)	CCTL-CRAM (5V)	All Other Groups (3V)
V_{CC} Reference	The reference voltage used to calculate signal quality for a signal group.	$V_{CC}5$	$V_{CC}5$	$V_{CC}3$
Maximum Signal Ringback	Absolute value of the maximum voltage at the receiving pin below V_{CC} (or above V_{SS}) relative to V_{CC} (or V_{SS}) level after the signal has reached its maximum voltage level. Measure at FAST corner V_{CC} levels (5.5V or 3.7V).	65% $V_{CC}3$ (low to high) 35% $V_{CC}3$ (high to low)	65% $V_{CC}5$ (low to high) 35% $V_{CC}5$ (high to low)	65% $V_{CC}3$ (low to high) 35% $V_{CC}3$ (high to low)
Absolute Maximum Signal Overshoot (Undershoot)	Absolute value of the maximum voltage at the receiving pin above V_{CC} (or below V_{SS}) relative to V_{CC} (or V_{SS}) level. (Assumes input diodes are not present.) See NOTE.	Overshoot ($V_{CC}5$)3.8Volts Undershoot (V_{SS})2.6Volts	3.8 Volts	2.6 Volts
Maximum Time Beyond Supply	Maximum time a signal may exceed V_{CC} (or V_{SS}). This value is ignored if overshoot does not exceed 0.5 Volts.	7 nsec	7 nsec	7 nsec
Maximum Settling Time (guideline)	Total time required for a signal to settle within 10% of its final value referenced from the unloaded driver's initial crossing of the 50% V_{CC} level.	12.5 nsec	12.5 nsec	12.5 nsec

NOTE:

When using 3.3V signal drivers on the 5VT signals it is important to note that the input protection diode string on the 5VT signals will not typically clamp a low to high driven signal. In this case there is no specification for overshoot but make sure to use the 65% and 35% levels for the ringback specification during simulation of this parameter.

14.3.2. External Interface

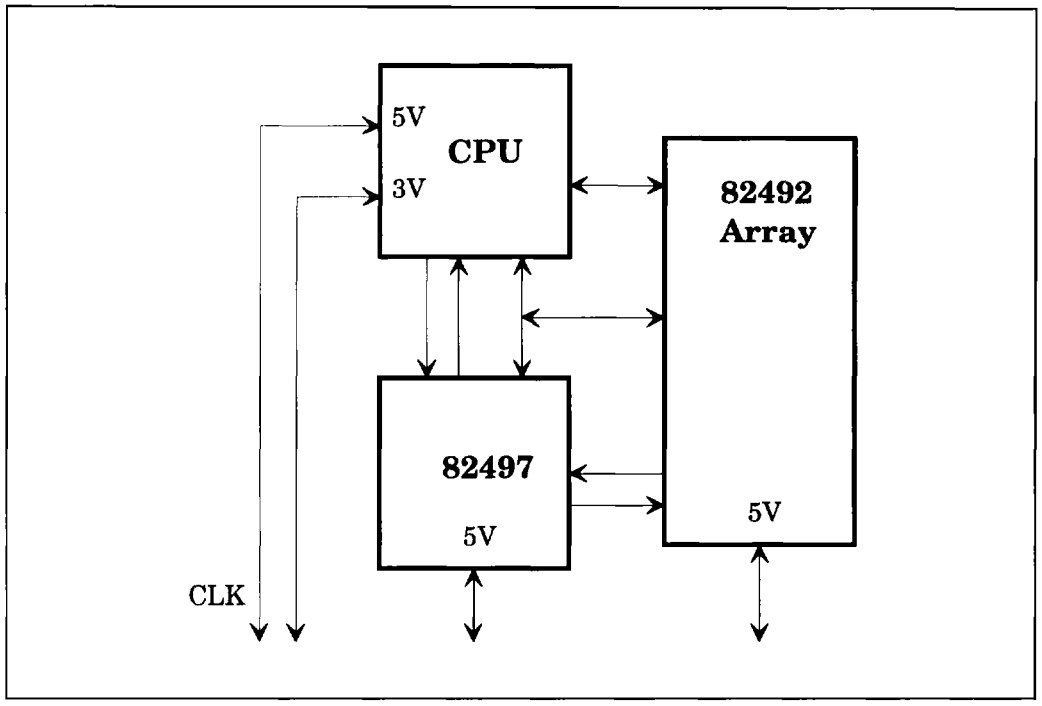


Figure 14-2. External Interface

The external interface is the interface between the chip set components and the memory bus controller, memory address bus, and memory data bus. All of the signals that interface to the memory bus from the 82497 Cache Controller and 82492 Cache SRAM are 5V TTL. See Table 14-16 for a specific listing of these signals. All signals that interface to the memory bus from the Pentium processor (735\90, 815\100, 1000\120, 1110\133), except the CLK and PICCLK inputs, are 3.3V TTL. The Pentium processor (735\90, 815\100, 1000\120, 1110\133) CLK and PICCLK inputs may be a 3.3V or 5V TTL clock.

For output signals, Intel supplies valid delays at 0pF and buffer models so the effect of various loadings at the signal's pin can be simulated.

For input signals, Intel provides setup times, hold times, and signal quality specifications.

Tables 14-19 to 14-23 list the AC specifications associated with the chip set's external interface signals.

All timings are referenced to 1.5 volts for both "0" and "1" logic levels unless otherwise specified. Within the sampling window, a synchronous input must be stable for correct Pentium processor (735\90, 815\100, 1000\120, 1110\133) operation.

Care should be taken to read all notes associated with a particular timing parameter. In addition, the following list of notes apply to the timing specification tables in general and are not associated with any one timing. They are 5, 13, 14, 15, 16, 47, 48, and 56.

14.3.2.1. EXTERNAL INTERFACE AC TIMINGS

In the following tables, the T_{CASE} temperature for the Pentium processor (735\90, 815\100, 1000\120, 1110\133) is 0° to 70° C and the 82497 Cache Controller and 82492 Cache SRAM have a T_{CASE} specification of 0° to 85°C.

Table 14-19. Chip Set Common Timings

$V_{CC}3$ = 3.135-3.6V, $V_{CC}5$ = 5V ±5%, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_1	CLK Frequency	33	66	MHz		Freq Selectable, (0), (49)
t_2	CLK Period	15	30	ns	14-3	
t_3	CLK High Time	4		ns	14-3	(1), (55)
t_4	CLK Low Time	4		ns	14-3	(2), (55)
t_5	CLK Rise Time	0.15	1.5	ns	14-3	(3), (55)
t_6	CLK Fall Time	0.15	1.5	ns	14-3	(3), (55)
t_7	CLK Stability		± 250	ps		Adjacent Clocks, (55), (57)
t_8	RESET, INIT Setup Time	5		ns	14-7	To guarantee recognition on a given CLK edge. (17), (18)
t_9	RESET, INIT Hold Time	1.0		ns	14-7	To guarantee recognition on a given CLK edge.
t_{10}	RESET Pulse Width, CLK and V_{CC} Stable	15		CLKs	14-7	(10), (18)
t_{11}	INIT Pulse Width, Async.	2		CLKs		To guarantee asynchronous recognition.
t_{13}	RESET Active After CLK and V_{CC} Stable	1		ms	14-7	Power Up (10), (12), (55)
t_{20}	TCK Frequency	--	16	MHz	14-3	PP
t_{20a}	TCK Frequency	--	16	MHz	14-3	82497 and 82492

Table 14-19. Chip Set Common Timings (Contd.)

$V_{CC}3$ = 3.135-3.6V, $V_{CC}5$ = 5V ±5%, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_{21}	TCK Period	62.5		ns	14-3	PP
t_{21a}	TCK Period	62.5		ns	14-3	82497 and 82492
t_{22}	TCK High Time	25		ns	14-3	(1)
t_{23}	TCK Low Time	25		ns	14-3	(2), (55)
t_{24}	TCK Rise Time		5	ns	14-3	(8), (3), (55)
t_{25}	TCK Fall Time		5	ns	14-3	(8), (3), (55)
t_{28}	TRST# Pulse Width	40		ns	14-13	(55), Asynchronous
t_{29}	TDI, TMS Setup Time	5		ns	14-12	(6)
t_{30}	TDI, TMS Hold Time	13		ns	14-12	(6)
t_{31}	TDO Valid Delay	3	20	ns	14-12	(7)
t_{32}	TDO Float Delay		25	ns	14-12	(7), (55)
t_{33}	All Non-Test Outputs Valid Delay	3	20	ns	14-12	(7), (9)
t_{34}	All Non-Test Outputs Float Delay		25	ns	14-12	(7), (9), (55)
t_{35}	All Non-Test Inputs Setup Time	5		ns	14-12	(6), (9)
t_{36}	All Non-Test Inputs Hold Time	13		ns	14-12	(6), (9)

NOTE:

PP = Pentium® processor (735\90, 815\100, 1000\120, 1110\133)

Table 14-20. Pentium® Processor (735\90, 815\100, 1000\120, 1110\133) Memory Bus Interface Timings

$V_{CC}3$ = 3.135-3.6V, $V_{CC}5$ = 5V ±5%, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
t_{40}	PP reset configurations (INIT, FLUSH#, FRCMC#) Setup Time	5		ns	14-7	
t_{41}	PP reset configurations (INIT, FLUSH#, FRCMC#) Hold Time	1.0		ns	14-7	
t_{42}	PP reset configurations (INIT, FLUSH#, FRCMC#) Setup Time Referenced to Falling Edge of RESET	2		CLKs	14-7	
t_{43}	PP reset configurations (INIT, FLUSH#, FRCMC#) Hold Time Reference to Falling Edge of RESET	2		CLKs	14-7	
t_{50}	HLDA Valid Delay	1.0	8.0 60-MHz 6.8 66-MHz	ns	14-4	(4)
t_{51}	BREQ Valid Delay	1.0	8.0 60-MHz 6.8 66-MHz	ns	14-4	
t_{52a}	APCHK#, FERR#, IERR# Valid Delay	1.0	8.3	ns	14-4	(4), (11)
t_{52b}	PCHK# Valid Delay	1.0	7.0	ns	14-4	(4), (11)
t_{54}	BP0-3, PM0-1 Valid Delay	1.0	10	ns	14-4	
t_{55}	A20M#, FLUSH#, IGNNE#, NMI, INIT, INTR, Setup Time	5		ns	14-5	(17), (18)
t_{56}	A20M#, FLUSH#, IGNNE#, NMI, INIT, INTR, Hold Time	1.0		ns	14-5	
t_{57}	FLUSH#, IGNNE#, NMI, INIT, Pulse Width, Async	2		CLKs		(18)
t_{58}	PEN#, BUSCHK# Setup Time	5.0 60-Mhz 4.8 66-MHz		ns	14-5	
t_{59}	PEN#, BUSCHK# Hold Time	1.0		ns	14-5	
t_{60}	HOLD Setup Time	5.0 60-Mhz 4.8 66-MHz		ns	14-5	
t_{61}	HOLD Hold Time	1.5		ns	14-5	

Table 14-21. Pentium® Processor (735\90, 815\100, 1000\120, 1110\133) Memory Bus Interface Timings (Contd.)

$V_{CC}3$ = 3.135-3.6V, $V_{CC}5$ = 5V ±5%, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Fig.**	**Notes**
t_{62}	BRDY# Setup Time	5		ns	14-5	
t_{63}	BRDY# Hold Time	1.0		ns	14-5	
t_{64}	R/S#, SMI# Setup Time	5		ns	14-5	(17), (18)
t_{65}	R/S#, SMI# Hold Time	1.0		ns	14-5	
t_{66}	R/S#, SMI# Pulse Width, Async	2		CLKs		(18)
t_{67a}	SMIACT# Valid Delay	1.0	7.6 60-Mhz 7.3 66-MHz	ns	14-4	
t_{67b}	PRDY Valid Delay	1.0	8.0	ns	14-4	

NOTE:

PP = Pentium® processor (735\90, 815\100, 1000\120, 1110\133)

Table 14-22. 82497 Memory Bus Interface Timings

$V_{CC}3$ = 3.135-3.6V, $V_{CC}5$ = 5V ±5%, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_{71a}	CFG0-2, CLDRV, HIGHZ#, MALDRV, SLFTST#, SNPMD, WWOR#, FLUSH#[V_{cc}] Setup Time	6		ns	14-7	(12), (22), (36)
t_{71b}	CFG0-2, CLDRV, HIGHZ#, MALDRV, SLFTST#, SNPMD, WWOR#, FLUSH#[V_{cc}] Hold Time	1		ns	14-7	(12), (23), (36)
t_{72}	CFG0-2, CLDRV, HIGHZ#, MALDRV, SLFTST#, SNPMD, WWOR#, FLUSH#[V_{cc}] Setup Time Referenced to Falling Edge of RESET	10		CLKs	14-7	(12), (36)
t_{73}	CFG0-2, CLDRV, HIGHZ#, MALDRV, SLFTST#, SNPMD, WWOR#, FLUSH#[V_{cc}] Hold Time Referenced to Falling Edge of RESET	0		CLKs	14-7	(12), (36)
t_{75}	FLUSH#, SYNC# Setup Time	6		ns	14-5	(34)
t_{76}	FLUSH#, SYNC#, Hold Time	1		ns	14-5	(34)
t_{77}	FLUSH#, SYNC#, Pulse Width, Async	2		CLKs		
t_{80}	CADS#, CDTS# Valid Delay	1.5	8.2	ns	14-4	Glitch Free
t_{81}	KLOCK#, MCACHE#, RDYSRC Valid Delay	1.5	8.2	ns	14-4	KLOCK# is Glitch Free
t_{82}	CW/R#, CD/C#, CMI/O# Valid Delay	1.5	8.2	ns	14-4	
t_{83}	CPWT, CPCD, CCACHE#, CSCYC Valid Delay	1.5	8.2	ns	14-4	
t_{84}	CAHOLD, CWAY, PALLC# Valid Delay	1.5	8.2	ns	14-4	
t_{85}	FSIOUT# Valid Delay	1.5	8.2	ns	14-4	
t_{86}	NENE#, SMLN# Valid Delay	1.5	12	ns	14-4	
t_{87}	APERR#, IPERR#, MAPERR# Valid Delay	1.5	8.2	ns	14-4	Glitch Free
t_{88}	APIC# Valid Delay	1.5	12	ns	14-4	
t_{89}	BLE# Valid Delay	1.5	8.2	ns	14-4	(35)
t_{90}	MCFA0-6, MSET0-10, MTAG0-11, MAP Valid Delay	1.5	11	ns	14-4	(25), (54)

Table 14-22. 82497 Memory Bus Interface Timings (Contd.)

$V_{CC}3$ = 3.135-3.6V, $V_{CC}5$ = 5V ±5%, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_{91}	MCFA0-6, MSET0-10, MTAG0-11, MAP Valid Delay	1.5	11	ns	14-8	(26), (54)
t_{92}	MCFA0-6, MSET0-10, MTAG0-11, MAP Valid Delay	1.5	10	ns	14-8	(27), (54)
t_{93}	MCFA0-6, MSET0-10, MTAG0-11, MAP Float Delay		11	ns	14-8	(28), (55)
t_{95}	BRDY#, CRDY# Setup Time	6.5		ns	14-5	
t_{96}	BRDY#, CRDY# Hold Time	1		ns	14-5	
t_{97}	BGT#, CNA#, KWEND#, SWEND# Setup Time	6		ns	14-5	
t_{98}	BGT#, CNA#, KWEND#, SWEND# Hold Time	1		ns	14-5	
t_{100a}	DRCTM#, MRO#, MWB/WT# Setup Time	6		ns	14-5	(24)
t_{100b}	MKEN# Setup Time	6.5		ns	14-5	(24)
t_{101a}	DRCTM#, MRO#, MWB/WT# Hold Time	1		ns	14-5	(24)
t_{101b}	MKEN# Hold Time	1		ns	14-5	(24)
t_{110}	SNPCLK Frequency	8.3	66.66	MHz		1X clock
t_{111}	SNPCLK Period	15	120	ns	14-3	
t_{112}	SNPCLK High Time	4		ns	14-3	(55)
t_{113}	SNPCLK Low Time	4		ns	14-3	(55)
t_{114}	SNPCLK Rise Time		1.5	ns	14-3	(38)
t_{115}	SNPCLK Fall Time		1.5	ns	14-3	(38)
t_{118}	SNPADS#, SNPCYC# Valid Delay	1.5	8.2	ns	14-4	Glitch Free.
t_{120}	MCFA0-6, MSET0-10, MTAG0-11, MAP Setup Time	6		ns	14-5	(29)
t_{121}	MCFA0-6, MSET0-10, MTAG0-11, MAP Hold Time	1		ns	14-5	(29)

Table 14-22. 82497 Memory Bus Interface Timings (Contd.)

$V_{CC}3$ = 3.135-3.6V, $V_{CC}5$ = 5V ±5%, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_{122}	MCFA0-6, MSET0-10, MTAG0-11, MAP Setup Time	6		ns	14-5	(30)
t_{123}	MCFA0-6, MSET0-10, MTAG0-11, MAP Hold Time	1		ns	14-5	(30)
t_{124}	MCFA0-6, MSET0-10, MTAG0-11, MAP Setup Time	1		ns	14-6	(31)
t_{125}	MCFA0-6, MSET0-10, MTAG0-11, MAP Hold Time	6		ns	14-6	(31)
t_{130}	MAOE#, MBAOE#, SNPINV, SNPNCA Setup Time	6		ns	14-5	(29)
t_{131}	MAOE#, MBAOE#, SNPINV, SNPNCA Hold Time	1		ns	14-5	(29)
t_{132}	MAOE#, MBAOE#, SNPINV, SNPNCA Setup Time	6		ns	14-5	(30)
t_{133}	MAOE#, MBAOE#, SNPINV, SNPNCA Hold Time	1		ns	14-5	(30)
t_{134}	MAOE#, MBAOE#, SNPINV, SNPNCA Setup Time	1		ns	14-6	(31)
t_{135}	MAOE#, MBAOE#, SNPINV, SNPNCA Hold Time	6		ns	14-6	(31)
t_{140}	SNPSTB# Setup Time	6		ns	14-5	(29)
t_{141}	SNPSTB# Hold Time	1		ns	14-5	(29)
t_{142}	SNPSTB# Setup Time	6		ns	14-5	(30)
t_{143}	SNPSTB# Hold Time	1		ns	14-5	(30)
t_{144}	SNPSTB# Active Time	6		ns	14-14	(32)
t_{145}	SNPSTB# Inactive Time	6		ns	14-14	(32)
t_{148}	MHITM#, MTHIT#, SNPBSY# Valid Delay	1.5	10	ns	14-14	

Table 14-23. 82492 Memory Bus Interface Timings

$V_{CC}3$ = 3.135-3.6V, $V_{CC}5$ = 5V ±5%, C_L = 0 pF						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_{150}	MDLDRV, MSTBM, MTR4/8#, MX4/8#, PAR# Setup Time	5		ns	14-7	(22), (53)
t_{151}	MDLDRV, MSTBM, MTR4/8#, MX4/8#, PAR# Hold Time	1		ns	14-7	(23), (53)
t_{152}	MDLDRV, MSTBM, MTR4/8#, MX4/8#, PAR# Setup Time Referenced to Falling Edge of RESET	4		CLKs	14-7	(41), (53), (55)
t_{153}	MDLDRV, MSTBM, MTR4/8#, MX4/8#, PAR# Hold Time Referenced to Falling Edge of RESET	0		CLKs	14-7	(41), (53), (55)
t_{155}	BRDY#, CRDY# Setup Time	5		ns	14-5	
t_{156}	BRDY#, CRDY# Hold Time	1		ns	14-5	
t_{160}	MDATA Setup to CLK (CLK before BRDY# Active)	5		ns	14-5	(44)
t_{161}	MDATA Valid Delay From CLK (CLK from CDTS# Valid, MDOE# Active)		13	ns	14-4	(49)
t_{162}	MDATA Valid Delay From MDOE# Active		8	ns	14-8	
t_{163}	MDATA Float Delay From MDOE# Inactive		10	ns	14-8	(55)
t_{165}	MBE# Valid Delay	1.5	8	ns	14-4	(51)
Clocked Mode						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_{170}	MCLK, MOCLK Frequency		66.66	MHz		1X clock, (49)
t_{171}	MCLK, MOCLK Period	15		ns	14-3	
t_{172}	MOCLK High Time	4		ns	14-3	(55)
t_{173}	MOCLK Low Time	4		ns	14-3	(55)
t_{174}	MCLK High Time	5		ns	14-3	(52), (55)

Table 14-23. 82492 Memory Bus Interface Timings (Contd.)

$V_{CC}3$ = 3.135-3.6V, $V_{CC}5$ = 5V ±5%, C_L = 0 pF						
Clocked Mode						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_{175}	MCLK Low Time	5		ns	14-3	(52), (55)
t_{176}	MCLK, MOCLK Rise Time		1.5	ns	14-3	(55)
t_{177}	MCLK, MOCLK Fall Time		1.5	ns	14-3	(55)
t_{180}	MOCLK Falling Edge To MCLK Rising Edge	2		ns		
t_{181}	MFRZ#, MZBT# Setup Time	5		ns	14-5	Referenced to MCLK
t_{182}	MFRZ#, MZBT# Hold Time	1		ns	14-5	Referenced to MCLK
t_{183}	MBRDY#, MSEL#, MEOC# Setup Time	5		ns	14-5	Referenced to MCLK
t_{184}	MBRDY#, MSEL#, MEOC# Hold Time	1		ns	14-5	Referenced to MCLK
t_{185}	MDATA Setup Time	5		ns	14-5	Referenced to MCLK
t_{186}	MDATA Hold Time	1		ns	14-5	Referenced to MCLK
t_{187}	MDATA Valid Delay From MCLKIMBRDY#	2	12	ns	14-4	
t_{188}	MDATA Valid Delay From MCLKIMEOC#	2	20	ns	14-4	
t_{189}	MDATA Valid Delay From MCLKIMSEL#	2	18	ns	14-4	(45)
t_{190}	MDATA Valid Delay From MOCLK	1.5	10	ns	14-4	
Strobed Mode						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_{195}	MEOC# High Time	8		ns	14-14	(49)
t_{196}	MEOC# Low Time	8		ns	14-14	
t_{197}	MISTB, MOSTB High Time	12		ns	14-14	(49)
t_{198}	MISTB, MOSTB Low Time	12		ns	14-14	
t_{199}	MEOC#, MISTB, MOSTB Rise Time		2	ns		

Table 14-23. 82492 Memory Bus Interface Timings (Contd.)

$V_{CC}3$ = 3.3V ±5%, $V_{CC}5$ = 5V ±5%, C_L = 0 pF						
Strobed Mode						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_{200}	MEOC#, MISTB, MOSTB Fall Time		2	ns		
t_{201}	MSEL# High Time for Restart	8		ns	14-14	
t_{202}	MSEL# Setup Before Transition on MISTB or MOSTB	5		ns	14-10	(49)
t_{203}	MSEL# Hold After Transition on MISTB or MOSTB	10		ns	14-10	
t_{204}	MSEL# Setup Before Transition on MEOC#	5		ns	14-10	
t_{205}	MSEL# Hold After Transition on MEOC#	1		ns	14-10	
t_{206}	MISTB, MOSTB Transition to/from MEOC# Falling Transition	10		ns		
t_{207}	MZBT# Setup To MSEL# or MEOC# Falling Edge	5		ns	14-9	
t_{208}	MZBT# Hold From MSEL# or MEOC# Falling Edge	1		ns	14-9	
t_{209}	MFRZ# Setup To MEOC# Falling Edge	5		ns	14-9	
t_{210}	MFRZ# Hold From MEOC# Falling Edge	1		ns	14-9	
t_{211}	MDATA Setup To MISTB transition or MEOC# Falling Edge	5		ns	14-9	
t_{212}	MDATA Hold From MISTB transition or MEOC# Falling Edge	1		ns	14-9	
t_{213}	MDATA Valid Delay From Transition on MOSTB	2	12	ns	14-11	
t_{214}	MDATA Valid Delay From MEOC# Falling Transition or MSEL# Deactivation	2	20	ns	14-11	

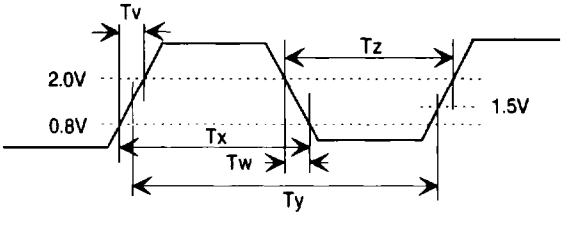
NOTES:

PP = Pentium® Processor (735\90, 815\100, 1000\120, 1110\133)

0. The following equations provide the change in AC specifications required to operate at lower frequencies:
   82497: (signals: SET0-10, ADS#, CFA2-6, and TAG0-11)
   D setup = 0.57 (D cycle time) ±0.5ns
   PP and 82492 do not change with frequency.
1. High times are measured between 2V crossing points.
2. Low times are measured between 0.8V crossing points.

3. Rise and Fall times are measured between 0.8V and 2.0V.
4. APCHK#, FERR#, HLDA, IERR#, and PCHK# are glitch free outputs. Glitch free signals monotonically transition without false transitions (i.e., glitches).
5. TTL input test waveforms are assumed to be 0 to 3V transitions with 1Volt/ns rise and fall times.
6. Referenced to TCK rising edge.
7. Referenced to TCK falling edge.
8. 1 ns can be added to the maximum TCK rise and fall times for every 10 MHz of frequency below 33 MHz. 1 ns must be added to t_{30} and t_{36} for every 10 MHz of frequency below 33 MHz.
9. Non-Test Outputs and Inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to boundary scan operations.
10. FRCMC# should be tied to V_{CC} (high) to ensure proper operation of the PP as a master PP.
11. PCHK# is seen 2 OR 3 clocks after the parity error, due to the bus/core frequency ratio.
12. If configuration signals with internal pullup resistors are left floating in the system, RESET pulse width must be at least 10 µs.
13. CLK skew between PP and 82497 assumed to be less than 0.2 ns. CLK skew is measured at 0.8V, 1.5V, and 2.V of the rising edge of CLK.
14. 0.8V/ns <= CLK input rise/fall time <= 8 V/ns.
15. 0.3V/ns <= Input rise/fall time <= 5 V/ns.
16. Glitch free signals monotonically transition without false transitions (i.e., glitches).
17. This input may be driven asynchronously.
18. When driven asynchronously, NMI, FLUSH#, R/S#, INIT, and SMI must be deasserted (inactive) for a minimum of 2 clocks before being returned active.
22. Setup time is required to guarantee recognition on a specific clock.
23. Hold time is required to guarantee recognition on a specific clock.
24. Only need to meet setup and hold times during the KWEND and SWEND sample times.
25. Valid delay from CLK only if MALE or MBALE, MAOE#, MBAOE# are active.
26. Valid delay from MALE or MBALE going active, if both MAOE# and MBAOE# are active.
27. Valid delay from MAOE#, MBAOE# going active.
28. Float delay from MAOE#, MBAOE# going inactive.
29. In Synchronous mode, referenced to CLK.
30. In Clocked mode, referenced to SNPCLK.
31. In Strobed mode, referenced to SNPSTB# falling edge.
32. In Strobed mode, must meet active/inactive times.
34. To guarantee recognition on a given CLK edge.
35. This signal is not used when using the 82497 Cache Controller with the 82492 Cache SRAM.
36. For proper configuration, t_{70}, t_{71}, t_{72}, and t_{73} must all be met.
38. 1 ns can be added to maximum SNPCLK rise/fall time for every 10 MHz of frequency below 66 MHz. 1 ns must be added to t_{123} and t_{133} for every 10 MHz of frequency below 66 MHz.
41. Timing is referenced to falling edge of RESET.
44. Must meet MDATA setup to CLK one full CLK before BRDY# active for first transfer on line fills and all non-cacheable transfers.
45. MSEL# sampled inactive resets burst counter. Data is re-driven beginning with data corresponding to first address requested.
47. Float and Enable times measured at $V_{CC}2$ level at gate of output device are guaranteed by design (not 100% tested).

48. CLK Skew between 82492 Cache SRAM and other devices (PP, 82497 Cache Controller, and other 82492 Cache SRAMs) assumed to be less than 0.7 ns.
49. Signal Restrictions
    a. For proper operation the following signals must have monotonic transitions:
       - CLK,
       - MCLK in clocked mode,
       - MISTB, MOSTB, and MEOC# in strobed mode.
    b. For proper operation the following signals must remain stable (must not glitch) throughout a cycle.
       - MDOE#,
       - MSEL#, when active during strobed mode.
51. From CLK in which BLEC# sampled active.
52. Tighter symmetry required since MCLK input does not use a PLL.
53. For proper configuration, t_{150}, t_{151}, t_{152}, and t_{153} must all be met.
54. AC timings assume MALDRV = low on reset. If MALDRV = high on reset, add .7 ns to t_{90}, t_{91}, and t_{92}.
55. Not 100% Tested. Guaranteed by design/characterization.
56. All TTL timings are referenced from 1.5V.
57. These signals are measured on the rising edge of adjacent CLKs at 1.5V. To ensure a 1:1 relationship between the amplitude of the input jitter and internal and external clocks, the jitter frequency should not have any power spectrum peaking between 500 kHz and 1/3 of the CLK operating frequency. The amount of jitter present must be accounted for as a component of CLK skew between devices.



Tv = t5, t24, t114, t174
Tw = t6, t25, t115, t175
Tx = t4, t23, t113, t173
Ty = t2, t20, t111, t171
Tz = t3, t22, t112, t172

PP1401

Figure 14-3. Clock Waveform

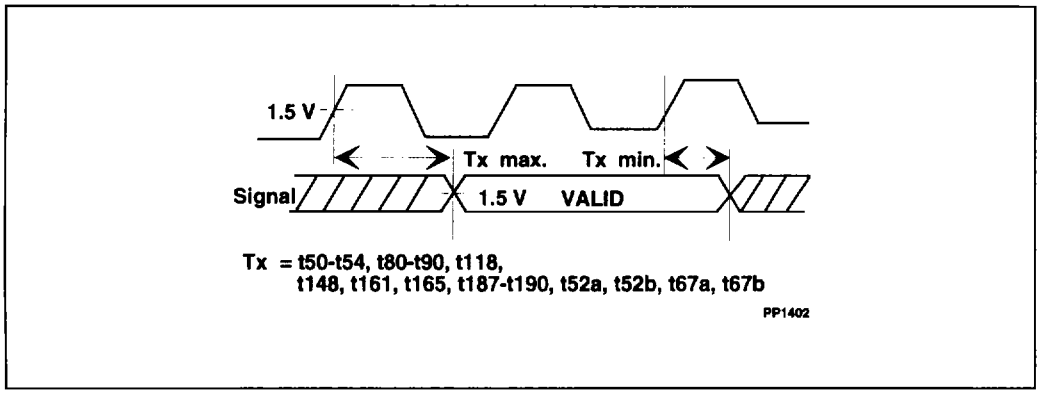


Figure 14-4. Valid Delay Timings

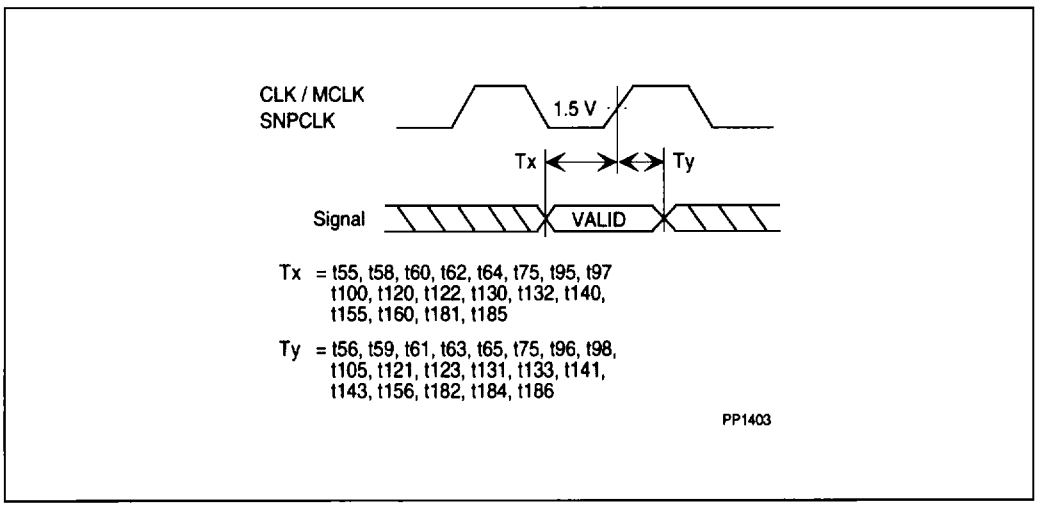


Figure 14-5. Setup and Hold Timings

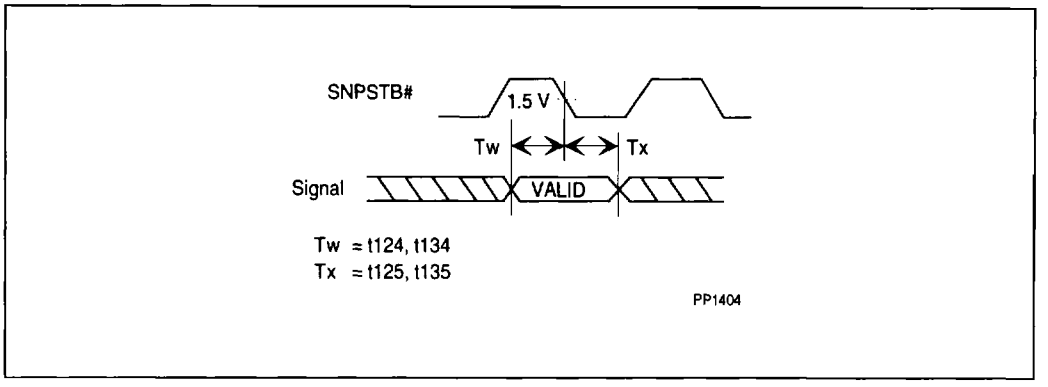


Figure 14-6. Setup and Hold Timings in Strobed Snooping Mode

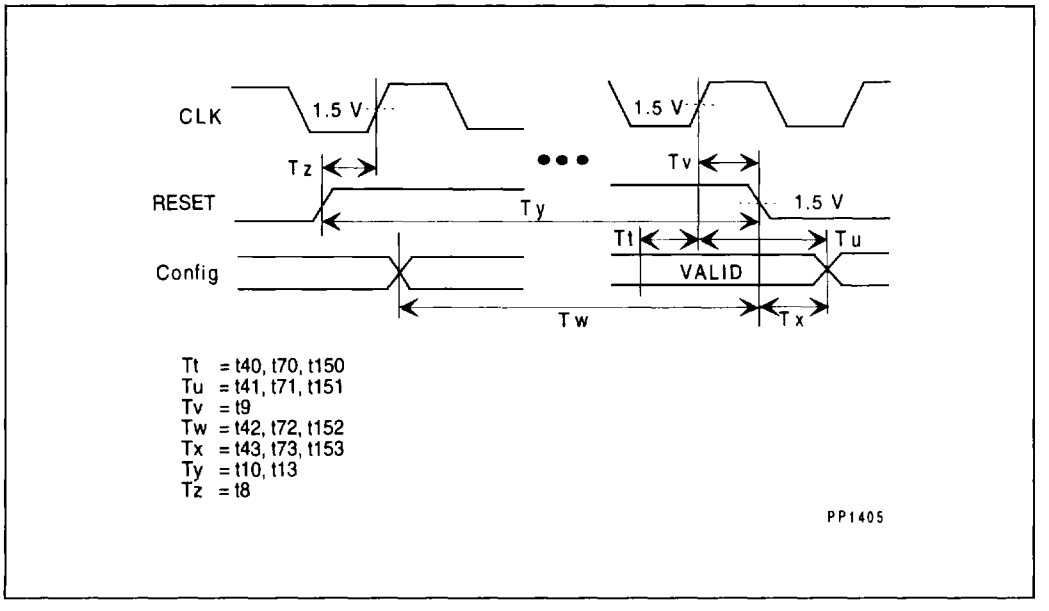


Figure 14-7. Reset and Configuration Timings

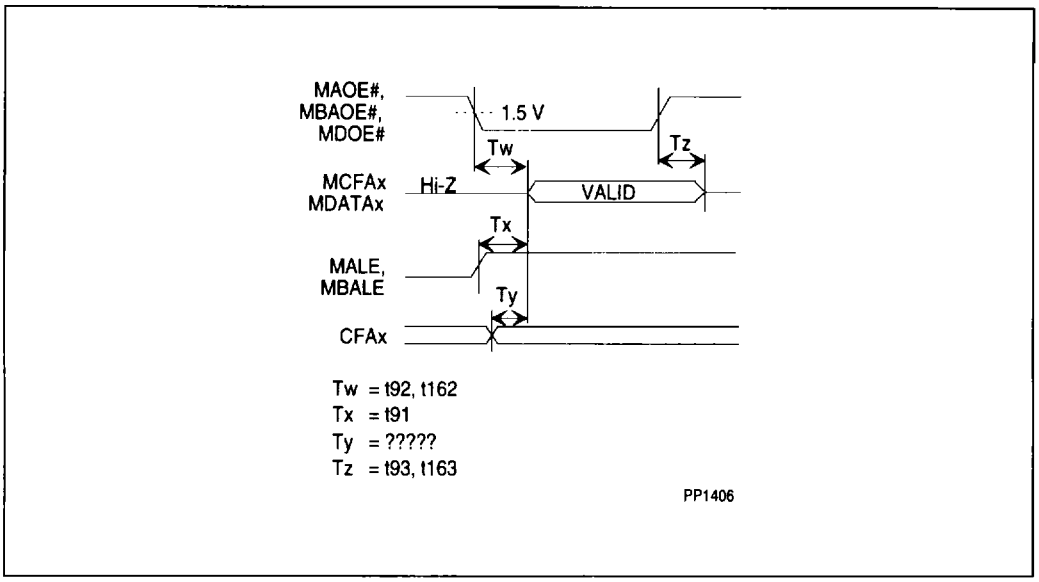


Figure 14-8. Memory Interface Timings

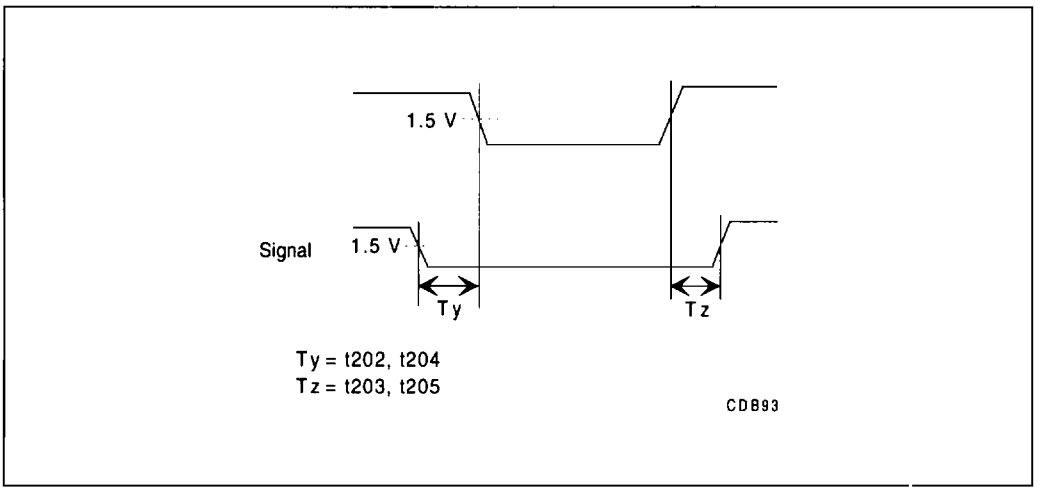


Figure 14-9. Setup and Hold Timings to Strobes

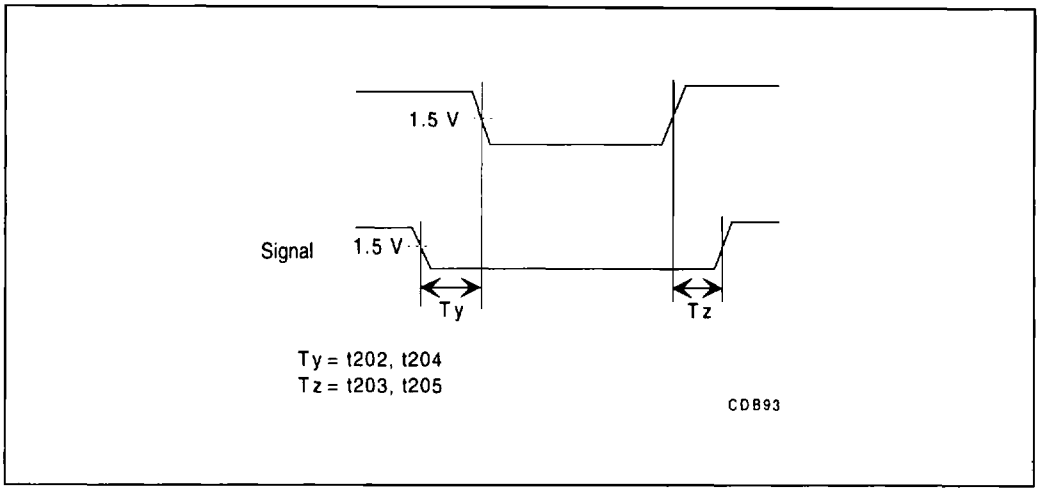


Figure 14-10. Setup and Hold Timings MxST

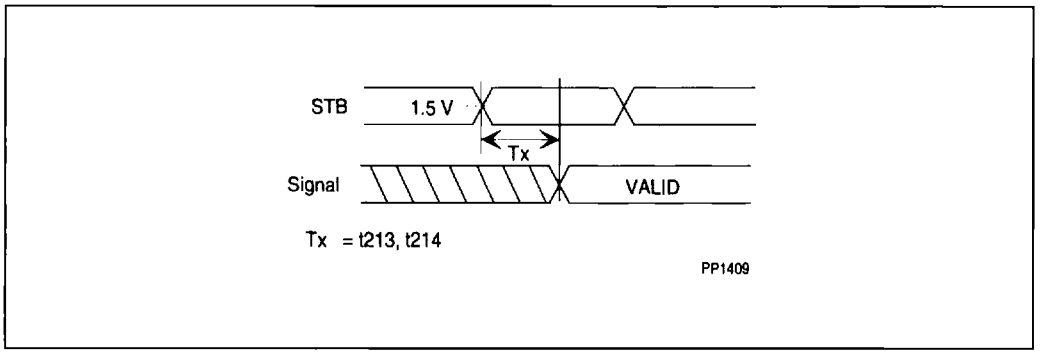


Figure 14-11. Valid Delay Timings From Strobes

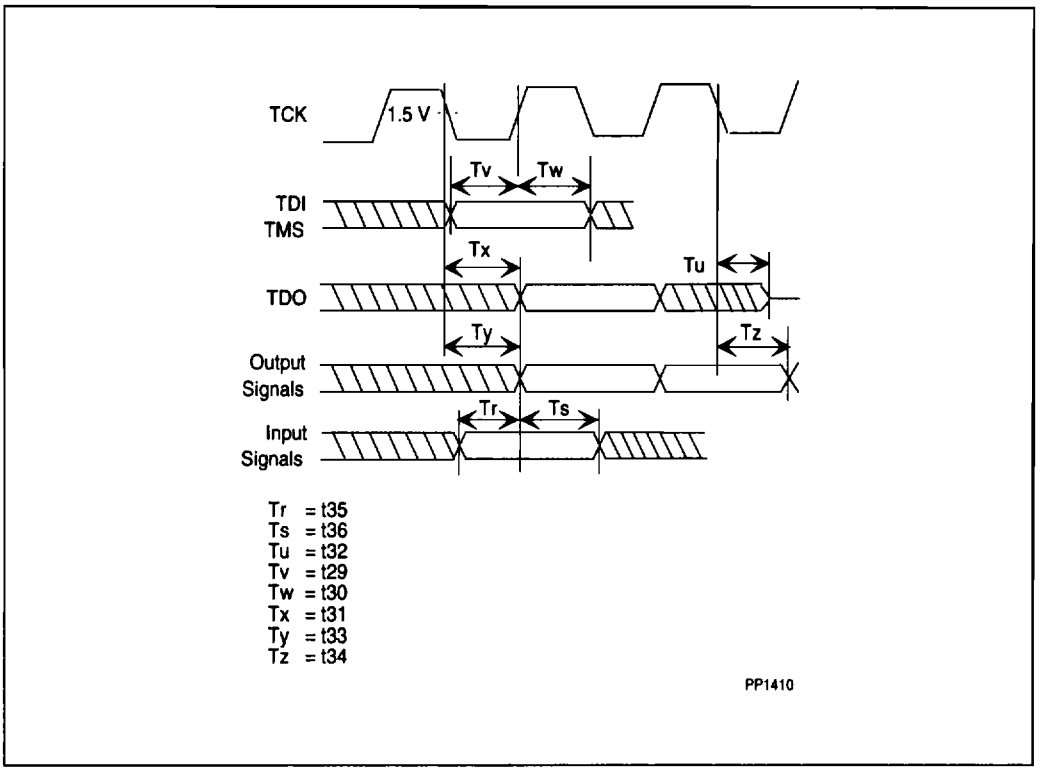


Figure 14-12. Test Timings

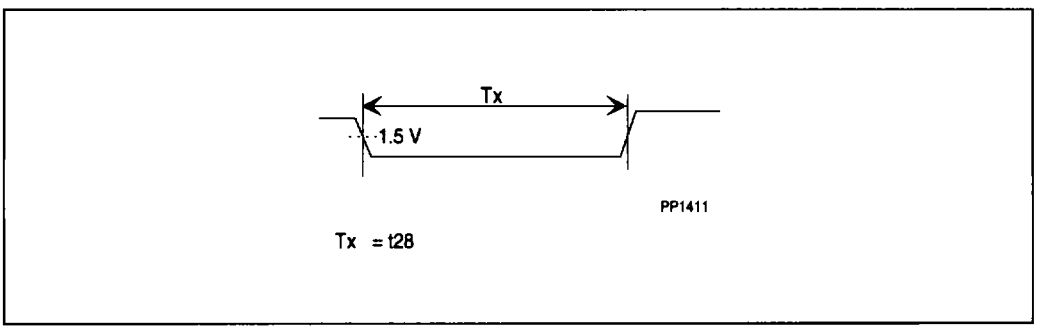


Figure 14-13. Test Reset Timings

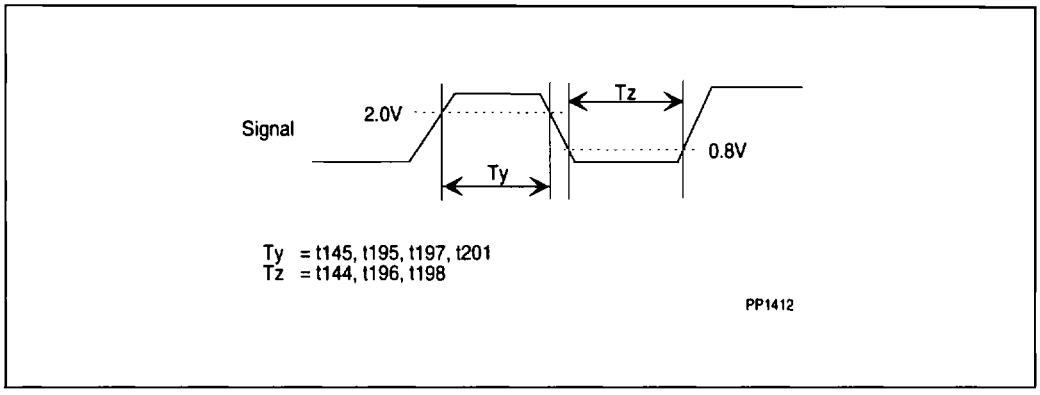


Figure 14-14. Active/Inactive Timings

14.3.2.2. EXTERNAL INTERFACE SIGNAL QUALITY

Signals driven by the system to the chip set must meet signal quality specifications to guarantee that the components read data properly and to ensure that incoming signals do not affect the reliability of the component. There are two signal quality parameters of the external interface: ringback and settling time

14.3.2.2.1. Ringback

Excessive ringback can contribute to long-term reliability degradation of the chip set. Ringback is simulated at the input pin of a component using the input buffer model. Ringback can be simulated with or without the diodes that are in the input buffer model.

If simulated without the input diodes, follow the maximum overshoot/undershoot specification. By meeting the overshoot/undershoot specification, the signal is guaranteed not to ringback excessively.

If simulated with the diodes present in the input model, follow the maximum ringback specification.

Overshoot (undershoot) is the absolute value of the maximum voltage above V_{CC} (below V_{SS}). The specification assumes the absence of diodes on the input.

Maximum overshoot/undershoot on 5V chip set (CLK and PICCLK only) inputs = 1.6V above $V_{CC}5$

(without diodes)

Maximum overshoot/undershoot on 3.3V Pentium processor (735\90, 815\100, 1000\120, 1110\133) inputs (not CLK and PICCLK) = 1.4V above $V_{CC}3$

(without diodes)

Ringback is the absolute value of the maximum voltage at the receiving pin below V_{CC} (or above V_{SS}) relative to V_{CC} (or V_{SS}) level after the signal has reached its maximum voltage level. The input diodes are assumed present.

Maximum ringback on inputs = 0.8V

(with diodes)

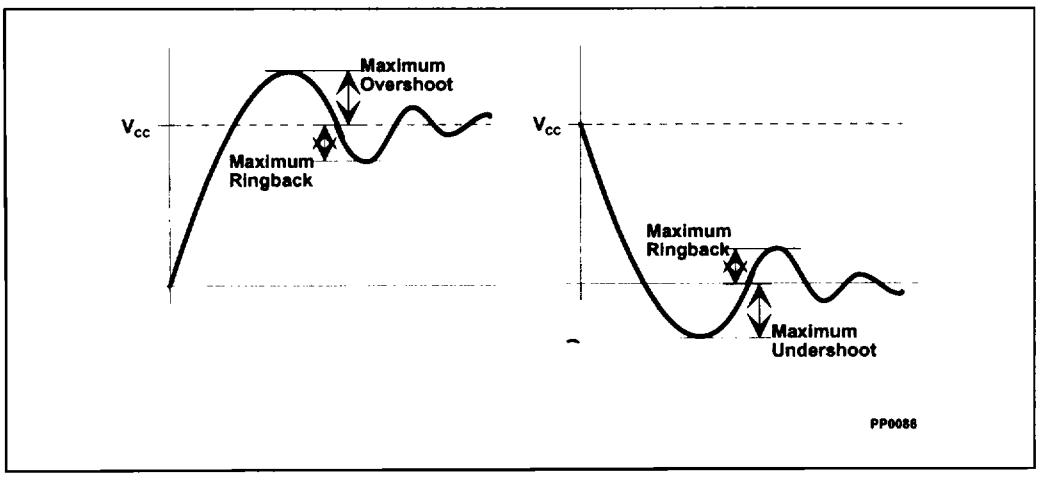


Figure 14-15. Overshoot/Undershoot and Ringback Specifications

14.3.2.2.2. Settling Time

The settling time is defined as the time a signal requires at the receiver to settle within 10% of V_{CC} or V_{SS}. Settling time is the maximum time allowed for a signal to reach within 10% of its final value. For 5V signals, the final value is $V_{IH}5$ max/min and $V_{IL}5$ max/min. For 3.3V signals, the final value is $V_{IH}3$ max/min and $V_{IL}3$ max/min. V_{IH} and V_{IL} may be found in the DC specifications.

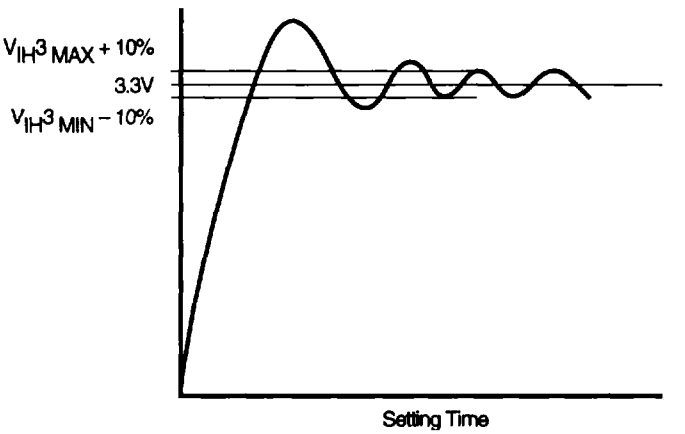
Most available simulation tools are unable to simulate settling time so that it accurately reflects silicon measurements. On a physical board, second order effects and other effects serve to dampen the signal at the receiver. Because of all these concerns, settling time is a recommendation or a tool for layout tuning and not a specification.

Settling time is simulated at the slow corner, to make sure that there is no impact on the flight times of the signals if the waveform has not settled. Settling time may be simulated with the diodes included or excluded from the input buffer model. If diodes are included, settling time recommendation will be easier to meet.

Although simulated settling time has not shown good correlation with physical, measured settling time, settling time simulations can still be used as a tool to tune layouts.

Use the following procedure to verify board simulation and tuning with concerns for settling time.

1. Simulate settling time at the slow corner for a particular signal.
2. If settling time violations occur (signal requires more than 12.5 ns to settle to ±10% of its final value), simulate signal trace with DC diodes in place at the receiver pin.
3. If settling time violations still occur, simulate flight times for 5 consecutive cycles for that particular signal.
4. If flight time values are consistent over the 5 simulations, settling time should not be a concern. If however, flight times are not consistent over the 5 simulations, tuning of the layout is required.
5. Note that, for signals that are allocated 2 cycles for flight time, the recommended settling time is doubled.



Maximum Settling Time to within 10% of V_{IH} or V_{IL} is 12.5ns.

Figure 14-16. Settling Time