GX4002 2x2 14.025Gb/s Crosspoint Switch with Trace Equalization and Output De-Emphasis

Key Features

- 2 x 2 crosspoint switch architecture
- Integrated CDR with 9.95 to 11.3Gb/s and 14.025Gb/s reference-free operation
- Automatic rate detect
- Dynamic on-chip power management control
- Multiple user-programmable power-down saving modes
- Independent programmable input trace equalization to reduce deterministic jitter (ISI)
- Independent programmable output pre-emphasis for driving long board traces
- Digital control through I^2C interface
- Integrated analog-to-digital converter, which provides access to digital diagnostic information on supply voltage and die temperature
- Integrated eye monitor and PRBS7 generator/checker
- Polarity invert, output mute functions available
- Single 3.3V supply (±5%)
- On-chip I/O termination
- Low power consumption: 600mW typical
  - Low power option for 4.25 & 8.5Gb/s operation: 415mW typical
- 5mm x 5mm 32-pin QFN package
- -40°C to +100°C case operation
- RoHS-compliant

Applications

- Enterprise and carrier applications
- 10GbE, Fibre Channel and InfiniBand networks
- Redundancy switching
- Retimer for 10Gb/s and 14Gb/s backplane and linecards

Description

The GX4002 is a low-power, high-speed 2 x 2 crosspoint switch, with robust signal conditioning circuits for driving and receiving high-speed signals through backplanes.

The device consumes as low as 600mW of power (typical) with all channels operational. Unused portions of the chip can be turned off in order to further reduce power consumption.

The signal conditioning features of the GX4002 include per-input clock and data recovery (CDR), programmable equalization and per-output programmable de-emphasis. The input equalizer removes ISI jitter—typically caused by PCB trace losses—by opening the input data eye in applications where long PCB traces are used. The integrated CDR "resets" the jitter budget, effectively erasing the signal distortion that can occur during transmission.

Output pre-emphasis capability provides a boost of the high-frequency content of the output signal, such that the data eye remains open after passing through a long interconnect of PCB traces and connectors.

The GX4002 features an integrated analog-to-digital converter, which, through the serial interface, provides digital diagnostic information about supply voltage and die temperature.

The GX4002 device is packaged in a small-outline 5mm × 5mm 32-pin, high-frequency QFN package with exposed pad.

The GX4002 is Pb-free, and the encapsulation compound does not contain halogenated flame retardant. This component and all homogeneous sub components are RoHS-compliant.

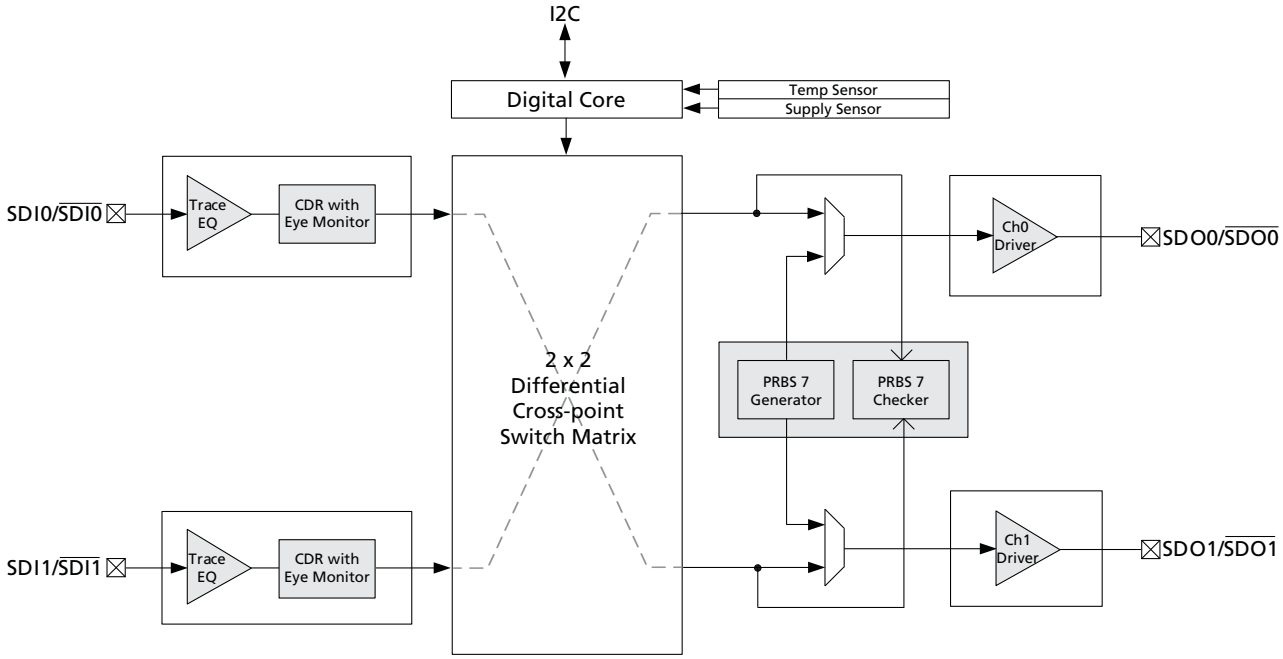


Figure A: GX4002 Functional Block Diagram

Revision History

Version	ECR	Date	Changes and / or Modifications
0	157889	March 2012	Ability to propagate loss of lock to Ch0FAULT pin was added.
C	157185	November 2011	Converted document to a Data Sheet. Updates throughout. Removed typical temperature monitor accuracy. Removed typical voltage monitor accuracy. Added AC common-mode channel characteristics. Added register 101 bits [5:3] to Table 7-1: Configuration and Status Register Map.
B	155955	March 2011	Correction to pin 21 and 23 in Table 1-1: Pin Descriptions.
A	155765	February 2011	New document.

Contents

1. Pin Out

1.1 Pin Assignment

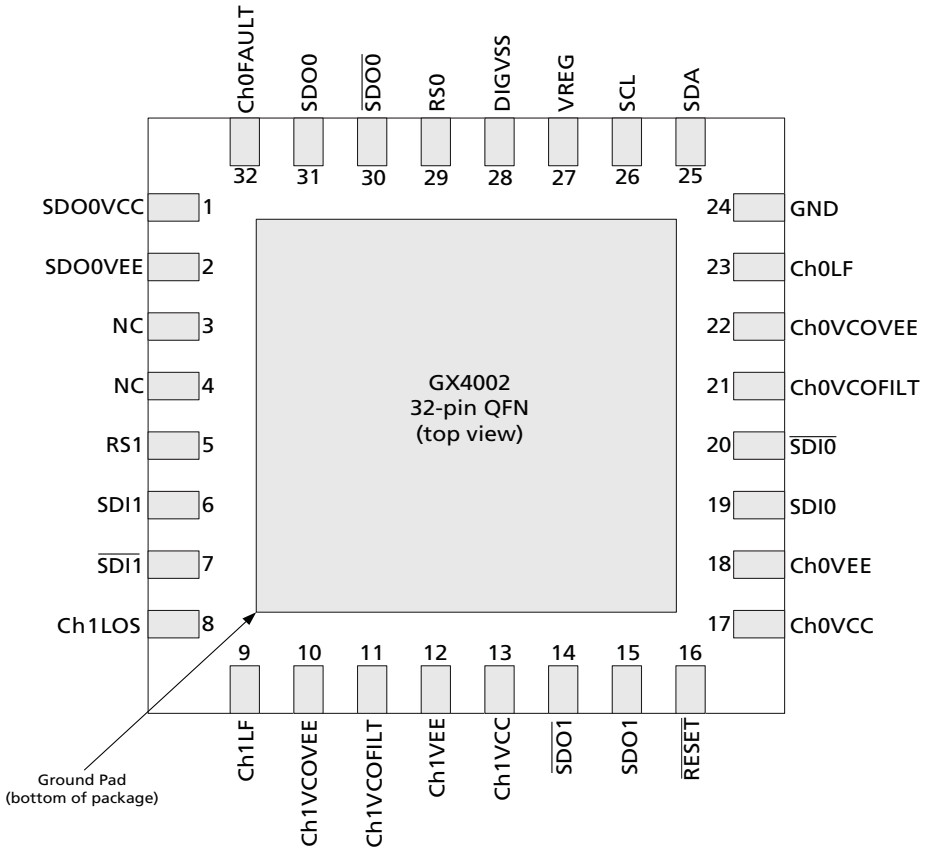


Figure 1-1: GX4002 Pin Assignment

1.2 Pin Descriptions

Table 1-1: Pin Descriptions

Pin #	Name	Type	Description
1	SDO0VCC	Power	Power supply for channel 0 path output.
2	SDO0VEE	Ground	Ground for channel 0 path output.
3, 4	NC	—	No connect.
5	RS1	Digital Input	Input Digital LVTTL/LVCMOS-compliant input. Rate Select Input for the Ch1 Signal Path. See Section 3.1 Multirate CDR Functionality for more details.
6, 7	SDI1, $\overline{\text{SDI1}}$	Input	High-speed input for the channel 1 signal path.
8	Ch1LOS	Digital Output	SFP+-compliant active-high digital output. Open-collector Loss-Of-Signal indicator for the channel 1 signal path. Requires an external pull-up resistor. When Ch1LOS is LOW, a valid channel 1 input signal has been detected. When Ch1LOS is high-impedance, a valid channel 1 input signal has not been detected. Configurable as LVTTL/LVCMOS-compliant output.
9	Ch1LF	Passive	Loop filter capacitor connection for the channel 1 signal path.
10	Ch1VCOVEE	Ground	Ground for the channel 1 signal path VCO.
11	Ch1VCOFILT	Passive	Filter for the channel 1 signal path VCO supply.
12	Ch1VEE	Ground	Ground for the channel 1 signal path and output.
13	Ch1VCC	Power	Power supply for the channel 1 signal path and output.
14, 15	$\overline{\text{SDO1}}$, SDO1	Output	High-speed differential output for the channel 1 signal path.
16	$\overline{\text{RESET}}$	Digital Input	Digital active-low LVTTL/LVCMOS-compliant Schmitt-trigger input. Device reset control pin. Includes an internal pull-down resistor to hold the device in a reset state during power-up, should this pin be externally disconnected.
17	Ch0VCC	Power	Power supply for the channel 0 signal path.
18	Ch0VEE	Ground	Ground for the channel 0 signal path.
19, 20	SDI0, $\overline{\text{SDI0}}$	Input	High-speed input for the channel 0 signal path.
21	Ch0VCOFILT	Passive	Filter for the channel 0 signal path VCO supply.
22	Ch0VCOVEE	Ground	Ground for the channel 0 signal path VCO.
23	Ch0LF	Passive	Loop filter capacitor connection for the Ch0 signal path.
24	GND	Ground	Connect to GND.
25	SDA	Digital Input/ Output	Digital active-high serial data signal for the host interface. Bi-directional, I^2C-compliant, open-drain driver/receiver.
26	SCL	Digital Input	Digital active-high clock input signal for the serial host interface.

Table 1-1: Pin Descriptions (Continued)

Pin #	Name	Type	Description
27	VREG	Passive	LDO regulator capacitor connection. (1.8V)
28	DIGVSS	Ground	Ground for low-speed digital I/O and internal logic.
29	RS0	Digital Input	Input Digital LVTTL/LVCMOS-compliant input. Rate Select Input for the Ch0 Signal Path. See Section 3.1 Multirate CDR Functionality for more details.
30, 31	$\overline{\text{SDO0}}$, SDO0	Output	High-speed differential output for the channel 0 signal path.
32	Ch0FAULT	Digital Output	SFP+-compliant active-high digital output. Open-collector Ch0FAULT indicator. Requires an external pull-up resistor. When Ch0FAULT is LOW, the channel 0 path output is operating properly. When Ch0FAULT is high-impedance, the device has detected a fault condition. The Ch0FAULT is latched, and may be cleared via the host interface or by strobing the Ch0DSBL pin. Can be configured as a LVTTL/LVCMOS compatible output.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Parameter	Value
Supply Voltage	-0.5 to +3.8V_{DC}
Input ESD Voltage	2kV
Storage Temperature Range	-50°C < T_A < 125°C
Input Voltage Range (any input pin)	-0.3 to 3.8V_{DC}*
Solder Reflow Temperature	260°C

***NOTE:** Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not applied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2.2 DC Electrical Characteristics

Table 2-1: DC Electrical Characteristics

V_{CC} = +2.8V to +3.47V, T_C = -40°C to 100°C. Typical values are V_{CC} = +3.3V and T_A = 25°C, unless otherwise specified.
Specifications assume default setting to end-terminated 50Ω transmission lines, unless otherwise stated. Typical Data Rate = 14.025Gb/s
Note: mApp refers to mA peak-to-peak value.

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
Supply Voltage		V_{CC}	2.8	3.3	3.47	V	—
Power			—	600	800	mW	1, 2
Control Logic Input Specifications							
Input Low Voltage		V_{IL}	0	—	0.4	V	—
Input High Voltage		V_{IH}	2.0	—	V_{CC}	V	—
Input Low Current	V_{IL} = 0V	I_{IL}	—	-100	—	µA	—
Input High Current	V_{IH} = 3.3V, V_{CC} = 3.3V	I_{IH}	—	100	—	µA	—
Status Indicator Output Specifications							
Indicator Output Logic LOW	I_{SINK}(max) = 3mA	V_{OL}	—	0.2	0.4	V	—

Table 2-1: DC Electrical Characteristics (Continued)

V_{CC} = +2.8V to +3.47V, T_C = -40°C to 100°C. Typical values are V_{CC} = +3.3V and T_A = 25°C, unless otherwise specified.
Specifications assume default setting to end-terminated 50Ω transmission lines, unless otherwise stated. Typical Data Rate = 14.025Gb/s
Note: mApp refers to mA peak-to-peak value.

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
Channel 0 Specifications							
Input Termination (SDI0)	Differential		80	100	120	Ω	—
Output Termination (SDO0)			—	50	—	Ω	—
Channel 1 Specifications							
Input Termination (Ch1SDIP/N)	Differential		80	100	120	Ω	—
Output Termination (Ch1SDOP/N)	Differential		80	100	120	Ω	—

NOTES:

1. Typical Conditions: T = 25°C, V = 3.3V. Maximum Conditions: T = 100°C, V = 3.467V.
2. Each output terminated.

2.2.1 Power Features

Table 2-2: Power Features

Configuration	Typical Baseline Power (mW)	Typical Incremental Power (mW)	Description	Feature Section
GX4002 Base	**600**			
SDO1 Pre-emphasis = 3dB @ 600mVppd	—	20	—	3.3.4
PRBS7 Generator	—	115	Path for PRBS7 generator to Ch1SDO is on.	3.6.1
PRBS7 Checker	—	125	PRBS7 checker is on.	3.6.1
Diag + ADC	—	14	Temperature, Supply Sensor, ADC.	3.7
Eye Monitor + ADC	—	50	All, Ch0 and Ch1 horizontal and vertical eye monitors are on.	3.6.2
Ch0 EQ Boost	—	0	—	3.2.1
GX4002 with Ch0 CDR bypassed and powered-down	—	-90mW	—	—
GX4002 with Ch1 & Ch0 CDR bypassed and powered-down	—	-185mW	—	—

2.3 AC Electrical Characteristics

Table 2-3: AC Electrical Characteristics

V_{CC} = +2.8V to +3.47V, T_C = -40°C to 100°C. Typical values are V_{CC} = +3.3V and T_A = 25°C, unless otherwise specified.
Specifications assume default setting to end-terminated 50Ω transmission lines, unless otherwise stated. Typical Data Rate = 14.025Gb/s

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
Data Rate	10G configuration		9.95	—	11.3	Gb/s	1
	16GFC configuration		—	14.025	—	Gb/s	1
Channel 0 Specifications							
Input Amplitude Range	differential		120	—	850	mVppd	—
LOS Threshold Level Setting Range			20	—	100	mVppd	—
Equalization Gain			—	6	—	dB	6
Jitter Transfer Bandwidth Setting Range	PRBS31 data		1	—	23	MHz	—
Total Output Jitter			—	0.1	0.25	UIpp	—
Ch0 CDR Lock Time	16G FC mode: loop filter cap = 100nF		—	—	0.5	ms	—
Ch0SDO Output Rise/Fall Time (minimum)	20% - 80%	t_r, t_f	—	—	20	ps	7
Ch0SDO Output Rise/Fall Time (maximum)	20% - 80%	t_r, t_f	40	—	—	ps	8
Channel 1 Specifications							
Input Sensitivity			—	—	10	mVppd	—
Input Overload			1200	—	—	mVppd	—
Limiting Amplifier Equalization	maximum EQ setting		14	—	—	dB	2
Jitter Transfer Bandwidth Setting Range			1	—	23	MHz	—
Ch1SDO Output Total Jitter	PRBS31 data	TJ	—	0.1	0.25	UIpp	—
Ch1SDO Output Rise/Fall time	20% - 80%	t_r, t_f	20	—	—	ps	—
Ch1SDO Output AC Common Mode Voltage			—	—	7.5	mVrms	3
Ch1LOS De-assert Threshold Level Setting Range	minimum programmable setting		—	5	—	mVppd	—
	maximum programmable setting		—	400	—	mVppd	—

Table 2-3: AC Electrical Characteristics (Continued)

V_{CC} = +2.8V to +3.47V, T_C = -40°C to 100°C. Typical values are V_{CC} = +3.3V and T_A = 25°C, unless otherwise specified.
Specifications assume default setting to end-terminated 50Ω transmission lines, unless otherwise stated. Typical Data Rate = 14.025Gb/s

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
Ch1LOS Threshold Level Variation	1 sigma, IC to IC		—	1.50	—	mVrms	—
	over V_{CC} Range		—	±0.5	—	dB	—
	over temperature range -40°C to +100°C		—	±0.5	—	dB	—
Ch1LOS Threshold Level Hysteresis Setting Range	electrical		0	—	6	dB	—
Ch1LOS Response Time			3	5	20	µs	—
Ch1 CDR Lock Time	16G FC mode: loop filter cap = 100nF		—	—	0.5	ms	4
Differential Output Voltage Setting Range	minimum swing setting		—	100	—	mVppd	—
	maximum swing setting		—	850	—	mVppd	—
Output Pre-emphasis Setting Range	maximum setting		3	—	—	dB	5

NOTES:

1. See Table 3-1 for details.
2. At 7GHz.
3. 600mVppd swing.
4. For loop bandwidth = 13MHz (as detailed in Table 3-4).
5. 600mVppd swing.
6. At 7GHz (dielectric loss).
7. Reg89[7:0] = "11001000" = Reg110[7:0]. Reg90[1:0] = "00" = Reg111[7:0]. Reg102[1:0] = "00". Reg118[4:3] = "11" = Reg119[4:3]. Reg80[7:0] = "11101110". Reg81[4:0] = "11100" = Reg103[4:0]. Reg82[4:0] = "11010" = Reg104[4:0].
8. Reg89[7:0] = "11111111" = Reg110[7:0]. Reg90[1:0] = "11" = Reg111[7:0]. Reg102[1:0] = "00". Reg118[4:3] = "00" = Reg119[4:3]. Reg80[7:0] = "01000100". Reg81[4:0] = "01000" = Reg103[4:0]. Reg82[4:0] = "10000" = Reg104[4:0].

2.4 Required Initialization Settings

The GX4002 configuration registers must be set as described in Table 2-4 below to meet the power specification listed in Table 2-1. The AC parametric specifications in Table 2-3 are also based on these settings:

Table 2-4: Required Initialization Settings

Register Name	Register Address (decimal)	Parameter Name	Bit Position	New Value (binary)	Valid Range (decimal)	Function
CH1_REG17	64	CH1PWR1	4:0	10101	0-31	Channel 1 power control
CH1_REG18	65	CH1PWR2	6:5	10	0-3	Channel 1 power control
CH0_REG15	45	CH0PWR1	4:0	10101	0-31	Channel 0 power control
CH0_REG16	46	CH0PWR2	4:3	10	0-3	Channel 0 power control

3. Detailed Description

3.1 Multirate CDR Functionality

There are two data rate ranges available for selection, so that a single part can be used for multiple applications. The GX4002 does not require a reference clock. Some example applications are as follows:

- 10Gb/s Ethernet (10.3Gb/s)
- 10Gb/s Ethernet with FEC (11.1Gb/s)
- 10G Fibre Channel (10.5Gb/s)
- 10G Fibre Channel with FEC (11.3Gb/s)
- Fibre Channel over Ethernet (10.3Gb/s)
- 16G Fibre Channel (14.025Gb/s)

Table 3-1: Mode Details

Mode	Description
10G	The part will retime in a continuous range from 9.95Gb/s to 11.3Gb/s.
14G	Through the serial interface, the part can be placed in 14G mode. In this mode, the CDRs will retime at 14.025Gb/s, and is intended for use in 16G Fibre Channel applications. An automatic rate detect circuit can be used that will determine if the incoming data rate is a legacy Fibre Channel rate, and will automatically bypass the CDRs. By using the automatic rate detect feature, RS0 and RS1 pins are not required. The automatic rate detect feature is not enabled by default when the device is configured in 14G mode.

3.1.1 Rate Selection and Rate Detection

The GX4002 has three different methods to select the data rate. The rate can be selected through the use of the RS0/RS1 pins, through the use of registers, or through automatic detection. The rate selection methods are described in more detail below.

The GX4002 also contains a set of data-dependent registers. This enables parameters such as rise and fall times to be automatically configured based on the data rate. There are two profiles, one for low data rates such as 4G or 8G Fibre Channel, and one for high data rates such as 10GbE or 16G Fibre Channel. The register map (Appendix: Configuration and Status Register Map) shows which registers contain both low data rate and high data rate options.

A configuration profile is invoked by one of three methods:

1. Using input pins RS0 and RS1 to invoke a “hard” rate select for either the Ch0 path or Ch1 path respectively (CH0PLLRATESELVAL is HIGH and/or CH1PLLRATESELVAL is HIGH).
2. Using host interface commands to invoke a “soft” rate select for either the Ch1 or Ch0 path, or for both Ch1 and Ch0 paths together using the CH1PLLRATESEL and CH0PLLRATESEL bits (CH1PLLRATESELVAL is HIGH and/or CH0PLLRATESELVAL is HIGH).

3. Using on-chip automatic rate detection circuitry to detect the new data rate, and to invoke an internal rate select in either the Ch1 or Ch0 path independently. The application is defined using the RATEDETFCGBEN bits (CH1PLLRATESELVAL is LOW and/or CH0PLLRATESELVAL is LOW).

Rate Selection Method	Rate Select Valid Register	RS0/RS1 Pins	Rate Select Registers	Fibre Channel/ Ethernet Register	Operation	Data Rate Dependent Register Set Used
Hard Rate Select	HIGH	LOW	LOW	Not Applicable	The CDRs are placed in bypass mode. Intended for 2G/4G/8G Fibre Channel or 1GbE	Low Data Rate Profile
		HIGH	Not Applicable	Fibre Channel	The CDR will lock to 14.025Gb/s data	High Data Rate Profile
				Ethernet	The CDR will lock to 9.95G to 11.3Gb/s data	High Data Rate Profile
Soft Rate Select	HIGH	Low or High Z	LOW	Not Applicable	The CDRs are place in bypass mode. Intended for 2G/4G/8G Fibre Channel or 1GbE	Low Data Rate Profile
		Not Applicable	High	Fibre Channel	The CDR will lock to 14.025Gb/s data	High Data Rate Profile
				Ethernet	The CDR will lock to 9.95G to 11.3Gb/s data	High Data Rate Profile
Automatic Rate Detect	LOW	Not Applicable	Not Applicable	Fibre Channel	If the input data is 14.025Gb/s, the CDR will lock to it. Otherwise, the CDRs are automatically bypassed	If 14.025Gb/s is detected: High Data Rate Profile If 14.025Gb/s is not detected: Low Data Rate Profile
				Ethernet	If the input data is 9.95G to 11.3G, the CDR will lock to it. Otherwise, the CDRs are automatically bypassed	If 9.95G to 11.3Gb/s is detected: High Data Rate Profile If 9.95G to 11.3Gb/s is not detected: Low Data Rate Profile

3.1.1.1 Hard Rate Select (Rate Select Pins)

The RS0 pin controls the rate-dependent profile of the Ch0 path, and the RS1 pin controls the rate-dependent profile of the Ch1 path. The rate select valid bit, CH0PLLRATESELVAL (or CH1PLLRATESELVAL), must be HIGH for RS0 (or RS1) to control the rate.

When the RS0 (or RS1) pin is held LOW, the low-speed rate-dependent registers of the channel 0 (or channel 1) path are active. When the RS0 (or RS1) pin is held HIGH, the high-speed rate-dependent profile of the channel 0 (or channel 1) path is active. RS0 is logically OR'ed with CH0PLLRATESEL, while RS1 is logically OR'ed with CH1PLLRATESEL. Due to the OR'ing operation, when RS0 and RS1 are used for rate control, CH0PLLRATESEL and CH1PLLRATESEL must be set LOW.

3.1.1.2 Soft Rate Select

The CH1PLLRATESEL and CH0PLLRATESEL bits can be programmed to select a rate profile using the host interface. Setting these parameters and their associated valid parameters (CH1PLLRATESELVAL and CH0PLLRATESELVAL) override the on-chip automatic rate detection circuitry. CH0PLLRATESEL is logically OR'd with the RS0 pin, while CH1PLLRATESEL is logically OR'd with RS1, so RS0 and RS1 must be LOW or hi-impedance for the PLLRATESEL bits to function properly.

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
CH0PLL_REG5	14	CH0PLLRATESEL	3:3	RW	1	0-1	Selects data rates: 0 = 1.25 - 8.5G, 1= 10.3G or 14.025G.
	14	CH0PLLRATESELVAL	4:4	RW	1	0-1	When HIGH, CH0PLLRATESEL or RS0 are valid, otherwise they are ignored.
CH1PLL_REG5	24	CH1PLLRATESEL	3:3	RW	1	0-1	Selects data rates: 0 = 1.25 - 8.5G, 1= 10.3G or 14.025G.
	24	CH1PLLRATESELVAL	4:4	RW	1	0-1	When HIGH, CH1PLLRATESEL or RS1 are valid, otherwise they are ignored.

The default setting is the high (10Gb/s or 14.025Gb/s) data-rate profile, with the on-chip automatic rate detection circuitry overridden.

3.1.1.3 Automatic Rate Detection

In addition to the controls outlined in the preceding tables, the auto rate detection circuitry has the following controls. To enable operation of the auto rate detection function, CH0RATEDETEN (or CH1RATEDETEN) can be set HIGH.

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
CH0RDET_REG1	67	CH0RATEDETRESET	0	RW	0	0-1	When HIGH, the Ch0 path rate detector is reset.
		CH0RATEDETEN	1	RW	1	0-1	When HIGH, enables the rate detector.
CH0RDET_REG2	68	CH0RATEDETRATEPER	3:0	RW	1000	0-15	Rate detector rate period (0.3µs to 13ms, 100µs default).
CH1RDET_REG1	72	CH1RATEDETRESET	0	RW	0	0-1	When HIGH, the Ch1 path rate detector is reset.
		CH1RATEDETEN	1	RW	1	0-1	When HIGH, enables the rate detector
CH1RDET_REG2	73	CH1RATEDETRATEPER	3:0	RW	1000	0-15	Rate detector rate period (0.3µs to 13ms, 100µs default).

If CH1RATEDETEN (or CH0RATEDETEN) is LOW, the CH1PLLRATESELVAL (or CH0PLLRATESELVAL) bit must be HIGH, otherwise the device will be in an undefined state.

CH0RATEDETPERIOD (address 68) and CH1RATEDETPERIOD (address 73) control the frequency at which the automatic rate detection block checks the lock state of the PLL. The recommended setting for shortest lock time is 1001b.

3.1.1.4 Application-Dependent Rate Select Profiles

The RATEDETFCGBEN and RATEDETFCGBENVAL bits indicate whether the application traffic is running Fibre Channel, Ethernet or unspecified (for example: the transceiver may be required to handle either Fibre Channel or Ethernet traffic in mission mode). The default setting is Fibre Channel traffic.

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
CH0RDET_REG1	67	RATEDETFCGBEN	2:2	RW	1	0-1	When HIGH, the application is Fibre Channel. When LOW, the application is Ethernet.
		RATEDETFCGBENVAL	3:3	RW	1	0-1	When HIGH, indicates that RATEDETFCGBEN is valid. When LOW, it is ignored.

Table 3-2: Summary of Rate Selection and Rate Detection Control

CH1PLLRATESELVAL CH0PLLRATESELVAL	RATEDETFCGBENVAL	Data Rate	Configuration Profile
0	0	Undefined	Undefined
0	1	Auto Rate Detect	Profile selected based on detected rate
1	0	Auto Rate Detect	Profile selected by hard or soft rate select
1	1	Fixed rate determined by the combination of RATEDETFCGBEN and rate select (hard or soft)	Profile selected by hard or soft rate select

3.1.2 Auto Retimer Bypass

The GX4002 supports an automatic rate detect feature for legacy Fibre Channel data rates when configured in 16G mode. Upon enabling the automatic rate detect feature, the device constantly monitors incoming data for a valid 14.025Gb/s data rate. If the input data rate is a legacy Fibre Channel rate, the CDR is automatically bypassed.

While the automatic rate detect feature is enabled, and the CDR is in bypass mode, the device continues monitoring the incoming data rate. If the data rate changes to 14.025Gb/s, the CDR goes back into retimed mode.

The auto retimer bypass feature also applies to Ethernet mode.

The following registers enable and configure the automatic rate detect feature:

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
CH0PLL_REG5	14	CH0PLLBYPASS	1:1	RW	0	0-1	When HIGH, forces CDR into bypass mode.
		CH0PLLAUTOBYPASSEN	2:2	RW	1	0-1	When HIGH, enables automatic bypass mode for the Ch0 CDR.
CH0RDET_REG1	67	CH0RATEDETRESET	0:0	RW	0	0-1	When HIGH, resets the Ch0 path rate detector.
		CH0RATEDETEN	1:1	RW	1	0-1	When HIGH, enables the Ch0 path automatic rate detector.
CH1RDET_REG1	72	CH1RATEDETRESET	0:0	RW	0	0-1	When HIGH, resets the Ch1 path rate detector.
		CH1RATEDETEN	1:1	RW	1	0-1	When HIGH, enables the Ch1 path automatic rate detector.

The device can be configured to manually bypass each of the Ch1 and Ch0 CDRs through the CH0PLLBYPASS and CH1PLLBYPASS controls when the automatic bypass is disabled.

3.2 Channel 0 Path (Ch0)

The channel 0 path is comprised of a trace equalizer, a multi-rate CDR and an output driver.

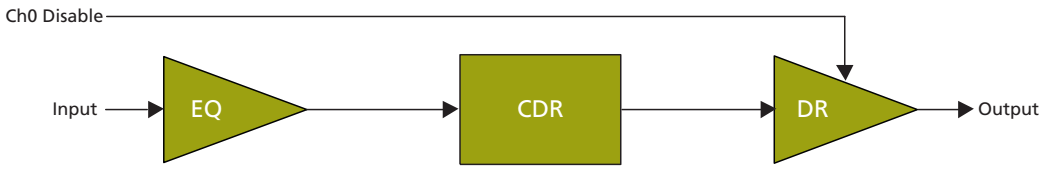


Figure 3-1: Channel 0 Path

3.2.1 Ch0 Equalization

The channel 0 path input has an equalizer with 6dB gain at 7GHz. The equalizer can be bypassed through the following register:

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
CH0_REG3	33	CH0EQBOOST	0:0	RW	1	0-1	When HIGH, applies a fixed CH0 EQ boost of 6dB. 0dB if LOW.

3.2.2 Ch0 PLL Variable Loop Bandwidth

The loop bandwidth of the channel 0 Phase Locked Loop (PLL) can be varied through the digital control interface. The loop bandwidths are individually controlled, and can cover the range of 1MHz to 23MHz through following five-bit registers (recommended settings are shown):

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
CH0PLL_REG1	10	CH0PLLLBWCURVT	4:0	RW	10011	0-31	Adjusts LBW positive temperature coefficient control.
CH0PLL_REG2	11	CH0PLLLBWCURVBE	4:0	RW	01110	0-31	Adjusts LBW negative temperature coefficient control.
CH0PLL_REG9	18	CH0PLLLBWMULT	1:0	RW	10	0-3	LBW multiplier; 00 = 0.67, 10 = 1, 01 = 1.33, 11 = 1.67

The temperature coefficient of the loop bandwidth can be adjusted by weighted summation of CH0PLLLBWCURVT, which has a positive temperature coefficient and CH0PLLLBWCURVBE, which has a negative temperature coefficient. The default reset values of the registers above produce an approximate loop bandwidth of 7MHz.

Table 3-3: Typical Loop Bandwidths for Various Register Settings

CH0PLLLBWMULT	CH0PLLLBWCURVT	CH0PLLLBWCURVBE	Loop Bandwidth
00	10011	01110	4.6MHz
10 (default)	10011	01110	7.3MHz
01	10011	01110	9.9MHz
10	11111	10110	13MHz
11	11000	11000	22.7MHz

3.2.3 Channel 0 Output Polarity Invert

The channel 0 output polarity can be inverted through the following register:

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
CH0PLL_REG5	14	CH0PLLPOLINV	0:0	RW	0	0-1	When HIGH, inverts the Ch0 data path polarity.

3.3 Channel 1 Path (Ch1)

The GX4002 channel 1 path contains a high-sensitivity limiting amplifier with optional equalization, a multi-rate CDR, and a pre-emphasis driver.

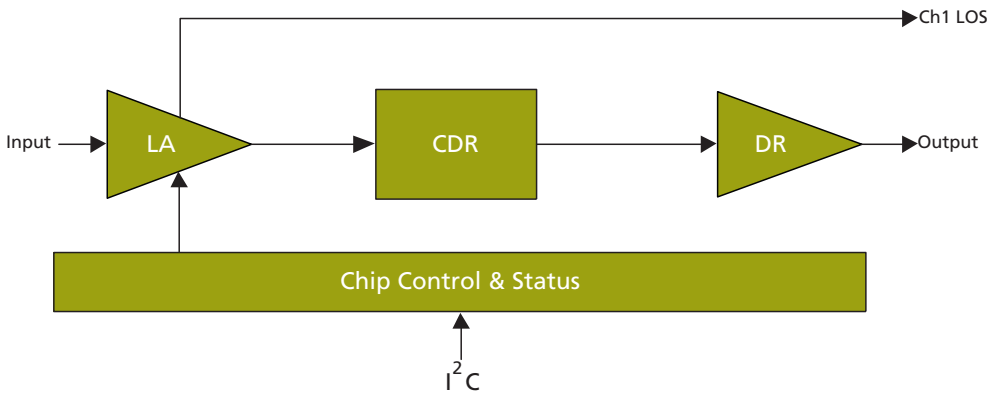


Figure 3-2: Channel 1 Path

3.3.1 Integrated Limiting Amplifier

The GX4002 has an integrated Limiting Amplifier (LA), with better than 10mV sensitivity. Optional equalization is available on the limiting amplifier input.

3.3.2 Ch1 Equalization

The channel 1 input implements an equalizer that provides peaking at 7GHz. This feature allows for optimal performance with extended reach connections.

The equalizer implements 0dB to 14dB of high-frequency boost in fifteen steps, while achieving optimal receive sensitivity at any given equalization setting. The equalization setting is set through the CH1LABOOST control.

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
CH1_REG1	48	CH1LABOOST	3:0	RW	0000	0-15	0: 0dB to 15: 14dB.

When the equalization setting is 0dB, the equalization function is bypassed and the receive sensitivity performance is the same as that of a limiting amplifier.

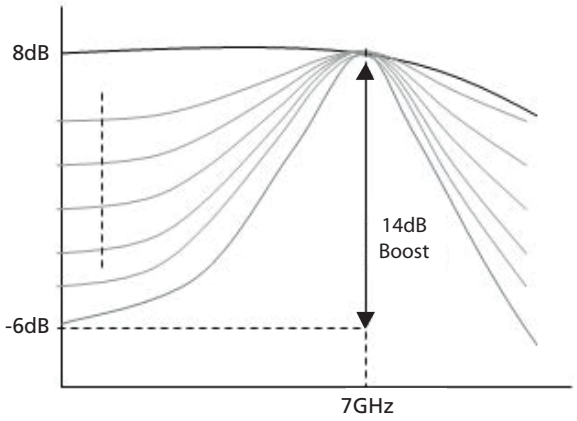


Figure 3-3: Channel 1 Equalization

3.3.3 Ch1 PLL Variable Loop Bandwidth

The loop bandwidth of the channel 1 Phase Locked Loops (PLLs) can be varied through the digital control interface. The loop bandwidths are individually controlled, and can cover a range of 1MHz to 23MHz through the following 5-bit registers:

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
CH1PLL_REG1	20	CH1PLLLBWCURVT	4:0	RW	10011	0-31	Adjusts LBW positive temperature coefficient control.
CH1PLL_REG2	21	CH1PLLLBWCURVBE	4:0	RW	01110	0-31	Adjusts LBW negative temperature coefficient control.
CH1PLL_REG9	28	CH1PLLLBWMULT	7:6	RW	10	0-3	LBW multiplier; 00 = 0.67, 10 = 1, 01 = 1.33, 11 = 1.67

The temperature coefficient of the loop bandwidth can be adjusted by a weighted summation of CH1PLLLBWCURVT, which has a positive temperature coefficient, and CH1PLLLBWCURVBE, which has a negative temperature coefficient. The default reset values of the above registers produce an approximate loop bandwidth of 7MHz.

Table 3-4: Typical Loop Bandwidths for Various Register Settings

CH1PLLLBWMULT	CH1PLLLBWCURVT	CH1PLLLBWCURVBE	Loop Bandwidth
00	10011	01110	4.6MHz
10 (default)	10011	01110	7.3MHz
01	10011	01110	9.9MHz

Table 3-4: Typical Loop Bandwidths for Various Register Settings (Continued)

CH1PLLLBWMULT	CH1PLLLBWCURVT	CH1PLLLBWCURVBE	Loop Bandwidth
10	11111	10110	13MHz
11	11000	11000	22.7MHz

3.3.4 Pre-Emphasis Driver with Auto-Mute

The channel 1 driver is a pre-emphasis driver that can be used to compensate for losses in the connector and trace between the module and ASIC. The pre-emphasis can compensate for up to 6dB of loss. The output swing can be set from 100mV to 800mV in steps of 50mV through the CH1SDOSWING[3:0] register. The pre-emphasis amplitude can be varied from 0dB to 6dB in eight non-linear steps through CH1SDOPECTRL[4:2].

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
CH1SDO_REG1	77	CH1SDOSWING	3:0	RW	1010	0-15	Driver swing. 0-15: 100-850mVppd, Default = 10: 600mV
CH1SDO_REG2	78	CH1SDOPECTRL	4:2	RW	000	0-7	Pre-emphasis amplitude. 0: 0dB, 7: 6dB for 200mVppd swing.

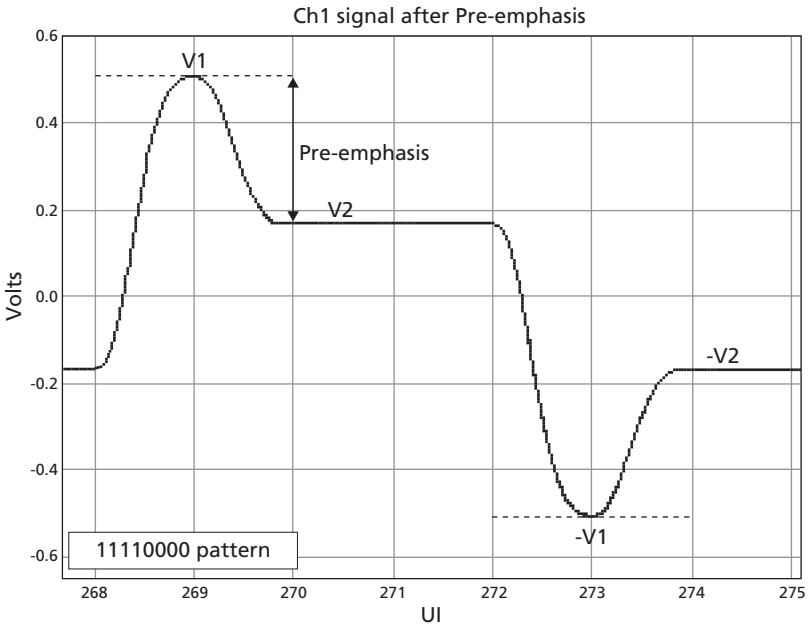


Figure 3-4: Pre-Emphasis Waveform Description

Figure 3-4 above shows the pre-emphasis waveform. Amplitudes V1, V2 and pre-emphasis in dB are defined as follows:

V1, ***V2*** and ***Pre-emphasis*** are defined as follows:

V1 which represents the “peak”
V2 which represents DC or Steady State
Pre-emphasis [dB] = 20 x log(V1/V2)

The amount of pre-emphasis varies with CH1SDOSWING as shown in Table 3-5:

Table 3-5: Pre-Emphasis vs. Ch1 SDO Swing

CH1SDOSWING	CH1SDOPECTRL	Pre-emphasis
0010 (200mV)	001	2.3dB
0101 (350mV)	001	1.8dB
1010 (600mV)	001	1.0dB
0010 (200mV)	011	4.7dB
0101 (350mV)	011	3.8dB
1010 (600mV)	011	3.1dB
0010 (200mV)	111	6.2dB
0101 (350mV)	111	5.5dB
1010 (600mV)	111	3.4dB

The output can be configured to automatically mute if Ch1 LOS is detected through the following registers. When muted, the output driver remains powered-up, and the output common mode is maintained. The output driver can be configured to power-down when muted by setting the CH1SDOPWRDNONMUTE bit:

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
CH1SDO_REG3	79	CH1SDOMUTE	5:5	RW	0	0-1	When HIGH, mutes driver and maintains output common mode when not in auto mute mode.
		CH1SDOAUTOMUTEEN	6:6	RW	1	0-1	When HIGH, enables muting the driver upon LOS. LOW disables muting.
		CH1SDOPWRDNONMUTE	7:7	RW	1	0-1	When HIGH, enables power-down on mute for output stage. LOW disables power-down.

3.3.5 Channel 1 Output Polarity Invert

The channel 1 output polarity can be inverted through the following register:

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
CH1PLL_REG5	24	CH1PLLPOLINV	0:0	RW	0	0-1	When HIGH, inverts the Ch1 data path polarity.

3.4 Crosspoint

The GX4002 provides eight different crosspoint paths, as shown in Table 3-6. The blocks referenced in the different crosspoint paths are shown in Figure 3-5.

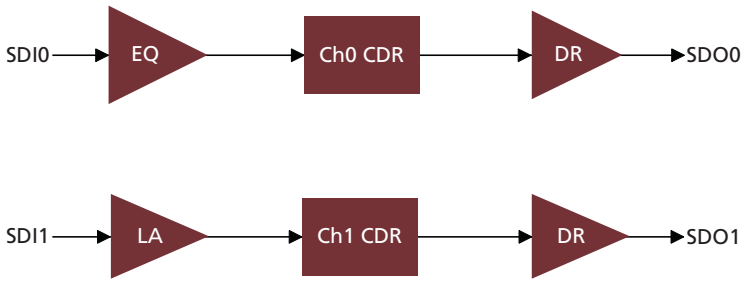


Figure 3-5: Crosspoint Block Diagram

Table 3-6: Crosspoint Paths

Mode	Crosspoint Path	Reference
1	SDI1 =>LA=>DR=>SDO0	Figure 3-6
2	SDI1 =>LA=>CH1CDR=>DR=>SDO0	Figure 3-6
3	SDI1 =>LA=>CH0CDR=>DR=>SDO0	Figure 3-7
4	SDI1 =>LA=>CH1CDR=>CH0CDR=>DR=>SDO0	Figure 3-7
5	SDI0=>EQ=>DR=>SDO1	Figure 3-8
6	SDI0=>EQ=>CH0CDR=>DR=>SDO1	Figure 3-8
7	SDI0=>EQ=>CH1CDR=>DR=>SDO1	Figure 3-9
8	SDI0=>EQ=>CH0CDR=>CH1CDR=>DR=>SDO1	Figure 3-9

When the crosspoint is enabled, the standard data path is not interrupted. For example: in Mode 1, the input to SDI1 will also be accessible at SDO1. When using crosspoint modes, the automute feature for SDO1 or SDO0 may have to be disabled if the corresponding SDI1 or SDI0 inputs are unused.

The relevant parameters in these registers and their values required to enable each of the crosspoint options indicated above, are shown in Table 3-7.

The selection of a crosspoint path impacts the following feature:

- Polarity inversion

Table 3-7 also captures the impact on these features in each crosspoint mode.

Table 3-7: Crosspoint Options

Crosspoint Mode (see Table 3-6)	LBCH1IINEN	LBCH1INPRBSGEN	LBCH1INCH0DATA	LBCH1OUTEN	LBCH1OUTCH0DATA	LBCh1OutPRBSGen	LBCH1OUTCH1CLK	CH1PLLBYPASS	LBCH0INEN	LBCH0INPRBSGEN	LBCH0INCH1DATA	LBCH0OUTEN	LBCH0OUTCH1DATA	LBCH0OUTPRBSGEN	LBCH0OUTCH0CLK	CH0PLLBYPASS	CH0PLLPOLINV Effective	CH0PLLPOLINV Effective
1	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0	Y	N
2	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	Y	N
3	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0	Y	N
4	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	Y	N
5	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	N	Y
6	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	N	Y
7	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	N	Y
8	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	N	Y
Control Register Address	7	7	7	7	7	7	7	24	8	8	8	8	8	8	8	14	—	—
Associated Bit Slice	0	1	2	4	5	6	7	1	0	1	2	4	5	6	7	1	—	—

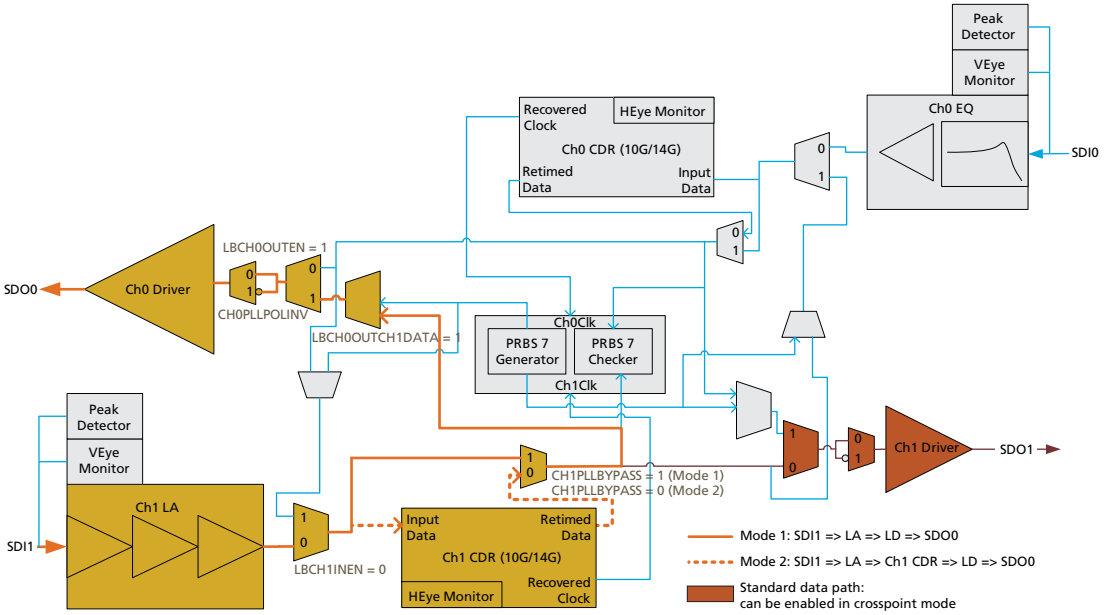


Figure 3-6: Crosspoint Modes 1 & 2

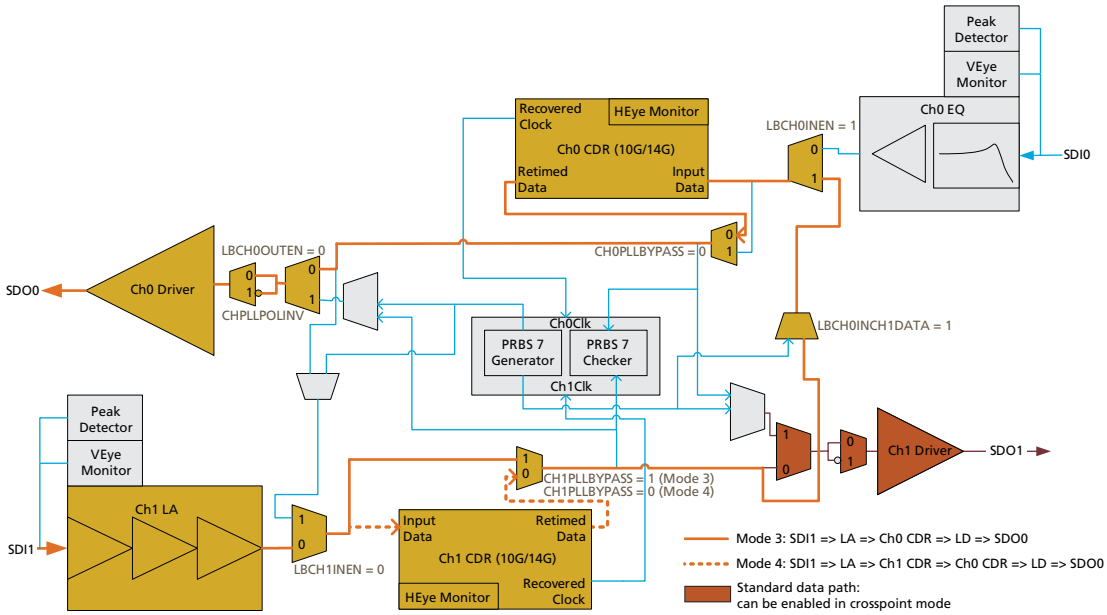


Figure 3-7: Crosspoint Modes 3 & 4

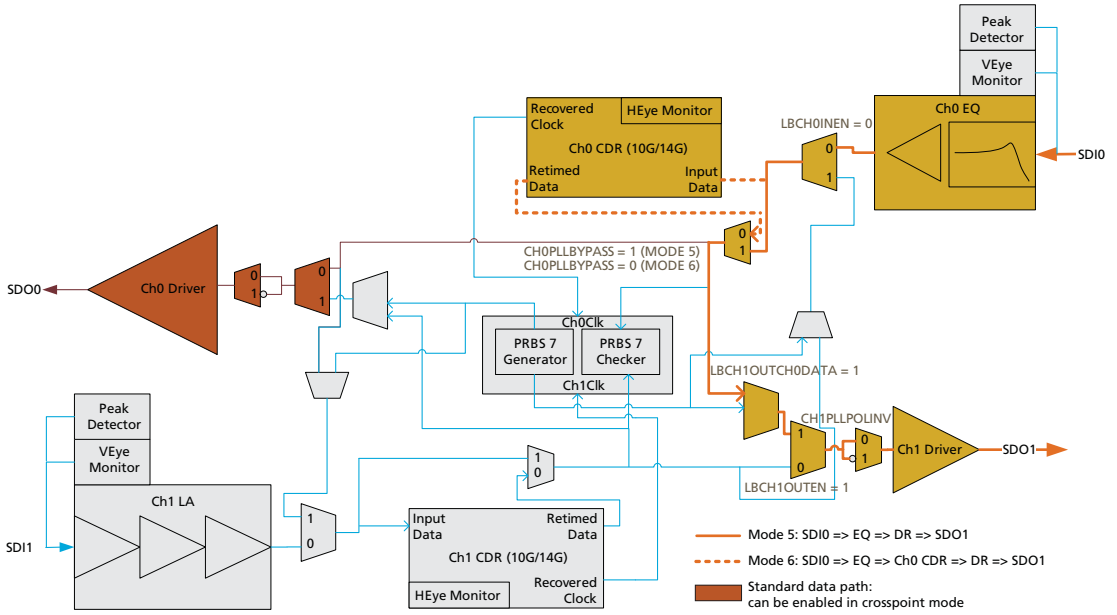


Figure 3-8: Crosspoint Modes 5 & 6

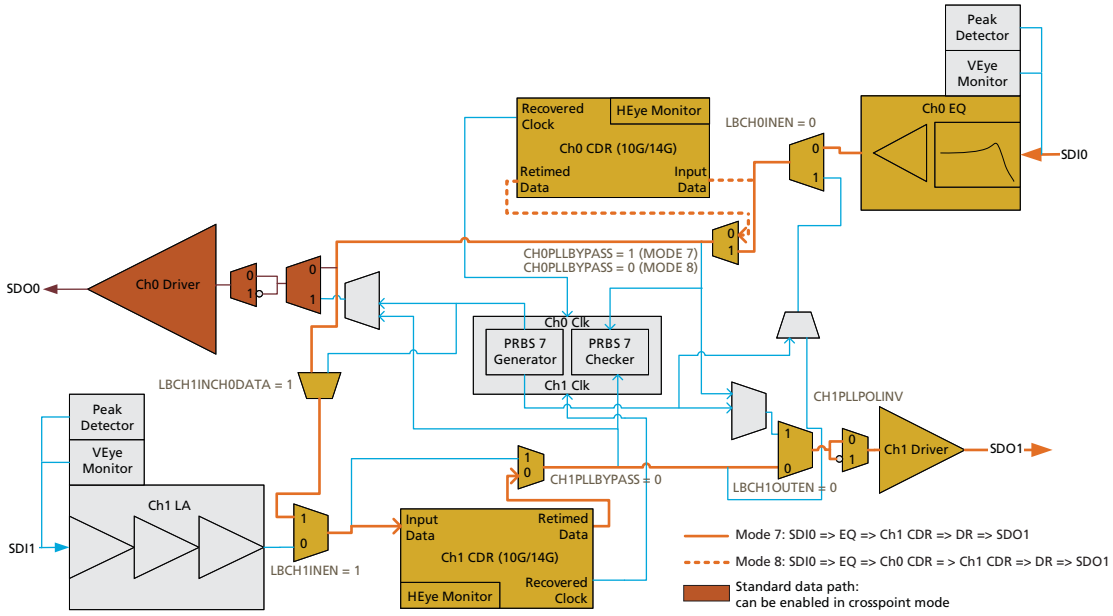


Figure 3-9: Crosspoint Modes 7 & 8

3.5 Status Indicators

The GX4002 supports three status indicators: Loss of Signal (LOS), Loss of Lock (LOL) and Channel 0 Fault (Ch0FAULT). LOS and LOL indicators are available on both the Ch1 and the Ch0 paths.

3.5.1 Ch0 Loss Of Signal (LOS)

The Ch0 LOS indicator status is available through a register. If desired, its status can be included in the generation of the Ch0FAULT output pin. The LOS assert threshold can be set from 20mV to 100mV in <1mV steps. In addition, the temperature coefficient of the LOS threshold can be adjusted to ensure consistent LOS operation over temperature. The LOS also has hysteresis that is programmable from 0dB to 6dB in steps of 0.5dB.

The following registers are used to control the Ch0 LOS feature:

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
CH0_REG9	39	CH0LOSTHNEG	7:0	RW	01010011	0-255	Negative temperature coefficient LOS threshold setting.
CH0_REG10	40	CH0LOSTHPOS	7:0	RW	00000000	0-255	Positive temperature coefficient LOS threshold setting.
CH0_REG11	41	CH0LOSHYS	3:0	RW	1001	0-15	Sets LOS hysteresis from 0dB to 6dB in steps of 0.5dB.
CH0_REG12	42	CH0LOSSOFTASSERT	3:3	RW	0	0-1	When HIGH, asserts LOS for internal functions, asserts LOS register (CH0PLLLOS) and asserts external indication through Ch0FAULT.
		CH0LOSSOFTASSERTEN	4:4	RW	0	0-1	When HIGH, LOS is controlled by CH0LOSSOFTASSERT.

3.5.1.1 Ch0 LOS Threshold

Figure 3-10 and Figure 3-11 show the typical recommended range of Ch0 LOS assert thresholds and corresponding CH0LOSTHNEG[7:0] setting to achieve these thresholds. It is recommended to keep CH0LOSPOS[7:0] = 0 to achieve a flat temperature coefficient for LOS threshold. The Ch0 LOS de-assert thresholds are the same as the Ch0 LOS assert thresholds for a hysteresis setting of 0.

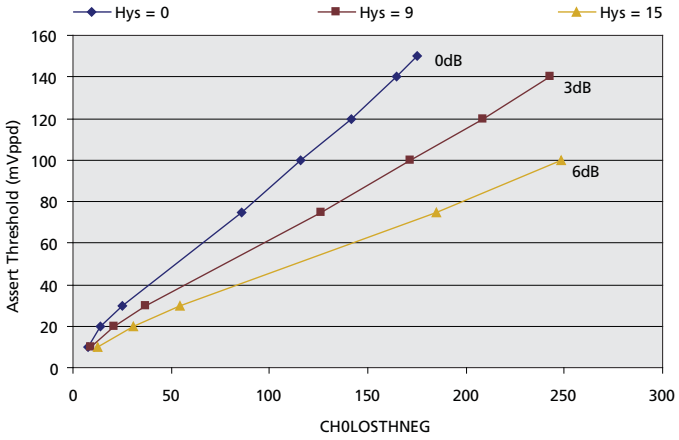


Figure 3-10: Ch0 LOS Assert Threshold – Typical

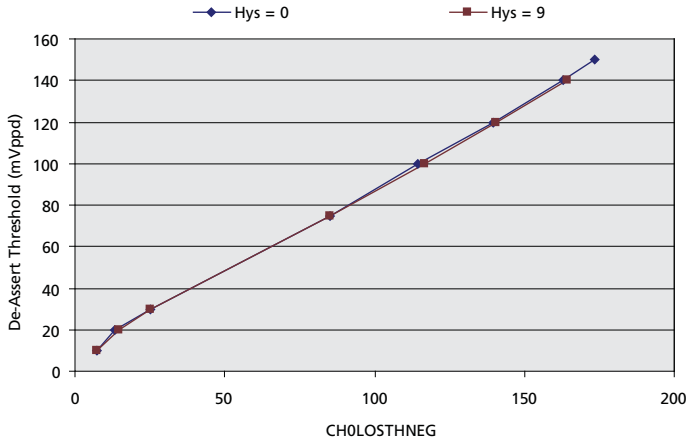


Figure 3-11: Ch0 LOS De-Assert Threshold – Typical

The LOS threshold will have a slight dependence on data rate.

3.5.1.2 Manual LOS Assert

The on-chip LOS circuit can be bypassed, and LOS asserted, through the host interface. This operation is initiated when **CH0LOSSOFTASSERTEN** is HIGH. The state of **CH0LOSSOFTASSERT** then controls the LOS register **CH0PLLLOS** and external indication through Ch0FAULT.

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
CH0_REG12	61	CH0LOSSOFTASSERT	3:3	RW	0	0-1	When HIGH, asserts LOS. CH0LOSSOFTASSERTEN must be HIGH to use this bit.
		CH0LOSSOFTASSERTEN	4:4	RW	0	0-1	When HIGH, LOS is controlled by CH0LOSSOFTASSERT.

3.5.2 Ch1 Loss Of Signal

The Ch1 Loss Of Signal (LOS) indicator status is available through a register and the Ch1LOS pin. The Ch1LOS pin is by default open-drain, active-high. However, the pin can be configured in a LVCMOS/LVTTL compatible mode by setting OPENDRAINCH1LOS to 0. In addition, Ch1LOS can be configured to be active-low by setting POLINVCH1LOS HIGH. The status of Ch1LOS can be read out through CH1PLLLOS.

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
TOP_REG2	2	POLINVCH1LOS	1:1	RW	0	0-1	When HIGH, inverts polarity of Ch1LOS output.
		OPENDRAINCH1LOS	2:2	RW	1	0-1	When HIGH, makes Ch1LOS output driver open-drain.
CH1PLL_REG10	29	CH1PLLLOS	0:0	RO	0	0-1	Ch1 CDR loss of signal when HIGH.

The LOS assert threshold can be set from 5mV to 400mV in three distinct ranges. The LOS assert threshold is a function of the CH1LABOOST setting. Figure 3-8 describes the selection of CH1LOSRANGE based on the required LOS assert threshold and CH1LABOOST settings.

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
CH1_REG14	61	CH1LOSRANGE	2:0	RW	001	0-7	1:0 - LOS range 0: highest - 3: lowest, 2 (MSB) unused.

Table 3-8: LOS Assert Ranges

CH1LABOOST [3:0]	LOS Assert Threshold Range		CH1LOSRANGE [1:0]	Resolution (controlled by CH1LOSTHNEG/POS)	Unit
	Min	Max			
	5	400	LOS Threshold - Total Range	—	mVppd
0-7	—	—	11 - Unused	—	—
0-7	5	30	10 - Low Range	<0.1mV	mVppd
0-7	30	100	01 - Mid Range	<1.0mV	mVppd
0-7	100	400	00 - High Range	<2.0mV	mVppd
8-15	5	30	11 - Low Range	<0.1mV	mVppd
8-15	30	100	10 - Mid Range	<1.0mV	mVppd
8-15	—	—	01 - Unused	—	—
8-15	100	400	00 - High Range	<2.0mV	mVppd

3.5.2.1 Ch1 LOS Threshold

The LOS assert threshold is set using the following registers. Apart from setting the assert thresholds, these registers also set the temperature coefficient. Through weighted summing of the CH1LOSTHNEG[7:0] and CH1LOSTHPOS[7:0] values, a range of temperature coefficients can be achieved to ensure consistent LOS operation over temperature:

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
CH1_REG9	56	CH1LOSTHNEG	7:0	RW	10000011	0-255	Negative temperature coefficient LOS threshold setting.
CH1_REG10	57	CH1LOSTHPOS	7:0	RW	00010001	0-255	Positive temperature coefficient LOS threshold setting.

Figure 3-12 to Figure 3-15 show the typical recommended range of CH1LOSASSERT thresholds and corresponding CH1LOSTHNEG[7:0] setting to achieve these thresholds. It is recommended to keep CH1LOSPOS[7:0] = 0. The CH1LOSDEASSERT thresholds are the same as the CH1LOSASSERT thresholds for a hysteresis setting of 0.

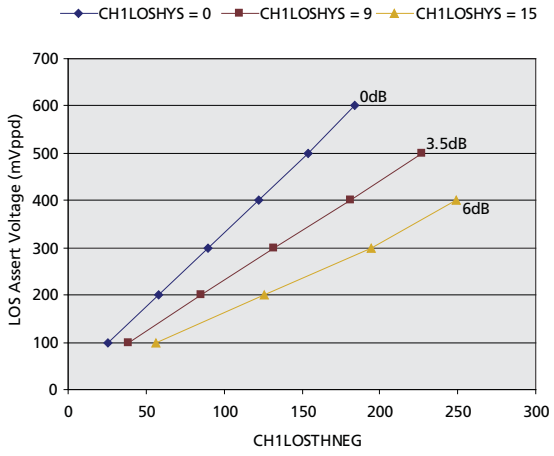


Figure 3-12: Ch1 LOS Threshold vs. Hysteresis (CH1LOSRANGE = 0)

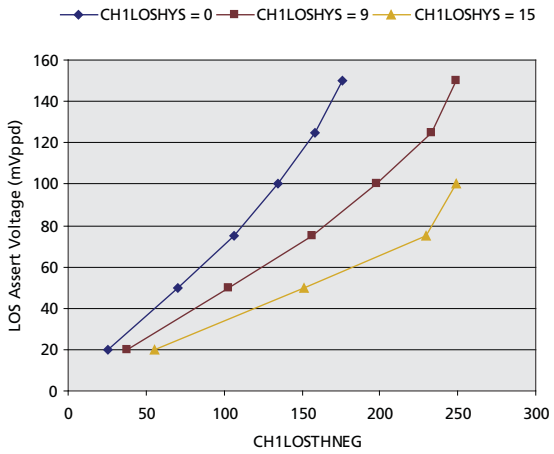


Figure 3-13: Ch1 LOS Threshold vs. Hysteresis (CH1LOSRANGE = 1)

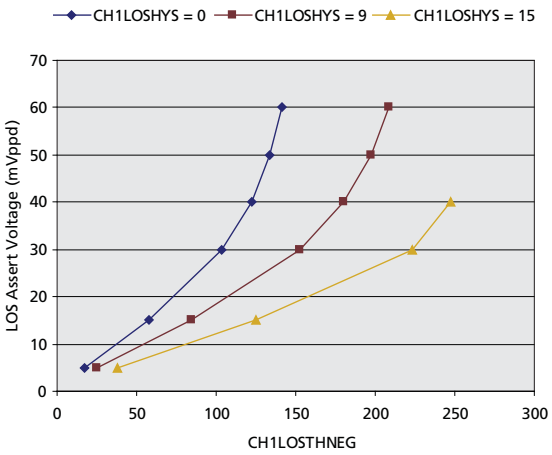


Figure 3-14: Ch1 LOS Threshold vs. Hysteresis (CH1LOSRANGE = 2)

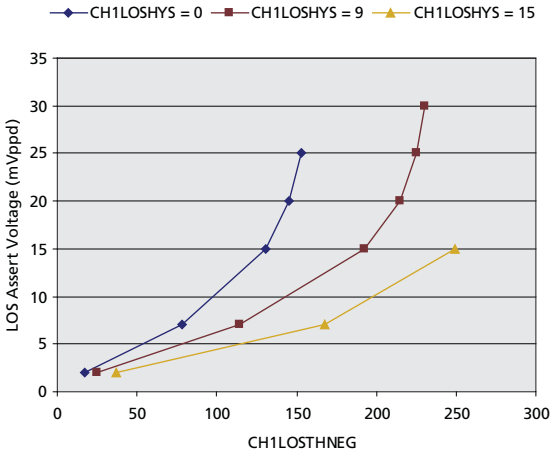


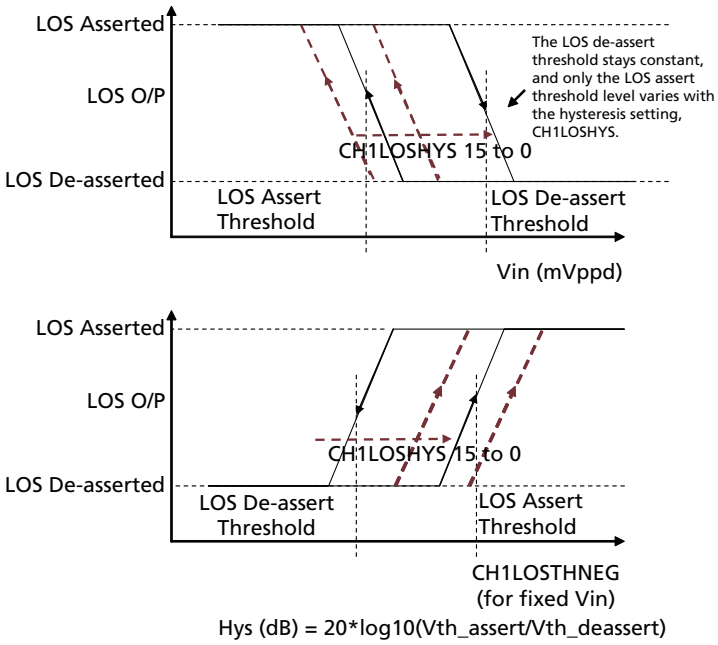
Figure 3-15: Ch1 LOS Threshold vs. Hysteresis (CH1LOSRANGE = 3)

3.5.2.2 Ch1 LOS Hysteresis

The LOS detector supports programmable hysteresis ranging from 0dB to 6dB, adjustable in steps of less than 0.5dB. The following register can be used to program the hysteresis. Note that the effective hysteresis is somewhat dependent on the threshold value:

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
CH1_REG13	60	CH1LOSHYS	3:0	RW	1001	0-15	Sets LOS hysteresis from 0dB to 6dB in steps of 0.5dB.

Hysteresis control only affects the assert threshold. The LOS de-assert threshold is set by CH1LOSTHNEG and CH1LOSTHPOS controls only. Figure 3-16 shows the hysteresis characteristics and the impact of CH1LOSHYS[3:0]:



CH1LOSHYS	Hys (dB)
0	0.1
1	0.3
2	0.7
3	1.1
4	1.4
5	1.8
6	2.1
7	2.5
8	3.0
9	3.4
10	3.9
11	4.4
12	4.8
13	5.4
15	6.7

Figure 3-16: Ch1 LOS Hysteresis

3.5.2.3 Manual LOS Assert

The on-chip LOS circuit can be bypassed, and LOS asserted, through the host interface. This operation is initiated when CH1LOSSOFTASSERTEN is HIGH. The state of CH1LOSSOFTASSERT then controls the LOS register CH1PLLLOS and external indication through Ch1LOS.

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
CH1_REG14	61	CH1LOSSOFTASSERT	6:6	RW	0	0-1	When HIGH, asserts LOS. CH1LOSSOFTASSERTEN must be HIGH to use this bit.
		CH1LOSSOFTASSERTEN	7:7	RW	0	0-1	When HIGH, LOS is controlled by CH1LOSSOFTASSERT.

3.5.3 Loss Of Lock (LOL)

The channel 0 and channel 1 LOL status indicators are both available in registers as shown below:

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
CH0PLL_REG10	19	CH0PLLLOL	1:1	RO	0	0-1	Ch0 CDR loss of lock when HIGH.
CH1PLL_REG10	29	CH1PLLLOL	1:1	RO	0	0-1	Ch1 CDR loss of lock when HIGH.

3.5.4 Ch0FAULT - Channel 0 Fault

Various status indicator pins are combined to generate a single Ch0FAULT indicator output. The Ch0FAULT output is, by default, an open-drain output. It can be configured in a LVCMOS/LVTTL compliant mode through register 2, bit 3 (OPENDRAINCH0FAULT). When set LOW, the Ch0FAULT output is configured as LVCMOS/LVTTL compatible output.

The Ch0FAULT output is active-high by default. Its polarity can be changed to make it active-low through register 2, bit 0 (POLINVCH0FAULT). When set HIGH, Ch0FAULT is configured as an active-low output.

The following status indicator controls can be combined to generate the Ch0FAULT output. Each of the indicators can be independently masked through the register controls. By default, the Ch0FAULT output combines (ORs) the status of all indicators.

The following registers control the masking of the various indicators for Ch0FAULT and the configuration of Ch0FAULT pin.

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
TOP_REG1	1	FAULTMASKCH1LOS	0:0	RW	1	0-1	When HIGH, masks out Ch1LOS from asserting CH0FAULT.
		FAULTMASKCH1LOL	1:1	RW	1	0-1	When HIGH, masks Ch1LOL from asserting Ch0FAULT.
		FAULTMASKCH0LOS	2:2	RW	1	0-1	When HIGH, masks outCh0LOS from asserting CH0FAULT.
		FAULTMASKCH0LOL	3:3	RW	1	0-1	When HIGH, masks Ch0LOL from asserting Ch0FAULT.
		FAULTMASKCH0FAULT	4:4	RW	0	0-1	When HIGH, masks out Ch0Fault from asserting CH0FAULT.
TOP_REG2	2	POLINVCH0FAULT	0:0	RW	0	0-1	When HIGH, inverts polarity of CH0FAULT output.
		OPENDRAINCH0FAULT	3:3	RW	1	0-1	When HIGH, makes CH0FAULT output driver open drain.
NOTE: To support system diagnostics, a manual Ch0FAULT assert feature is available through the following register:							
TOP_REG4	4	FORCECH0FAULT	4:4	RW	0	0-1	When HIGH, asserts CH0FAULT.

3.6 Test Features

The GX4002 contains built-in test features that can be used during module test, mission mode, or system testing.

3.6.1 PRBS Generator and Checker

The GX4002 has a built in PRBS7 generator and checker. The generator and checker are disabled by default to save power, and can be enabled through the digital control interface. There are multiple ways to use the PRBS generator/checker, as shown in Table 3-9 below:

Table 3-9: PRBS Generator/Checker Modes of Operation

Mode	Description
Lock to data pattern on Ch1 input	A data pattern, such as PRBS data or Fibre Channel/10GbE traffic, can be sent to the Ch1 path input. A PRBS7 pattern can be viewed at the Ch1 path output, or can be looped back to the Ch0 side to use the PRBS checker.
Lock to data pattern on Ch0 input	A data pattern, such as PRBS data or Fibre Channel/10GbE traffic, can be sent to the Ch0 path input. A PRBS7 pattern can be viewed at the Ch0 path output, or can be looped back to the Ch1 side to use the PRBS checker.
Lock to low-speed reference on Ch1 input	A reference at 1/8 (14G) or 1/4 (10G) of the desired rate can be sent to the Ch1 input. A PRBS7 pattern can be viewed at the Ch1 path output, or can be looped back to the Ch0 side to use the PRBS checker. This mode can be used when testing a module so that high-speed test equipment is not required. See Figure 3-17.
Lock to low-speed reference on Ch0 input	A reference at 1/8 (14G) or 1/4 (10G) of the desired rate can be sent to the Ch0 input. A PRBS7 pattern can be viewed at the Ch0 path output, or can be looped back to the Ch1 side to use the PRBS checker. This mode can be used when testing a module so that high-speed test equipment is not required. See Figure 3-18.

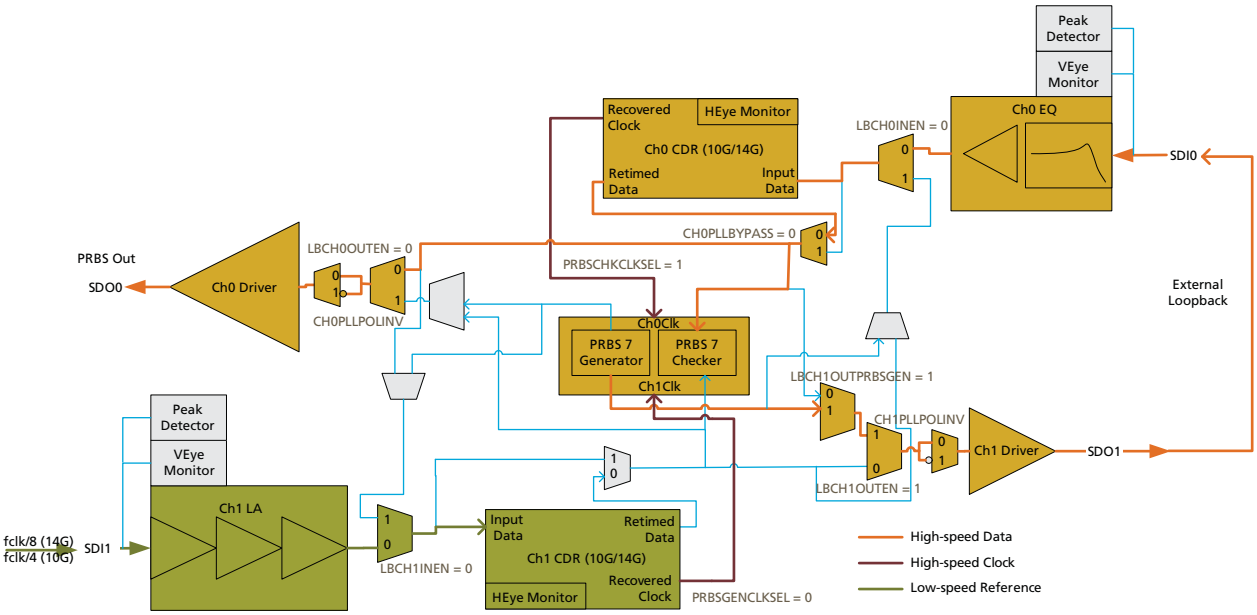


Figure 3-17: PRBS Generator on Ch1 Output and PRBS Check Monitoring Ch0 Input

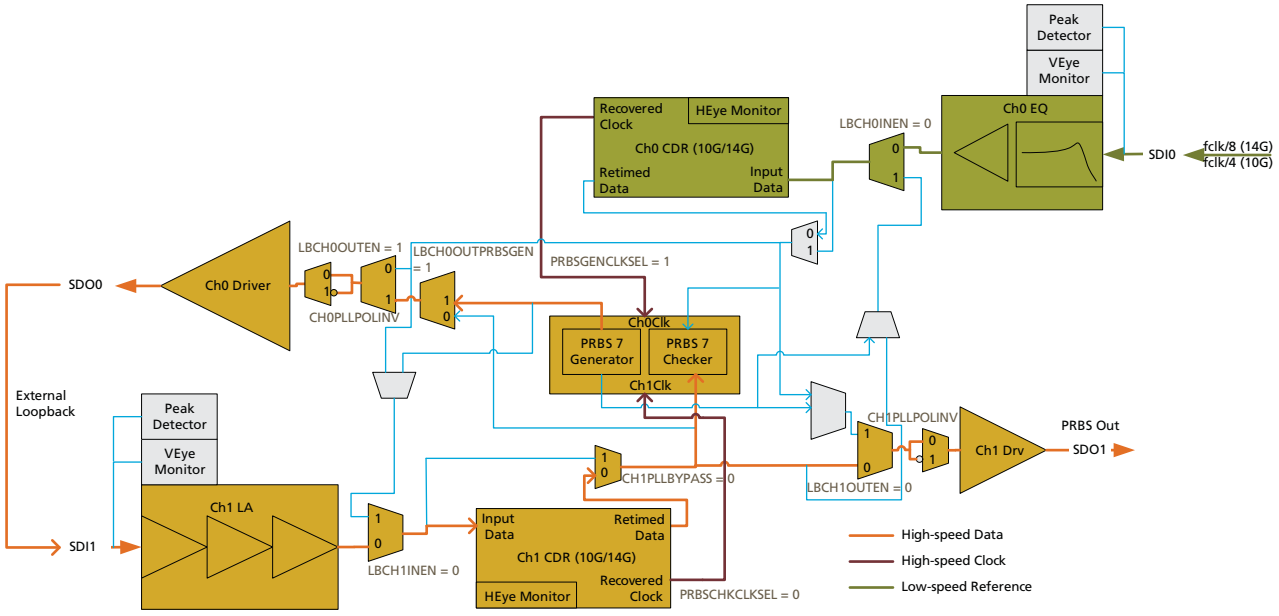


Figure 3-18: PRBS Generator on Ch0 Output and PRBS Check Monitoring Ch1 Input

The following registers enable and configure the PRBS generator and checker:

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
TOP_REG3	3	PRBSGENSTART	0:0	RW	0	0-1	When pulsed HIGH and LOW, starts off the PRBS generator.
		PRBSCHKCLEARERR	1:1	RW	0	0-1	When HIGH, clears the latched error flag from checker.
TOP_REG6	6	PRBSCHKSTATUS	0:0	RO	0	0-1	When HIGH, checker detected an error.
LOOPBK_REG1	7	LBCH1INPRBSGEN	1:1	RW	0	0-1	Selects PRBS generator output into Ch1 CDR.
		LBCH1OUTPRBSGEN	6:6	RW	0	0-1	Selects PRBS generator output into Ch1 Driver.
LOOPBK_REG2	8	LBCH0INPRBSGEN	1:1	RW	0	0-1	Selects PRBS generator output into Ch0 CDR.
		LBCH0OUTPRBSGEN	6:6	RW	0	0-1	Selects PRBS generator output into Ch0 Driver.
LOOPBK_REG3	9	PRBSGENCLKSEL	0:0	RW	0	0-1	When HIGH, selects Ch0 recovered clock. LOW selects Ch1 clock.
		PRBSCHKCLKSEL	1:1	RW	0	0-1	When HIGH, selects Ch0 recovered clock. LOW selects Ch1 clock.
PWRDN_REG2	161	PDPRBSGEN	1:1	RW	1	0-1	When HIGH, power-down the PRBS generator and associated buffers.
		PDPRBSCHK	2:2	RW	1	0-1	When HIGH, power-down the PRBS generator and associated checkers.

To ensure proper operation of the PRBS7 generator, PRBSGENSTART needs to be set HIGH and then LOW once after the generator is powered-up through PDPRBSGEN.

To ensure proper operation of the PRBS7 checker, PRBSCHKCLEARERR needs to be set HIGH and then LOW after application of valid PRBS7 pattern to clear any spurious errors. PRBSCHKSTATUS, may be polled to check for errors flagged by the checker.

The PRBS generator can be configured to apply the PRBS7 pattern to SDO1 or SDO0 or internally. Apply to either the Ch1 or the Ch0 CDR for retiming before transmitting out through SDO. Controls LBCH1INPRBSGEN, LBCH1OUTPRBSGEN, LBCH0INPRBSGEN and LBCH0OUTPRBSGEN determine the path of the PRBS pattern.

Both PRBS generator and checker can be clocked off either the Ch0 or Ch1 recovered clocks independently through controls PRBSGENCLKSEL and PRBSCHKCLKSEL. The PRBS checker automatically selects retimed data from the CDR which is chosen to provide its clock through PRBSCHKCLKSEL.

3.6.2 Eye Monitor & Peak Detector

The GX4002 has built-in eye monitors in both the horizontal and vertical direction for the inner eye. These eye monitors are available for both Ch1 and Ch0 paths. In addition, both Ch1 and Ch0 inputs have peak detectors available to provide outer eye information. The information from these monitors can be used to indicate if the input to the module has degraded. These features can be used during mission mode.

Figure 3-19 shows where the eye monitoring functions are implemented:

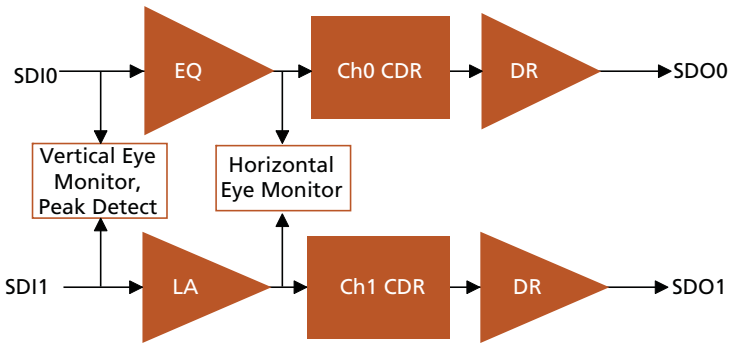


Figure 3-19: Eye Monitor Implementation

The vertical eye monitor outputs a value proportional to the inner eye opening. The output of the eye monitor can be sampled and read out digitally through the ADC (see Section 3.7.1). The acquisition time for the eye monitor is approximately 10ms.

The peak detector outputs a value proportional to the outer eye amplitude. The output of the peak detector can be sampled and read out digitally through the ADC. The acquisition time is approximately 10ms.

The horizontal eye monitor outputs a value that is proportional to the horizontal eye opening, as shown in Figure 3-20 below. The output of the horizontal eye monitor can be sampled and read out digitally through the ADC. The acquisition time is approximately 10ms.

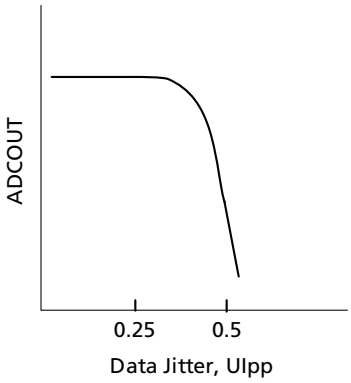


Figure 3-20: Horizontal Eye Monitor

All eye monitoring functions can be independently enabled to optimize power. The following register can be used to enable and control the eye monitors. See Section 3.7 for details on sampling and reading out the monitors:

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
CH0_REG13	43	CH0VEYETHADJ	7:0	RW	00000000	0-255	Vertical eye monitor threshold adjustment, 0-255.
CH0_REG14	44	CH0VEYETHPOL	0:0	RW	0	0-1	Vertical eye monitor threshold polarity. HIGH is positive.
		CH0VEYELORANGE	1:1	RW	0	0-1	When HIGH, reduces the range to 0-600mVppd.
		CH0VEYEOFFCALEN	2:2	RW	0	0-1	Vertical eye monitor offset calibration enable.
CH1_REG15	62	CH1VEYETHADJ	7:0	RW	00000000	0-255	Vertical eye monitor threshold adjustment, 0-255.
CH1_REG16	63	CH1VEYETHPOL	0:0	RW	0	0-1	Vertical eye monitor threshold polarity. HIGH is positive.
		CH1VEYELORANGE	1:1	RW	0	0-1	When HIGH, reduces the range to 0-600mVppd.
		CH1VEYEOFFCALEN	2:2	RW	0	0-1	Vertical eye monitor offset calibration enable.
CH0PWRDN_REG3	153	CH0PDVEYEMON	1:1	RW	1	0-1	Power-down for the Ch0 vertical eye monitor.
		CH0PDHEYEMON	2:2	RW	1	0-1	Power-down for the Ch0 horizontal eye monitor.
		CH0PDPKDET	3:3	RW	1	0-1	Power-down for the Ch0 peak detector.
CH1PWRDN_REG3	158	CH1PDVEYEMON	1:1	RW	1	0-1	Power-down for the Ch1 vertical eye monitor.
		CH1PDHEYEMON	2:2	RW	1	0-1	Power-down for the Ch1 horizontal eye monitor.
		CH1PDPKDET	3:3	RW	1	0-1	Power-down for the Ch1 peak detector.

3.7 Digital Diagnostics

The GX4002 has an on-chip ADC to provide diagnostic information through the digital interface. Temperature and voltage can be monitored.

3.7.1 Analog to Digital Converter (ADC)

The ADC converts several analog quantities including temperature, supply, vertical and horizontal eye monitor outputs, and peak detector outputs.

The ADC is a sigma-delta converter with programmable resolution allowing trade-off between conversion time and accuracy. The full scale dynamic range of the ADC is 0 to 1.8V. The various sources can be selected into the ADC for conversion and read-out.

Offset calibration signals are provided to zero-out the selected sources to facilitate the calibration. Calibrated offsets can be programmed-in, such that the data read-out has corrected offsets.

Furthermore, a user-defined offset can be programmed-in to account for external systemic shifts. For example: if the temperature at the case is desired instead of the device temperature, the temperature delta between device and case can be programmed-in. Subsequent temperature read-outs will account for the temperature delta, and provide the case temperature.

3.7.1.1 Usage Model

Two usage models are possible, manual conversion and auto conversion.

3.7.1.1.1 Manual Conversion Mode

For manual conversion mode, register controls provide a conversion-on-demand interface. Polling or timing is required at the master end to read out the converted values in manual mode.

The user is expected to select the desired source and to write a 1 to the ADCSTARTCONV bit to initiate the conversion. The user can poll the ADCDONECONV bit or time the conversion based on the requested resolution before reading out the data.

To read out the data in the timed mode, a block read transfer can be performed on the ADCDONECONV, ADCOUTLO and ADCOUTHI registers. If the ADCDONECONV bit is HIGH, then the data is valid.

The ADCSTARTCONV bit does not have to be reset before initiating another conversion. Similarly, the ADCDONECONV bit does not have to be reset before initiating another conversion. This minimizes the host interface transaction overhead while using the ADC.

3.7.1.1.2 Auto Conversion Mode

The user selects the desired source, and enables the auto conversion mode by setting ADCAUTOCONVEN HIGH. The ADC will continuously convert the selected source and update the ADCOUTHI/LO registers.

The ADCDONECONV bit will always remain HIGH, indicating a valid converted value is available for read-out. This flag may be cleared by writing to the ADCSTARTCONV bit if positive indication of valid data is required.

3.7.1.2 ADC Control Registers

The following registers are used to select the various sources for conversion and read-out through the ADC. The offset calibration controls ADCOFFCALEN[3:0] facilitate calibrating the offsets of the selected sources:

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
ADC_REG1	143	ADCSRCSEL	3:0	RW	0000	0-15	Selects input for ADC (see Table 3-3: ADC Source Select).
		ADCOFFCALEN	7:4	RW	0000	0-15	Selects source for offset calibration (see Table 3-2).

Table 3-3: ADC Source Select

ADCSRCSEL[3:0]	Source
0000	0.9V
0001	Ch0 Vertical Eye
0010	Ch1 Vertical Eye
0011	Ch0 Horizontal Eye
0100	Ch1 Horizontal Eye
0101	Ch0 Peak Detector
0110	Ch1 Peak Detector
0111	RSVD
1000	RSVD
1001	RSVD
1010	Temperature Sensor
1011	Supply Sensor
1100	0.45V
1101	1.35V
1110	RSVD
1111	RSVD

The following registers are used to program a calibrated offset for automatic offset correction. ADCOFFMODE and ADCRESOLUTION determine how the offset values are interpreted.

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
ADC_REG7	149	ADCOFFSETLO	7:0	RW	00000000	0-255	ADC offset LSB, unsigned binary.
ADC_REG8	150	ADCOFFSETHI	7:0	RW	00000000	0-255	ADC offset MSB, unsigned binary.

The following registers are used to configure the ADC:

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
ADC_REG0	142	ADCRESET	0:0	RW	1	0-1	Reset for the ADC.
		ADCAUTOCONVEN	1:1	RW	1	0-1	When HIGH, enables auto conversion. Set LOW for manual.
		ADCJUSTLSB	2:2	RW	1	0-1	When HIGH, justify towards LSB. LOW justifies towards MSB.
		ADCOFFMODE	3:3	RW	0	0-1	When LOW, offset is subtracted from the ADC output. When HIGH, offset is added to the ADC output. **NOTE:** When HIGH, ADCOFFSETHI[7] is sign and rest of the bits are magnitude. A sign value of 1 represents negative numbers.
ADC_REG2	143	ADCRESOLUTION	2:0	RW	001	0-7	ADC resolution control.
		ADCCLKRATE	5:3	RW	0101	0-15	ADC clock divide ratio.

Table 3-4: ADC Resolution

ADCRESOLUTION	ADC Resolution (bits)	Number of ADC Clocks for Conversion
000	4	15
001	6	63
010	8	255
011	10	1023
100	12	4095
101	14	16383
110	16	65535
111	Unused	Unused

Table 3-5: ADC Clock Rate

ADCCLKRATE[2:0]	ADC Sampling Clock Rate (MHz)	ADC Conversion Time (µs) Res = 10 bits
000	1	1023
001	1.6	651

Table 3-5: ADC Clock Rate (Continued)

ADCCLKRATE[2:0]	ADC Sampling Clock Rate (MHz)	ADC Conversion Time (µs) Res = 10 bits
010	2.1	477
011	2.7	377
100	3.3	311
101	3.9	265 (default)
110	4.4	231
111	5	205

The following registers are used to control the conversion, and read-out the converted data:

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
ADC_REG3	145	ADCSTARTCONV	0:0	RW	0	0-1	ADC starts conversion.
ADC_REG4	146	ADCDONECONV	0:0	RO	0	0-1	ADC conversion done flag.
ADC_REG5	147	ADCOUTLO	7:0	RO	00000000	0-255	ADC output LOW MSB.
ADC_REG6	148	ADCOUTHI	7:0	RO	00000000	0-255	ADC output HIGH MSB.
PWRDN_REG2	161	PDTEMPSENSOR	3:3	RW	1	0-1	When HIGH, power-down the temperature sensor.
		PDSUPPLYSENSOR	4:4	RW	1	0-1	When HIGH, power-down the supply sensor.
		PDADC	5:5	RW	1	0-1	When HIGH, power-down the ADC.

3.7.1.3 ADC Offset Calibration

The ADC supports conversion of several different sources. Each source can have a different offset associated with it. To allow accurate conversion for each source, it is recommended that the offset be calibrated for each source, so that the appropriate correction can be applied when converting a given source.

There are two steps involved in the calibration of offsets:

1. Offset measurement.
2. Offset correction.

3.7.1.3.1 Offset Measurement

Offset measurement of any source requires zeroing-out the source, such that its output constitutes the offset only. With the source zeroed-out, the output of the ADC is then the cumulative offset. This offset is subtracted from subsequent measurements of the same source to get an accurate offset corrected conversion.

The device supports offset measurement of each source through the ADCSRCSEL and ADCOFFCALEN register controls. ADCOFFCALEN selects the source to zero-out, as shown in Table 3-2:

Table 3-2: Offset Measurement Sources

ADCOFFCALEN[3:0]	Source	ADC Offset Calibration Input (Vcal)
0000	0.9V	0.9V
0001	Ch0 Vertical Eye	0.9V
0010	Ch1 Vertical Eye	0.9V
0011	Ch0 Horizontal Eye	0.9V
0100	Ch1 Horizontal Eye	0.9V
0101	Ch0 Peak Detector	0.45V
0110	Ch1 Peak Detector	0.45V
0111	RSVD	N/A
1000	RSVD	N/A
1001	RSVD	N/A
1010	Temperature Sensor	0.9V
1011	Supply Sensor	0.9V
1100	0.45V	0.45V
1101	1.35V	1.35V
1110	RSVD	N/A
1111	RSVD	N/A

When a selected source is zeroed-out, the input to the ADC is set to its calibration voltage (Vcal) as per Table 3-2. The ideal code for that calibration voltage for a given resolution, can be subtracted from the output code to get the offset. Refer to the formula shown below:

Equation 3-1

$$Offset = ADCOut - (2^N \frac{Vcal}{1.8} - 1)$$

For example: if the temperature sensor is selected as the source, then it's Vcal = 0.9V. Assuming that the ADC resolution (N) is set to 10 bits; by setting ADCOFFCALEN = "1010", and reading-out the ADC, (in this example) ADCOUT = 521.
Therefore, Offset = 521 - 511 = 10.

This measured offset can be subtracted from subsequent measurements automatically, as described in the next section.

3.7.1.3.2 OFFSET CORRECTION

The ADC supports offset correction for both internal offsets as well as external systematic offsets through the ADCOFFSETLO and ADCOFFSETHI registers.

The offset correction behaviour depends on the ADCOFFMODE control bit. Table 3-3 describes the offset correction operation:

Table 3-3: Offset Correction Operation

ADCOFFMODE	Operation	Description
0	ADCOUTLO,HI = uncorrected ADC Out[15:0] - ADCOFFSETLO,HI	ADCOFFSETLO,HI is un-signed. Result is unsigned. Output is all 0s for negative results.
1	ADCOUTLO,HI = uncorrected ADC Out[15:0] + ADCOFFSETLO,HI	ADCOFFSETLO,HI is sign + mag. Bit 15 is sign, and 1 represents positive. Result is unsigned. Output is all 0s for negative results.

Supporting both subtraction and addition of offsets allows the user the flexibility to adjust for systematic shifts. However, the default mode 0 (subtraction) should suffice for most applications.

In the previous example, the offset was measured to be 10 for ADCOUT = 521 for the temperature sensor. This offset can be automatically subtracted for all subsequent measurements of the temperature sensor by setting ADCOFFSETLO = 10 and ADCOFFSETHI = 0. With these values, ADCOUT will read 511 (instead of 521).

3.7.1.4 ADC Conversion Sequence

The following sequence is recommended for ADC conversions:

1. Power-up the ADC.
2. Bring the ADC out of reset.
3. Setup the ADC mode of operation (Auto or Manual).
4. Setup the ADC resolution.
5. Setup the ADC conversion rate (clock rate).
6. Select the ADC source to convert.
7. Setup the ADC offset and offset modes.
8. Start the ADC conversion.
9. Read the ADC-done conversion flag to confirm a successful conversion.
10. Read the ADC output, first the low byte, immediately followed by high byte.

The following section gives a detailed example of performing an ADC conversion in manual mode.

Example ADC Conversion in Manual Mode

The following example illustrates how to use the ADC to read-out the supply sensor in manual conversion mode:

1. Power-up the ADC and the supply sensor.
   Register: PWRDN_REG2, Address: 161, PDADC = 0.
   Register: PWRDN_REG2, Address: 161, PDSUPPLYSENSOR = 0.
2. Bring the ADC out of reset.
   Register: ADC_REG0, Address: 142, ADCRESET = 0
3. Set the ADC mode of operation to manual mode.
   Register: ADC_REG0, Address: 142, ADCAUTOCONVEN = 0.
   Note that this must be a separate write operation than the reset exit, even though it's the same register.
4. Set the ADC resolution to 12 bits.
   Register: ADC_REG2, Address: 144, ADCRESOLUTION = 4.
5. Set the ADC conversion rate.
   Register: ADC_REG2, Address: 144, ADCCLKRATE = 5 (default).
6. Select the ADC source as the supply sensor.
   Register: ADC_REG1, Address: 143, ADCSRCSEL = 11 (decimal).
7. Set the ADC offset and offset mode (in this example, an offset of 0 is assumed).
   Register: ADC_REG0, Address: 142, ADCOFFMODE = 0 (default).
   Register: ADC_REG7, Address: 149, ADCOFFSETLO = 0.
   Register: ADC_REG8, Address: 150, ADCOFFSETHI = 0.
8. Start the ADC conversion.
   Register: ADC_REG3, Address: 145, ADCSTARTCONV = 1.
   Note that it is not required to reset the ADCSTARTCONV to 0 before starting another conversion. Writing a value of 1 to the ADCSTARTCONV bit again will initiate a new conversion.

Read the ADC-done flag and output.
Register: ADC_REG4,5,6 Address: 146-148, ADCDONECONV, ADCOUTLO, ADCOUTHI.
These three registers can be read-out as burst read. Note that it is important that the LOW byte be read-out first, immediately followed by a HIGH byte. This is required to ensure data consistency. The ADCDONECONV flag can be checked to confirm successful conversion.

3.7.1.5 ADC Transfer Functions for Each Source

The following subsections show the typical transfer functions for each source that can be read-out from ADC.

Peak Detectors

Table 3-4 and Figure 3-21 show typical peak detector outputs:

Table 3-4: Peak Detector Outputs

Peak Detector Input Amplitude (mVppd)	ADC (12-bit resolution)	ADC (10-bit resolution)
10	806	201
30	810	202
50	817	204
75	830	207
100	849	212
140	887	222
180	931	233
220	975	244
240	998	250
280	1044	261
320	1092	273
360	1139	285
400	1184	296
1000	1828	457
1200	1993	498

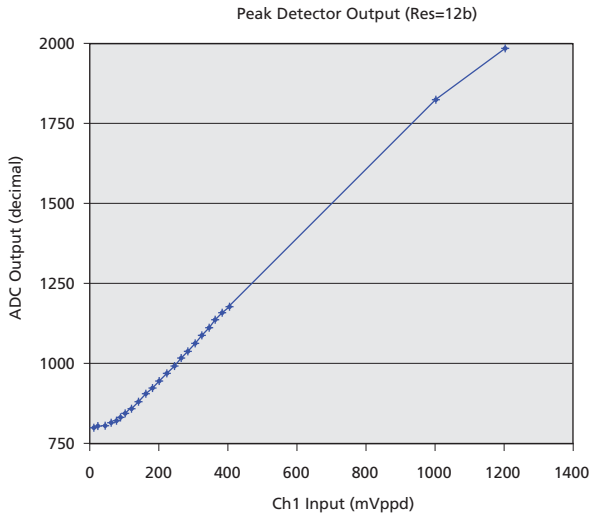


Figure 3-21: Peak Detector Output

Temperature Sensor

Table 3-5 and Figure 3-22 show typical temperature sensor outputs:

Table 3-5: Typical Temperature Sensor Output

Temperature (°C)	ADC (12-bit resolution)	ADC (10-bit resolution)
-20.00	653	163
0.00	896	223
20.00	1138	284
40.00	1381	345
60.00	1623	405
80.00	1866	466
90.00	1987	496
120.00	2351	587

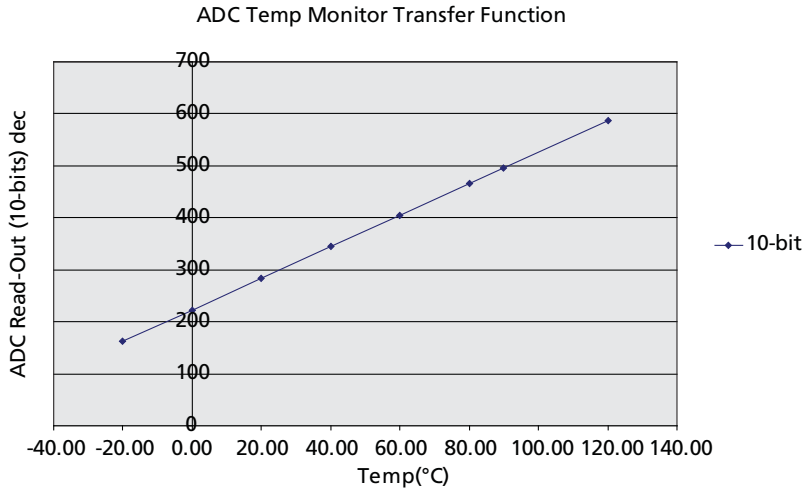


Figure 3-22: ADC Temperature Monitor Transfer Function

Supply Sensor

Table 3-6 and Figure 3-23 show typical Ch0SDOVCC supply sensor outputs:

Table 3-6: Typical Ch0SDOVCC Supply Sensor Output

Ch0SDOVCC (V)	ADC (12-bit resolution)	ADC (10-bit resolution)
2.3	644	161
2.4	771	192
2.5	898	224
2.6	1025	256
2.7	1152	288
2.8	1279	319
2.9	1406	351
3.0	1532	383
3.1	1659	414
3.2	1786	446
3.3	1913	478
3.4	2040	510
3.5	2167	605
3.6	2294	573
3.7	2421	605

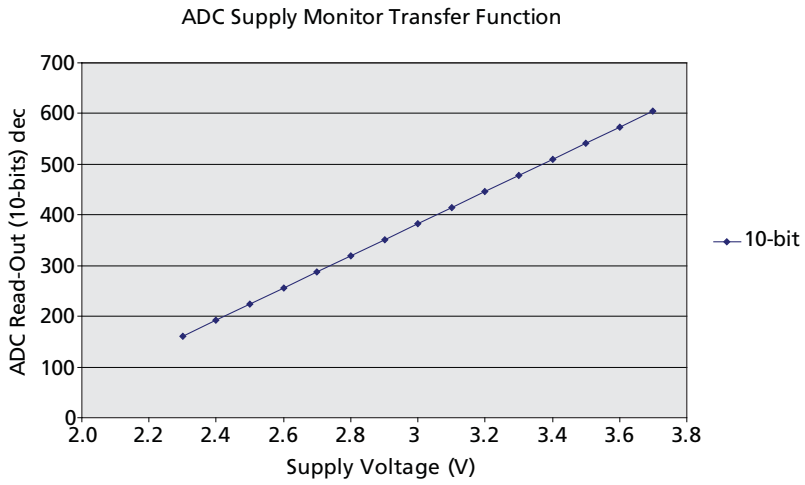


Figure 3-23: ADC Supply Monitor Transfer Function

3.8 Power Control Options

The GX4002 provides a high-degree of flexibility in configuring the device for optimal power through power-down and power adjustment registers. Typical usage scenarios are shown. For further description on each of the individual control bits, see Table 7-1, registers 134 to 137. This section describes the power-down controls for the following sub-systems:

1. Ch1 CDR & SDO Power-Down
2. Ch0 CDR Power-Down
3. Ch0 SDO Power-Down

Table 3-7: Ch1 CDR & SDO Power-Down

CH1PLLBYPASS	CH1PDPATH	CH1PDCH1CDR	CH1PDHEYEMON	CH1PDCKDIVOUT	CH1PDSDO	Description
0	1	x	x	x	1	Completely powers-down the Ch1 CDR and Ch1 SDO.
0	x	1	x	x	1	Completely powers-down the Ch1 CDR and Ch1 SDO
1	0	x	x	x	0	Main data path through Ch1 CDR and Ch1 SDO is powered-up for bypass mode. (Ch1LA has to be powered-up).
0	0	0	1	1	0	Mission mode, Ch1 CDR & SDO enabled in low-power mode.
0	0	0	1	1	0	Mission mode for fibre channel. Ch1 CDR & SDO are enabled with automatic bypass through rate detection.
0	0	0	0	1	0	Diagnostic mode with horizontal eye monitor enabled.
0	0	0	1	0	0	Diagnostic mode with divided recovered clock available through Ch1 SDO. Requires appropriate configuration of loopback registers.

Table 3-8: Ch0 CDR Power-Down

CH0PLLBYPASS	CH0PDPATH	CH0PDCH0CDR	CH0PDHEYEMON	CH0PDCKDIVOUT	CH0PDCH0SDO	Description
0	1	1	x	x	1	Completely powers-down the Ch0 CDR
1	0	1	x	x	0	Main data path through Ch0 CDR is powered-up for bypass mode. (Ch0Eq has to be powered-up).
0	0	0	1	1	0	Mission mode, Ch0 CDR is enabled in low power mode.

Table 3-8: Ch0 CDR Power-Down (Continued)

CH0PLLBYPASS	CH0PDPATH	CH0PDCH0CDR	CH0PDHEYEMON	CH0PDCKDIVOUT	CH0PDCH0SDO	Description
0	0	0	0	1	0	Diagnostic mode with horizontal eye monitor enabled.
0	0	0	1	0	0	Diagnostic mode with divided recovered clock available through Ch0 SDO. Requires appropriate configuration of loopback registers.

Table 3-9: Ch0 SDO Power-Down

CH0PDPATH	CH0PDCH0SDO	CH0PDCH0CDR	PDCH0SDOCPA	Description
1	x	x	x	Completely powers-down the Ch0 SDO.
x	1	x	x	Completely powers-down the Ch0 SDO.
0	0	x	1	Independently powers-down the Ch0 SDO cross point adjust feature.
0	0	0	0	Ch0 SDO with all features enabled.

3.9 Device Reset

$\overline{\text{RESET}}$ is an active-low signal with LVTTL/LVCMOS compatible signalling levels. $\overline{\text{RESET}}$ has a weak pull-down to keep the device in reset upon power-up. $\overline{\text{RESET}}$ does not have schmitt trigger since reset negation is internally synchronized. See Figure 6-7.

3.9.1 Reset State During Power-up

The device requires $\overline{\text{RESET}}$ to be continuously asserted LOW during power ramp up. $\overline{\text{RESET}}$ must continue to be held in an asserted LOW state for the minimum specified time after the power supply has reached 90% of its final settling value. Following a $\overline{\text{RESET}}$ assertion at power-up, the device may be reset again at any time with the minimum specified pulse width on $\overline{\text{RESET}}$. Refer to Figure 3-24.

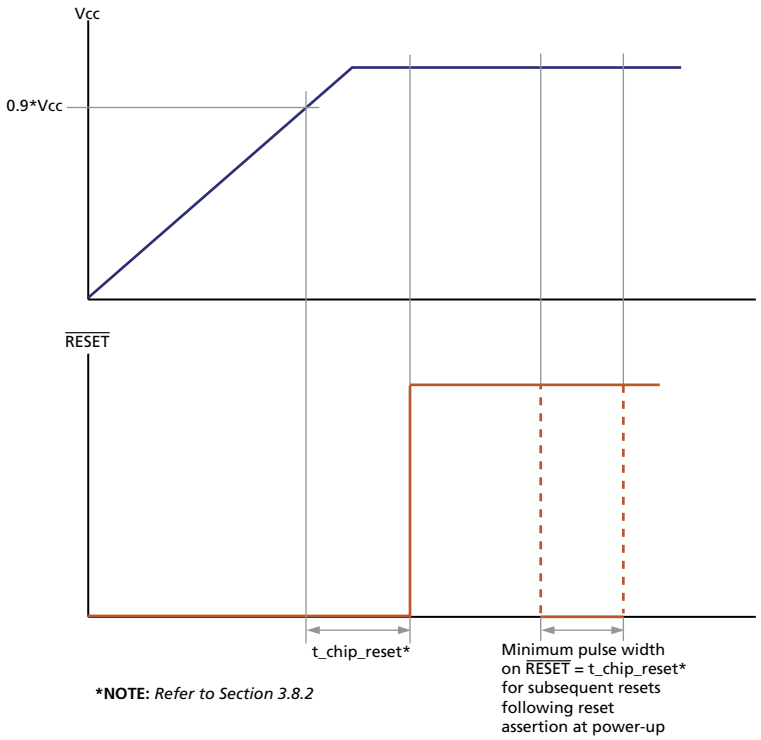


Figure 3-24: Reset State During Power-up

3.9.2 RESET Timing

The following RESET timing specifications apply:

t_chip_reset: 10µs

Defined as the minimum duration that RESET must be asserted after the supply has reached 90% of final settling value. The device can be accessed 1µs after RESET goes HIGH.

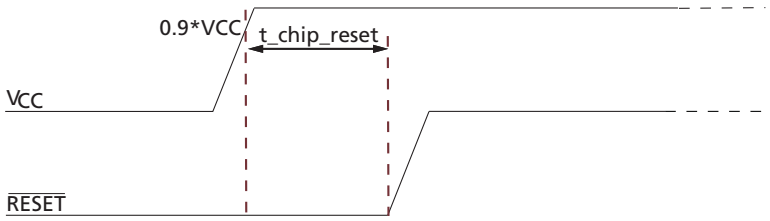


Figure 3-25: GX4002 Device Reset Timing Diagram

3.9.3 I/O and Register States During and After Reset

All configuration registers are set to their post-reset defaults state immediately following $\overline{\text{RESET}}$ assertion.

The following I/O states are applicable upon $\overline{\text{RESET}}$ assertion:

Table 3-10: I/O and Register States During and After Reset

Pin Name	I/O State upon $\overline{\text{RESET}}$ Assertion
SDA	This pin is configured as an input while $\overline{\text{RESET}}$ is asserted and immediately following $\overline{\text{RESET}}$ negation. When configured as an input, this pin is high-impedance.
SCL	This pin is configured as an input while $\overline{\text{RESET}}$ is asserted, and immediately following $\overline{\text{RESET}}$ negation. When configured as an input, this pin is high-impedance.
Ch0FAULT	This pin is configured as an open-drain output while $\overline{\text{RESET}}$ is asserted and immediately following $\overline{\text{RESET}}$ negation. This output will be high-impedance, and its state will depend on the external pull-up.
Ch1LOS	This pin is configured as an open-drain output while $\overline{\text{RESET}}$ is asserted and immediately following $\overline{\text{RESET}}$ negation. If a signal is present, the output will be pulled LOW. Otherwise, this output will be high-impedance and it's state will depend on the external pull-up.

3.10 Digital Control Interface

The GX4002 has a serial control interface to communicate with the part. An I^2C protocol can be used.

3.10.1 I^2C Host Interface Mode

The I^2C mode supports standard-mode (100kb/s) and fast-mode (400kb/s) signalling. The device only supports slave mode. The pins SDA and SCL are used for bi-directional serial data and clock respectively.

The GX4002 device slave address is 24h (= 0100100x).

The I^2C protocol is implemented as per the following description:

Each access begins with a 7-bit I^2C slave address word, an 8-bit register address word, followed by two 8-bit data words written to, or read from, the GX4002.

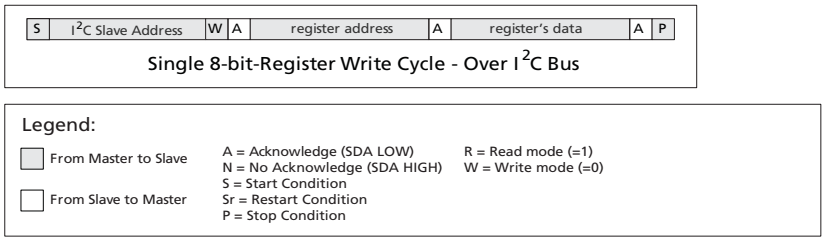


Figure 3-26: Single Register Write Cycle over I^{2}C Bus

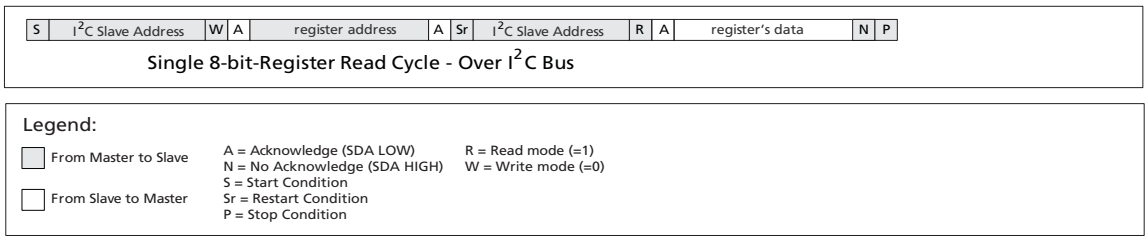


Figure 3-27: Single Register Read Cycle over I^{2}C Bus

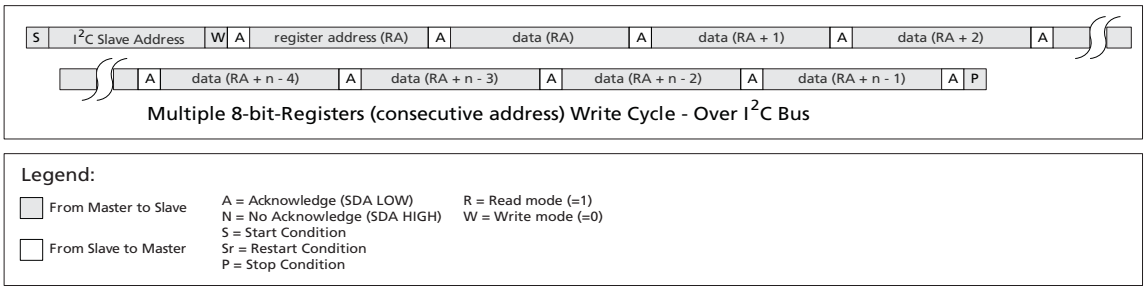


Figure 3-28: Bulk Register Write Cycle over I^{2}C Bus

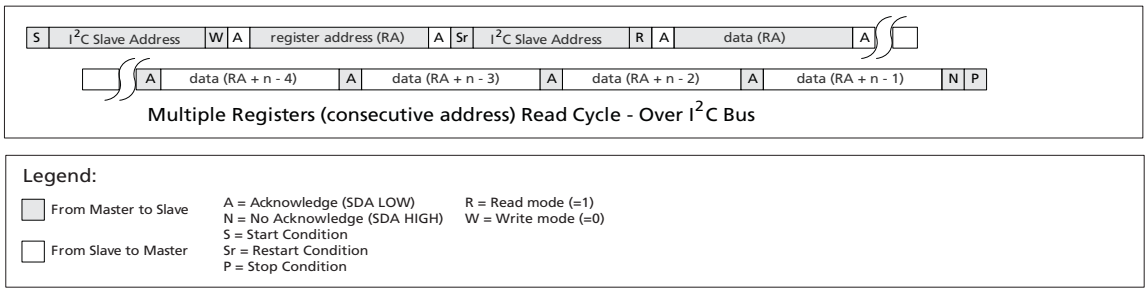


Figure 3-29: Bulk Register Read Cycle over I^{2}C Bus

4. Typical Application Circuit

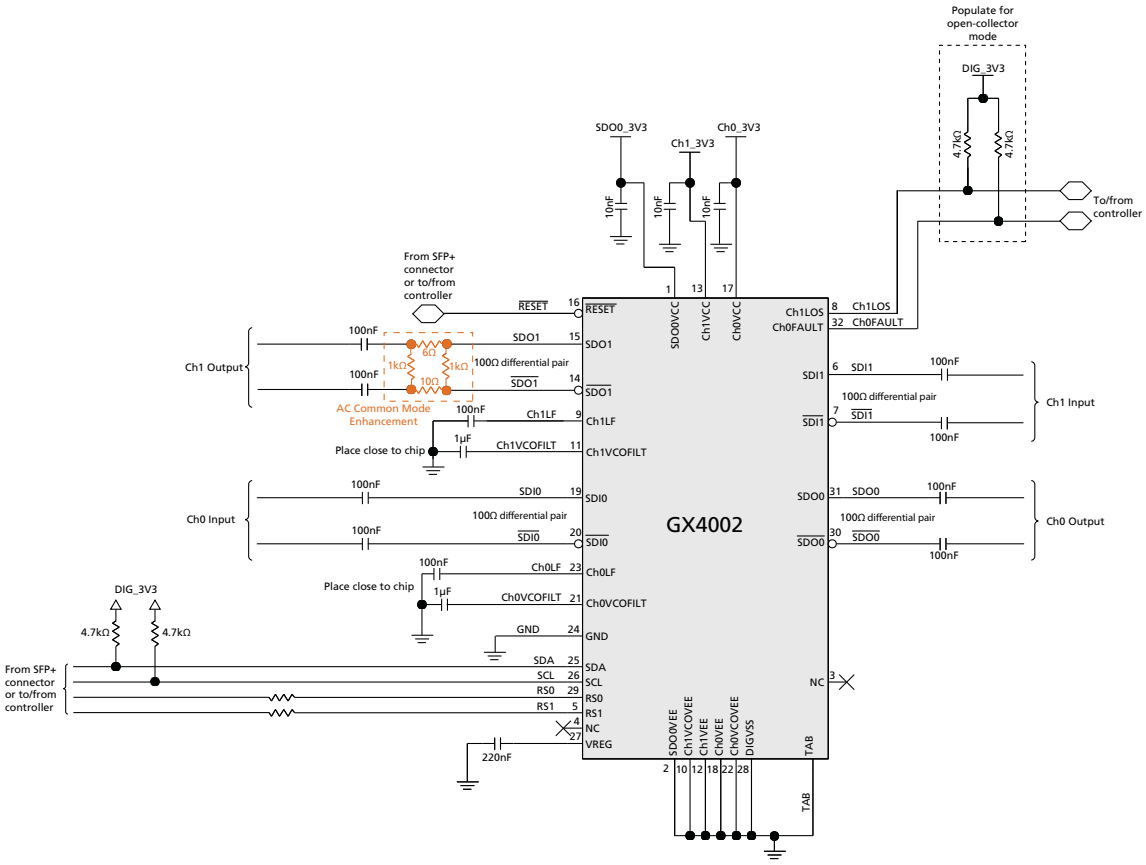


Figure 4-1: GX4002 Typical Application Circuit

- Place lowest value decoupling capacitor closest to the device
- Status indicator connections are shown for a LVCMOS/LVTTL compatible mode. These I/Os can be configured as open-drain with pull-up

4.1 Power Supply Filter Recommendations

RC filters for isolating supplies are not recommended due to the large currents drawn from each supply.

- The Ch0 and Ch1 VCOs do not have independent supplies. Both of the Ch0 and Ch1 VCOs have internal regulators sourced from Ch0VCC and Ch1VCC respectively. As a result, additional filtering for the VCOs is not required

For improved isolation between the Ch0 and Ch1 paths, and to achieve the best Ch1 Sensitivity and Ch0 Jitter Generation, a supply filter such as the one shown in Figure 4-2 is recommended.

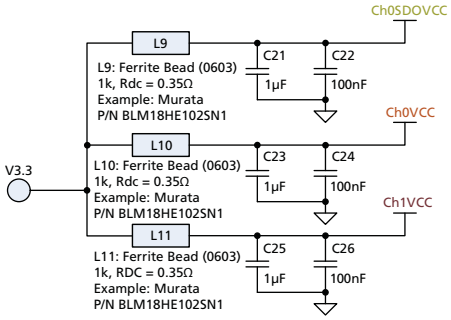


Figure 4-2: Power Supply Filter Recommendations

4.2 Power Supply Domains

Figure 4-3 shows the power supply domains for the GX4002:

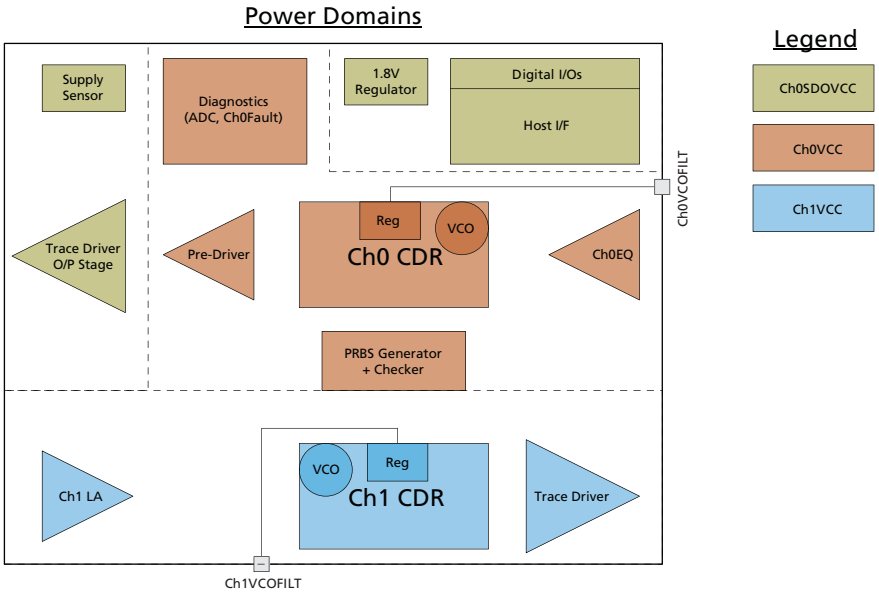


Figure 4-3: Power Supply Domains

5. Layout Considerations

The following high-frequency design rules should be considered to achieve optimum performance of the GX4002:

- Use carefully designed controlled-impedance transmission lines with minimal local discontinuities for all high-speed data signals
- Place decoupling capacitors as close as possible to the supply pins
- For optimal electrical and thermal performance, the QFN'S exposed pad should be soldered to the module ground plane
- It is recommended to have LF cap ground and VCO caps ground to be common with multiple stitching of vias to ground. Capacitors should be placed from smallest value to largest value away from chip
- All supply decoupling capacitors should have multiple vias to ground/power planes, and placed as close to chip as possible
- All supplies/grounds should be routed to corresponding decoupling capacitors pads, and never to the centre pad
- The recommended PCB layout for the GX4002 device is shown in Section 7.2
- Some sample layouts are shown in Figure 5-1

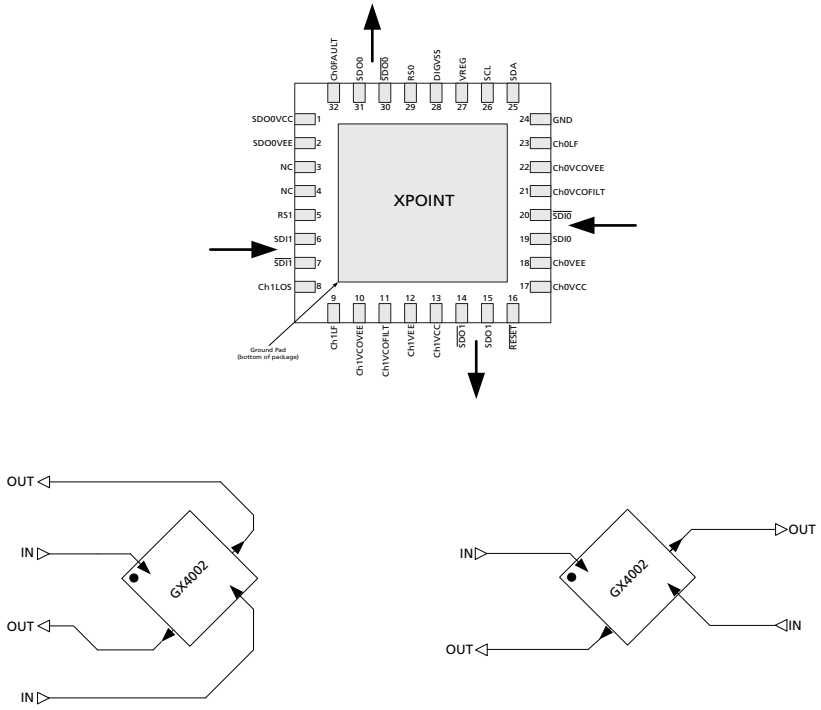


Figure 5-1: Sample Layouts

6. Input/Output Equivalent Circuits

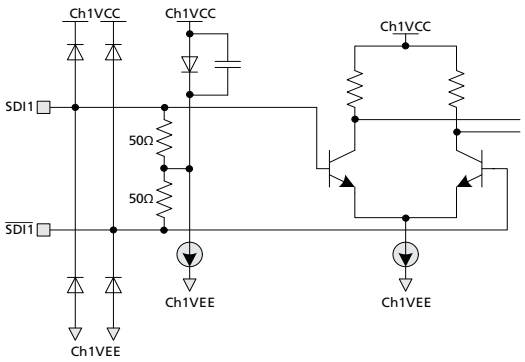


Figure 6-1: SDI1

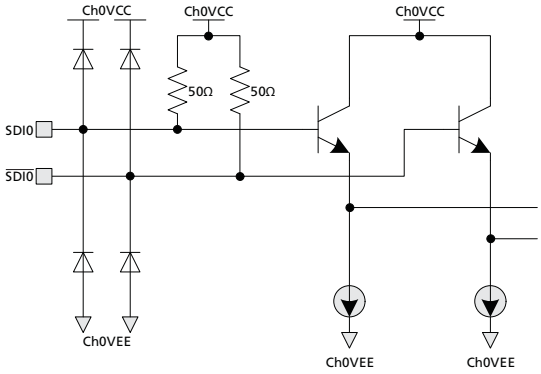


Figure 6-2: SDI0

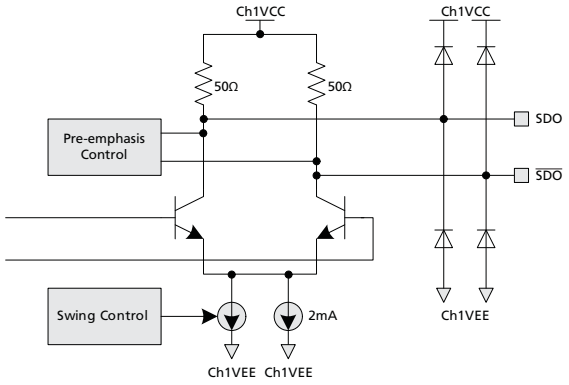


Figure 6-3: SDO1

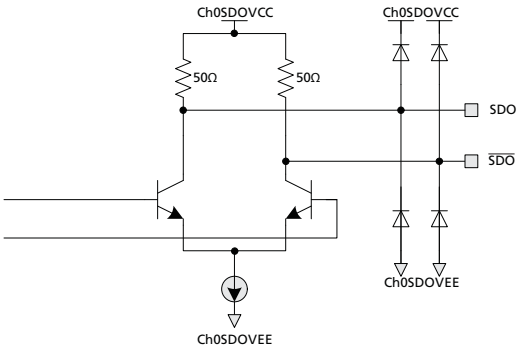
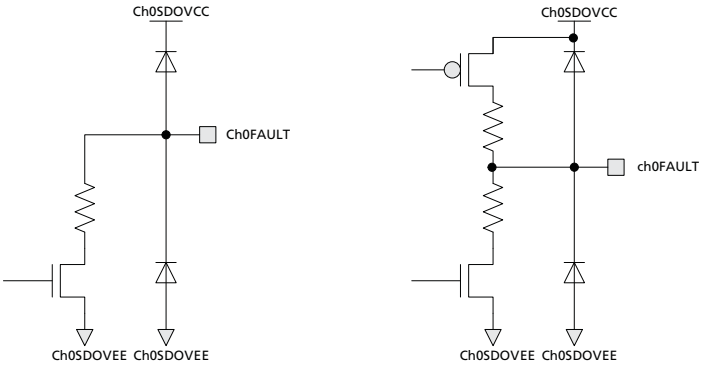
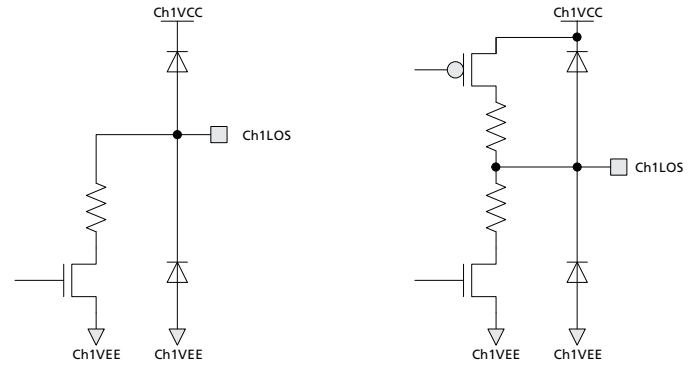


Figure 6-4: SDO0



Configured as open-drain Configured as LVCMOS

Figure 6-5: Ch0FAULT



Configured as open-drain Configured as LVCMOS

Figure 6-6: Ch1LOS

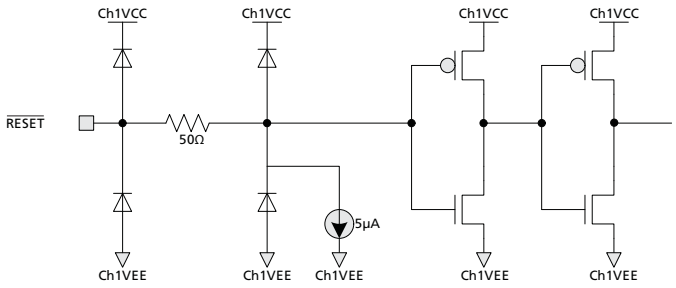


Figure 6-7: $\overline{\text{RESET}}$

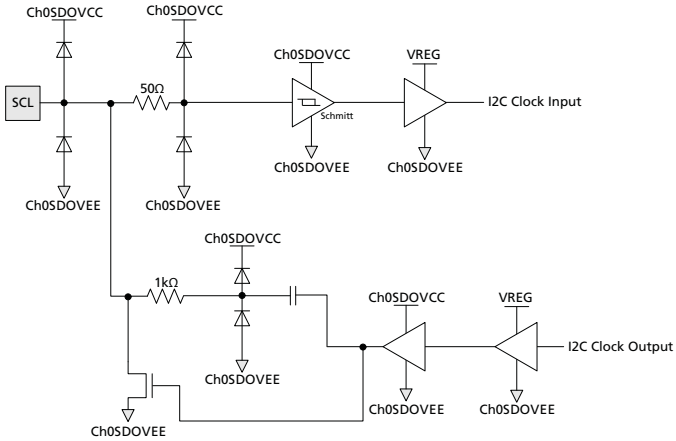


Figure 6-8: I^2C, SCL, SDA

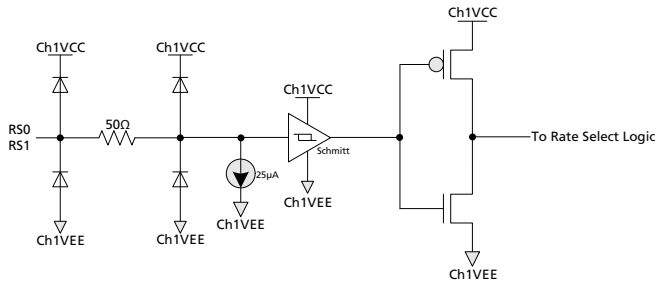
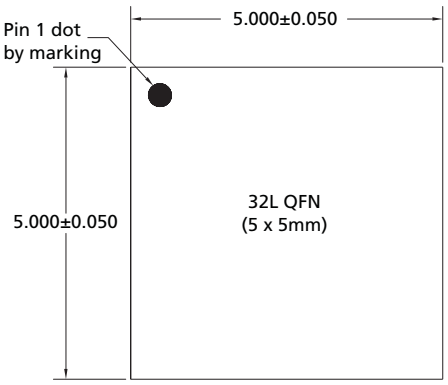


Figure 6-9: RS0, RS1

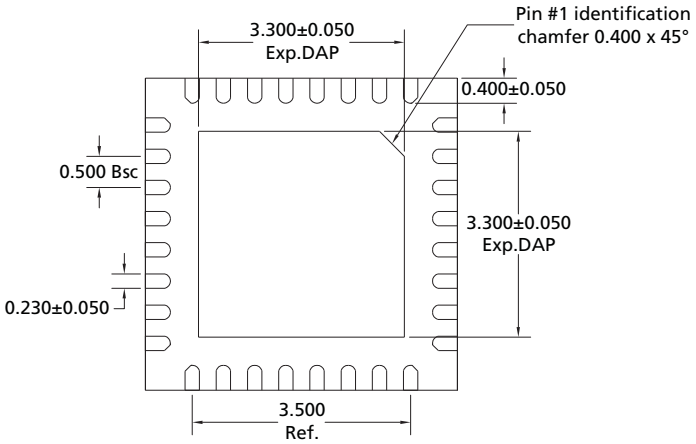
7. Package and Ordering Information

7.1 Package Dimensions

The GX4002 is a 5mm x 5mm, 32-pin QFN.

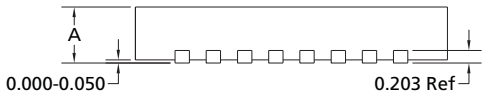


Top View



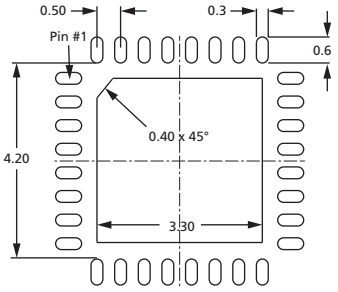
Bottom View

A	MAX.	0.900
	NOM.	0.850
	MIN.	0.800



Side View

7.2 Recommended PCB Footprint



Notes:
1. All dimensions in mm.
2. Drawing not to scale.
3. 16 thermal relief pins, evenly spaced on centre paddle, connected to ground plane.
4. Drill size: 0.254mm.

7.3 Packaging Data

Parameter	Value
Package Type	32-pin QFN / 5mm x 5mm / 0.5mm pad pitch
Moisture Sensitivity Level	3
Junction to Case Thermal Resistance, θ_{j-c}	17.8°C/W
Junction to Air Thermal Resistance (at zero airflow), θ_{j-a}	26.4°C/W
Psi = Junction-to-Top (of Package) Characterization Parameter, Ψ	0.4°C/W
Pb-free and RoHS compliant	Yes

7.4 Solder Reflow Profile

The device is manufactured with Matte-Sn terminations and is compatible with both standard eutectic and Pb-free solder reflow profiles. MSL qualification was performed using the maximum Pb-free reflow profile shown in Figure 7-1.

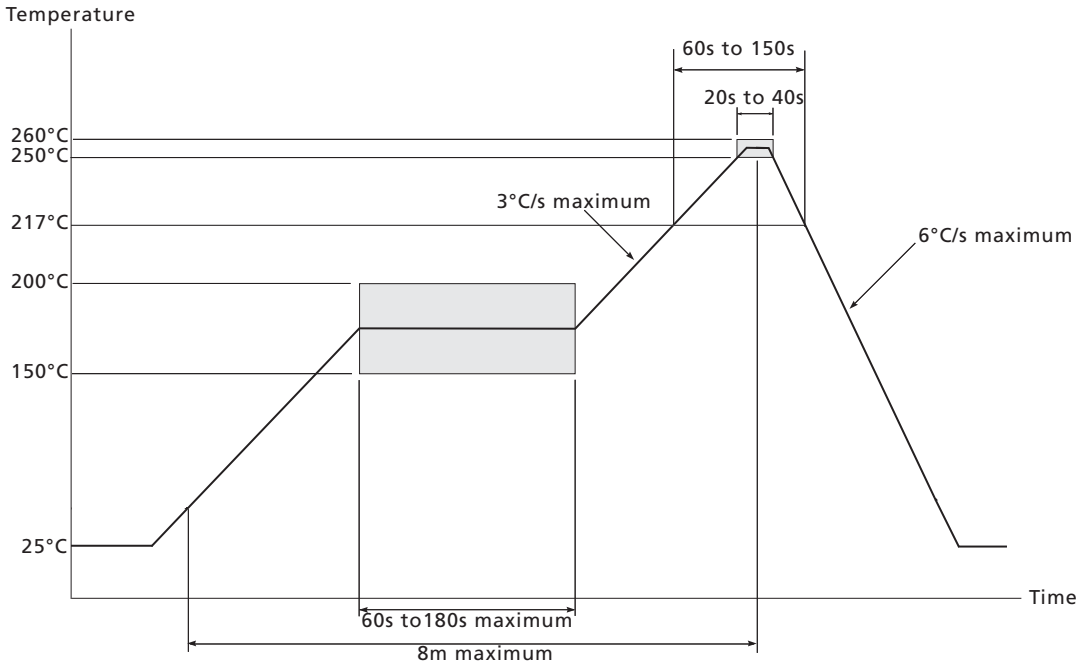
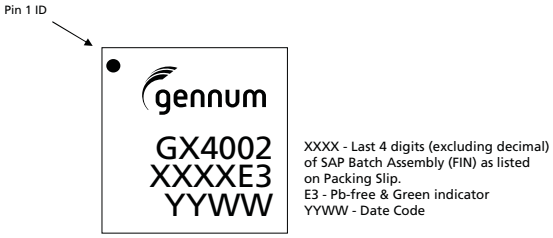


Figure 7-1: Maximum Pb-free Solder Reflow Profile

7.5 Marking Diagram



7.6 Ordering Information

Part Number	Package	Temperature Range
GX4002-INE3	32-pin QFN	-40°C to 100°C

Appendix: Configuration and Status Register Map

NOTE: *Indicates bits for lower data rates (below 10G operation).

Table 7-1: Configuration and Status Register Map

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
RSVD	0	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
TOP_REG1	1	FAULTMASKCH1LOS	0:0	RW	1	0-1	When HIGH, masks out Ch1LOS from asserting Ch0FAULT.
		FAULTMASKCH1LOL	1:1	RW	1	0-1	When HIGH, masks Ch1LOL from asserting Ch0FAULT.
		FAULTMASKCH0LOS	2:2	RW	1	0-1	When HIGH, masks out Ch0LOS from asserting Ch0FAULT.
		FAULTMASKCH0LOL	3:3	RW	1	0-1	When HIGH, masks Ch0LOL from asserting Ch0FAULT.
		FAULTMASKCH0FAULT	4:4	RW	0	0-1	When HIGH masks out Ch0FAULT from asserting Ch0FAULT.
		RSVD	7:5	RW	000	0-7	Reserved. Do not change.
TOP_REG2	2	POLINVCH0FAULT	0:0	RW	0	0-1	When HIGH, inverts polarity of Ch0FAULT output.
		POLINVCH1LOS	1:1	RW	0	0-1	When HIGH, inverts polarity of Ch1LOS output.
		OPENDRAINCH1LOS	2:2	RW	1	0-1	When HIGH, makes Ch1LOS output driver open-drain.
		OPENDRAINCH0FAULT	3:3	RW	1	0-1	When HIGH, makes Ch0FAULT output driver open-drain.
		RSVD	7:4	RW	0000	0-15	Reserved. Do not change.
TOP_REG3	3	PRBSGENSTART	0:0	RW	0	0-1	When pulsed HIGH and LOW, starts off the PRBS generator.
		PRBSCHKCLEARERR	1:1	RW	0	0-1	When HIGH, clears the latched error flag from checker.
		RSVD	7:2	RW	000000	0-63	Reserved. Do not change.
TOP_REG4	4	RSVD	3:0	RW	1111	0-15	Reserved. Do not change.
		FORCECH0FAULT	4:4	RW	0	0-1	When HIGH, asserts CH0FAULT.
		RSVD	7:5	RW	000	0-7	Reserved. Do not change.
RSVD	5	RSVD	7:0	RW	00001111	0-255	Reserved. Do not change.
TOP_REG6	6	PRBSCHKSTATUS	0:0	RO	0	0-1	When HIGH, checker detected an error.
		RSVD	7:1	RW	0000000	0-127	Reserved. Do not change.

NOTE: * Indicates bits for lower data rates (below 10G operation)

Table 7-1: Configuration and Status Register Map (Continued)

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
LOOPBK_REG1	7	LBCH1INEN	0:0	RW	0	0-1	Selects LB input into Ch1 CDR.
		LBCH1INPRBSGEN	1:1	RW	0	0-1	Selects PRBS generator output into Ch1 CDR.
		LBCH1INCH0DATA	2:2	RW	0	0-1	Selects Ch0 data into Ch1 CDR.
		RSVD	3:3	RW	0	0-1	Reserved. Do not change.
		LBCH1OUTEN	4:4	RW	0	0-1	Selects LB input into Ch1 Driver.
		LBCH1OUTCH0DATA	5:5	RW	0	0-1	Selects Ch0 data into Ch1 Driver.
		LBCH1OUTPRBSGEN	6:6	RW	0	0-1	Selects PRBS generator output into Ch1 Driver.
		LBCH1OUTCH1CLK	7:7	RW	0	0-1	Selects Ch1 Clock into Ch1 Driver.
LOOPBK_REG2	8	LBCH0INEN	0:0	RW	0	0-1	Selects LB input into Ch0 CDR.
		LBCH0INPRBSGEN	1:1	RW	0	0-1	Selects PRBS generator output into Ch0 CDR.
		LBCH0INCH0DATA	2:2	RW	0	0-1	Selects Ch0 data into Ch0 CDR.
		RSVD	3:3	RW	0	0-1	Reserved. Do not change.
		LBCH0OUTEN	4:4	RW	0	0-1	Selects LB input into Ch0 Driver.
		LBCH0OUTCH0DATA	5:5	RW	0	0-1	Selects Ch1 data into Ch0 Driver.
		LBCH0OUTPRBSGEN	6:6	RW	0	0-1	Selects PRBS generator output into Ch0 Driver.
		LBCH0OUTCH1CLK	7:7	RW	0	0-1	Selects Ch1 clock into Ch0 Driver.
LOOPBK_REG3	9	PRBSGENCLKSEL	0:0	RW	0	0-1	When HIGH, selects Ch0 recovered clock. LOW selects Ch1 clock.
		PRBSCHKCLKSEL	1:1	RW	0	0-1	When HIGH selects Ch0 recovered clock. LOW selects Ch1 clock.
		RSVD	7:2	RW	000111	0-63	Reserved. Do not change.
CH0PLL_REG1	10	CH0PLLLBWCURVT	4:0	RW	10011	0-31	Adjusts LBW positive temperature coefficient control.
		RSVD	7:5	RW	000	0-7	Reserved. Do not change.
CH0PLL_REG2	11	CH0PLLLBWCURVBE	4:0	RW	01110	0-31	Adjusts LBW negative temperature coefficient control.
		RSVD	7:5	RW	000	0-7	Reserved. Do not change.
RSVD	12	RSVD	1:0	RW	01	0-3	Reserved. Do not change.
		CH0PLLCUR	3:2	RW	01	0-3	CH0PLL control current.
		RSVD	7:4	RW	0000	0-15	Reserved. Do not change.
RSVD	13	RSVD	7:0	RW	00100000	0-255	Reserved. Do not change.

NOTE: * Indicates bits for lower data rates (below 10G operation)

Table 7-1: Configuration and Status Register Map (Continued)

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
CH0PLL_REG5	14	CH0PLLPOLINV	0:0	RW	0	0-1	When HIGH, inverts data path polarity.
		CH0PLLBYPASS	1:1	RW	0	0-1	When HIGH, forces CDR into bypass mode.
		CH0PLLAUTOBYPASSEN	2:2	RW	1	0-1	When HIGH, enables automatic bypass mode.
		CH0PLLRATESEL	3:3	RW	1	0-1	Selects data rates: 0 = 1.25 - 8.5G, 1= 10.3G or 14.025G
		CH0PLLRATESELVAL	4:4	RW	1	0-1	When HIGH, CH0PLLRATESEL is valid, otherwise it is ignored.
		RSVD	7:5	RW	000	0-7	Reserved. Do not change.
RSVD	15	RSVD	7:0	RW	00001010	0-255	Reserved. Do not change.
RSVD	16	RSVD	7:0	RW	00100000	0-255	Reserved. Do not change.
RSVD	17	RSVD	7:0	RW	00000101	0-255	Reserved. Do not change.
CH0PLL_REG9	18	RSVD	5:0	RW	000000	0-63	Reserved. Do not change.
		CH0PLLBWMULT	7:6	RW	10	0-3	LBW multiplier: 00 = 0.67, 10 = 1, 01 = 1.33, 11 = 1.67
CH0PLL_REG10	19	CH0PLLLOS	0:0	RO	0	0-1	Loss of signal when HIGH.
		CH0PLLLOL	1:1	RO	0	0-1	Loss of lock when HIGH.
		RSVD	7:2	RW	000000	0-63	Reserved. Do not change.
CH1PLL_REG1	20	CH1PLLLBWCURVT	4:0	RW	10011	0-31	Adjusts LBW positive temperature coefficient control.
		RSVD	7:5	RW	000	0-7	Reserved. Do not change.
CH1PLL_REG2	21	CH1PLLLBWCURVBE	4:0	RW	01110	0-31	Adjusts LBW negative temperature coefficient control.
		RSVD	7:5	RW	000	0-7	Reserved. Do not change.
CH1PLL_REG3	22	RSVD	1:0	RW	01	0-3	Reserved. Do not change.
		CH1PLLCUR	3:2	RW	01	0-3	Ch1 PLL control current.
		RSVD	7:4	RW	0000	0-15	Reserved. Do not change.
RSVD	23	RSVD	7:0	RW	00100000	0-255	Reserved. Do not change.
CH1PLL_REG5	24	CH1PLLPOLINV	0:0	RW	0	0-1	When HIGH, inverts data path polarity.
		CH1PLLBYPASS	1:1	RW	0	0-1	When HIGH, forces CDR into bypass mode.
		CH1PLLAUTOBYPASSEN	2:2	RW	1	0-1	When HIGH, enables automatic bypass mode.
		CH1PLLRATESEL	3:3	RW	1	0-1	Selects data rates: 0 = 1.25 - 8.5G, 1 = 10.3G or 14.025G
		CH1PLLRATESELVAL	4:4	RW	1	0-1	When HIGH, CH1PLLRATESEL is valid. Otherwise, it is ignored.
		RSVD	7:5	RW	000	0-7	Reserved. Do not change.
RSVD	25	RSVD	7:0	RW	00001010	0-255	Reserved. Do not change.
RSVD	26	RSVD	7:0	RW	00100000	0-255	Reserved. Do not change.
RSVD	27	RSVD	7:0	RW	00000101	0-255	Reserved. Do not change.

NOTE: * Indicates bits for lower data rates (below 10G operation)

Table 7-1: Configuration and Status Register Map (Continued)

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
CH1PLL_REG9	28	RSVD	5:0	RW	001000	0-63	Reserved. Do not change.
		CH1PLLBWMULT	7:6	RW	10	0-3	LBW multiplier: 00 = 0.67, 10 = 1, 01 = 1.33, 11 = 1.67
CH1PLL_REG10	29	CH1PLLLOS	0:0	RO	0	0-1	Loss of signal when HIGH.
		CH1PLLLOL	1:1	RO	0	0-1	Loss of lock when HIGH.
		RSVD	7:2	RW	000000	0-63	Reserved. Do not change.
RSVD	30	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
RSVD	31	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
RSVD	32	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
CH0_REG3	33	CH0EQBOOST*	0:0	RW	1	0-1	When HIGH, applies fixed Ch0 equalizer boost of 6dB. 0dB if LOW. Valid for below 10G operation.
		CH0EQBOOST	1:1	RW	1	0-1	When HIGH, applies a fixed Ch0 Equalizer boost of 6dB, 0dB if LOW. Valid for 10G to 14G operation.
		RSVD	7:2	RW	000000	0-63	Reserved. Do not change.
CH0_REG4	34	CH0EQOFFOVRVAL	6:0	RW	0111111	0-127	Offset correction. 63 for 0 correction with +64/-63 steps.
		RSVD	7:7	RW	0	0-1	Reserved. Do not change.
RSVD	35	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
RSVD	36	RSVD	7:0	RW	00000101	0-255	Reserved. Do not change.
RSVD	37	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
RSVD	38	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
CH0_REG9	39	CH0LOSTHNEG	7:0	RW	01010011	0-255	Negative temperature coefficient LOS threshold setting.
CH0_REG10	40	CH0LOSTHPOS	7:0	RW	00000000	0-255	Positive temperature coefficient LOS threshold setting.
CH0_REG11	41	CH0LOSHYS	3:0	RW	1001	0-15	0: minimum hysteresis, 15: maximum hysteresis.
		RSVD	7:4	RW	0000	0-15	Reserved. Do not change.
CH0_REG12	42	RSVD	2:0	RW	000	0-7	Reserved. Do not change.
		CH0LOSSOFTASSERT	3:3	RW	0	0-1	When HIGH, does a software LOS assert.
		CH0LOSSOFTASSERTEN	4:4	RW	0	0-1	When HIGH, selects software LOS. LOW selects hardware LOS.
		RSVD	7:5	RW	000	0-7	Reserved. Do not change.
CH0_REG13	43	CH0VEYETHADJ	7:0	RW	00000000	0-255	Vertical eye monitor threshold adjustment, 0-255.
CH0_REG14	44	CH0VEYETHPOL	0:0	RW	0	0-1	Vertical eye monitor threshold polarity. HIGH is positive.
		CH0VEYELORANGE	1:1	RW	0	0-1	When HIGH, reduces the range to 0-600mVppd.
		CH0VEYEOFFCALEN	2:2	RW	0	0-1	Vertical eye monitor offset calibration enable.
		RSVD	7:3	RW	00000	0-31	Reserved. Do not change.

NOTE: * Indicates bits for lower data rates (below 10G operation)

Table 7-1: Configuration and Status Register Map (Continued)

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
CH0_REG15	45	CH0PWR1	4:0	RW	01010	0-31	Main power configuration register for the Ch0 path. Default is the high-power setting. Refer to Section 2.4.
		RSVD	7:5	RW	000	0-7	Reserved. Do not change.
CH0_REG16	46	RSVD	2:0	RW	111	0-31	Reserved. Do not change.
		CH0PWR2	4:3	RW	01	0-3	Secondary power configuration register for the Ch0 path. Default is the high-power setting. Refer to Section 2.4.
		RSVD	7:5	RW	000	0-1	Reserved. Do not change.
RSVD	47	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
CH1_REG1	48	CH1LABOOST*	3:0	RW	0000	0-15	0: 0dB to 15: 14dB. Valid for below 10G operation.
		RSVD	7:4	RW	0000	0-15	Reserved. Do not change.
CH1_REG2	49	CH1LABOOST	3:0	RW	0000	0-15	0: 0dB to 15: 14dB. Valid for 10G to 14G operation.
		RSVD	7:4	RW	0000	0-15	Reserved. Do not change.
RSVD	50	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
CH1_REG4	51	CH1LAOFFOVRVAL	6:0	RW	0111111	0-127	Offset correction. 63 for 0 correction with +64/-63 steps.
		RSVD	7:7	RW	0	0-1	Reserved. Do not change.
RSVD	52	RSVD	7:0	RW	00010000	0-255	Reserved. Do not change.
RSVD	53	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
RSVD	54	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
RSVD	55	RSVD	7:0	RW	00001010	0-255	Reserved. Do not change.
CH1_REG9	56	CH1LOSTHNEG*	7:0	RW	10000011	0-255	Negative temperature coefficient LOS threshold setting. Valid for below 10G operation.
CH1_REG10	57	CH1LOSTHPOS*	7:0	RW	00010001	0-255	Positive temperature coefficient LOS threshold setting. Valid for below 10G operation.
CH1_REG11	58	CH1LOSTHNEG	7:0	RW	10000011	0-255	Negative temperature coefficient LOS threshold setting. Valid for 10G to 14G operation.
CH1_REG12	59	CH1LOSTHPOS	7:0	RW	00010001	0-255	Positive temperature coefficient LOS threshold setting. Valid for 10G to 14G operation.
CH1_REG13	60	CH1LOSHYS*	3:0	RW	1001	0-15	0: minimum hysteresis, 15: maximum hysteresis. Valid for below 10G operation.
		CH1LOSHYS	7:4	RW	1001	0-15	0: minimum hysteresis, 15: maximum hysteresis. Valid for 10G to 14G operation.

NOTE: * Indicates bits for lower data rates (below 10G operation)

Table 7-1: Configuration and Status Register Map (Continued)

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
CH1_REG14	61	CH1LOSRANGE*	2:0	RW	001	0-7	1:0 - LOS range 0: highest - 3: lowest, 2 (MSB) unused. Valid for below 10G operation.
		CH1LOSRANGE	5:3	RW	001	0-7	1:0 - LOS range 0: highest - 3: lowest, 2 (MSB) unused. Valid for 10G to 14G operation.
		CH1LOSSOFTASSERT	6:6	RW	0	0-1	When HIGH, selects a software LOS. LOW selects hardware LOS.
		CH1LOSSOFTASSERTEN	7:7	RW	0	0-1	When HIGH, selects software LOS. LOW selects hardware LOS.
CH1_REG15	62	CH1VEYETHADJ	7:0	RW	00000000	0-255	Vertical eye monitor threshold adjustment, 0-255.
CH1_REG16	63	CH1VEYETHPOL	0:0	RW	0	0-1	Vertical eye monitor threshold polarity. HIGH is positive.
		CH1VEYELORANGE	1:1	RW	0	0-1	When HIGH, reduces the range to 0-600mVppd
		CH1VEYEOFFCALEN	2:2	RW	0	0-1	Vertical eye monitor offset calibration enable.
		RSVD	7:3	RW	00000	0-31	Reserved. Do not change.
CH1_REG17	64	CH1PWR1	4:0	RW	01010	0-31	Main power configuration register for the Ch1 path. Default is the high-power setting. Refer to Section 2.4.
		RSVD	7:5	RW	000	0-7	Reserved. Do not change.
CH1_REG18	65	RSVD	4:0	RW	11100	0-31	Reserved. Do not change.
		CH1PWR2	6:5	RW	00	0-3	Secondary power configuration register for the Ch1 path. Default is the high-power setting. Refer to Section 2.4.
		RSVD	7:7	RW	0	0-1	Reserved. Do not change.
CH1_REG19	66	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
CH0RDET_REG1	67	CH0RATEDETRESET	0:0	RW	0	0-1	When HIGH, the rate detector is reset.
		CH0RATEDETEN	1:1	RW	1	0-1	When HIGH, the rate detector is enabled.
		RATEDETFCGBEN	2:2	RW	1	0-1	When HIGH, the application is Fibre Channel, when LOW the application is Ethernet.
		RATEDETFCGBENVAL	3:3	RW	1	0-1	When HIGH, FCGBEn is valid.
		RSVD	7:4	RW	0000	0-15	Reserved. Do not change.
CH0RDET_REG2	68	CH0RATEDETRATEPER	3:0	RW	1000	0-15	Rate detector rate period (0.3µs to 13ms, 100µs default).
		RSVD	7:4	RW	0000	0-15	Reserved. Do not change.
RSVD	69	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
RSVD	70	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
RSVD	71	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
CH1RDET_REG1	72	CH1RATEDETRESET	0:0	RW	0	0-1	When HIGH, the rate detector is reset.
		CH1RATEDETEN	1:1	RW	1	0-1	When HIGH, the rate detector is enabled.
		RSVD	7:2	RW	000000	0-63	Reserved. Do not change.

NOTE: * Indicates bits for lower data rates (below 10G operation)

Table 7-1: Configuration and Status Register Map (Continued)

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
CH1RDET_REG2	73	CH1RATEDETRATEPER	3:0	RW	1000	0-15	Rate detector rate period (0.3µs to 13ms, 100µs default).
		RSVD	7:4	RW	0000	0-15	Reserved. Do not change.
RSVD	74	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
RSVD	75	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
RSVD	76	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
CH1SDO_REG1	77	CH1SDOSWING*	3:0	RW	1010	0-15	Driver swing. 0-15: 100-850mVppd, default=10: 600mV. Valid for below 10G operation.
		CH1SDOSWING	7:4	RW	1010	0-15	Driver swing. 0-15: 100-850mVppd, default=10: 600mV. Valid for 10G to 14G operation.
CH1SDO_REG2	78	CH1SDOPERTCTRL*	1:0	RW	00	0-3	Rise time control. 0:18ps, 1 & 2:22ps, 3: 30ps for 450mVppd swing. Valid for below 10G operation.
		CH1SDOPECTRL*	4:2	RW	000	0-7	Pre-emphasis amplitude. 0: 1.3dB, 7: 6dB for 450mVppd swing. Valid for below 10G operation.
		RSVD	7:5	RW	000	0-7	Reserved. Do not change.
CH1SDO_REG3	79	CH1SDOPERTCTRL	1:0	RW	00	0-3	Rise time control. 0:18ps, 1 & 2:22ps, 3: 30ps for 450mVppd swing. Valid for 10G to 14G operation.
		CH1SDOPECTRL	4:2	RW	000	0-31	Pre-emphasis amplitude. 0: 1.3dB, 7: 6dB for 450mVppd swing. Valid for 10G to 14G operation.
		CH1SDOMUTE	5:5	RW	0	0-1	When HIGH, mutes driver and maintains common mode when not in auto mute mode.
		CH1SDOAUTOMUTEEN	6:6	RW	1	0-1	When HIGH, enables muting the driver upon LOS.
		CH1SDOPWRDNONMUTE	7:7	RW	1	0-1	When HIGH, enables power-down on mute for output stage.
RSVD	80	RSVD	7:0	RW	0000000	0-255	Reserved. Do not change.
RSVD	81	RSVD	7:0	RW	0000000	0-255	Reserved. Do not change.
RSVD	82	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
RSVD	83	RSVD	7:0	RW	00000100	0-255	Reserved. Do not change.
RSVD	84	RSVD	70	RW	00000010	0-255	Reserved. Do not change.
RSVD	85	RSVD	7:5	RW	00000100	0-255	Reserved. Do not change.
RSVD	86	RSVD	7:0	RW	10000010	0-255	Reserved. Do not change.
RSVD	87	RSVD	7:0	RW	00101111	0-255	Reserved. Do not change.
RSVD	88	RSVD	7:0	RW	01010000	0-255	Reserved. Do not change.
SDO0_REG10	89	CH0SWINGSETLO	7:0	RW	00000000	0-255	Ch0 swing setting LSB. 0x0 = 0mVppd, 0xC8 = 400mVppd, 0x190 = 800mVppd swing. Valid for below 10G operation.

NOTE: * Indicates bits for lower data rates (below 10G operation)

Table 7-1: Configuration and Status Register Map (Continued)

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
SDO0_REG11	90	CH0SWINGSETHI	1:0	RW	00	0-3	Ch0 swing setting MSB. 0x0 = 0mVppd, 0xC8 = 400mVppd, 0x190 = 800mVppd swing. Valid for below 10G operation.
		RSVD	7:2	RW	000000	0-63	Reserved. Do not change.
RSVD	91	RSVD	7:0	RW	00011111	0-255	Reserved. Do not change.
RSVD	92	RSVD	7:0	RW	00011111	0-255	Reserved. Do not change.
RSVD	93	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
RSVD	94	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
RSVD	95	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
RSVD	96	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
RSVD	97	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
RSVD	98	RSVD	7:0	RW	11110000	0-255	Reserved. Do not change.
RSVD	99	RSVD	7:0	RW	01010101	0-255	Reserved. Do not change.
RSVD	100	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
CH0SDO_REG25	101	RSVD	2:0	RW	000	0-7	Reserved. Do not change.
		CH0SDOMUTE	3:3	RW	0	0-1	When HIGH, mutes driver and maintains common mode when not in auto mute mode.
		CH0SDOAUTOMUTEEN	4:4	RW	1	0-1	When HIGH, enables muting the driver upon LOS.
		CH0SDOPWRDNONMUTE	5:5	RW	1	0-1	When HIGH, enables power-down on mute for output stage.
		RSVD	7:6	RW	00	0-3	Reserved. Do not change.
RSVD	102	RSVD	7:0	RW	00010011	0-255	Reserved. Do not change.
RSVD	103	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
RSVD	104	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
RSVD	105	RSVD	7:0	RW	00000010	0-255	Reserved. Do not change.
RSVD	106	RSVD	7:0	RW	00000100	0-255	Reserved. Do not change.
RSVD	107	RSVD	7:0	RW	10000010	0-255	Reserved. Do not change.
RSVD	108	RSVD	7:0	RW	00101111	0-255	Reserved. Do not change.
RSVD	109	RSVD	7:0	RW	01010000	0-255	Reserved. Do not change.
SDO0_REG34	110	CH0SWINGSETLO	7:0	RW	00000000	0-255	Ch0 swing setting LSB. 0x0 = 0mVppd, 0xC8 = 400mVppd, 0x190 = 800mVppd swing. Valid for 10G to 14G operation.
SDO0_REG35	111	CH0SWINGSETHI	1:0	RW	00	0-3	Ch0 swing setting MSB. 0x0 = 0mVppd, 0xC8 = 400mVppd, 0x190 = 800mVppd swing. Valid for 10G to 14G operation.
		RSVD	7:2	RW	000000	0-63	Reserved. Do not change.
RSVD	112	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
RSVD	113	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
RSVD	114	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.

NOTE: * Indicates bits for lower data rates (below 10G operation)

Table 7-1: Configuration and Status Register Map (Continued)

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
RSVD	115	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
RSVD	116	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
RSVD	117	RSVD	7:0	RW	11110000	0-255	Reserved. Do not change.
RSVD	118	RSVD	7:0	RW	11111010	0-255	Reserved. Do not change.
RSVD	119	RSVD	7:0	RW	11111010	0-255	Reserved. Do not change.
RSVD	120	RSVD	7:0	RW	00000001	0-255	Reserved. Do not change.
RSVD	121	RSVD	7:0	RW	01010000	0-255	Reserved. Do not change.
RSVD	122	RSVD	7:0	RW	01010000	0-255	Reserved. Do not change.
RSVD	123	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
RSVD	124	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
RSVD	125	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
RSVD	126	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
RSVD	127	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
RSVD	128	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
RSVD	129	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
RSVD	130	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
RSVD	131	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
RSVD	132	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
RSVD	133	RSVD	7:0	RO	00000000	0-255	Reserved. Do not change.
CH0FLT_REG1	134	CH0FAULTEN	0:0	RW	1	0-1	Enable all Ch0 Faults.
		RSVD	5:1	RW	01111	0-31	Reserved. Do not change.
		CH0FAULTCLEARSTATUS	6:6	RW	0	0-1	When HIGH, clears the latched Ch0 fault status.
		RSVD	7:7	RW	0	0-1	Reserved. Do not change.
RSVD	135	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
RSVD	136	RSVD	7:0	RW	11111111	0-255	Reserved. Do not change.
RSVD	137	RSVD	7:0	RW	11111111	0-255	Reserved. Do not change.
RSVD	138	RSVD	7:0	RW	11111111	0-255	Reserved. Do not change.
RSVD	139	RSVD	7:0	RW	00001111	0-255	Reserved. Do not change.
CH0FLT_REG7	140	RSVD	4:0	RO	00000	0-31	Reserved. Do not change.
		CH0FAULTMUTE	5:5	RO	0	0-1	Hardware Fault mask.
		CH0FAULTCH0FAULT	6:6	RO	0	0-1	Latched signal from CH0FAULT output pin of Ch0Fault.
		RSVD	7:7	RW	0	0-1	Reserved. Do not change.
RSVD	141	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.

NOTE: * Indicates bits for lower data rates (below 10G operation)

Table 7-1: Configuration and Status Register Map (Continued)

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
ADC_REG0	142	ADCRESET	0:0	RW	1	0-1	Reset for the ADC.
		ADCAUTOCONVEN	1:1	RW	1	0-1	When HIGH, enables auto conversion. Set LOW for manual.
		ADCJUSTLSB	2:2	RW	1	0-1	When HIGH, justify towards LSB. LOW justifies towards MSB.
		ADCOFFMODE	3:3	RW	0	0-1	When LOW, offset is subtracted from the ADC output. When HIGH, offset is added to the ADC output. NOTE: When HIGH, ADCOFFSETHI[7] is sign and rest of the bits are magnitude. A sign value of 1 represents negative numbers.
		RSVD	7:4	RW	0000	0-15	Reserved. Do not change.
ADC_REG1	143	ADCSRCSEL	3:0	RW	0000	0-15	Select input for ADC (see Section 3.7.1).
		ADCOFFCALEN	7:4	RW	0000	0-15	Select source for offset calibration.
ADC_REG2	144	ADCRESOLUTION	2:0	RW	001	0-7	ADC resolution control: 0-7 -> 4b to 16b.
		ADCCLKRATE	5:3	RW	101	0-7	ADC clock divide ratio.
		RSVD	7:6	RW	00	0-3	Reserved. Do not change.
ADC_REG3	145	ADCSTARTCONV	0:0	RW	0	0-1	ADC start conversion.
		RSVD	7:1	RW	0000000	0-127	Reserved. Do not change.
ADC_REG4	146	ADCDONECONV	0:0	RO	0	0-1	ADC conversion done flag.
		RSVD	7:1	RW	0000000	0-127	Reserved. Do not change.
ADC_REG5	147	ADCOUTLO	7:0	RO	00000000	0-255	ADC output LOW MSB.
ADC_REG6	148	ADCOUTHI	7:0	RO	00000000	0-255	ADC output HIGH MSB.
ADC_REG7	149	ADCOFFSETLO	7:0	RW	00000000	0-255	ADC offset LSB, unsigned binary.
ADC_REG8	150	ADCOFFSETHI	7:0	RW	00000000	0-255	ADC offset MSB, unsigned binary
CH0PWRDN_REG1	151	CH0PDCH0PATH	0:0	RW	0	0-1	When HIGH, power-down for the entire Ch0 path.
		CH0PDCH0CDR*	1:1	RW	0	0-1	When HIGH, power-down for the entire CDR. Valid for below 10G operation.
		CH0PDCH0CDR	2:2	RW	0		When HIGH, power-down for the entire CDR. Valid for 10G to 14G operation.
		CH0PDCH0SDO	3:3	RW	1	0-1	When HIGH, power-down for the entire driver.
		RSVD	7:4	RW	0010	0-15	Reserved. Do not change.
CH0PWRDN_REG2	152	CH0PDEQ	0:0	RW	0	0-1	When HIGH, power-down for the equalizer.
		CH0PDLOS	1:1	RW	0	0-1	When HIGH, power-down for the LOS.
		RSVD	7:2	RW	100000	0-63	Reserved. Do not change.

NOTE: * Indicates bits for lower data rates (below 10G operation)

Table 7-1: Configuration and Status Register Map (Continued)

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
CH0PWRDN_REG3	153	CH0PDRATEDET	0:0	RW	1	0-1	When HIGH, power-down for rate detector.
		CH0PDVEYEMON	1:1	RW	1	0-1	When HIGH, power-down for the Ch0 vertical eye monitor.
		CH0PDHEYEMON	2:2	RW	1	0-1	When HIGH, power-down for the Ch0 horizontal eye monitor.
		CH0PDPKDET	3:3	RW	1	0-1	When HIGH, power-down for the Ch0 peak detector.
		RSVD	4:4	RW	1	0-1	Reserved. Do not change.
		CH0PDCKDIVOUT	5:5	RW	1	0-1	When HIGH, power-down for the divided Ch0 clock divider.
		RSVD	7:6	RW	01	0-3	Reserved. Do not change.
RSVD	154	RSVD	7:0	RW	00001111	0-255	Reserved. Do not change.
CH1PWRDN_REG0	155	CH1PDCH1PATH	0:0	RW	0	0-1	When HIGH, power-down for the entire Ch1 path.
		CH1PDCH1CDR*	1:1	RW	0	0-1	When HIGH, power-down for the entire CDR. Valid for below 10G operation.
		CH1PDCH1CDR	2:2	RW	0	0-1	When HIGH, power-down for the entire CDR. Valid for 10G to 14G operation.
		CH1PDCH1SDO	3:3	RW	0	0-1	When HIGH, power-down the trace driver.
		RSVD	7:4	RW	0001	0-15	Reserved. Do not change.
CH1PWRDN_REG1	156	RSVD	7:0	RW	00000000	0-255	Reserved. Do not change.
CH1PWRDN_REG2	157	CH1PDLA	0:0	RW	0	0-1	When HIGH, power-down for the LA.
		RSVD	1:1	RW	1	0-1	Reserved. Do not change.
		CH1PDLOS	2:2	RW	0	0-1	When HIGH, power-down for the LOS.
		RSVD	7:3	RW	00000	0-31	Reserved. Do not change.
CH1PWRDN_REG3	158	CH1PDRATEDET	0:0	RW	1	0-1	When HIGH, power-down for rate detector.
		CH1PDVEYEMON	1:1	RW	1	0-1	When HIGH, power-down for the Ch1 vertical eye monitor.
		CH1PDHEYEMON	2:2	RW	1	0-1	When HIGH, power-down for the Ch1 horizontal eye monitor.
		CH1PDPKDET	3:3	RW	1	0-1	When HIGH, power-down for the Ch0 peak detector.
		CH1PDDELMON	4:4	RW	1	0-1	When HIGH, power-down for the delay monitor.
		CH1PDCKDIVOUT	5:5	RW	1	0-1	When HIGH, power-down for the divided Ch1 clock divider.
		RSVD	7:6	RW	01	0-3	Reserved. Do not change.
RSVD	159	RSVD	7:0	RW	00001111	0-255	Reserved. Do not change.
RSVD	160	RSVD	7:0	RW	00011111	0-255	Reserved. Do not change.

NOTE: * Indicates bits for lower data rates (below 10G operation)

Table 7-1: Configuration and Status Register Map (Continued)

Register Name	Register Address[d]	Parameter Name	Bit Position	Access	Reset Value[b]	Valid Range[d]	Function
PWRDN_REG2	161	RSVD	0:0	RW	1	0-1	Reserved. Do not change.
		PDPRBSGEN	1:1	RW	1	0-1	When HIGH, power-down the PRBS generator and associated buffers.
		PDPRBSCHK	2:2	RW	1	0-1	When HIGH, power-down the PRBS checker and associated buffers.
		PDTEMPSENSOR	3:3	RW	1	0-1	When HIGH, power-down the temperature sensor(s).
		PDSUPPLYSENSOR	4:4	RW	1	0-1	When HIGH, power-down the supply sensor.
		PDADC	5:5	RW	1	0-1	When HIGH, power-down the ADC.
		RSVD	7:6	RW	00	0-3	Reserved. Do not change.
RSVD	162 to 195	RSVD	7:0	RW	N/A	0-255	Reserved. Do not change.

NOTE: * Indicates bits for lower data rates (below 10G operation)

DATA SHEET

The product is in production. Gennum reserves the right to make changes to the product at any time without notice to improve reliability, function or design, in order to provide the best product possible.

CAUTION

ELECTROSTATIC SENSITIVE DEVICES

DO NOT OPEN PACKAGES OR HANDLE EXCEPT AT A STATIC-FREE WORKSTATION

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