Datasheet

HD74LS74A

Dual D-type Positive Edge-triggered Flip-Flops (with Preset and Clear)

R04DS0012EJ0400
(Previous: REJ03D0415-0300)
Rev.4.00
Dec 21, 2011

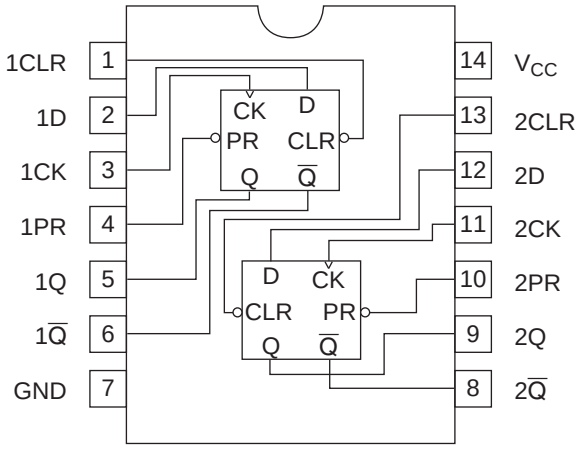
Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS74AP	DILP-14 pin	PRDP0014AB-B (DP-14AV)	P	—
HD74LS74AFPEL	SOP-14 pin (JEITA)	PRSP0014DF-B (FP-14DAV)	FP	EL (2,000 pcs/reel)
HD74LS74ARPEL	SOP-14 pin (JEDEC)	PRSP0014DE-A (FP-14DNV)	RP	EL (2,500 pcs/reel)

Note: Please consult the sales office for the above package availability.

Pin Arrangement



(Top view)

Function Table

Input				Output	
Preset	Clear	Clock	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H; high level, L; low level, X; irrelevant, ↑; transition from low to high level,
Q_0; level of Q before the indicated steady-state input conditions were established.
$\overline{Q}_0$; complement of $\overline{Q}_0$ or level of Q before the indicated steady-state input conditions were established.
*;This configuration is nonstable, that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_{IN}	7	V
Power dissipation	P_T	400	mW
Storage temperature	Tstg	–65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item		Symbol	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}	—	—	–400	μA
		I_{OL}	—	—	8	mA
Operating temperature		Topr	–20	25	75	°C
Clock frequency		f_{clock}	0	—	25	MHz
Pulse width	Clock High	t_w	25	—	—	ns
	Clear Preset	t_w	25	—	—	
Setup time	"H" Data	t_{su}	20↑	—	—	ns
	"L" Data	t_{su}	20↑	—	—	
Hold time		t_h	5↑	—	—	ns

Note: ↑; The arrow indicates the rising edge.

Electrical Characteristics

(Ta = –20 to +75 °C)

Item		Symbol	min.	typ.*	max.	Unit	Condition
Input voltage		V_{IH}	2.0	—	—	V	
		V_{IL}	—	—	0.8	V	
Output voltage		V_{OH}	2.7	—	—	V	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = –400 μA
		V_{OL}	—	—	0.5	V	I_{OL} = 8 mA, V_{CC} = 4.75 V, V_{IL} = 0.8 V, V_{IH} = 2 V
			—	—	0.4		I_{OL} = 4 mA
Input current	D	I_{IH}	—	—	20	μA	V_{CC} = 5.25 V, V_I = 2.7 V
	Clear		—	—	40		
	Preset		—	—	40		
	Clock		—	—	20		
	D	I_{IL}	—	—	–0.4	mA	V_{CC} = 5.25 V, V_I = 0.4 V
	Clear		—	—	–0.8		
	Preset		—	—	–0.8		
	Clock		—	—	–0.4		
	D	I_I	—	—	0.1	mA	V_{CC} = 5.25 V, V_I = 7 V
	Clear		—	—	0.2		
	Preset		—	—	0.2		
	Clock		—	—	0.1		
Short-circuit output current		I_{OS}	–20	—	–100	mA	V_{CC} = 5.25 V
Supply current		I_{CC}**	—	4	8	mA	V_{CC} = 5.25 V
Input clamp voltage		V_{IR}	—	—	–1.5	V	V_{CC} = 4.75 V, I_{IN} = –18 mA

Notes: * V_{CC} = 5 V, Ta = 25°C

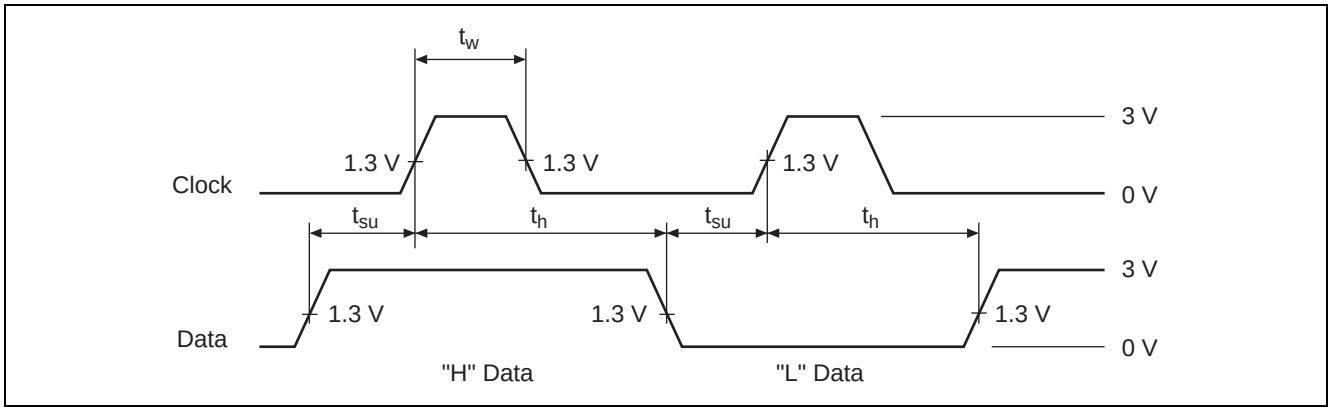
** With all output open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

Switching Characteristics

(V_{CC} = 5 V, Ta = 25°C)

Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	f_{max}			25	33		MHz	C_L = 15 pF, R_L = 2 kΩ
Propagation delay time	t_{PLH}	Clear, Clock or Preset	Q, $\overline{Q}$	—	13	25	ns	
	t_{PHL}			—	25	40	ns	

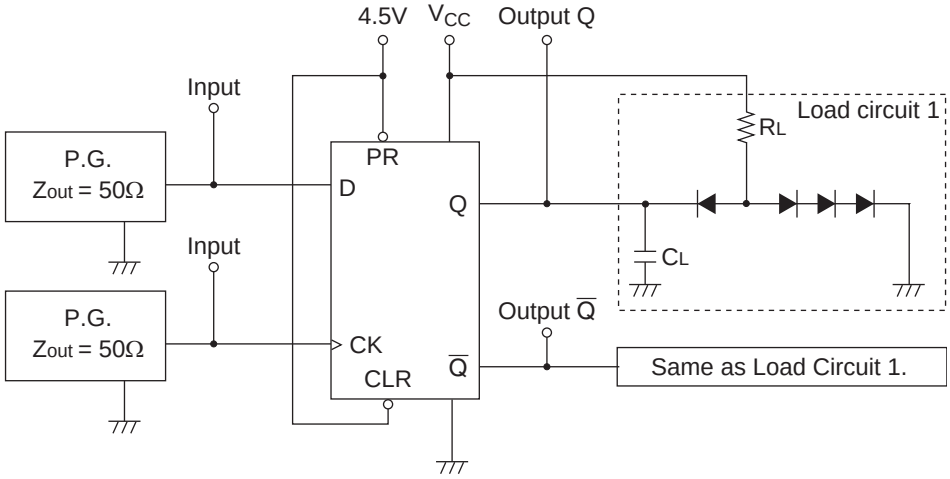
Timing Definition



Testing Method

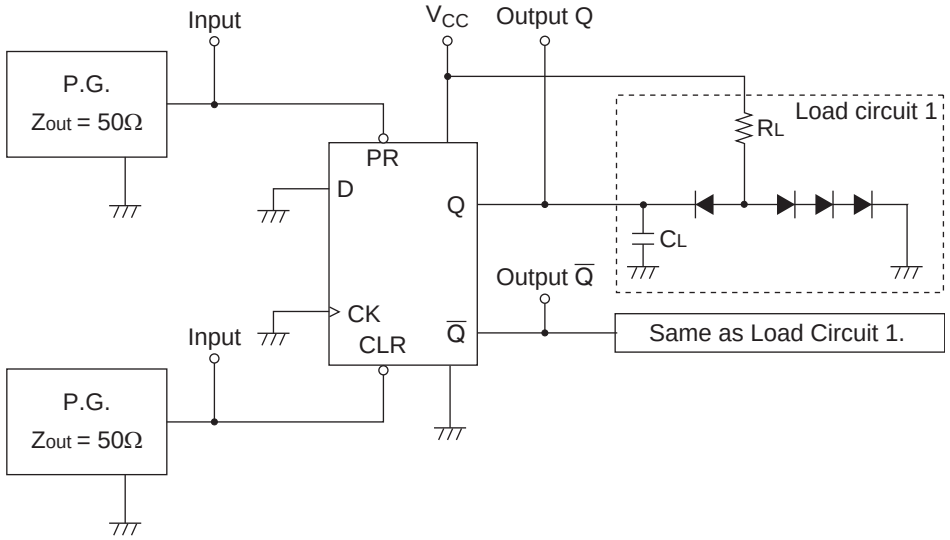
Test Circuit

1. f_{max}, t_{PLH}, t_{PHL} (Clock→Q, $\overline{Q}$)



Notes:
1. Test is put into the each flip-flop.
2. C_L includes probe and jig capacitance.
3. All diodes are 1S2074(H).

2. t_{PHL}, t_{PLH} (Clear or Preset→ Q, $\overline{Q}$)



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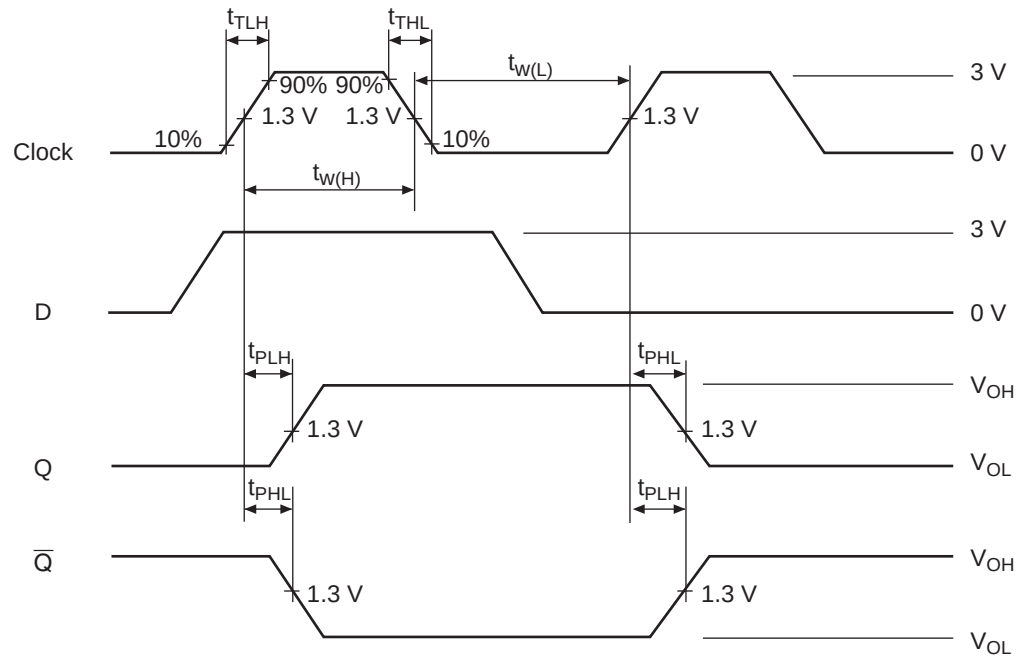
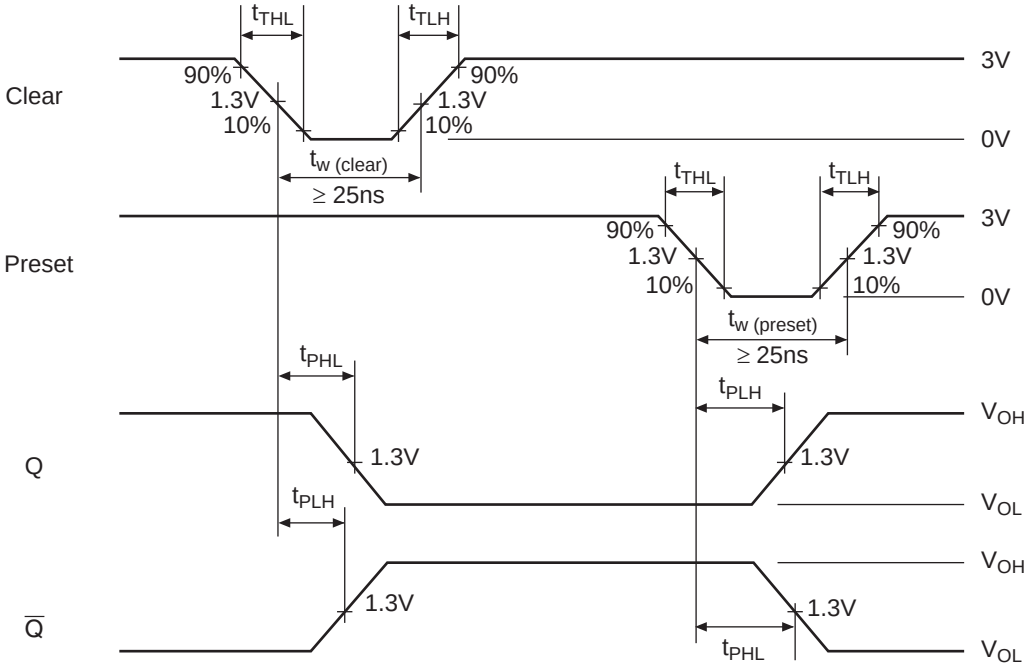
3. All diodes are 1S2074(H).

Waveforms 1



Note: Clock input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz, duty cycle = 50% and for f_{max}, $t_{TLH} = t_{THL} \leq 2.5$ ns

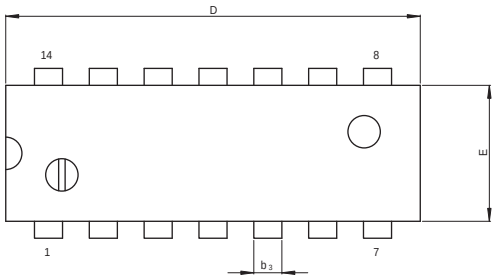
Waveforms 2

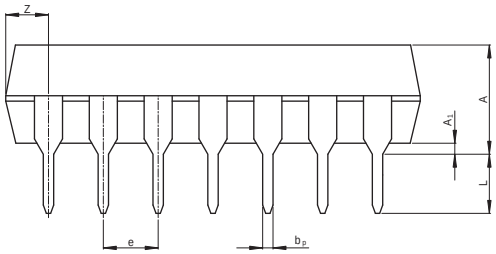


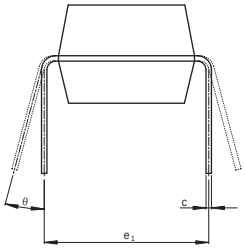
Note: Crear and presel input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz,

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP14-6.3x19.2-2.54	PRDP0014AB-B	DP-14AV	0.97g





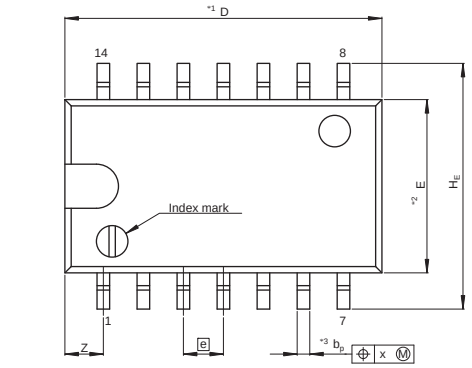


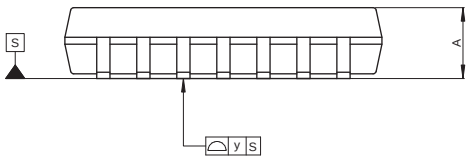
(Ni/Pd/Au plating)

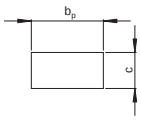
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e_1	—	7.62	—
D	—	19.2	20.32
E	—	6.3	7.4
A	—	—	5.06
A_1	0.51	—	—
b_p	0.40	0.48	0.56
b_3	—	1.30	—
c	0.19	0.25	0.31
θ	0°	—	15°
e	2.29	2.54	2.79
Z	—	—	2.39
L	2.54	—	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP14-5.5x10.06-1.27	PRSP0014DF-B	FP-14DAV	0.23g

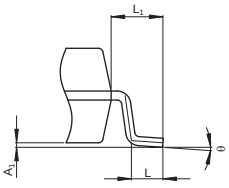
NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2"
   DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT
   INCLUDE TRIM OFFSET.







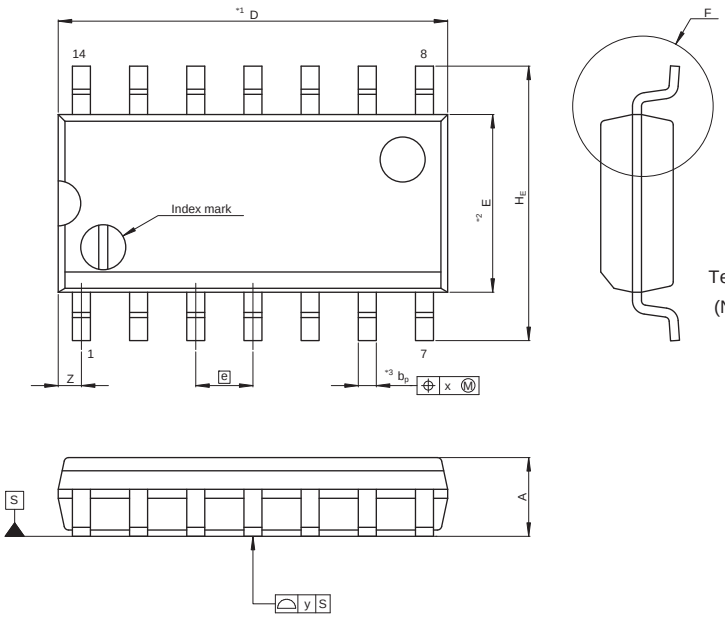
Terminal cross section
(Ni/Pd/Au plating)



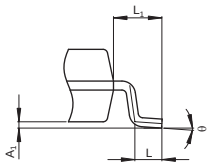
Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	10.06	10.5
E	—	5.50	—
A_2	—	—	—
A_1	0.00	0.10	0.20
A	—	—	2.20
b_p	0.34	0.40	0.46
b_1	—	—	—
c	0.15	0.20	0.25
c_1	—	—	—
θ	0°	—	8°
H_E	7.50	7.80	8.00
e	—	1.27	—
x	—	—	0.12
y	—	—	0.15
Z	—	—	1.42
L	0.50	0.70	0.90
L_1	—	1.15	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP14-3.95x8.65-1.27	PRSP0014DE-A	FP-14DNV	0.13g



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.



Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	8.65	9.05
E	—	3.95	—
A_2	—	—	—
A_1	0.10	0.14	0.25
A	—	—	1.75
b_p	0.34	0.40	0.46
b_1	—	—	—
c	0.15	0.20	0.25
c_1	—	—	—
θ	0°	—	8°
H_E	5.80	6.10	6.20
e	—	1.27	—
x	—	—	0.25
y	—	—	0.15
Z	—	—	0.635
L	0.40	0.60	1.27
L_1	—	1.08	—

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