

Agilent Technologies

Innovating the HP Way

Four Character 5.0 mm (0.20 inch) 5 x 7 Alphanumeric Displays

Technical Data

HDSP-2301
HDSP-2302
HDSP-2303

Features

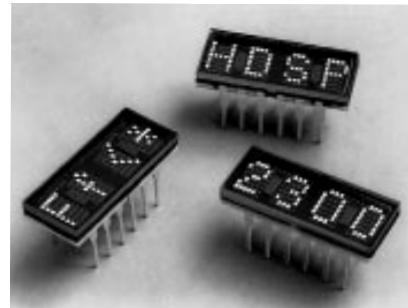
- Integrated Shift Registers with Constant Current Drivers
- Compact Ceramic Package
- Wide Viewing Angle
- End Stackable Four Character Package
- TTL Compatible
- 5 x 7 LED Matrix Displays Full ASCII Set
- Categorized for Luminous Intensity
- **HDSP-2301/2303**
Categorized for Color

Applications

- Avionics
- Business Machines
- Medical Instruments
- Portable Data Entry Devices

Description

The HDSP-2301/2302/2303 series of displays are 5.0 mm (0.20 inch) 5 x 7 LED arrays for display of alphanumeric information. These devices are available in yellow, high efficiency red, and high performance green. Each four character cluster is contained in a 12 pin dual-in-line package. An

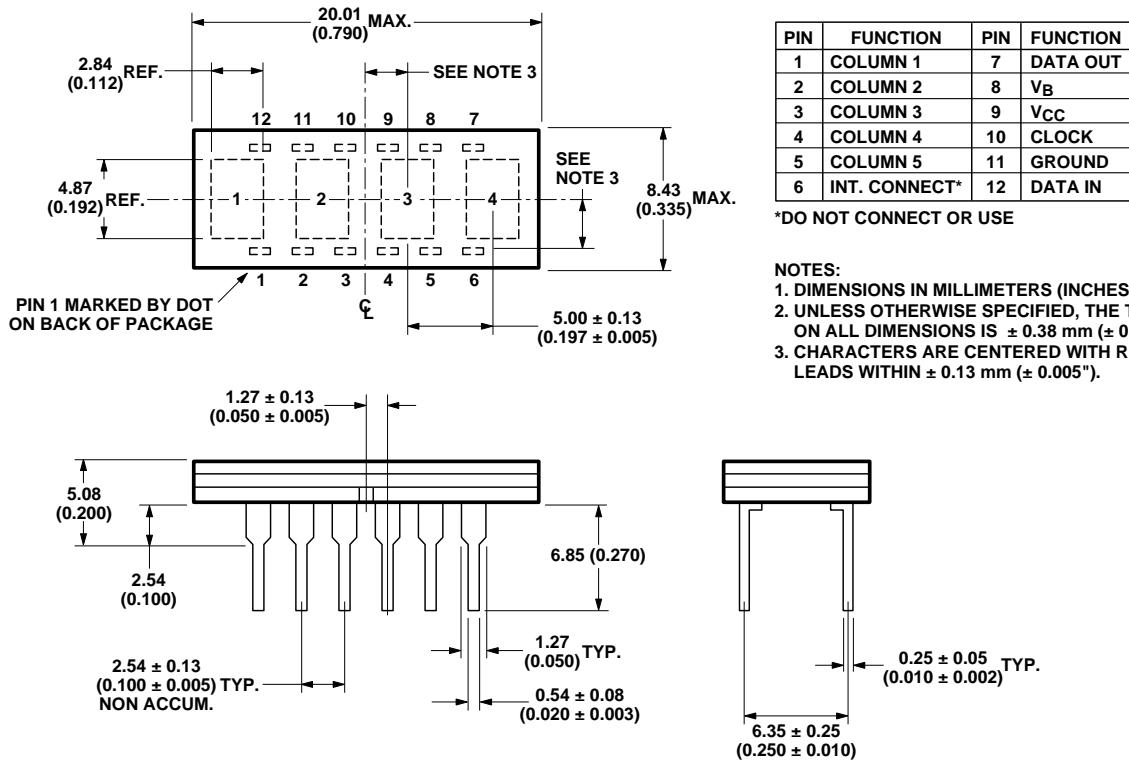


on-board SIPO (Serial-In-Parallel-Out) 7-bit shift register associated with each digit controls constant current LED row drivers. Full character display is achieved by external column strobing.

Devices

Yellow	High Efficiency Red	Green
HDSP-2301	HDSP-2302	HDSP-2303

Package Dimensions



Absolute Maximum Ratings (HDSP-2301/-2302/-2303)

Supply Voltage, V_{CC} to Ground	-0.5 V to 6.0 V
Inputs, Data Out and V_B	-0.5 V to V_{CC}
Column Input Voltage, V_{COL}	-0.5 V to +6.0 V
Free Air Operating Temperature Range, T_A ^[1,2]	-20°C to +85°C
Storage Temperature Range, T_S	-55°C to +100°C
Maximum Allowable Package Dissipation at $T_A = 25^\circ\text{C}$ ^[1,2,3]	
HDSP-2301/-2302/-2303	1.46 Watts
Maximum Solder Temperature	1.59 mm (0.63")	
Below Seating Plane $t < 5$ sec	260°C

Recommended Operating Conditions (HDSP-2301/-2302/-2303)

Parameter	Symbol	Min.	Nom.	Max.	Units	Fig.
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
Data Out Current, Low State	I_{OL}			1.6	mA	
Data Out Current, High State	I_{OH}			-0.5	mA	
Column Input Voltage, Column On HDSP-2301/-2302/-2303	V_{COL}	2.75		3.5	V	4
Setup Time	t_{setup}	70	45		ns	1
Hold Time	t_{hold}	30	0		ns	1
Width of Clock	$t_w(\text{Clock})$	75			ns	1
Clock Frequency	f_{clock}	0		3	MHz	1
Clock Transition Time	t_{THL}			200	ns	1
Free Air Operating Temperature Range ^[1,2]	T_A	-20		85	°C	2

Electrical Characteristics over Operating Temperature Range

(Unless otherwise specified)

Yellow HDSP-2301/High Efficiency Red HDSP-2302/ High Performance Green HDSP-2303

Description		Symbol	Test Conditions		Min.	Typ.*	Max.	Units	Fig.
Supply Current		I _{CC}	V _{CC} = 5.25 V V _{CLOCK} = V _{DATA} = 2.4 V All SR Stages = Logical 1		V _B = 0.4 V		45	60	mA
					V _B = 2.4 V		73	95	mA
Column Current at any Column Input		I _{COL}	V _{CC} = 5.25 V V _{COL} = 3.5 V All SR Stages = Logical 1		V _B = 0.4 V		500	μA	4
Column Current at any Column Input		I _{COL}			V _B = 2.4 V		380	520	
V _B , Clock or Data Input Threshold High		V _{IH}	V _{CC} = V _{COL} = 4.75 V		2.0			V	
V _B , Clock or Data Input Threshold Low		V _{IL}					0.8	V	
Input Current Logical 1	V _B , Clock	I _{IH}	V _{CC} = 5.25 V, V _{IH} = 2.4 V			20	80	μA	
	Data In	I _{IH}				10	40	μA	
Input Current Logical 0	V _B , Clock	I _{IL}	V _{CC} = 5.25 V, V _{IL} = 0.4V			-500	-800	μA	
	Data In	I _{IL}				-250	-400	μA	
Data Out Voltage		V _{OH}	V _{CC} = 4.75 V, I _{OH} = -0.5 mA, I _{COL} = 0 mA		2.4	3.4		V	
		V _{OL}	V _{CC} = 4.75 V, I _{OL} = 1.6 mA, I _{COL} = 0 mA			0.2	0.4	V	
Power Dissipation Per Package**		P _D	V _{CC} = 5.0 V, V _{COL} = 3.5 V, 17.5% DF 15 LEDs on per character, V _B = 2.4 V			0.78		W	2
Thermal Resistance IC Junction-to-Case		R _{θJ-C}				25		°C/W/ Device	2

*All typical values specified at V_{CC} = 5.0 V and T_A = 25°C unless otherwise noted.

**Power dissipation per package with four characters illuminated.

Notes:

1. Operation above 85°C ambient is possible provided the following conditions are met. The junction temperature should not exceed 125°C T_j and the case temperature (as measured at pin 1 or the back of the display) should not exceed 100°C T_C.
2. The HDSP-2301/-2302/-2303 should be derated linearly above 37°C at 16.7 mW/°C. This derating is based on a device mounted in a socket having a thermal resistance from case to ambient at 35°*** C/W per device. See Figure 2 for power deratings based on a lower thermal resistance.
3. Maximum allowable dissipation is derived from V_{CC} = 5.25 V, V_B = 2.4 V, V_{COL} = 3.5 V 20 LEDs on per character, 20% DF.

Optical Characteristics

Yellow HDSP-2301

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED ^[4,8] (Character Average)	$I_{v\text{Peak}}$	$V_{CC} = 5.0 \text{ V}$, $V_{COL} = 3.5 \text{ V}$ $T_i = 25^\circ\text{C}^{[6]}$, $V_B = 2.4 \text{ V}$	650	1140		μcd	3
Peak Wavelength	λ_{PEAK}			583		nm	
Dominant Wavelength ^[5,7]	λ_d			585		nm	

High Efficiency Red HDSP-2302

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED ^[4,8] (Character Average)	$I_{v\text{Peak}}$	$V_{CC} = 5.0 \text{ V}$, $V_{COL} = 3.5 \text{ V}$ $T_i = 25^\circ\text{C}^{[6]}$, $V_B = 2.4 \text{ V}$	650	1430		μcd	3
Peak Wavelength	λ_{PEAK}			635		nm	
Dominant Wavelength ^[7]	λ_d			626		nm	

High Performance Green HDSP-2303

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED ^[4,8] (Character Average)	$I_{v\text{Peak}}$	$V_{CC} = 5.0 \text{ V}$, $V_{COL} = 3.5 \text{ V}$ $T_i = 25^\circ\text{C}^{[6]}$, $V_B = 2.4 \text{ V}$	1280	2410		μcd	3
Peak Wavelength	λ_{PEAK}			568		nm	
Dominant Wavelength ^[5,7]	λ_d			574		nm	

*All typical values specified at $V_{CC} = 5.0 \text{ V}$ and $T_A = 25^\circ\text{C}$ unless otherwise noted.

**Power dissipation per package with four characters illuminated.

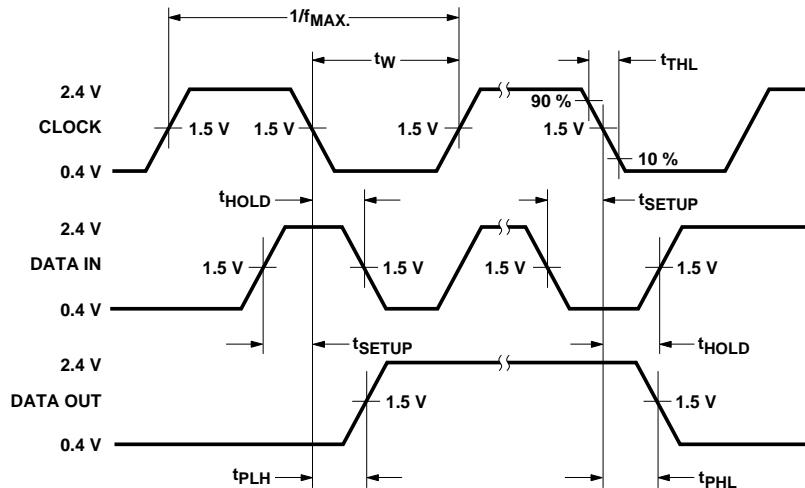
Notes:

- The characters are categorized for luminous intensity with the intensity category designated by a letter code on the bottom of the package.
- The HDSP-2301/-2303 are categorized for color with the color category designated by a number code on the bottom of the package.
- T_i refers to the initial case temperature of the device immediately prior to the light measurement.
- Dominant wavelength λ_d , is derived from the CIE chromaticity diagram, and represents the single wavelength which defines the color of the device.
- The luminous sterance of the LED may be calculated using the following relationships:

$$L_v (\text{cd/m}^2) = l_v (\text{Candela})/A (\text{Metre})^2$$

$$L_v (\text{Footlamberts}) = \pi i_v (\text{Candela})/A (\text{Foot})^2$$

$$A = 5.3 \times 10^{-8} \text{ M}^2 = 5.8 \times 10^{-7} (\text{Foot})^2$$



PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
f_{CLOCK} CLOCK RATE				3	MHz
t_{PLH}, t_{PHL} PROPAGATION DELAY CLOCK TO DATA OUT	$C_L = 15 \text{ pF}$ $R_L = 2.4 \text{ k}\Omega$			125	ns

Figure 1. Switching Characteristics HDSP-2301/-2302/-2303 ($T_A = -20^\circ\text{C}$ to $+85^\circ\text{C}$).

HDSP-2301/-2302/-2303

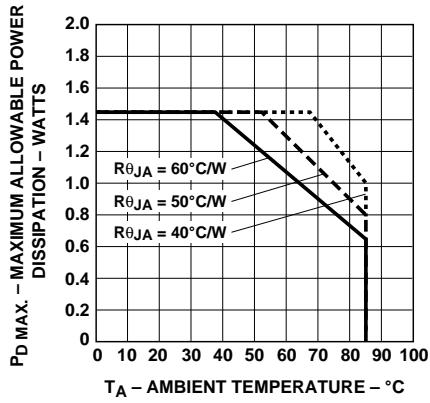


Figure 2. Maximum Allowable Power Dissipation vs. Temperature.

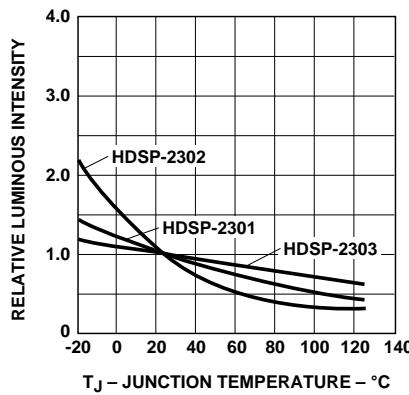


Figure 3. Relative Luminous Intensity vs. Temperature.

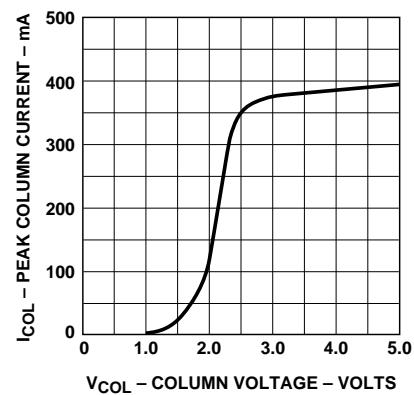


Figure 4. Peak Column Current vs. Column Voltage.

Electrical Description

The HDSP-230X series of four character alphanumeric displays have been designed to allow the user maximum flexibility in interface electronics design. Each four character display module features Data In and Data Out terminals arrayed for easy PC board interconnection. Data Out represents the output of the 7th bit of digit number 4 shift register. Shift register clocking occurs on the high to low transition of the Clock input. The like columns of each character in a display cluster are tied to a single pin. Figure 5 is the block diagram for the displays. High true data in the shift register enables the output current mirror driver stage associated with each row of LEDs in the 5 x 7 diode array.

The TTL compatible V_B input may either be tied to V_{CC} for maximum display intensity or pulse width modulated to achieve intensity control and reduction in power consumption.

The normal mode of operation input data for digit 4, column 1,

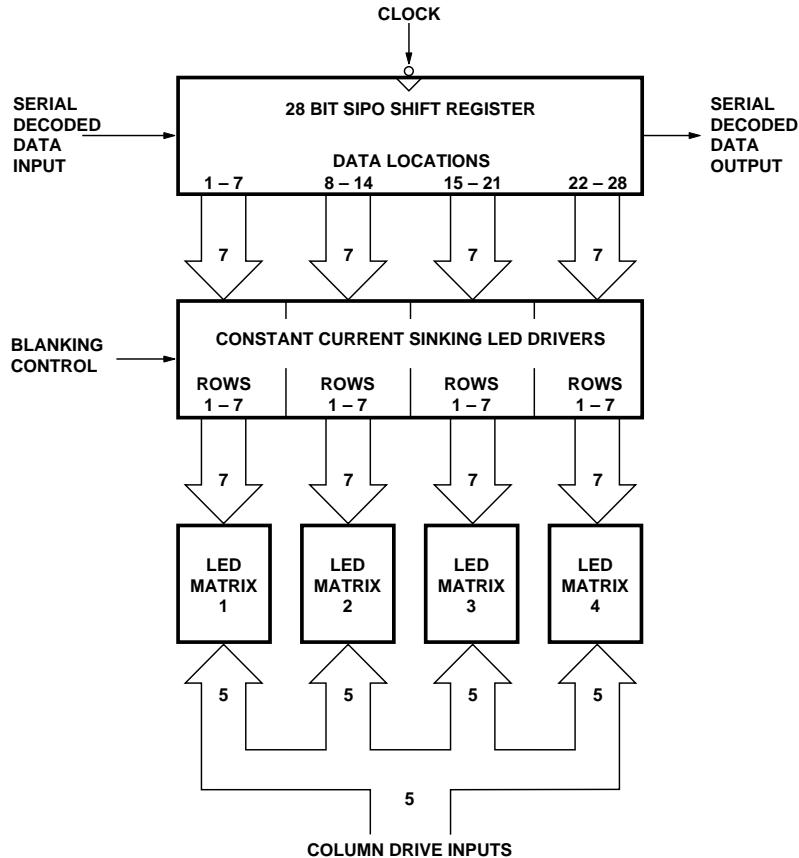


Figure 5. Block Diagram of HDSP-2301/-2302/-2303.

The normal mode of operation input data for digit 4, column 1,

Display Color	Ambient Lighting		
	Dim	Moderate	Bright
HDSP-2301 (Yellow)	Panelgraphic Yellow 27 Chequers Amber 107	Polaroid HNCP37 3M Light Control Film Panelgraphic Gray 10	Polaroid HNCP10
HDSP-2302 (HER)	Panelgraphic Ruby Red 60 Chequers Red 112	Chequers Grey 105	
HDSP-2303 (HP Green)	Panelgraphic Green 48 Chequers Green 107		

Figure 6. Contrast Enhancement Filters.

is loaded into the 7 on-board shift register locations 1 through 7. Column 1 data for digits 3, 2, and 1 is similarly shifted into the display shift register locations. The column 1 input is now enabled for an appropriate period of time, T. A similar process is repeated for columns 2, 3, 4, and 5. If the time necessary to decode and load data into the shift register is t, then with five columns, each column of the display is operating at a duty factor of:

$$D.F. = \frac{T}{5(t + T)}$$

The time frame, $t + T$, allotted to each column of the display is generally chosen to provide the maximum duty factor consistent with the minimum refresh rate necessary to achieve a flicker free display. For most strobed display systems, each column of the display should be refreshed (turned on) at a minimum rate of 100 times per second.

With columns to be addressed, this refresh rate then gives a value for the time $t + T$ of:

$$1/[5 \times (100)] = 2 \text{ msec}$$

If the device is operated at 3.0 MHz clock rate maximum, it is possible to maintain $t \ll T$. For short display strings, the duty factor will then approach 20%.

For further applications information, refer to Agilent Application Note 1016.

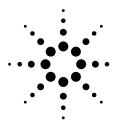
Mechanical and Thermal Considerations

The HDSP-2301/-2302/-2303 are available in standard ceramic dual-in-line packages. They are designed for plugging into sockets or soldering into PC boards. The packages may be horizontally or vertically stacked for character arrays of any desired size. The HDSP-2301/-2302/-2303 utilize a high output current IC to provide excellent readability in bright ambient lighting. Full power operation ($V_{CC} = 5.25 \text{ V}$, $V_B = 2.4 \text{ V}$, $V_{COL} = 3.5 \text{ V}$) with worst case thermal resistance from IC junction to ambient of $60^\circ\text{C}/\text{watt}/\text{device}$ is possible up to ambient temperature of 37°C . For operation above 37°C , the maximum device dissipation should be derated linearly at $16.7 \text{ mW}/^\circ\text{C}$ (see Figure 2). With an improved thermal design, operation at higher ambient temperatures without derating is possible.

The HDSP-2301/-2302/-2303 displays have glass windows. A front panel contrast enhancement filter is desirable in most actual display applications. Some suggested filter materials are provided in Figure 6. Additional information on filtering and contrast enhancement can be found in Agilent Application Note 1015.

For more information on soldering and post-solder cleaning, please see Application Note 1027, Soldering LED Components.

Power derating for this family of displays can be achieved in several ways. The power supply voltage can be lowered to a minimum of 4.75 V . Column Input Voltage, V_{COL} , can be decreased to the recommended minimum value of 2.75 V for the HDSP-2301/-2302/-2303. Also, the average drive current can be decreased through pulse width modulation of V_B .



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Obsoletes 5953-7749E

5966-2487E (11/99)



Using the HDSP-2000 Alphanumeric Display Family

Application Note 1016

Introduction

First introduced in 1975, the HDSP-2000 alphanumeric display has been designed into a variety of applications. The HDSP-2000 display was originally designed for commercial, industrial, instrumentation, and business equipment applications. However, the introduction of high efficiency red, yellow, and high performance green devices as well as several display sizes has opened up a multitude of new applications for the HDSP-2000 alphanumeric display family. The high efficiency red, yellow, and high performance green devices use gallium phosphide (GaP) LEDs. The GaP displays are readable in direct sunlight with proper contrast enhancement techniques. For this reason, the HDSP-2000 family displays have been designed into a variety of avionic and process control applications. The HDSP-2000 family displays are available in three character sizes of 3.8 mm (0.15"), 4.9 mm (0.19"), and 6.9 mm (0.27") to allow the designer to optimize display compactness versus long distance readability. Versions of the HDSP-2000 family alphanumeric displays are available with a true hermetic package and an operat-

ing temperature range of -55°C to +85°C to allow designers to utilize the proven reliability of LED display technology in military and aerospace applications.

This note is intended to serve as a design and application guide for users of the HDSP-2000 family of alphanumeric display devices. The information presented will cover: the theory of the device design and operation; considerations for specific circuit designs; thermal management, power derating and heat sinking; intensity modulation techniques.

The HDSP-2000 family has been designed to provide a high resolution information display subsystem. Each character of the 4 character package consists of a 5 x 7 array of LEDs which can display a full range of alphabetic and numeric characters plus punctuation, mathematical and other special symbols. The HDSP-2000 family is available in four colors: red, high efficiency red, yellow, and high performance green.

The character height, character spacing, color and part number of each member of the HDSP-2000 family of displays is shown in

Table 1. The overall package size is designed to allow end stacking of multiple clusters to form character strings of any desired length.

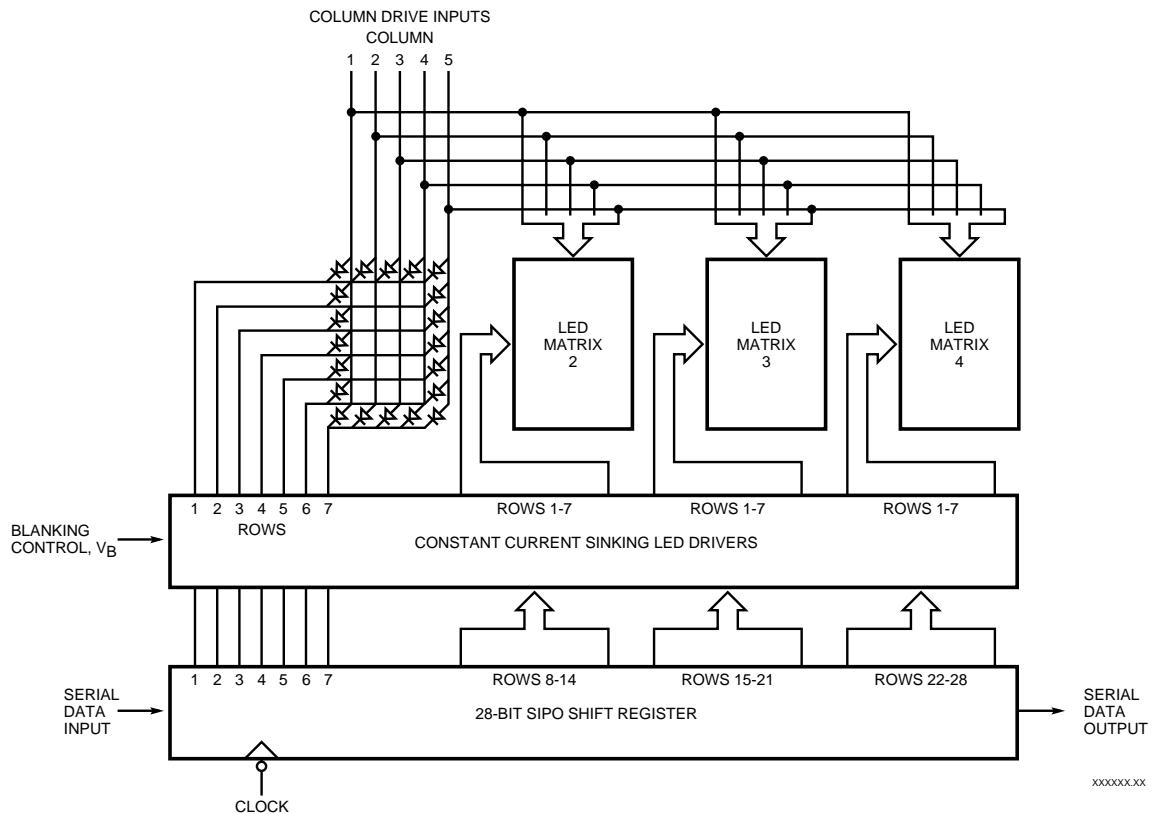
Electrical Description

The on-board electronics of the HDSP-2000 display family eliminates some of the classical difficulties associated with the use of alphanumeric displays. Traditionally, single digit LED dot matrix displays have been organized in an x-y addressable array requiring 12 interconnect pins per digit plus extensive row and column drive support electronics. All members of the HDSP-2000 display family provide on-board storage of decoded row data plus constant current sinking row drivers for each of the 28 rows in the 4 character display. This approach allows the user to address each display package through just 11 active interconnections vs. the 176 interconnections and 36 components required to effect a similar function using conventional LED matrices.

Figure 1 is a block diagram of the internal circuitry of the HDSP-2000 display. The device consists of four LED matrices and

Table 1. The HDSP-2000 Alphanumeric Display Family

Device	Color	Character Height	Character Spacing	Operating Temperature
HDSP-2000	Red	3.8 mm (0.15 in.)	4.5 mm (0.175 in.)	-20°C to +85°C
HDSP-2001	Yellow	3.8 mm (0.15 in.)	4.5 mm (0.175 in.)	-20°C to +85°C
HDSP-2002	High Efficiency Red	3.8 mm (0.15 in.)	4.5 mm (0.175 in.)	-20°C to +85°C
HDSP-2003	High Performance Green	3.8 mm (0.15 in.)	4.5 mm (0.175 in.)	-20°C to +85°C
HDSP-2300	Red	4.9 mm (0.192 in.)	5.0 mm (0.197 in.)	-20°C to +85°C
HDSP-2301	Yellow	4.9 mm (0.192 in.)	5.0 mm (0.197 in.)	-20°C to +85°C
HDSP-2302	High Efficiency Red	4.9 mm (0.192 in.)	5.0 mm (0.197 in.)	-20°C to +85°C
HDSP-2303	High Performance Green	4.9 mm (0.192 in.)	5.0 mm (0.197 in.)	-20°C to +85°C
HDSP-2490	Red	6.9 mm (0.27 in.)	8.9 mm (0.35 in.)	-20°C to +85°C
HDSP-2491	Yellow	6.9 mm (0.27 in.)	8.9 mm (0.35 in.)	-20°C to +85°C
HDSP-2492	High Efficiency Red	6.9 mm (0.27 in.)	8.9 mm (0.35 in.)	-20°C to +85°C
HDSP-2493	High Performance Green	6.9 mm (0.27 in.)	8.9 mm (0.35 in.)	-20°C to +85°C
HDSP-2010	Red	3.8 mm (0.15 in.)	4.5 mm (0.175 in.)	-40°C to +85°C
HDSP-2310	Red	4.9 mm (0.192 in.)	5.0 mm (0.197 in.)	-55°C to +85°C
HDSP-2311	Yellow	4.9 mm (0.192 in.)	5.0 mm (0.197 in.)	-55°C to +85°C
HDSP-2312	High Efficiency Red	4.9 mm (0.192 in.)	5.0 mm (0.197 in.)	-55°C to +85°C
HDSP-2450	Red	6.9 mm (0.27 in.)	8.9 mm (0.35 in.)	-55°C to +85°C
HDSP-2451	Yellow	6.9 mm (0.27 in.)	8.9 mm (0.35 in.)	-55°C to +85°C
HDSP-2452	High Efficiency Red	6.9 mm (0.27 in.)	8.9 mm (0.35 in.)	-55°C to +85°C

**Figure 1. Block Diagram**

two 14-bit serial-in-parallel-out shift registers. The LED matrix for each character is a 5 x 7 diode array organized with the anodes of each column tied in common and the cathodes of each row tied in common. The 7 row cathode commons of each character are tied to the constant current sinking outputs of 7 successive stages of the shift register. The like columns of the 4 characters are tied together and brought to a single address pin (i.e., column 1 of all 4 characters is tied to pin 1, etc.). In this way, any diode in the four 5 x 7 matrices may be addressed by shifting data to the appropriate shift register location and applying a voltage to the appropriate column.

The serial-in-parallel-out (SIPO) shift register has a constant current sinking output associated with each shift register stage. This constant current output drives each LED at a nominal peak current of 12 to 14 mA peak. The output stage is a current mirror design with a nominal current gain of 10. A logical 1 loaded into each shift register bit will turn "ON" the corresponding current source provided that a logical 1 is applied to the Blanking Input, V_B . If V_{COL} is applied to the appropriate Column Input, the corresponding LED diode will be turned "ON". Since the row drivers have a constant current output, the LED current will remain constant as long as the Column Input voltage exceeds 2.4 V for red and 2.75 V for high efficiency red, yellow, and high performance green devices.

Data is loaded serially into the shift register on the high to low transition of the Clock Input.

During the time that data is being loaded into the display, the column current must be disabled to minimize the generation of "current spikes" between V_{CC} , the columns, and ground. The resulting power supply noise could induce noise on the Clock and Data Inputs. The column current can be disabled either by switching off the column drivers or by applying a logical 0 to the Blanking Input.

The Data Output terminal is a TTL buffer interface to the 28th bit of the shift register (i.e., the 7th row of character 4 in each package). The Data Output is arranged to directly interconnect to the Data Input on a succeeding 4 digit HDSP-2000 display package. The Data, Clock and V_B inputs are all buffered to allow direct interface to any TTL logic family.

Theory of Operation

Dot matrix alphanumeric display systems generally have a logical organization which prescribes that any character be generated as a combination of several subsets of data. In a 5 x 7 matrix, this could be either 5 subsets of 7 bits each or 7 subsets of 5 bits each. This technique is utilized to reduce from 35 to 5 or 7 the number of outputs required from the character generator. In order to display a complete character, these subsets of data are then presented sequentially to the appropriate locations of the display matrix. If this process is repeated at a rate which insures that each of the appropriate matrix locations is reenergized a minimum of 100 times per second, the eye will perceive a continuous image of the entire character. The apparent intensity of each of the display elements will be equal to

the intensity of that element during the "ON" period multiplied by the ratio of "ON" time to refresh period. This ratio is referred to as the display duty factor, and the technique is referred to as "strobing". In the case of HDSP-2000, each character is made up of 5 subsets of 7 bits. For a four character display, 28 bits representing the first subset of each of the four characters are loaded serially into the on-board SIPO shift register and the first column is then energized for a period of time, T . This process is then repeated for columns 2 through 5. If the time required to load the 28 bits into the SIPO shift register is t , then the duty factor is:

$$D.F. = \frac{T}{5(t+T)}; \quad (1)$$

the term $5(t+T)$ is then the refresh period. For satisfactory display, the refresh period should be:

$$1/[5(t+T)] \geq 100 \text{ Hz} \quad (2)$$

or conversely

$$5(t+T) \leq 10 \text{ m sec}, \quad (3)$$

which gives

$$(t+T) \leq 2 \text{ m sec.} \quad (4)$$

The time averaged luminous intensity of the display can be varied continuously over a range greater than 1000 to 1 by turning off or blanking the display before loading new data into the SIPO shift register. If the time that the display is blanked is T_B , then the duty factor of the display becomes:

$$D.F. = \frac{T}{5(t + T + T_B)} \quad (5)$$

where

$$(t + T + T_B) \leq 2 \text{ m sec.} \quad (5a)$$

Drive Circuit Concepts

A practical display system utilizing the HDSP-2000 family of displays requires interfacing with a character generator, refresh memory and some timing circuitry. A block diagram of such a display system is depicted in Figure 2. This circuit provides for ASCII data storage and decoding and properly refreshes the display at a 100 Hz refresh rate. In this figure, the display length is shown as N characters with the leftmost display character labeled as character 1 and the right most character of the display labeled as character N. The refreshing of the display is accomplished by a series of counters.

The $\div N$ counter sequentially accesses N coded information symbols from the $N \times 7$ RAM. Note that for the normal configuration of the HDSP-2000 displays, character 1 is the leftmost character, character 4 is the rightmost character and shift register cascades from left to right. Thus, the symbol corresponding to character N is decoded first, then the symbol corresponding to character (N-1), and the symbol corresponding to character 1 is decoded last.

Each coded information symbol is read from the $N \times 7$ RAM and decoded by a 5×7 decoder. The decoder can be selected to decode ASCII, EBDIC, or any customized character font. In this example, the ASCII decoder is organized as 128 x 7 words of 5 bits each. The ASCII symbol and row select information is applied to the decoder and the decoder outputs information for all 5 columns for the selected row and symbol.

The $\div 7$ counter sequentially accesses all seven rows of each ASCII symbol. Note that row 7 must be decoded first, then row 6, and row 1 is decoded last. The $\div M$ counter is used to periodically load new serial data into the HDSP-2000 display. During one count, the display clock is enabled and 7N bits of serial data are loaded into the display. During the remaining (M-1) counts, this data is displayed. Thus the duty factor for the circuit in Figure 2 is

$$D.F. = \frac{(M-1)}{5M} = .20 \left(1 - M^{-1}\right) \quad (6)$$

The $\div 5$ counter sequentially refreshes all 5 columns of the display. The outputs of the $\div 5$ counter are connected to a data multiplexer which selects one of the 5 outputs from the ASCII decoder and loads it into the Data Input of the HDSP-2000 display string. The $\div 5$ counter also enables one of the 5 column driver

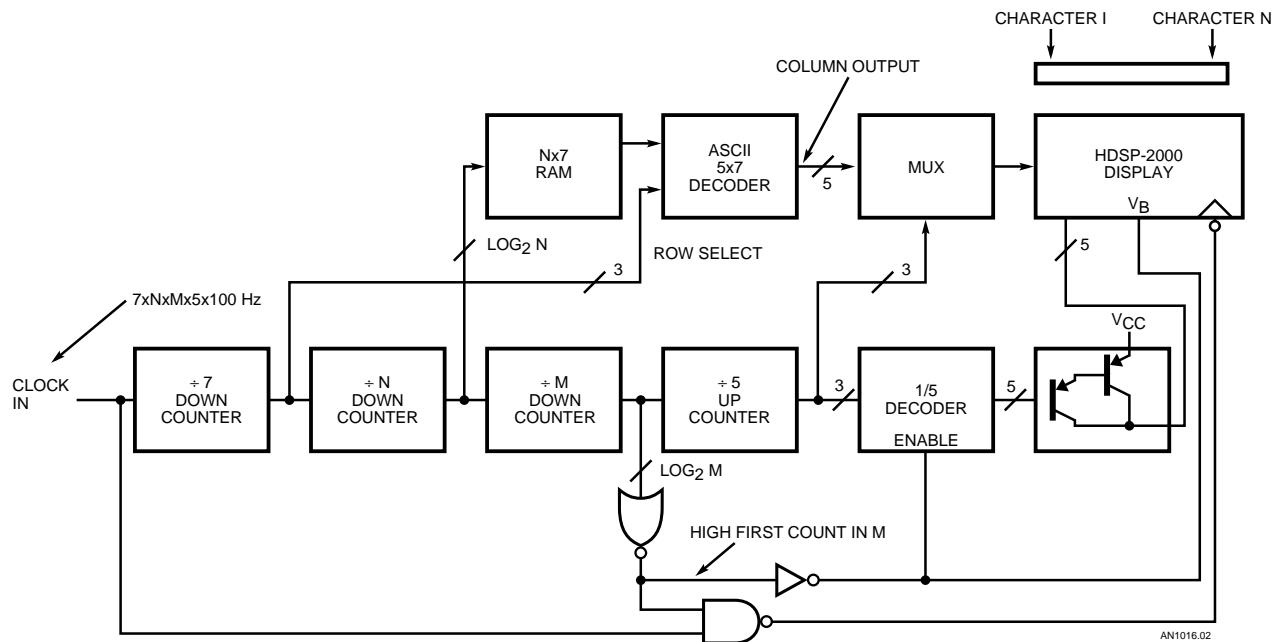


Figure 2. CKT Block Diagram

transistors. Note that the display is blanked via the V_B input and also that the column driver transistors are turned off during the time that new data is being loaded into the HDSP-2000 display string. This will eliminate any high current transients between the column inputs and ground during the data shifting operation.

Since data is loaded for all of the like columns in the display string and these columns are then enabled simultaneously, only five column switch transistors are required regardless of the number of characters in the string. The column switch transistors should be selected to handle 105 to 130 mA per character in the display string. The collector emitter saturation voltage characteristics and column voltage supply should be chosen to provide $2.4 \text{ V} \leq V_{COL} \leq V_{CC}$ for the standard red displays and $2.75 \text{ V} \leq V_{COL} \leq V_{CC}$ for the high efficiency red, yellow, and high performance green displays. To save on power supply costs and improve efficiency, this supply may be a fullwave rectified unregulated DC voltage as long as the PEAK value does not exceed the value of V_{CC} and the minimum value does not drop below 2.4 V or 2.75 V depending on display color.

Figures 13 and 16 show practical implementations of the block diagram shown in Figure 2. In those circuits, the display is mounted upside down, so that pin 1 is in the upper right hand corner. With this technique, data is loaded into display character N and data shifts from right to left as new data is loaded. The first bit loaded into the display would be row 1, character 1, then row 2, etc., and the last bit loaded would be row 7

of character N. This allows the $\div 7$, $\div N$ and $\div M$ counters to be implemented as up counters instead of down counters. Since the display is upside down, column 5 of the display appears to be column 1 and column 4 of the display appears to be column 2. Thus, column 1 data for the display must be loaded into the display and column 5 must subsequently be enabled. This is accomplished by reversing the outputs of the 5×7 decoder. The D_0 , D_1 , D_2 , D_3 , and D_4 outputs of the MCM6674 decoder output column 5, column 4, column 3, column 2, and column 1 information.

Interfacing the HDSP-2000 Display to Microprocessors

Because of the complexity of dealing with alphanumeric information, a microprocessor based system is typically used in conjunction with the HDSP-2000 family displays. Depending upon overall systems configuration, microprocessor time available to dedicate to display support, and the type of information to be displayed, one may choose several different partitioning schemes to drive such a display.

Figure 3 shows four different techniques to interface the HDSP-2000 family displays to microprocessor systems:

1. The REFRESH CONTROLLER interrupts the microprocessor at a 500 Hz rate to request refresh data for the display.
2. The DECODED DATA CONTROLLER accepts 5×7 matrix data from the microprocessor and then automatically refreshes the display with the

same information until new data is supplied by the microprocessor.

3. The CODED DATA CONTROLLER accepts ASCII data and interfaces like a RAM to the microprocessor.
4. The DISPLAY PROCESSOR CONTROLLER (HDSP-247X series) employs a dedicated single chip microprocessor as a data display/control/keyboard interface which has many of the features of a complete terminal.

The interface techniques depicted are specifically for the 8080A or 6800 microprocessor families. Extension of these techniques to other processors should be a relatively simple software chore with little or no hardware changes required.

The choice of a particular interface is an important consideration because it affects the design of the entire microprocessor system. The REFRESH CONTROLLER provides the lowest cost interface because it uses the microprocessor to provide ASCII decoding and display strobing. Because the ASCII decoder is located within the microprocessor system, the designer has total control over the display font within the program. This feature is particularly important when the system will be used to display different languages and special graphic symbols. However, the REFRESH CONTROLLER requires a significant amount of microprocessor time. Furthermore, while the interrupt allows the refresh program to operate asynchronously from the main program, this technique

limits some of the software techniques that can be used in the main program.

The DECODED DATA CONTROLLER requires microprocessor interaction only when the display message is changed. Like the REFRESH CONTROLLER, the ASCII decoder is located within the microprocessor program. However, the time required to decode the ASCII string and store the resulting 5 x 7 display data into the interface requires several milliseconds of microprocessor time.

The CODED DATA CONTROLLER also requires interaction from the microprocessor system only when the display message is changed. Because the ASCII decoder is located within the display interface, the microprocessor requires much less time to load a new message into the display.

The DISPLAY PROCESSOR CONTROLLER, the HDSP-247X series, is the most powerful interface. The software within the DISPLAY PROCESSOR CONTROLLER further reduces the host

microprocessor interaction by providing more powerful left and right data entry modes compared to the RAM entry mode of the DECODED DATA and CODED DATA CONTROLLERS. The DISPLAY PROCESSOR CONTROLLER can also provide features such as a Blinking Cursor, Editing Commands, and a Data Out function. One version of the DISPLAY PROCESSOR CONTROLLER allows the user to provide a custom ASCII decoder for applications needing a special character font.

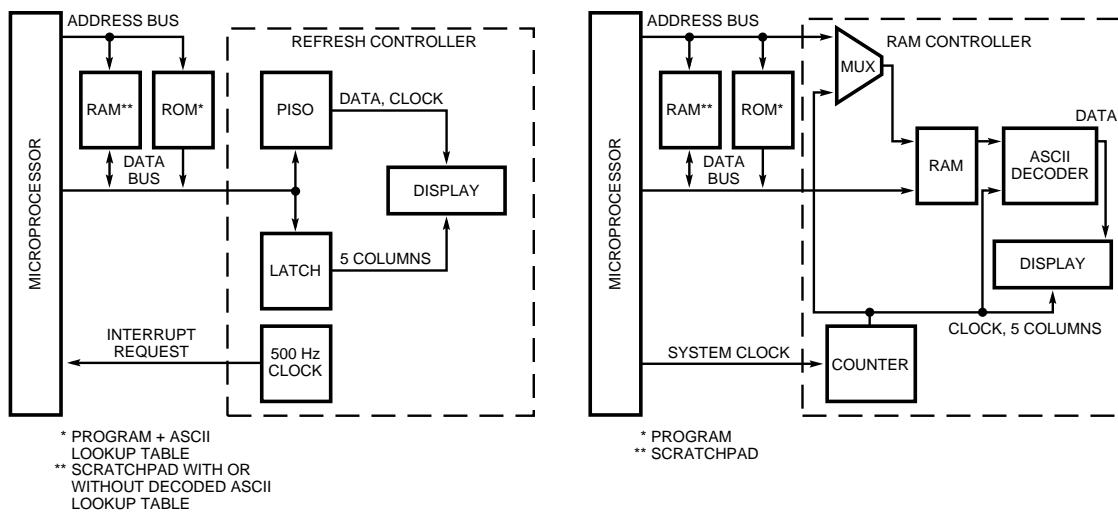


Figure 3. Four Different Techniques to Interface the HDSP-2000 Alphanumeric Display to a Microprocessor System

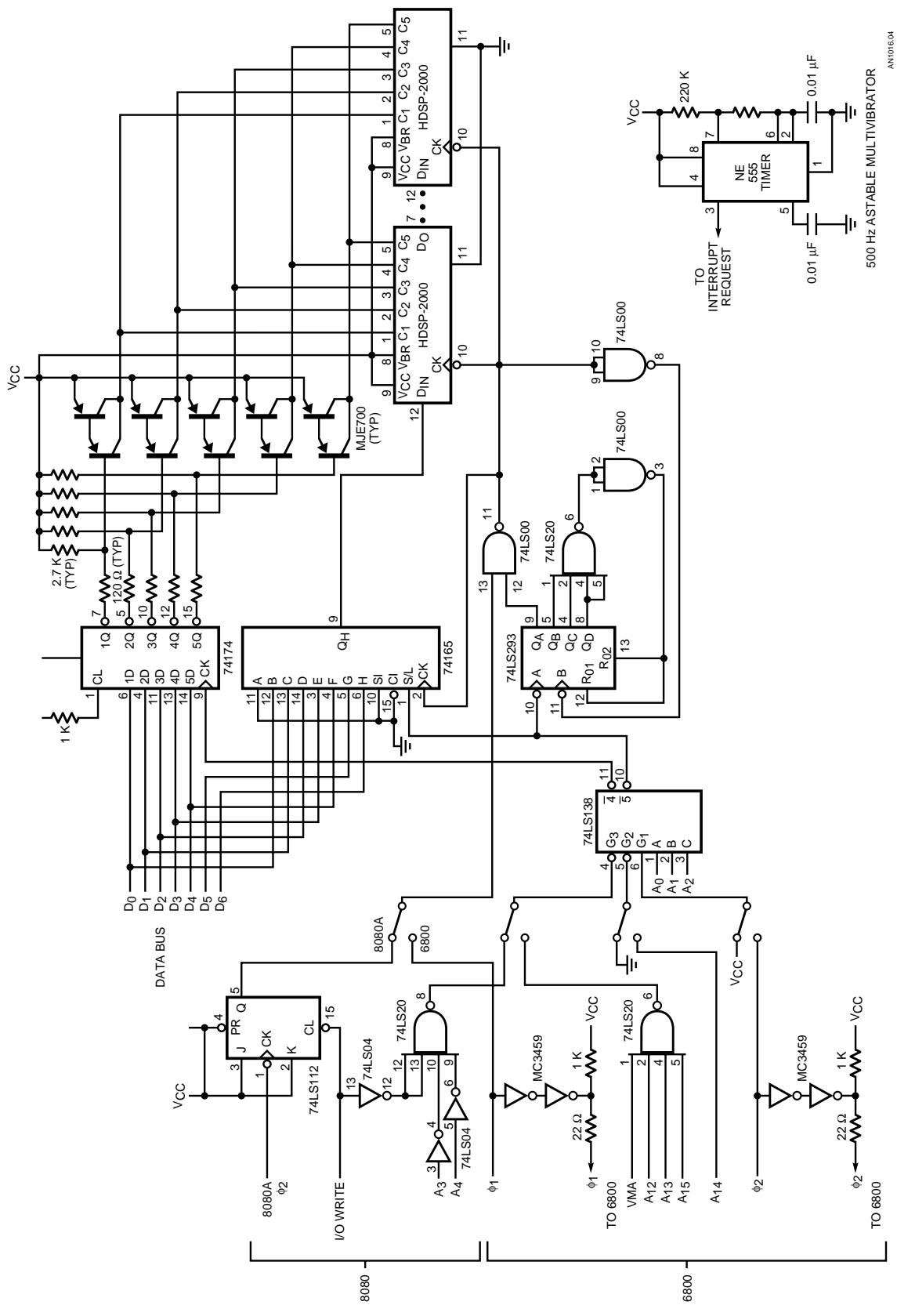


Figure 4. 6800 or 8080A Microprocessor Interface to the HDSP-2000 REFRESH CONTROLLER

Refresh Controller

The REFRESH CONTROLLER circuit depicted in Figure 4 operates by interrupting the microprocessor every two milliseconds to request a new block of display data and column select data. Display data is loaded from the data bus into the serial input of the HDSP-2000 via a 74165 parallel in, serial out shift register. The 74LS293 counter and associated gates insure that only seven clock pulses are delivered to the shift register and the HDSP-2000 for each word loaded. Column Select data is loaded into a 74174 latch which, in turn, drives the column switch transistors. The circuit timing relative to the microprocessor clock and I/O is depicted in Figure 5.

The 6800 software necessary to support this interface is divided

into two separate subroutines, "RFRSH" and "LOAD" (Figure 6). This approach is desirable to minimize microprocessor involvement during display refresh. The subroutine "RFRSH" loads a new set of decoded display data from the microprocessor scratchpad memory into the interface at each interrupt request. The subroutine "LOAD" is utilized to decode a string of 32 ASCII characters into 5×7 formatted display data and store this data in the scratchpad memory used by "RFRSH".

Figures 7 and 8 depict two different software routines for interfacing the REFRESH CONTROLLER to an 8080A microprocessor. The two subroutines shown in Figure 7 are functional replacements for the 6800 program shown in Figure 6. The programs shown in Figures 6

and 7 require a $5N$ byte scratchpad memory where N is the display length. The routine in Figure 8 eliminates this scratchpad memory by decoding and loading data each time a new interrupt request is received.

Because the microprocessor system is interrupted every 2 ms, proper software design is especially important for the REFRESH CONTROLLER. The use of the scratchpad memory significantly reduces the time required to refresh the display. The fastest program, shown in Figure 6, uses in-line code to access data from the buffer and output it to the display. This program requires $3.7\% + .50\%$ of the available microprocessor time for a 1 MHz clock. The program shown in Figure 7 is similar to the one shown in Figure 6, except that it uses a program

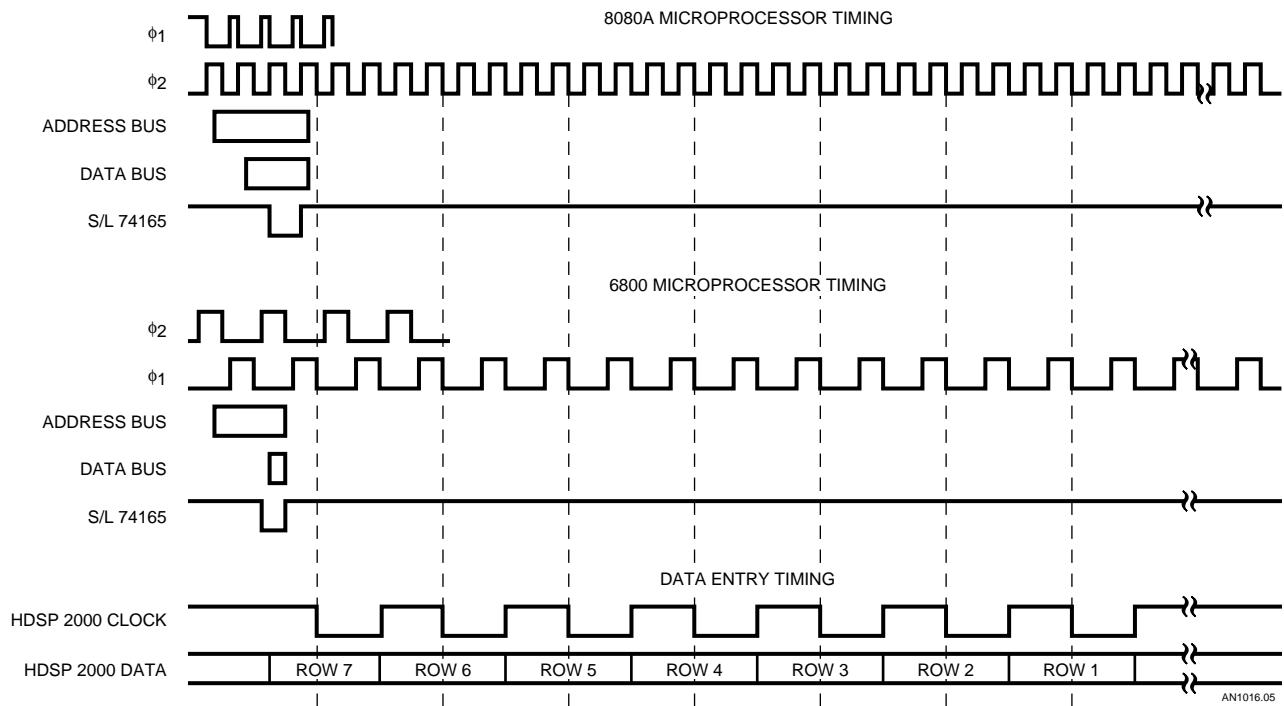


Figure 5. REFRESH CONTROLLER Timing

loop instead of the in-line code. This program uses 5.4% + .93N% of the microprocessor time for a 2 MHz clock. These programs utilize a subroutine "LOAD" which is called whenever the display message is changed. This subroutine executes in 10.2 ms and 7.5 ms respectively for Figure 6 and Figure 7. The program in Figure 8 uses 7.6% + 1.35N% of the microprocessor time for a 2 MHz clock. A 50% reduction in the previously described microprocessor times can be achieved by using faster versions of the 6800 and 8080A microprocessors.

The ASCII to 5 x 7 dot matrix decoder used by the programs in Figures 6, 7, and 8 is located within the microprocessor program. This decoder requires 640 bytes of storage to decode the 128 character ASCII set. The decoder used by these controllers is formatted so that the first 128 bytes contain column 1 information; the next 128 bytes contain column 2 information, etc. Each byte of this decoder is formatted such that D_6 through D_0 contain Row 7 through Row 1 display data respectively. The data is coded so that a HIGH bit will turn the corresponding 5 x 7 display dot ON. This decoder table is shown in Figure 9. The resulting 5 x 7 dot matrix display font is shown in the HDSP-2471 data sheet.

Decoded Data Controller
The DECODED DATA CONTROLLER circuit schematic for a 32 character display is depicted in Figure 10. The circuit is specifically designed for interface to an 8080A microprocessor. This circuit is designed to accept and store in local memory all of the display data for a 32 character HDSP-2000 display (1120 bits).

The microprocessor loads 160 bytes of display data into the two 1 K x 1 RAM's via the 74165 parallel in, serial out shift register. Each byte of data represents one column of display data. The counter string automatically generates the proper address location for each serial bit of data after initialization by MEM W, the character address, and the desired column. Once the loading is complete, the counter sequentially loads and displays each column (224 bits) of data at a 90 Hz rate (2 MHz input clock rate). The timing for this circuit is shown in Figure 11. The software required to decode a 32 character ASCII string is shown in Figure 12. This program decodes the 32 ASCII characters into 160 bytes of display data which are then stored in the controller. The program requires about 6.6 ms, for a 2 MHz clock, to decode and load the message into the DECODED DATA CONTROLLER. This program also uses the same decoder table as shown in Figure 9.

Coded Data Controller

The CODED DATA CONTROLLER (Figure 13) is designed to accept ASCII coded data for storage in a local 128 x 8 RAM. After the microprocessor has loaded the RAM, local scanning circuitry controls the decoding of the ASCII, the display data loading, and the column select function. With minor modification, the circuit can be utilized for up to 128 display characters. The RAM used in this circuit is an MCM6810P with the Address and Data inputs isolated via 74LS367 tri-state buffers. This allows the RAM to be accessed either by the microprocessor or by the local electronics. The protocol is arranged such that the microprocessor always takes

precedence over the local scanning electronics. The "Write" cycle timing for the CODED DATA CONTROLLER is depicted in Figure 14. This circuit, as with the DECODED DATA CONTROLLER, requires no microprocessor time once the local RAM has been loaded with the desired data.

The circuit shown in Figure 13 shows a CODED DATA CONTROLLER designed for a 32 character HDSP-2000 alphanumeric display. The key waveforms shown in Figure 15, labeled ①, ②, and ③, are shown to simplify the analysis of this circuit. Label ① is the 1 MHz clock. Label ② is the output of 7404 pin 2 which is the inverted Q_D output of the 74197. Label ③ is the output of the 7404 pin 6 which is the ANDed output of $2Q_B$, $2Q_C$, and $2Q_D$ of the 74393. The Motorola 6810 RAM stores 32 bytes of ASCII data which is continuously read, decoded, and displayed. The ASCII data from the RAM is decoded by the Motorola 6674 128 character ASCII decoder. The 6674 decoder has five column outputs which are gated to the Data Input of the display via a 74151 multiplexer. Strobing of the display is accomplished via the 74197, 74393, and 7490 counter string. The 74197 is connected as a divide by 8 counter that sequentially selects the seven rows within the 6674. As shown by waveform ②, the 74197 also enables seven clock cycles to be gated to the clock input of the display. The 74393 is a divide by 256 counter connected so that the five lowest order outputs select each of the 32 ASCII characters within the RAM. The three highest order outputs determine the relationship between load time and column on time. When $2Q_B = 2Q_C = 2Q_D = 1$ of the

74393, waveform ③ goes to a logical 1. The circuit then scans 32 characters from the RAM and serializes the column data by counting through each of the seven rows of the 6674 and gating the appropriate column of the display. During the seven counts when $2Q_B$, $2Q_C$, and $2Q_D$ of the 74393 are not equal to a logical 1, the column data is displayed, as shown in waveform ④). The duty factor of the display shown in Figure 13 is 17.5%.

Changing the display length to 64 characters is a simple modification. This configuration can be easily realized by disconnecting $2Q_B$ of the 74393 from the 7410 and connecting it through the remaining tri-state buffer on the 74LS367 and using the 6810 RAM to store 64 ASCII characters. By leaving only $2Q_C$ and $2Q_D$ attached to the 7410, the column on time of the display is reduced from 17.5% to 15%. This reduction is caused because the relationship between actual column on time and theoretical column on time is $3/4$ as opposed to $7/8$ for the 32 characters. Since the display length has been doubled, the drive transistors must be upgraded to handle the higher column currents.

To implement a 128 character display, several modifications are needed. These changes are incorporated into the circuit in Figure 16. First, the input clock frequency has been increased to 2 MHz. This has been done to maintain a refresh rate of approximately 100 Hz for each digit, thus providing a flicker-free display. This higher speed of operation causes propagation delay problems within the MCM6674 (NMOS) whose maximum access time is 350 ns. For this reason, the

LOC	OBJECT CODE	SOURCE STATEMENTS		
		*		
		*		
		BF 05 CDVR EQU \$BF05		
		BL 04 RDVR EQU \$BF04		
		06 00 DECDR EQU \$0600		
0000		POINT RMB 2		
0002		COLMN RMB 1		
0003		COUNT RMB 2		
0005	00 AD	ASCII FDB DATA		
0007		DISPNT RMB 2		
0009		DCRPNT RMB 2		
000B		COLCNT RMB 1		
000C		DIGCNT RMB 1		
000D		BUFFR RMB 160		
00AD		DATA RMB 32		
0400		ORG \$0400		
0400	86 FF	RFRSH LDA A I, SF		
0402	B7 BF 05	STA A E, CDVR		
0405	DE 00	LDX D, POINT		
0407	A6 00	LOOPHH LDA A X, 0		
0409	B7 BF 04	STA A E, RDVR		
040C	A6 01	LDA A X, I		
040E	B7 BF 04	STA A E, RDVR		
		•		
		•		
04A2	A6 1F	LDA A X, 31		
04A4	B7 BF 04	STA A E, RDVR		
04A7	96 02	LDA A D, COLMN		
04A9	B7 BF 05	STA A E, CDVR		
04AC	81 EF	CMP A I, SEF		
04AE	27 10	BEQ LOOPB		
04B0	D6 00	LDA B D, POINT +1		
04B2	CB 20	ADD B I, 32		
04B4	D7 00	STA B D, POINT +1		
04B6	24 03	BCC LOOPA		
04B8	7C 00 00	INC E, POINT		
04BB	OD 00	LOOPA SEC		
04BC	79 00 02	ROL E, COLMN		
04BF	3B	RTI		
04C0	CE 00 OD	LOOPB LDX I, BUFFER		
04C3	DF 00	STX D, POINT		
04C5	DE 03	LDX D, COUNT		
04C7	09	DEX		
04C8	DF 03	STX D, COUNT		
04CA	86 FE	LDA A I, SF		
04CC	97 02	STA A D, COLMN		
04CE	3B	RTI		
04CF	5F	LOAD CLR B		
04D0	CE 00 OD	LDX I, BUFFER		
04D3	DF 07	STX D, DISPNT		
04D5	86 06	LDA A I, <DECDR		
04D7	97 09	STA A D, DCRPNT		
04D9	86 05	LDA A I, 5		
04DB	97 0B	STA A D, COLCNT		
04DD	86 20	LOOP I LDA A I, 32		
04DF	97 0C	STA A D, DIGCNT		
04E1	9B 06	ADD A D, ASCII+1		
04E3	24 03	BCC LOOP2		
04E5	7C 00 05	INC E, ASCII		
04E8	97 06	LOOP2 STA A D, ASCII+1		
04EA	DE 05	LOOP3 LDX D, ASCII		
04EC	09	DEX		
04ED	A6 00	LDA A X, 0		
04EF	DF 05	STX D, ASCII		
04F1	1B	ABA		
04F2	97 0A	STA A D, DCRPNT+1		
04F4	DE 09	LDX D, DCRPNT		
04F6	A6 00	LDA A X, 0		
04F8	DE 07	LDX D, DISPNT		
04FA	A7 00	STA A X, 0		
04FC	08	INX		
04FD	DF 07	STX D, DISPNT		
04FF	7A 00 0C	DEC E, DIGCNT		
0502	26 E6	BNE LOOP3		
0504	CB 80	ADD B I, S80		
0506	24 03	BCC LOOP4		
0508	7C 00 09	INC E, DCRPNT		
050B	7A 00 0B	DEC E, COLCNT		
050E	26 CD	BNE LOOP1		
0510	39	RTS		

Figure 6. 6800 Microprocessor Program Utilizing a 160 Byte RAM Buffer that Interfaces to the REFRESH CONTROLLER

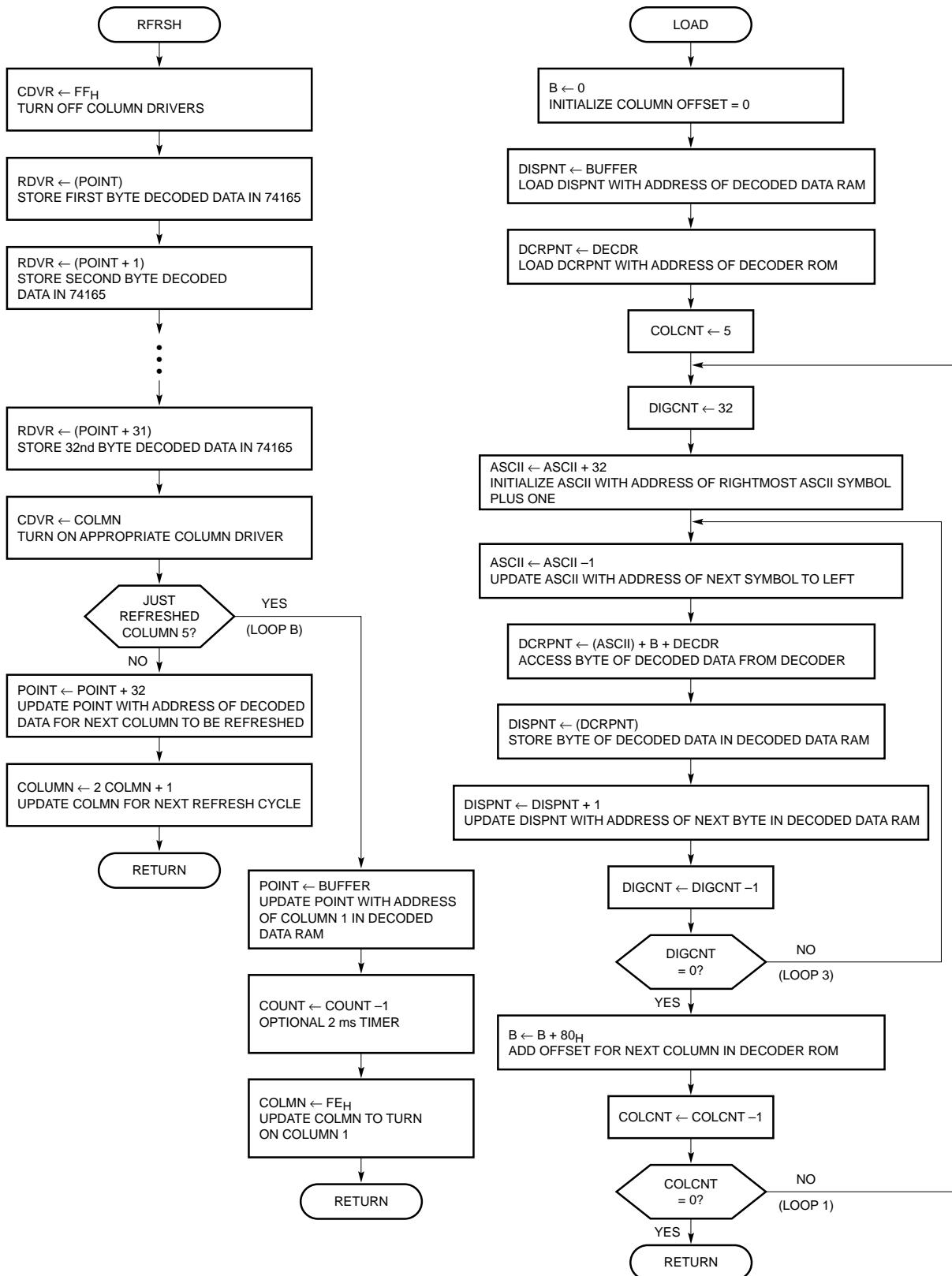


Figure 6. 6800 Microprocessor Program Utilizing a 160 Byte RAM Buffer that Interfaces to the REFRESH CONTROLLER (cont.)

MCM6674 must be replaced by a faster Bipolar PROM. If this PROM is programmed with the code listed in Figure 17, it will decode a character font identical to the MCM6674. This same propagation delay problem is present with the MCM6810 RAM. Following worst case design procedures, the MCM68A10 1.5 MHz RAM should be used. To accommodate the additional address line made necessary by the display length expansion, the two 74LS367 tri-state buffers have been replaced with the 74LS244 octal version. Strobing of the display is accomplished using the 74197, 74393, and 7490 counter string. The 74197 is connected as a divide by 8 counter that sequentially selects the seven rows within the 82S2708. The 74393 is a divide by 256 counter connected so that the seven lowest outputs select each of the 128 ASCII characters within the RAM. The previously unused input A/output QA of the 7490 has been used as an additional divide by 2 counter. Thus, when the highest output of the 74393, 2QD, and the QA output of the 7490 are NANDed through 7437, the basic relationship between load time and column on time is established. However, the external gating that has been added does affect the duty factor slightly. Although these additional gates increase the total package count by one, they perform the necessary function of ensuring that the column drivers are turned off before the clock is gated to the display. This prevents noise from being generated on the clock of the display and eliminates erroneous display data. The resultant duty factor is (23/32) (1/5) or 14.4%. Since the HDSP-2000 is rated at $I_{col(max)} = 410$ mA and

LOC	OBJECT CODE		SOURCE STATEMENTS			
0004			RDVR	EQU	0004H	
0005			CDVR	EQU	0005H	
E500			DECDR	EQU	0E500H	
				ORG	0E000H	
E000	05	E0	POINT	DW	BUFFR	
E002	FE		COLMN	DB	0FEH	
E003	FF	FF	COUNT	DW	0FFFFH	
E005	00		BUFFR	DS	160	
				ORG	0E0A5H	
E0A5	A7	E0	ASCII	DW	DATA	
E0A7	00		DATA	DS	32	
				RFRSH	ORG	0E400H
E400	F5			PUSH	PSW	
E401	C5			PUSH	B	
E402	E5			PUSH	H	
E403	2A	00	E0	LHLD	POINT	
E406	06	20		MVI	B, 32	
E408	3E	FF		MVI	A, 0FFH	
E40A	D3	05		OUT	CDVR	
E40C	7E			MOV	A, M	
E40D	D3	04		OUT	RDVR	
E40F	23			INX	H	
E410	05			DCR	B	
E411	C2	0C	E4	JNZ	LOOP	
E414	3A	02	E0	LDA	COLMN	
E417	D3	05		OUT	CDVR	
E419	FE	EF		CPI	0EFH	
E41B	CA	28	E4	JZ	FIRST	
E41E	22	00	E0	SHLD	POINT	
E421	07			RLC		
E422	32	02	E0	STA	COLMN	
E425	C3	3A	E4	JMP	END	
E428	21	05	E0	FIRST	LXI	H, BUFFR
E42B	22	00	E0		SHLD	POINT
E42E	3E	FE			MVI	A, 0FEH
E430	32	02	E0		STA	COLMN
E433	2A	03	E0		LHLD	COUNT
E436	2B				DCX	H
E437	22	03	E0		SHLD	COUNT
E43A	E1			END	POP	H
E43B	C1				POP	B
E43C	F1				POP	PSW
E43D	C9				RET	
E43E	11	24	E0	LOAD	LXI	D, BUFFR+31
E441	0E	20			MVI	C, 32
E443	2A	A5	E0	LOOP1	LHLD	ASCII
E446	7E				MOV	A, M
E447	23				INX	H
E448	22	A5	E0		SHLD	ASCII
E44B	26	E5			MVI	H, DECDR/256
E44D	6F				MOV	L, A
E44E	06	05			MVI	B, 5
E450	7E			LOOP2	MOV	A, M
E451	12				STAX	D
E452	7D				MOV	A, L
E453	C6	80			ADI	80H
E455	6F				MOV	L, A
E456	D2	5A	E4		JNC	LOOP3
E459	24				INR	H
E45A	7B			LOOP3	MOV	A, E
E45B	C6	20			ADI	32
E45D	5F				MOV	E, A
E45E	05				DCR	B
E45F	C2	50	E4		JNZ	LOOP2
E462	7B				MOV	A, E
E463	C6	5F			ADI	5FH
E465	5F				MOV	E, A
E466	0D				DCR	C
E467	C2	43	E4		JNZ	LOOP1
E46A	C9				RET	

Figure 7. 8080A Microprocessor Program Utilizing a 160 Byte RAM Buffer that Interfaces to the REFRESH CONTROLLER

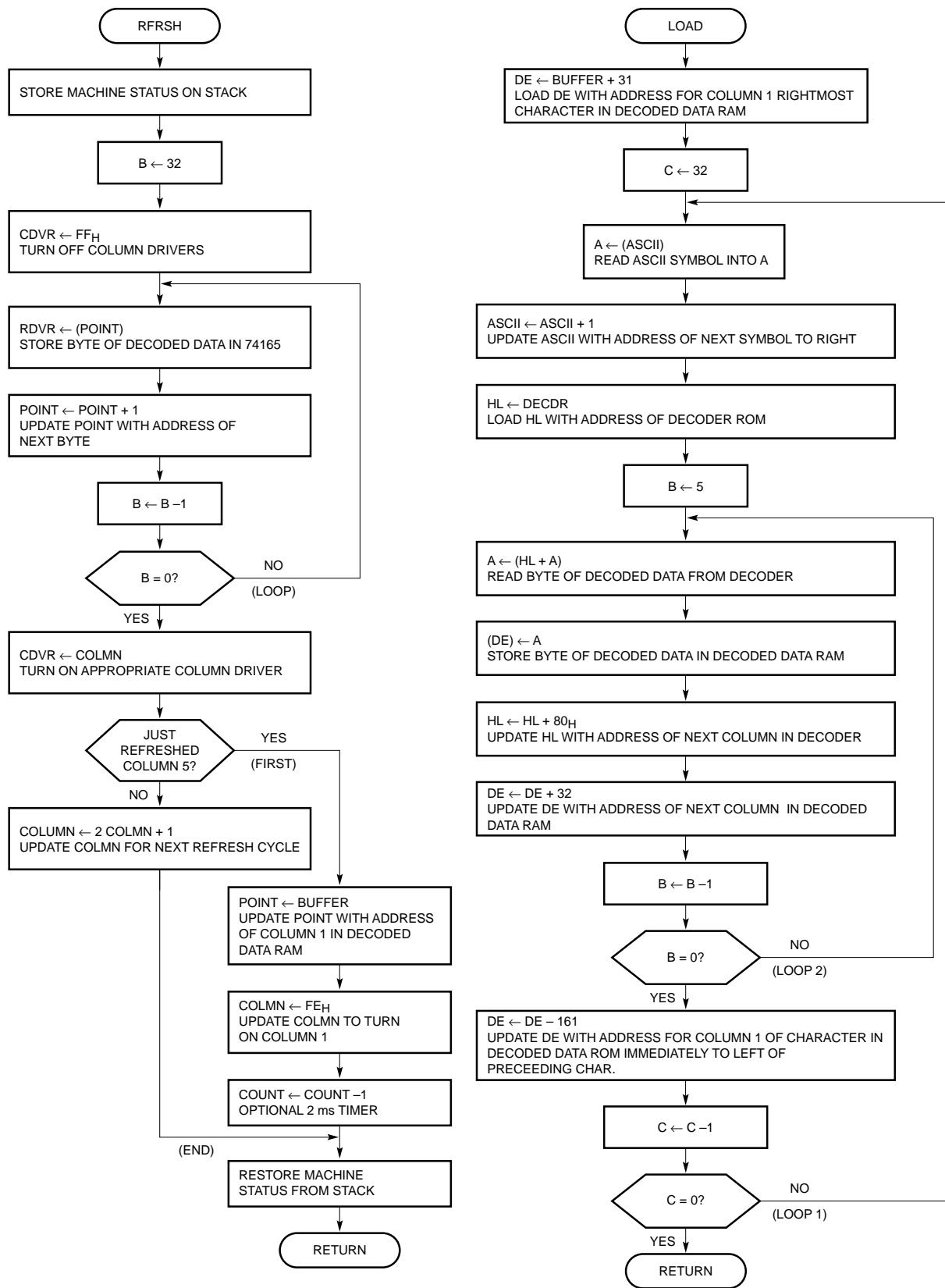


Figure 7. 8080A Microprocessor Program Utilizing a 160 Byte RAM Buffer that Interfaces to the REFRESH CONTROLLER (cont.)

LOC	OBJECT CODE		SOURCE STATEMENTS
0004			RDVR EQU 0004H
0005			CDVR EQU 0005H
E500			DECDR EQU 0E500H
E000	07 E0		ORG 0E000H
E002	FE		COLMN DB 0FEH
E003	FF FF		COUNT DW 0FFFFH
E005	00 E5		BASE DW DECDR
E007	00		DATA DS 32
E400	F5	RFRSH	ORG 0E400H
E401	C5		PUSH PSW
E402	D5		PUSH B
E403	E5		PUSH D
E404	2A 05 E0		PUSH H
E407	EB		LHLD BASE
E408	2A 00 E0		XCHG
E40B	01 1F 00		COLMN DB B, 31
E40E	09		DAD B
E40F	43		MOV B, E
E410	0E 20		MVI C, 32
E412	3E FF		MVI A, 0FFH
E414	D3 05	LOOP	OUT CDVR
E416	78		MOV A, B
E417	86		ADD M
E418	5F		MOV E, A
E419	1A		LDA D
E41A	D3 04		OUT RDVR
E41C	2B		DCX H
E41D	0D		DCR C
E41E	C2 16 E4		JNZ LOOP
E421	EB		XCHG
E422	3A 02 E0		LDA COLMN
E425	D3 05		OUT CDVR
E427	FE EF		CPI 0FEH
E429	CA 3B E4	FIRST	JZ FIRST
E42C	07		RLC
E42D	32 02 E0		STA COLMN
E430	68		MOV L, B
E431	01 80 00		LXI B, 0080H
E434	09		DAD B
E435	22 05 E0		SHLD BASE
E438	C3 4D E4		JMP END
E43B	3E FE		MVI A, 0FEH
E43D	32 02 E0		STA COLMN
E440	21 00 E5		LXI H, DECDR
E443	22 05 E0		SHLD BASE
E446	2A 03 E0		LHLD COUNT
E449	2B		DCX H
E44A	22 03 E0		SHLD COUNT
E44D	E1	END	POP H
E44E	D1		POP D
E44F	C1		POP B
E450	F1		POP PSW
E451	C9		RET

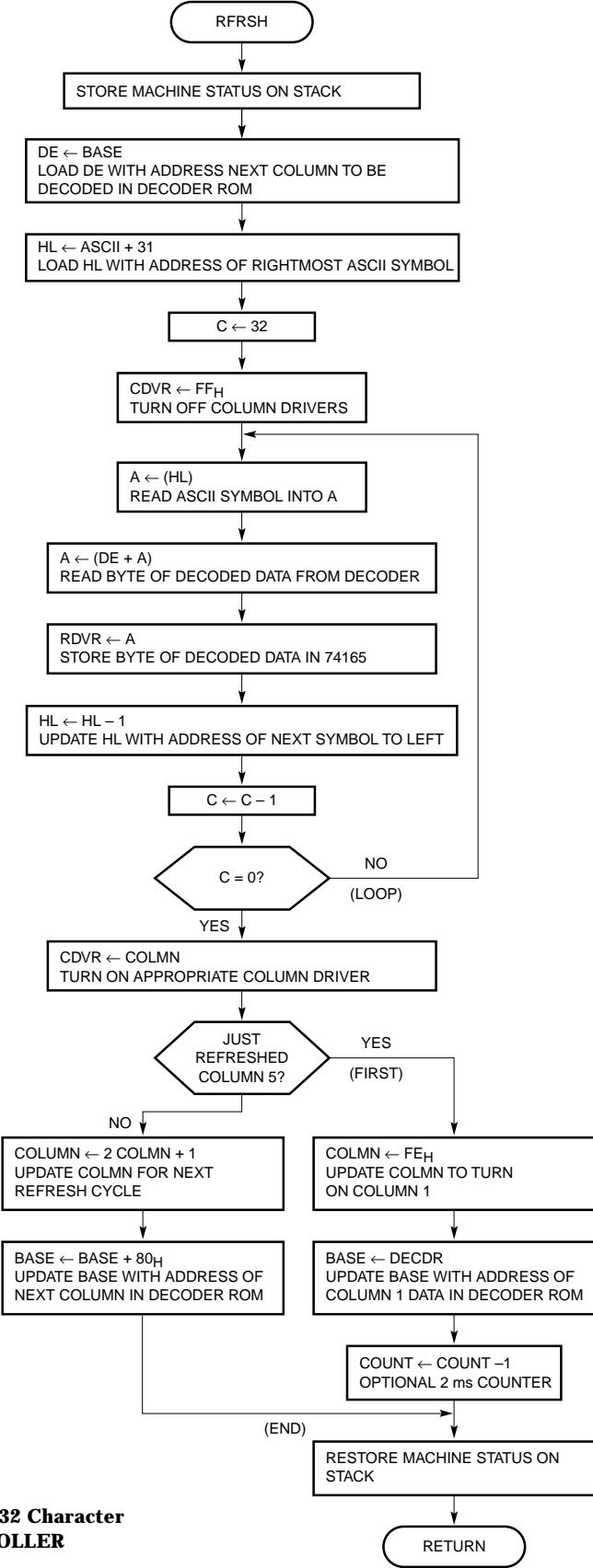


Figure 8. 8080A Microprocessor Program that Decodes a 32 Character ASCII String Prior to Loading into the REFRESH CONTROLLER

there are 32 modules of four digits each, the transistors must source up to 32 times 410 mA or approximately 13 A. Darlington PNP power transistors (2N6285) with the proper resistors have been used to accomplish this task.

Display Processor Controller

The previously mentioned interface techniques provide only for the display of ASCII coded data. Such important features as a blinking cursor, editing routines, and character addressing must be provided by other subroutines in

the microprocessor software. The DISPLAY PROCESSOR CONTROLLER is a system which utilizes a dedicated 8048 single chip microprocessor to provide these important features. This controller, as depicted in Figure 18, is a series of printed circuit board subsystems available from

DECODER ADDRESS FOR FIG. 7,8,12	DECODER ADDRESS FOR FIG. 6	HDSP-2471 ROM ADDRESS	HEXIDECLIMAL DATA																			
			08	30	45	7D	7D	38	7E	30	60	1E	3E	62	40	08	38	41	COLUMN ₁			
E500	0600	080	08	30	45	7D	7D	38	7E	30	60	1E	3E	62	40	08	38	41	COLUMN ₁			
		090	10	18	5E	78	38	78	38	3C	38	3C	38	08	20	12	48	01				
		0A0	00	00	00	14	24	23	36	00	00	00	08	08	00	08	00	20				
		0B0	3E	00	62	22	18	27	3C	01	36	06	00	00	00	14	41	06				
		0C0	3E	7E	7F	3E	7F	7F	7F	3E	7F	00	20	7F	7F	7F	7F	3E				
		0D0	7F	3E	7F	26	01	3F	07	7F	63	03	61	00	02	41	04	40				
		0E0	00	38	7F	38	38	38	08	08	7F	00	20	00	00	78	7C	38				
		0F0	7C	18	00	48	04	3C	1C	3C	44	04	44	00	00	00	08	2A				
E580	0680	100	1C	48	29	09	09	44	01	4A	50	04	49	14	3C	7C	44	63	COLUMN ₂			
		110	08	24	61	14	44	15	45	49	45	41	42	08	7E	19	7E	12				
		120	00	5F	03	7F	2A	13	49	0B	00	41	2A	08	58	08	30	10				
		130	51	42	51	41	14	45	4A	71	49	49	36	5B	08	14	22	01				
		140	41	09	49	41	41	49	09	41	08	41	40	08	40	02	04	41				
		150	09	41	09	49	01	40	18	20	14	04	51	00	04	41	02	40				
		160	07	44	48	44	44	54	7E	14	08	44	40	7F	41	04	08	44				
		170	14	24	7C	54	3E	40	20	40	28	48	64	08	00	41	04	55				
E600	0700	180	3E	45	11	11	05	44	29	4D	48	04	49	08	20	04	44	55	COLUMN ₃			
		190	78	7E	01	15	45	14	44	42	44	40	40	2A	02	15	49	7C				
		IA0	00	00	00	14	7F	08	56	07	3E	3E	1C	3E	38	08	30	08				
		IB0	49	7F	49	49	12	45	49	09	49	49	36	3B	14	14	14	51				
		IC0	5D	09	49	41	41	49	09	41	08	7F	40	14	40	0C	08	41				
		ID0	09	51	19	49	7F	40	60	18	08	78	49	7F	08	7F	7F	40				
		IE0	0B	44	44	44	44	54	09	54	04	7D	44	10	7F	18	04	44				
		IF0	24	14	08	54	44	40	40	30	10	30	54	36	77	36	08	2A				
E680	0780	200	7F	40	29	21	05	38	2E	49	50	38	49	10	20	7C	3C	49	COLUMN ₄			
		210	08	24	61	14	3C	15	3D	43	45	41	42	1C	02	12	41	12				
		220	00	00	03	7F	2A	64	20	00	41	00	2A	08	00	08	00	04				
		230	45	40	49	49	7F	45	49	05	49	29	00	00	22	14	08	09				
		240	55	09	49	41	41	49	09	51	08	41	40	22	40	02	10	41				
		250	09	21	29	49	01	40	18	20	14	04	45	41	10	00	02	40				
		260	00	3C	44	44	48	54	02	54	04	40	3D	28	40	04	04	44				
		270	24	7C	04	54	20	20	20	40	28	08	4C	41	00	08	10	55				
E700	0800	280	00	30	45	7D	79	44	10	30	60	40	3E	60	1C	02	04	41	COLUMN ₅			
		290	04	18	5E	78	40	78	40	3C	38	3C	38	08	02	00	42	01				
		2A0	00	00	00	14	12	62	50	00	00	00	08	08	00	08	00	02				
		2B0	3E	00	46	36	10	39	30	03	36	1E	00	00	41	14	00	06				
		2C0	1E	7E	36	22	3E	41	01	72	7F	00	3F	41	40	7F	7F	3E				
		2D0	06	5E	46	32	01	3F	07	7F	63	03	43	41	20	00	04	40				
		2E0	00	40	38	20	7F	08	00	3C	78	00	00	44	00	78	78	38				
		2F0	18	40	04	20	00	7C	1C	3C	44	04	44	00	00	00	08	2A				

Figure 9. 128 Character ASCII Decoder Table Used by the 6800 Refresh Program in Figure 6. 8080A Refresh Programs in Figures 7, 8, and 12, and the HDSP-2471 DISPLAY PROCESSOR CONTROLLER. Decoded 5x7 Display Font is shown in the HDSP-247X Data Sheet

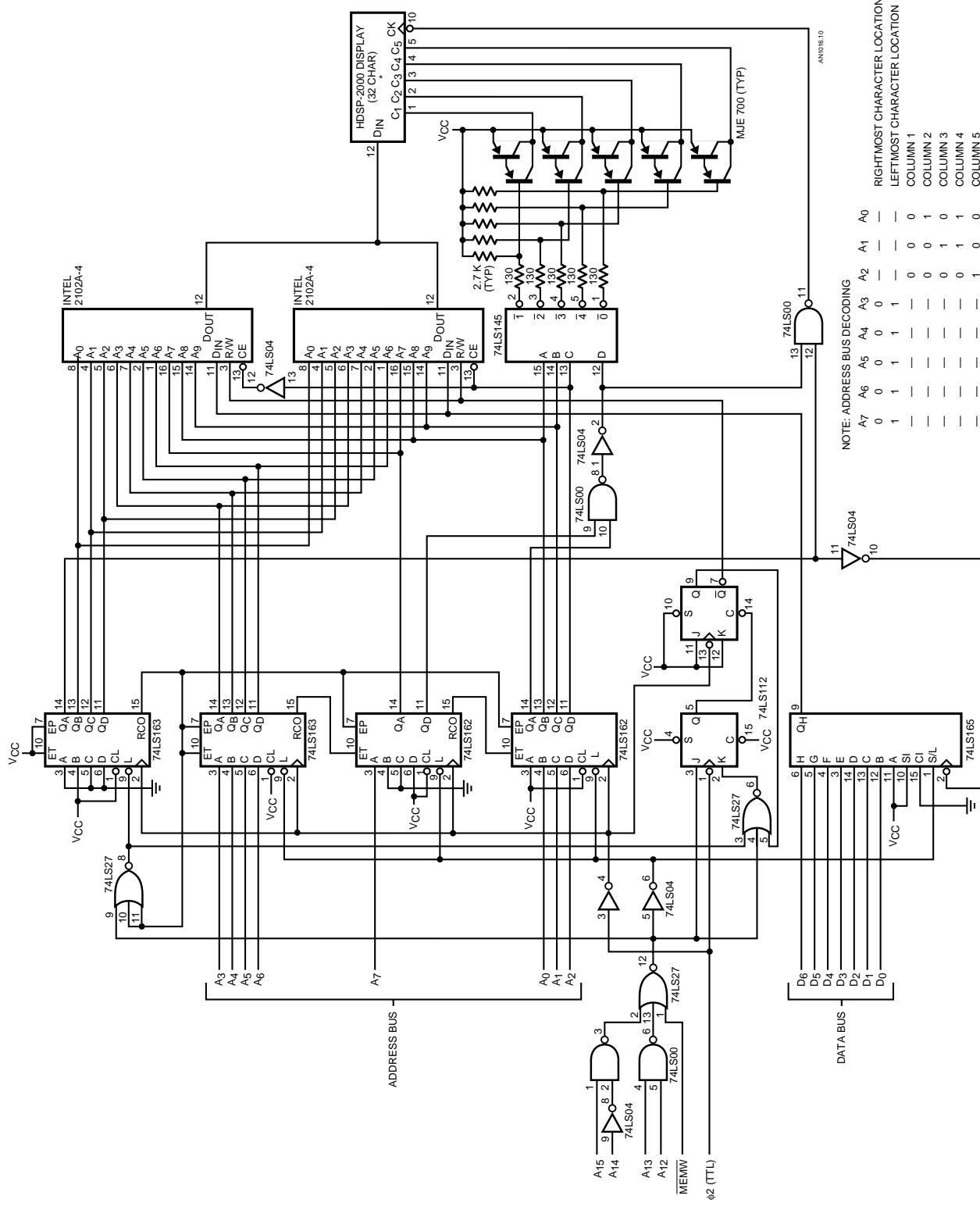


Figure 10. 8080A Microprocessor Interface to the HDSP-2000 DECODED DATA CONTROLLER

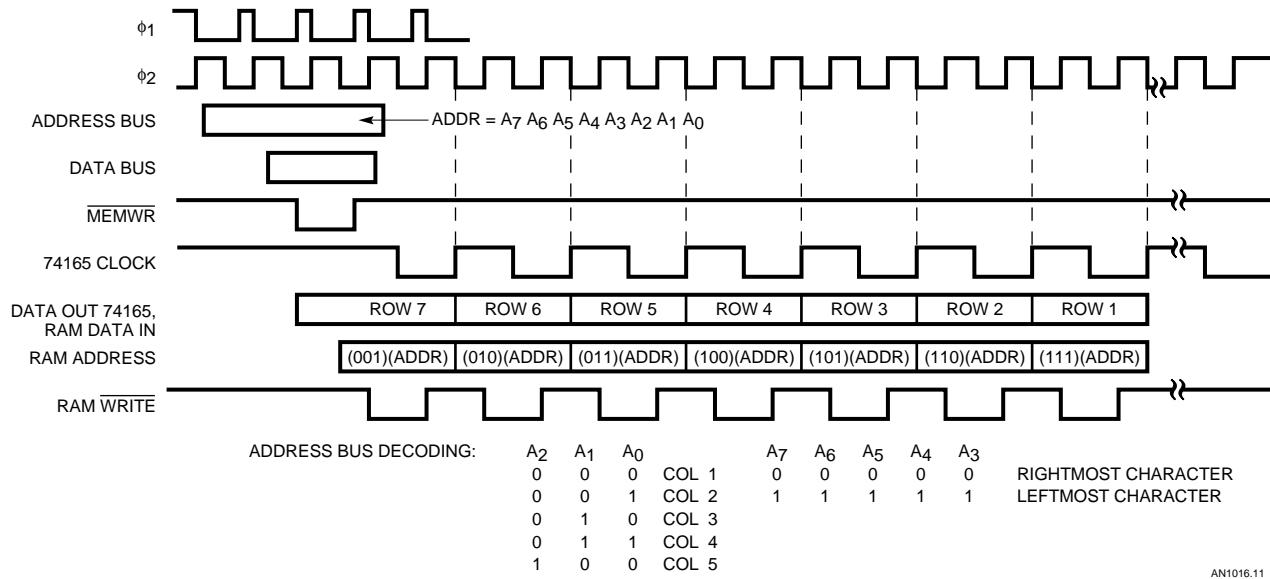


Figure 11. Data Entry Timing for DECODED DATA CONTROLLER

Agilent Technologies under the following part numbers:

HDSP-2470 – Controller with 64 character ASCII to 5 x 7 decoder

HDSP-2471 – Controller with 128 character universal ASCII to 5 x 7 decoder

HDSP-2472 – Controller with socket for user supplied custom coded ROM/PROM/EPROM.

All of the controllers have the following features:

- Choice of character string length: 4 to 48 characters in increments of four characters
- Four modes of data entry
 - Left Entry
 - Right Entry
 - RAM Entry (\leq 32 characters only)
 - Block Entry

- Flashing Cursor – Left Entry Only
- Data Out (\leq 32 characters only)
- Edit Functions

Clear	RIGHT ENTRY
Display	
Backspace	
Cursor	
Forward Cursor	
Insert	
- Delete

These controllers have been designed to eliminate the burden of data handling between keyboard, display, and microprocessor. The product data sheet describes the technical function of the controllers in detail.

Interfacing the controller to microprocessor systems depends on the needs of the particular application. Figure 19 depicts a latched interface from a master microprocessor to the HDSP-247X series of controllers. These interfaces are utilized to avoid having the master processor wait for the controller to accept data.

In sophisticated systems, it may be desirable to have the HDSP-247X controller handle all of the keyboard/display interface while the microprocessor reads edited messages from the controller DATA OUT port. This function can be achieved through the use of peripheral interface adapters (PIA) available from the microprocessor manufacturers. Figure 20 depicts a 6800 based system in which data may enter the display from either a keyboard or a microprocessor. This interface uses a 6821 PIA configured so that PB₇ controls whether the microprocessor or keyboard enters data into the controller. The 6800 program is shown in Figure 21. Subroutine "LOAD" uses CA₁ and CA₂ to provide a data entry handshake that allows the 6800 to load data into the controller as fast as the controller can accept it. After the prompting message has been loaded, the microprocessor turns the control of data entry over to the keyboard. A signal from the keyboard ("ER" in the example) sets a flag within the 6821. Depending on how the 6821 is configured, the microprocessor

AN1016.11

LOC	OBJECT CODE		SOURCE STATEMENTS		
B000				DISPL	EQU 0B000H
E500				DECDDR	EQU 0E500H
			ORG 0E000H		
E000 02	E0	00	ASCII DATA	DW DATA	
E002			DS 32		
			ORG 0E400H		
E400 11	F8	B0	LOAD LXI D, DISPL+00F8H		
E403 0E	20		MVI C, 32		
E405 2A	00	E0	LOOP1 LHLD ASCII		
E408 7E			MOV A, M		
E409 23			INX H		
E40A 22	00	E0	SHLD ASCII		
E40D 26	E5		MVI H, DECDDR/256		
E40F 6F			MOV L, A		
E410 06	05		MVI B, 5		
E412 7E		LOOP2	MOV A, M		
E413 12			STAX D		
E414 13			INX D		
E415 7D			MOV A, L		
E416 C6	80		ADI 80H		
E418 6F			MOV L, A		
E419 D2	1D	E4	JNC L00P3		
E41C 24			INR H		
E41D 05		L00P3	DCR B		
E41E C2	12	E4	JNZ L00P2		
E421 7B			MOV A, E		
E422 D6	0D		SUI 13		
E424 5F			MOV E, A		
E425 0D			DCR C		
E426 C2	05	E4	JNZ LOOP1		
E429 C9			RET		

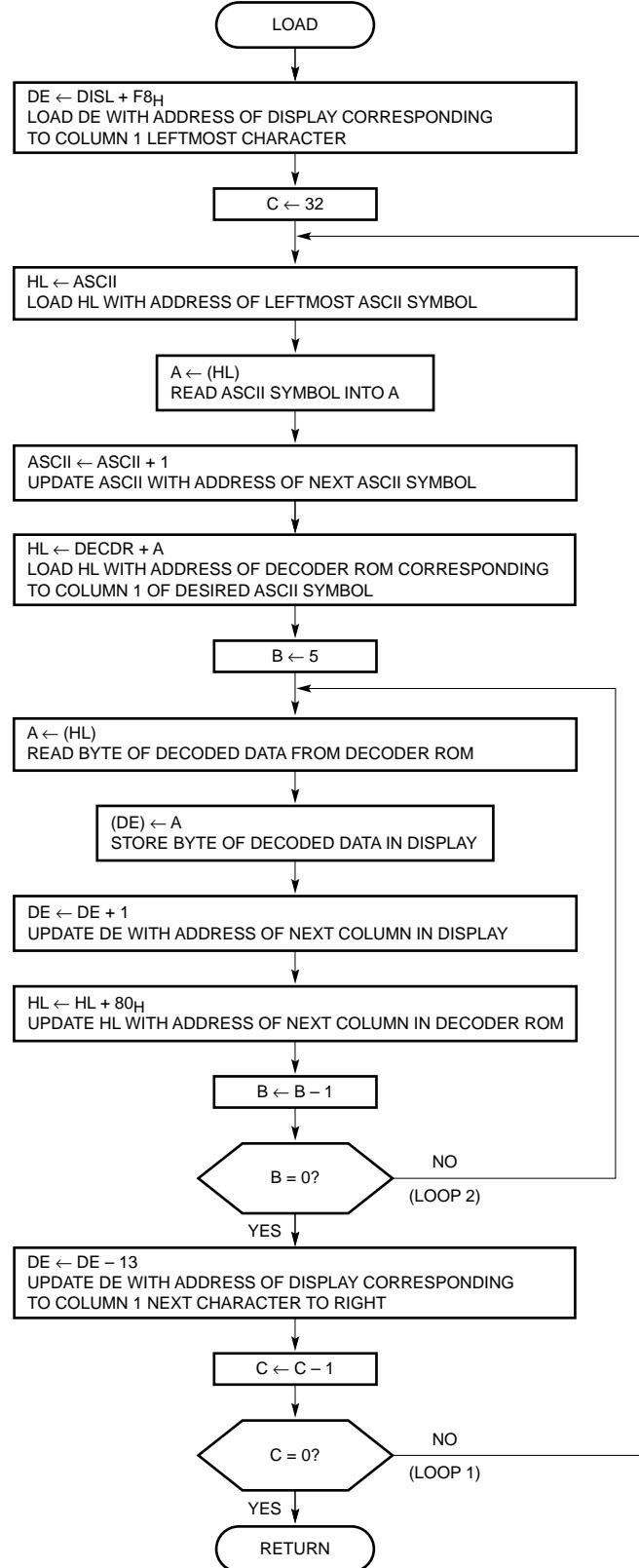


Figure 12. 8080A Microprocessor Program that Decodes a 32 Character ASCII String Prior to Loading into the DECODED DATA CONTROLLER

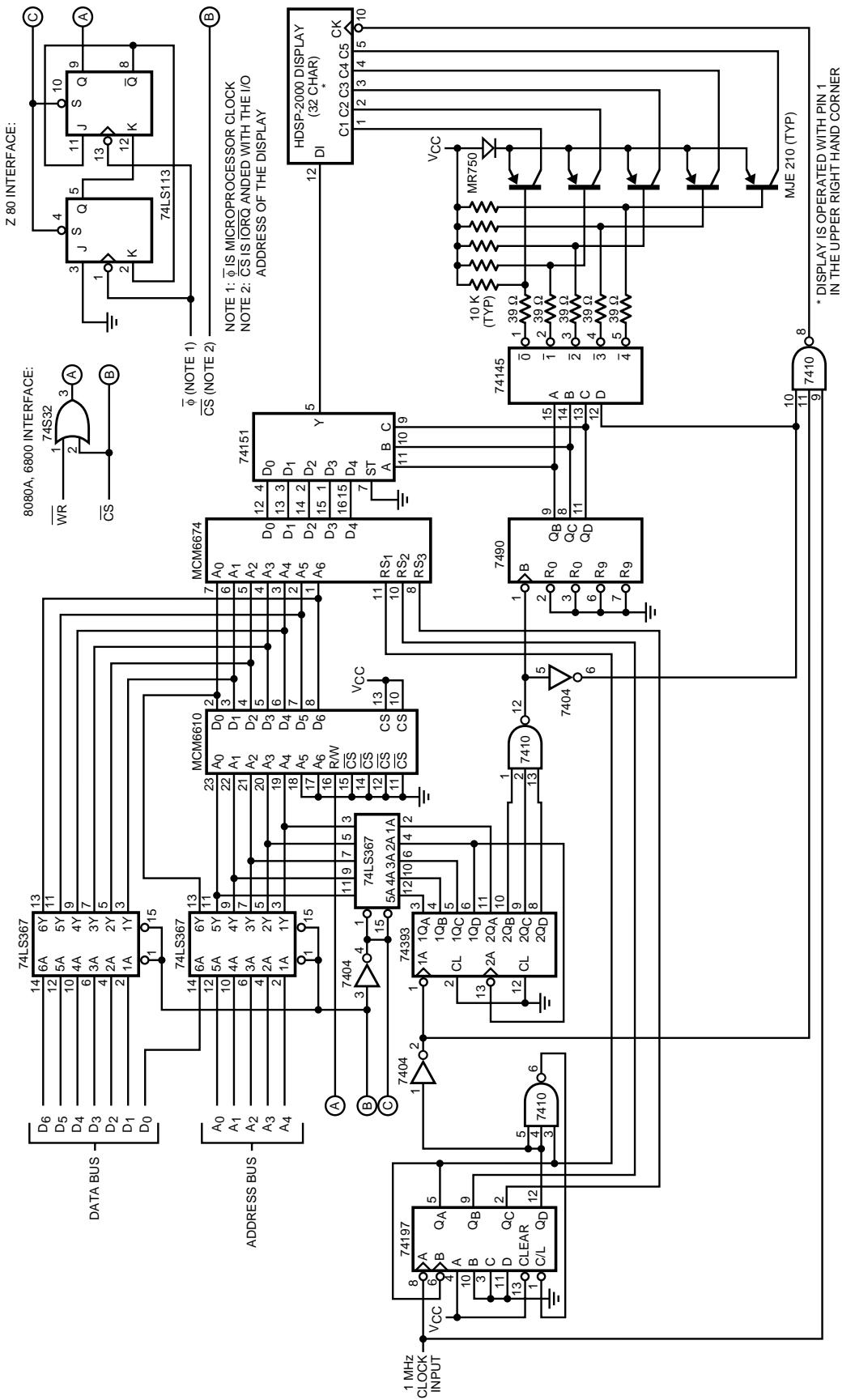


Figure 13. 8080A Microprocessor Interface to the 32 Character HDSP-2000 Coded Data Controller

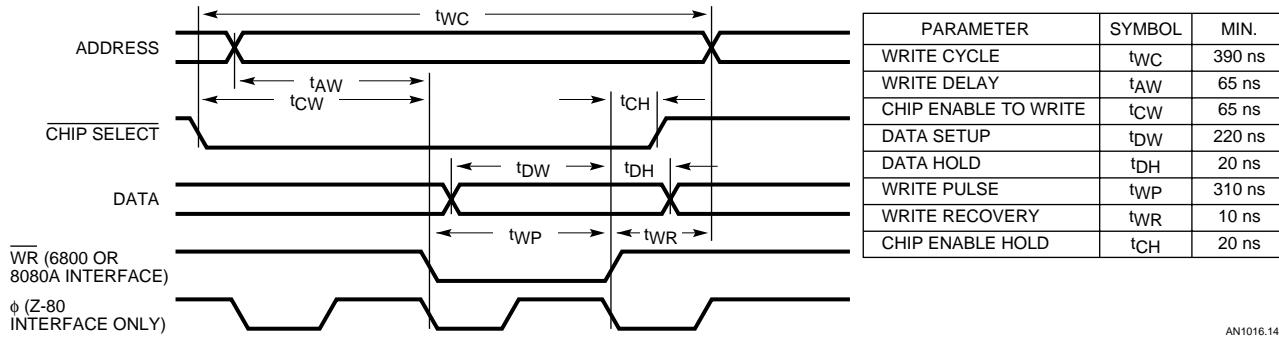


Figure 14. Memory Write Timing for the 32 Character HDSP-2000 CODED DATA CONTROLLER

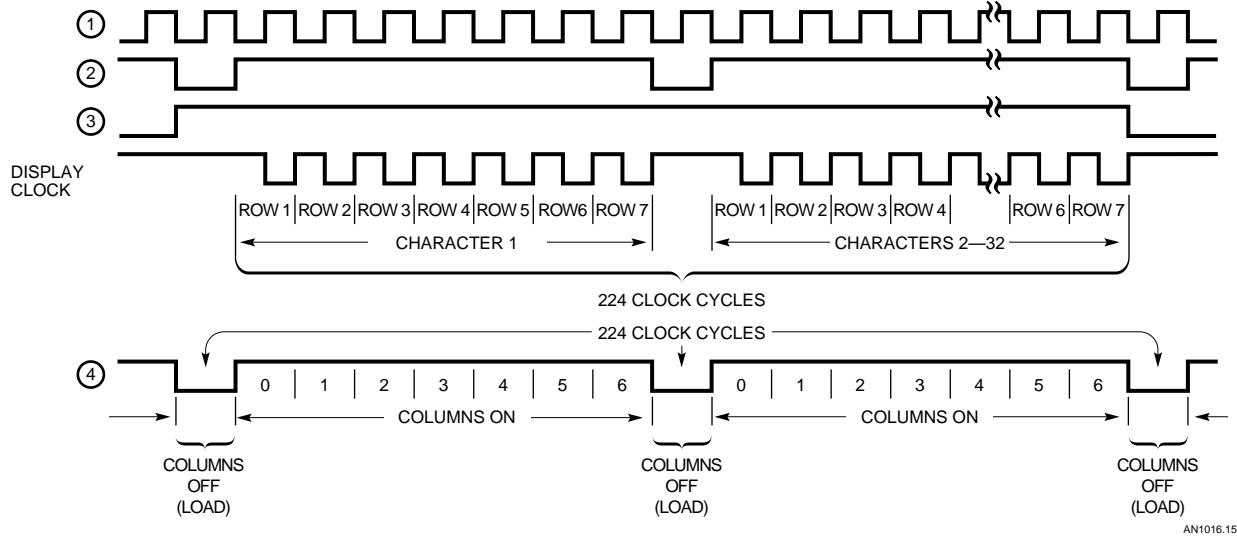


Figure 15. Timing Information for the 32 Character HDSP-2000 CODED DATA CONTROLLER

can either test the flag or allow the flag to automatically interrupt the microprocessor. Subroutine "READ" would then be used to read the DATA OUT outputs from the controller into the microprocessor system. The microprocessor uses the CB₁ input of the 6821 PIA to determine when to read each of the 34 data output words into the system.

A similar PIA interface for the 8080A microprocessor is depicted in Figures 22 and 23.

The HDSP-247X series of controllers are programmed to default to "Left Entry" mode for a 32 character string of displays. If some other entry mode or string length is desired, it is necessary to either load the appropriate control word from the microprocessor or to

provide a control word during POWER ON RESET. The controller will read the DATA IN lines during RESET and interpret the contents as the control word. The circuit depicted in Figure 24 can be utilized to load any desired preprogrammed word into the HDSP247X controller, during power on.

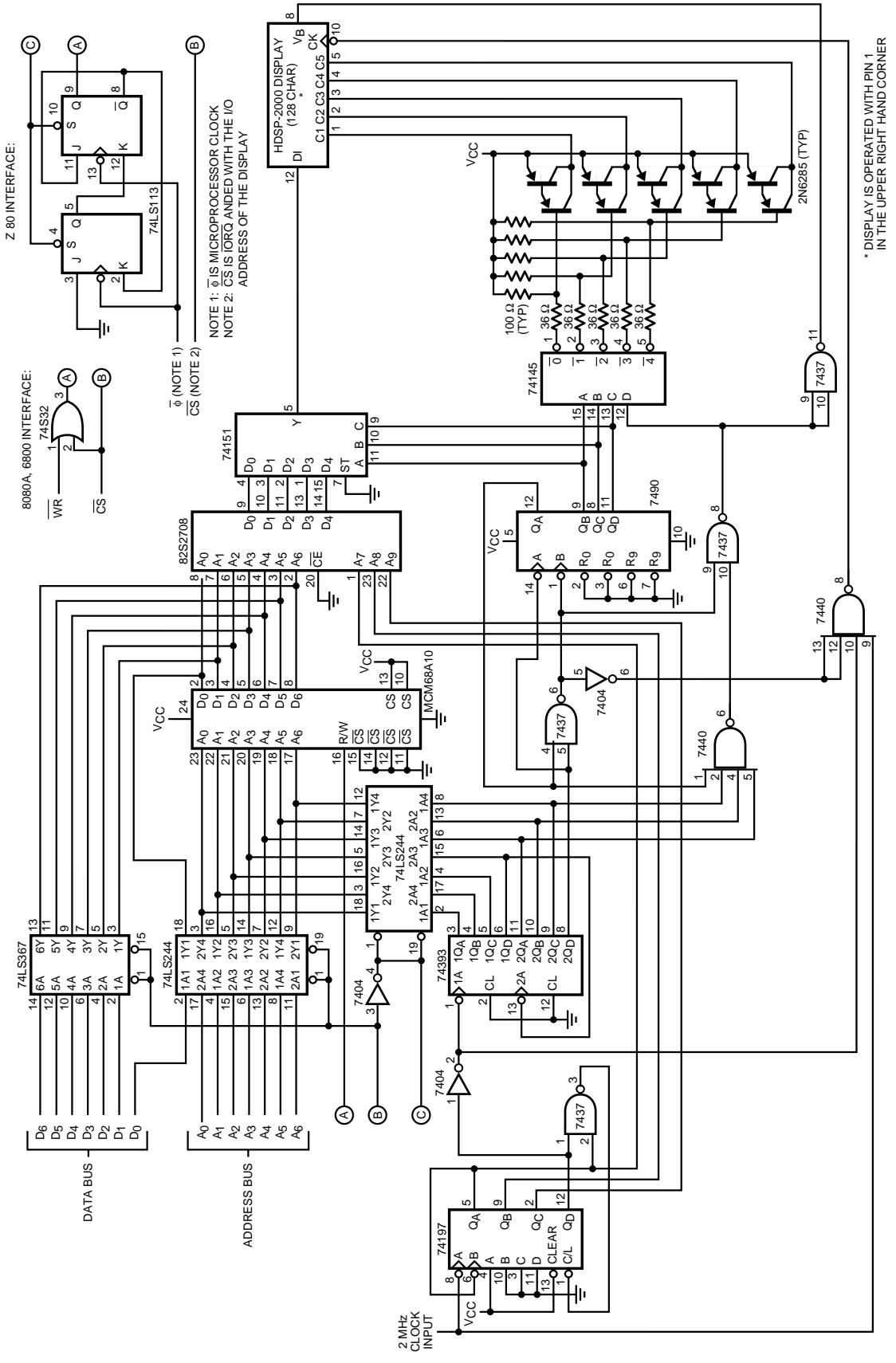


Figure 16. 6800, 8080A, and Z-80 Interface to the 128 Character HDSP-2000 CODED DATA CONTROLLER

PROM ADDRESS	HEXIDECIMAL DATA																ROW 4																																																																																																																
	200	F1	F0	E4	E1	EF	F5	F4	FF	E9	FF	FF	F5	E4	FF	F5	F5																																																																																																																
080	FF	FF	E4	E1	E8	FF	E0	EE	E4	E0	EE	EE	200	F1	F0	E4	E1	EF	F5	F4	FF	E9	FF	FF	F5	E4	FF	F5	F5	ROW 5																																																																																																			
090	FF	EE	EE	EE	EE	E0	EE	E1	FF	E4	EE	EE	210	FF	F7	F7	F0	FD	F5	EA	FF	E4	EE	E8	F0	FD	FD	F7	F7	ROW 5																																																																																																			
0A0	E0	E4	EA	EA	E4	F8	E8	EC	E2	E8	E4	E0	220	E0	E4	E0	EA	EE	E4	E5	F2	E1	FE	E4	EE	E0	EC	FF	E0	E4	ROW 5																																																																																																		
0B0	EE	E4	EE	E2	FF	E6	FF	EE	E0	EC	E2	E0	230	F5	E4	EE	E6	F2	E1	FE	E4	EE	E0	EC	F0	E0	E1	E2	240	ED	F1	EE	F0	E9	FC	FC	F3	FF	E4	E1	F8	F0	F5	F3	F1	ROW 5																																																																																			
0C0	EE	E4	FE	EE	FF	FF	FF	E1	E1	F1	F0	F1	250	FE	F1	FE	EE	E4	F1	EA	F1	E4	E4	E8	E4	E2	E0	E0	E0	260	E2	E1	F9	F1	F3	F1	EE	ED	F9	E4	E1	F4	E4	F5	F9	F1	ROW 5																																																																																		
0D0	FE	EE	FE	EE	FF	F1	F1	F1	F1	FF	EE	E0	270	F9	F3	F9	F0	E4	F1	F1	F1	E4	EE	E2	E8	E0	E2	E0	F5	280	F1	F0	E4	E1	E4	F8	EA	E5	E2	E0	EE	F5	E8	FB	F1	F1	ROW 6																																																																																		
0E0	E6	E0	F0	E0	E1	E0	E2	ED	F0	E4	E1	EC	290	F1	F1	F5	F5	F1	F8	EA	E1	EA	E4	E4	F1	F1	F5	F5	F1	ROW 6																																																																																																			
0F0	F6	ED	E0	E0	E4	E0	E0	E0	E1	E0	E2	E4	2A0	E0	E4	E0	FF	E5	E8	F5	E0	E8	E2	EE	E4	E0	E0	E8	2B0	F9	E4	F0	E1	FF	E1	F8	F1	E1	EC	EC	E8	FF	E2	E4	2C0	F5	FF	E9	F0	E9	F0	F0	F1	F1	E4	E1	F4	F0	F1	F1	F1	ROW 6																																																																			
100	F1	F0	E4	E1	E4	F1	E1	E8	E4	E0	E4	F5	2D0	F0	F5	F4	E1	E4	F1	EA	F5	EA	E4	E8	E8	E2	E0	E0	2E0	E0	EF	F1	F0	F1	FF	E4	E1	F1	E4	F5	F1	F1	2F0	F6	ED	F0	EE	E4	E1	F1	F5	E4	E1	E4	E4	E0	EA	280	F1	F0	E4	E1	E4	F8	EA	E5	E2	E0	EE	F5	E8	FB	F1	F1	ROW 6																																																						
110	F1	F5	F1	F1	F5	E5	EA	E1	F1	E4	F1	F1	290	F1	F1	F5	F5	F1	F8	EA	E1	F1	E4	E0	F1	F1	F5	F5	F1	ROW 6																																																																																																			
120	E0	E4	EA	EA	EF	F9	F4	EC	E4	E4	F5	E4	2A0	E0	E4	E0	FF	E5	E8	F5	E0	E8	E2	EE	E4	E0	E0	E8	2B0	E0	E0	E0	EA	FE	F3	F2	E0	E4	E4	F5	E4	E8	E0	EC	F0	300	F1	F0	E4	E1	E4	F8	EA	E1	E4	E0	E4	E4	E4	F1	F1	F1	ROW 6																																																																		
130	F1	EC	F1	F1	E6	F0	E8	E1	F1	EC	EC	E4	230	E0	E0	E0	EA	FE	F3	F2	E0	E4	E4	F5	E4	E8	E0	EC	F0	310	F1	F1	F5	F5	F1	F8	EA	E1	F1	E4	E0	F1	F1	F5	F5	F1	ROW 6																																																																																		
140	F1	EA	E9	F1	F9	F0	F0	F1	E1	F2	F0	FB	240	F1	E4	F0	F1	E2	F1	F0	F1	E4	F1	F2	F0	F1	F1	F1	320	E0	E0	E0	EA	FE	F3	F2	E0	E4	E4	F5	E4	E8	E0	EC	F0	330	F1	E4	F0	F1	E2	F1	F0	F1	E4	F1	E2	EC	E8	E0	E4	E0	ROW 6																																																																		
150	F1	F1	F1	F1	E4	F1	F1	F1	F1	E1	E8	F0	250	F5	F1	E9	F1	E9	F0	F0	F1	E4	F1	F2	F0	F1	F1	F1	340	F0	F2	F2	F1	E4	F1	E4	FB	F1	E4	F1	F2	F0	F1	F1	350	E0	F1	F9	F1	F3	F0	E4	F1	F1	E4	F1	F4	E4	F5	F1	F1	ROW 6																																																																			
160	E6	E0	F0	E0	E1	E0	E5	F3	F0	E0	E0	F0	260	E0	F1	F9	F1	F3	F0	E4	E0	E0	E0	E0	E0	E0	E0	360	E0	F1	F9	F1	F3	F0	E4	F1	F1	E4	F1	F4	E4	F5	F1	F1	ROW 6																																																																																				
170	F9	F3	E0	E0	E4	E0	E0	E0	E1	E0	E4	E4	270	F0	E1	F0	E1	E5	F3	EA	F5	EA	F1	E8	E4	E4	E0	F5	370	F0	E1	F0	E1	E5	F3	EA	F5	EA	F1	E8	E4	E4	E0	F5	380	FF	F0	FF	FF	E1	FF	E0	FB	E1	E0	FF	E0	E4	E0	EE	EE	ROW 7																																																																			
180	F1	F0	E4	E1	E2	FB	E2	F1	FE	E0	E4	EE	290	FF	EE	EE	EE	EE	FF	E0	FB	E1	FF	E4	E4	E4	E4	E4	390	FF	EE	EE	EE	EE	FF	E0	FB	E1	FF	E4	E4	E4	FF	FF	FF	FF	ROW 7																																																																																		
190	F1	F5	F1	F1	F5	E2	EA	E1	EA	EE	F0	F1	2A0	E0	E4	E0	EA	E4	E3	ED	E0	E2	E8	E4	E0	F0	E0	EC	E0	3A0	E0	E4	E0	EA	E4	E3	ED	E0	E2	E8	E4	E0	E0	E8	E4	3B0	EE	EE	FF	EE	E2	EE	FF	E0	EE	EC	E0	F0	E2	E0	E8	E4	3C0	EE	F1	FE	EE	E2	FF	E0	EF	F1	EE	EE	F1	FF	F1	F1	EE	3D0	F0	ED	F1	EE	E4	E4	F1	F1	E4	FF	E0	EE	E0	FF	3E0	E0	EF	F6	EE	ED	EE	E4	E1	EE	EE	F2	EE	F5	F1	EE	EE	3F0	F0	E1	F0	FE	E2	ED	E4	EA	F1	EE	FF	E2	E4	E8	E0	EA	ROW 7
1A0	E0	E4	EA	FF	F4	E2	F4	E8	E8	E2	EE	E4	2B0	E0	E4	E0	EA	E4	E3	ED	E0	E2	E8	E4	E0	E0	E8	E4	3C0	EE	F1	FE	EE	E2	FF	E0	EF	F1	EE	EE	F1	FF	F1	F1	EE	3D0	F0	ED	F1	EE	E4	E4	F1	F1	E4	FF	E0	EE	E0	FF	3E0	E0	EF	F6	EE	ED	EE	E4	E1	EE	EE	F2	EE	F5	F1	EE	EE	3F0	F0	E1	F0	FE	E2	ED	E4	EA	F1	EE	FF	E2	E4	E8	E0	EA	ROW 7																																		
1B0	F3	E3	E1	E1	EA	FE	F0	F2	F1	E1	EC	E8	2C0	E8	FF	E2	E1	E8	FF	E0	EE	E4	E3	ED	E0	E2	E8	E4	3C0	EE	F1	FE	EE	E2	FF	E0	EF	F1	EE	EE	F1	FF	F1	F1	EE	3D0	F0	ED	F1	EE	E4	E4	F1	F1	E4	FF	E0	EE	E0	FF	3E0	E0	EF	F6	EE	ED	EE	E4	E1	EE	EE	F2	EE	F5	F1	EE	EE	3F0	F0	E1	F0	FE	E2	ED	E4	EA	F1	EE	FF	E2	E4	E8	E0	EA	ROW 7																																		
1C0	E1	F1	E9	F0	F0	F0	F1	F1	F1	E4	F4	F0	2D0	F5	F5	F5	F1	F1	F1	F1	F1	F1	F1	F1	3C0	EE	F1	FE	EE	E2	FF	E0	EF	F1	EE	EE	F1	FF	F1	F1	EE	3D0	F0	ED	F1	EE	E4	E4	F1	F1	E4	FF	E0	EE	E0	FF	3E0	E0	EF	F6	EE	ED	EE	E4	E1	EE	EE	F2	EE	F5	F1	EE	EE	3F0	F0	E1	F0	FE	E2	ED	E4	EA	F1	EE	FF	E2	E4	E8	E0	EA	ROW 7																																						
1D0	F1	F1	F1	F0	F4	F1	F1	F1	EA	E2	E8	E8	2E0	E2	F1	E0	E0	E0	E0	E0	E0	E0	E0	3C0	EE	F1	FE	EE	E2	FF	E0	EF	F1	EE	EE	F1	FF	F1	F1	EE	3D0	F0	ED	F1	EE	E4	E4	F1	F1	E4	FF	E0	EE	E0	FF	3E0	E0	EF	F6	EE	ED	EE	E4	E1	EE	EE	F2	EE	F5	F1	EE	EE	3F0	F0	E1	F0	FE	E2	ED	E4	EA	F1	EE	FF	E2	E4	E8	E0	EA	ROW 7																																							
1E0	E4	EE	F6	EE	ED	EE	E4	F3	F6	EC	E1	F2	2F0	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	3C0	EE	F1	FE	EE	E2	FF	E0	EF	F1	EE	EE	F1	FF	F1	F1	EE	3D0	F0	ED	F1	EE	E4	E4	F1	F1	E4	FF	E0	EE	E0	FF	3E0	E0	EF	F6	EE	ED	EE	E4	E1	EE	EE	F2	EE	F5	F1	EE	EE	3F0	F0	E1	F0	FE	E2	ED	E4	EA	F1	EE	FF	E2	E4	E8	E0	EA	ROW 7																																							
1F0	F1	F1	F6	EF	FF	F1	F1	F1	F1	FF	E4	E4	280	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	3C0	EE	F1	FE	EE	E2	FF	E0	EF	F1	EE	EE	F1	FF	F1	F1	EE	3D0	F0	ED	F1	EE	E4	E4	F1	F1	E4	FF	E0	EE	E0	FF	3E0	E0	EF	F6	EE	ED	EE	E4	E1	EE	EE	F2	EE	F5	F1	EE	EE	3F0	F0	E1	F0	FE	E2	ED	E4	EA	F1	EE	FF	E2	E4	E8	E0	EA	ROW 7																																							

Display Power Dissipation
The HDSP-2000 combines a significant amount of logic and display capability in a very small package. As such, on-board power dissipation is relatively high and thermal design of the display mounting becomes an important consideration. The HDSP-2000 is designed to permit operation over a wide range of temperature and supply voltages. The design of a heat sink to maintain a junction temperature of less than 125°C for a multiple package system where every electrical input operates at maximum voltage and current would be difficult at best. However, in virtually all applications, the actual power dissipation is only a small fraction of the maximum power dissipation, since V_{COL} is less than 5.25 V, only a fraction of the 35 LEDs are on at any time, and the duty factor is never 20%. The calculation of

power dissipation is important since the result is largely a function of external circuit parameters. The minimization of power dissipation will reduce the amount of heat sinking required for the displays. Furthermore, by the Arrhenius model, the display reliability is increased by 40% for a 10°C reduction in junction temperature. Thus, reduced power dissipation or better heat sinking can also increase the reliability of the display system.

Calculation of power dissipation in the HDSP-2000 display family can be made using the following formulas:

$$P_D = P(I_{CC}) + P(I_{REF}) + P(I_{COL}) \quad (7)$$

where

$$P(I_{CC}) = I_{CC1} V_{CC} \quad (8)$$

when V_{CC} is applied continuously to the display

$$P(I_{REF}) = 5 (I_{CC2} - I_{CC1}) V_{CC} / (n/35) D.F. \quad (11)$$

when V_B is logical 0 during times t and T_B

$$P(I_{COL}) = 5 I_{COL} V_{COL} / (n/35) D.F. \quad (12)$$

where

where

n = average number of diodes illuminated per character

D.F. = column on time from equation (1) or (5)

$$I_{CC1} = I_{CC} (V_B = 0.4 \text{ V})$$

$$I_{CC2} = I_{CC} (V_B = 2.4 \text{ V})$$

$P(I_{CC})$ is the power which is dissipated in the logic within the shift register. $P(I_{CC})$ is constant regardless of n , or D.F. as long as voltage is applied to the V_{CC} pin. However, for low D.F., I_{CC} can be switched off during the time the display is blanked. $P(I_{REF})$ is the power dissipated in the logic to drive the current mirror output. Thus, if the output of the shift register and the V_B input are both logical 1, $P(I_{REF})$ will be dissipated. $P(I_{COL})$ is the power dissipated within the LEDs and the constant current outputs during the time that V_{COL} is applied and the LEDs are on.

As can be seen from formulas (7) through (12) there are several techniques by which total power dissipation can be reduced:

- Reduce n
- Reduce V_{COL}
- Reduce D. F.
- Reduce V_{CC}
- Turn off V_{CC} when display is blanked

For most applications, $n \leq 20$ dots. For example, the HDSP-2470 character generator has 3 characters with 20 dots on (#, @, B), 1 character with 19 dots on (zero), and 6 characters with 18 dots on (A,D,E,M,R,W). With custom

PROM programming these 4 symbols (#, @, B, zero) can be modified to reduce the total number of dots on to 18 or less. The average of all 36 alphabetic and numeric symbols is 14.7 dots on. The calculations assume that every character has the same number of illuminated dots. This assumption can overstate the maximum power dissipation if the application includes a fixed number of spaces in the display.

Above 2.4 V V_{COL} for standard red devices and 2.75 V V_{COL} for GaP devices, I_{COL} is nearly constant. While it is possible to operate the columns of the HDSP-2000 display using fullwave rectified unregulated DC, lower power dissipation can be achieved by using the regulated V_{CC} supply. Then, V_{COL} is equal to V_{CC} minus the collector to emitter saturation voltage across the column switching transistors. Since the minimum recommended V_{COL} is 2.4 V or 2.75 V, PNP Darlington transistors with a silicon diode in series with the emitter can be used to lower the power dissipation within the display.

The time averaged luminous intensity for the display is equal to the peak luminous intensity on the data sheet times D.F. Thus, reduction in D.F. will also reduce the time averaged luminous intensity as well as power dissipation. For most indoor applications, a D.F. of 10% for standard red and 5% for GaP displays will provide satisfactory luminous intensity. For example, the 40 character HDSP-2470 system has a D.F. of 11.6%. However, a D.F. of 17% or higher is recommended for sunlight viewable applications for the GaP displays.

The HDSP-2000 family of alphanumeric displays are specified for operation with a 5% tolerance 5 volt supply. A tighter tolerance supply will also reduce the power dissipation in the display.

I_{CC} can be switched off during the time the display is blanked. Thus, power would be applied to the display; the shift register would be loaded with information; the columns would be turned on; and then the column current, V_B , and V_{CC} would be switched off until the next column refresh cycle. For low D.F., this can significantly reduce the power dissipation within the display. As D.F. increases, the display is blanked for a smaller portion of the refresh cycle and the power reduction is reduced. When the blanking time goes to zero, the power reduction also goes to zero.

For example, the maximum power dissipation for a four character HDSP-2000 display ($n = 20$, $V_{COL} = 3.5$ V, $V_B = 2.4$ V, D.F. = 17.5%, $V_{CC} = 5.25$ V) can be calculated as shown below:

$$\begin{aligned} P(I_{CC}) &= (60 \text{ mA}) (5.25 \text{ V}) \\ &= 315 \text{ mW} \end{aligned} \quad (13)$$

$$\begin{aligned} P(I_{REF}) &= 5 (95 \text{ mA} - 60 \text{ mA}) \\ &\quad (5.25 \text{ V}) (20/35) \\ &\quad (0.175) \\ &= 92 \text{ mW} \end{aligned} \quad (14)$$

$$\begin{aligned} P(I_{COL}) &= 5 (410 \text{ mA}) (3.5 \text{ V}) \\ &\quad (20/35) (0.175) \\ &= 718 \text{ mW} \end{aligned} \quad (15)$$

$$\begin{aligned} P_D &= P(I_{CC}) + P(I_{REF}) + \\ &\quad P(I_{COL}) \\ &= 1125 \text{ mW} \end{aligned} \quad (16)$$

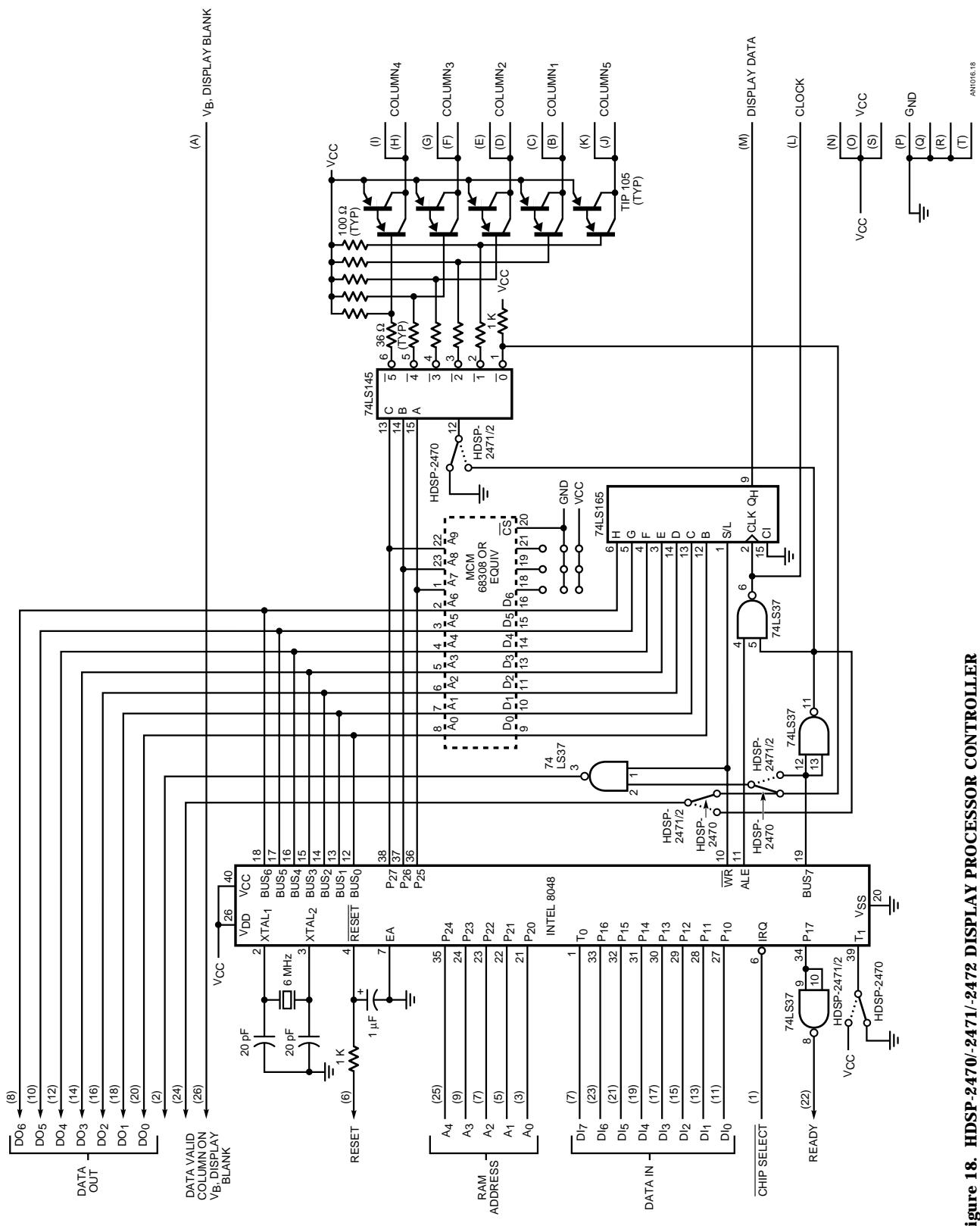


Figure 18. HDSP-2470/-2471/-2472 DISPLAY PROCESSOR CONTROLLER

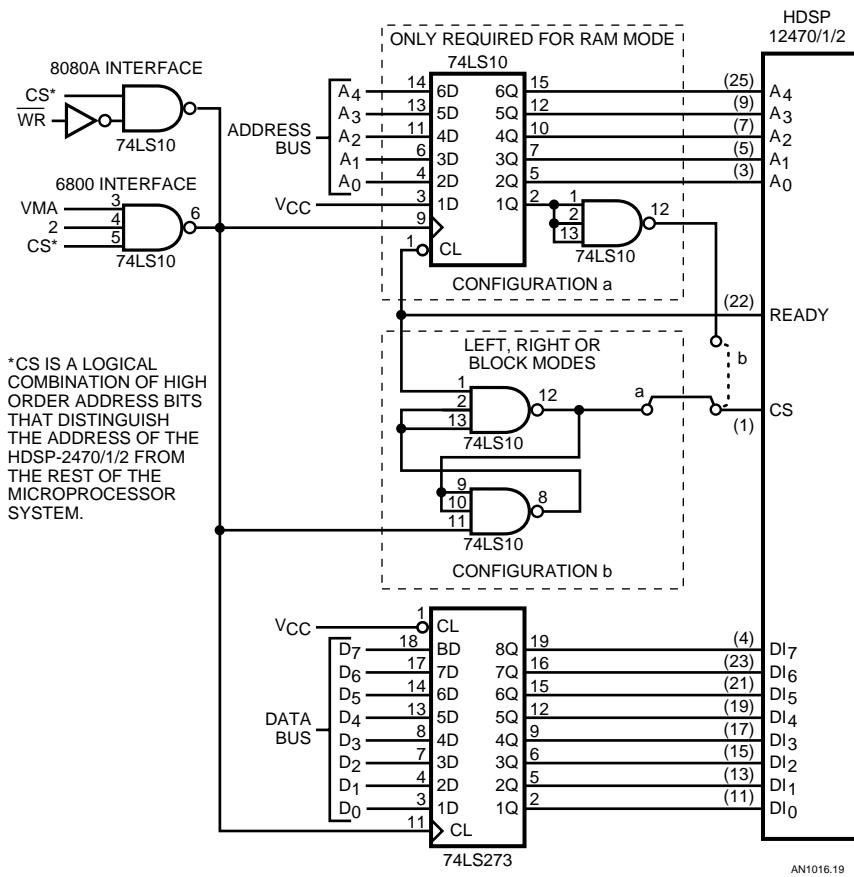


Figure 19. Latched Interface to the HDSP-2470/-2471/-2472 DISPLAY PROCESSOR CONTROLLER

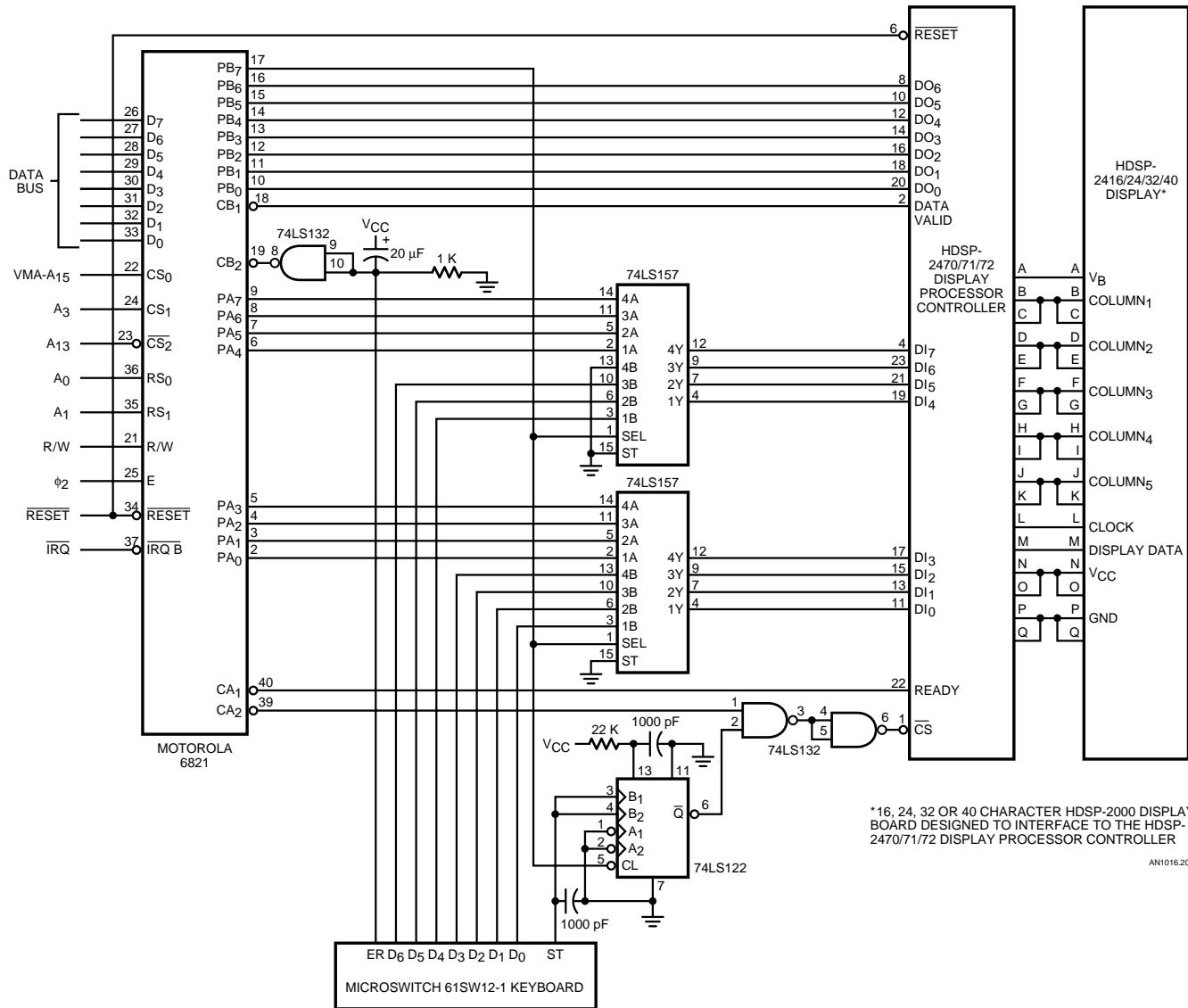
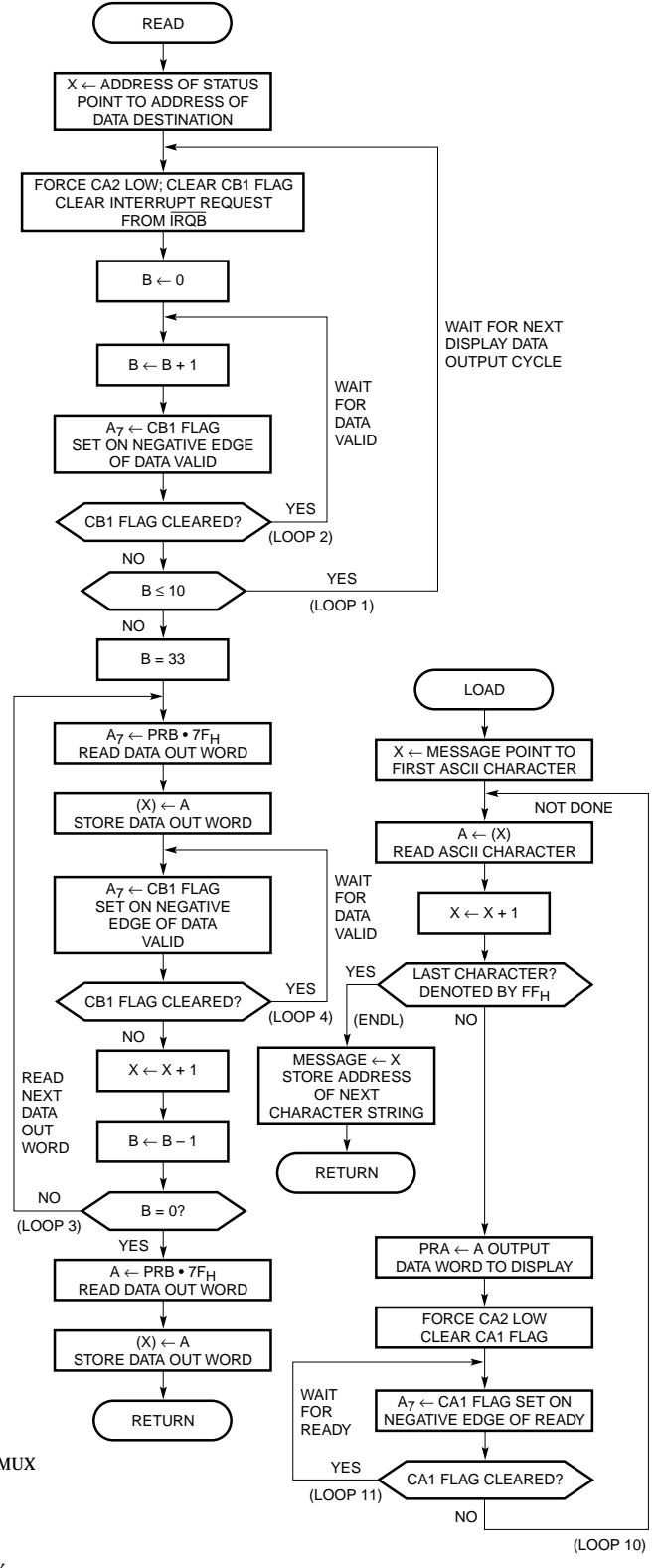


Figure 20. 6800 Microprocessor Interface Utilizing a 6820 PIA for an HDSP-2470/-2471/-2472 Alphanumeric Terminal

* PORT CONFIGURATION:
* 1. PORT A:
* PA0-PA7 OUTPUTS TO DATA IN OF HDSP-247X
* CA1 (INPUT) MODE 00 SET FLAG NEG EDGE OF READY
* CA2 (OUTPUT) MODE 100 CLEARED MPU READ PRA, SET
* NEG EDGE OF READY
* 1. PORT B:
* PB0-PB6 INPUTS DATA TO 6800 FROM DATA OUT OF HDSP-247X
* CB1 (INPUT) MODE 00 SETS FLAG NEG EDGE OF DATA VALID
* CB2 (INPUT) MODE 000 SETS FLAG NEG EDGE OF ER KEY
* CB2 (INPUT) MODE 001 SETS FLAG NEG EDGE OF ER KEY
* CAUSING IRQ
* PB7 (OUTPUT) LOW ENABLES PA0-PA7 TO MUX
* HIGH ENABLES KEYBOARD TO MUX

LOC	OBJECT	CODE	SOURCE STATEMENT
		8008	PRA EQU \$8008
		8008	DRA EQU \$8008
		8009	CRA EQU \$8009
		800A	PRB EQU \$800A
		800A	DRB EQU \$800A
		800B	CRB EQU \$800B
0000	MESSAGE	ORG RMB 2	
0100	STATUS	ORG RMB 1	
0101	CURSOR	RMB 1	
0102	DATA	RMB 32	
0400	CE 0100	READ LDX I, STATUS	ORG \$0400
0403	B6 800A	LOOP1 LDA A E, PRB	CLEAR CB1 AND CB2
0406	5F	CLR B	
0407	5C	INC B	
0408	B6 800B	LDA A E, CRB	WAIT FOR DATA VALID
040B	2A FA	BPL LOOP2	
040D	C1 0A	CMP B I, 10	
040F	23 F2	HLS LOOP1	
0411	C6 21	LDA B I, 33	
0413	B6 800A	LDA A E, PRB	READ AND CLEAR CB1
0416	84 7F	AND A I, \$7F	
0418	A7 00	STA A X, 0	STORE IN RAM
041A	B6 800B	LDA A E, CRB	WAIT FOR DATA VALID
041D	2A FB	BPL LOOP4	
041F	08	INX	
0420	5A	DEC B	
0421	26 F0	BNE LOOP3	READ DATA
0423	B6 800A	LDA A E, PRB	
0426	84 7F	AND A I, \$7F	
0428	A7 00	STA A X, 0	
042A	39	RTS	
042B	DE 00	LOAD LDX D, MESSGE	
042D	A6 00	LOOP10 LDA A X, 0	
042F	08	INX	
0430	81 FF	CMP A I, SFF	LAST WORD IN STRING
0432	27 0D	BEQ ENDL	JUMP WHEN DONE
0434	B7 8008	STA A E, PRA	
0437	7D 8008	TST E, PRA	CLEAR CA1 AND CA2
043A	B6 8009	LDA A E, CRA	
043D	2A FB	BPL LOOP11	WAIT
043F	20 EC	BRA LOOP10	
0441	DF 00	STX D, MESSGE	
0443	39	RTS	
0500	7F 8009	START ORG \$0500	
0503	7F 800B	CLR E, CRA	
0506	86 FF	CLR E, CRB	
0508	B7 8008	LDA A I, SFF	
050B	86 24	STA A E, DRA	
050D	B7 8009	LDA A I, S24	
0510	86 80	STA A E, CRA	
0512	B7 800A	LDA A I, \$80	
0515	86 04	STA A E, DRB	
0517	B7 800B	LDA A I, \$04	
		STA A E, CRB	
* PROCEDURE TO LOAD HDSP-247X SYSTEM			
051A	OE	CLI	
051B	7F 800A	CLR E, PRB	DISABLE KEYBD FROM MUX
051E	BD 042B	JSR E, LOAD	
* PROCEDURE TO READ DATA OUT OF HDSP-247X SYSTEM			
0521	7D 800A	TST E, PRB	CLEAR CB1, CB2
0524	86 80	LDA A I, \$80	
0526	B7 800A	STA A E, PRB	ENABLE KEYBD TO MUX
0529	86 0C	LDA A I, \$0C	
042B	B7 800B	STA A E, CRB	ENABLE IRQ,
052E	0F	SEI	IRQ CAUSE JSR TO READ



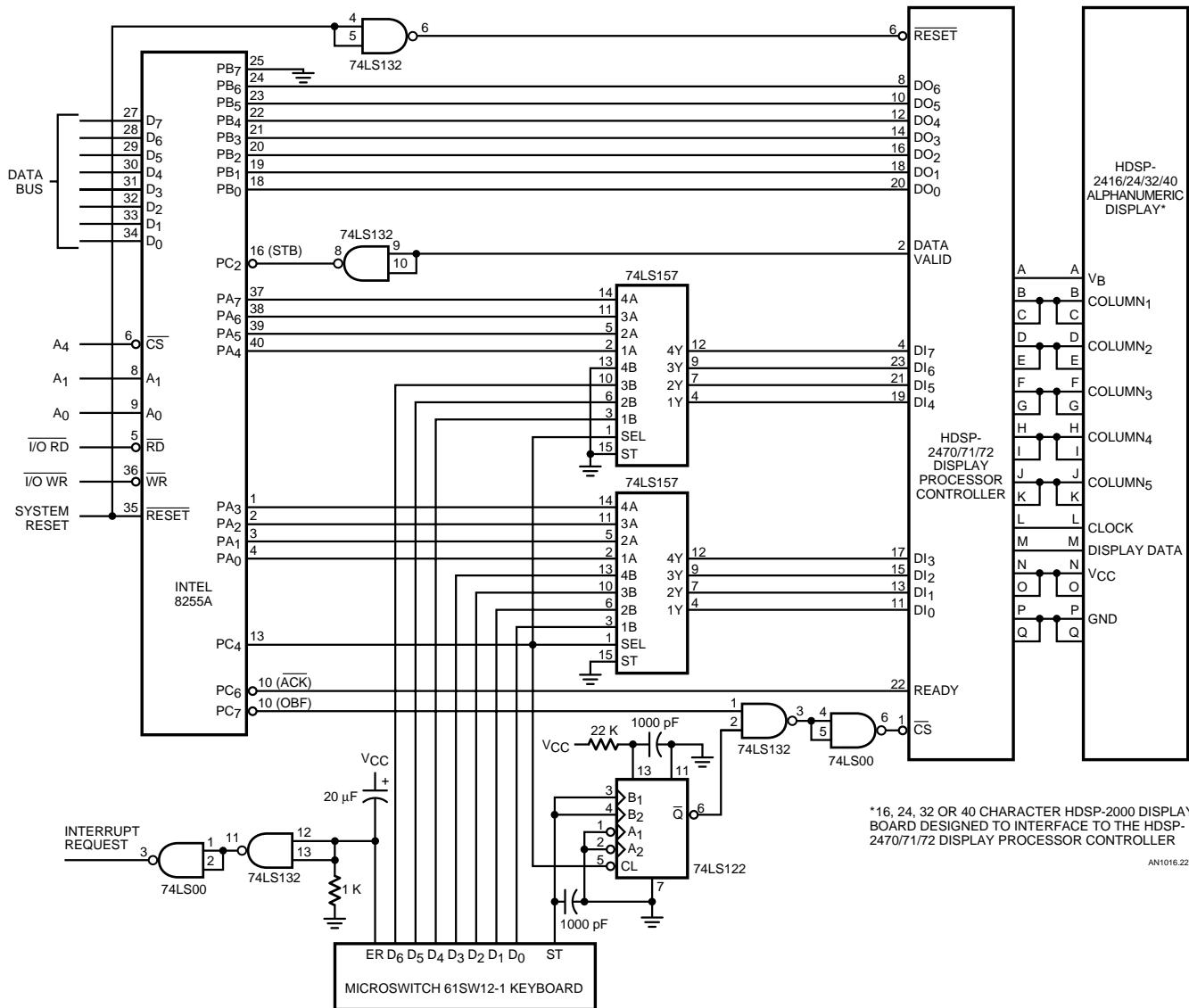


Figure 22. 8080A Microprocessor Interface Utilizing an 8255 PIA for an HDSP-2470/2471/2472 Alphanumeric Terminal

Similarly, a typical power dissipation for a four character HDSP-2000 display ($n = 15$, $V_{COL} = 3.0$ V, D.F. = 17.5%, $V_{CC} = 5.00$ V) can be calculated as:

$$P(I_{CC}) = (45 \text{ mA}) (5.00 \text{ V}) = 225 \text{ mW} \quad (17)$$

$$\begin{aligned} P(I_{REF}) &= 5 (73 \text{ mA} - 45 \text{ mA}) (5.00 \text{ V}) (15/35) \\ &\quad (0.175) \\ &= 52 \text{ mW} \end{aligned} \quad (18)$$

$$\begin{aligned} P(I_{COL}) &= 5 (335 \text{ mA}) (3.0 \text{ V}) (15/35) (0.175) \\ &= 377 \text{ mW} \end{aligned} \quad (19)$$

$$\begin{aligned} P_D &= P(I_{CC}) + P(I_{REF}) + \\ &\quad P(I_{COL}) \\ &= 654 \text{ mW} \end{aligned} \quad (20)$$

Some typical power dissipations for other values of n , V_{COL} , D.F., V_{CC} , are shown in Figure 25. Note that at a D.F. of 17.5%, which would be appropriate for a sun-light viewable application, the

* PORT CONFIGURATION:
 * 1. PORT A (MODE 1 OUTPUT):
 * PA0-PA7 OUTPUTS TO DATA IN OF HDSP-247X
 * PC7 (OBF) OUTPUT; TO CHIP SELECT
 * PC6 (ACK) INPUT; TO READY
 * FLAG PC7 (OBF) CLEARED BY OUTPUT; SET BY READY
 *
 * 2. PORT B (MODE 1 INPUT):
 * PB0-PB6 INPUTS DATA OUT OF HDSP-247X
 * PC2 (STB) INPUT; LOADS DATA ON NEG EDGE OF DATA VALID
 * FLAG PC0 (INTR) CLEARED BY INPUT; SET BY DATA VALID
 *
 * 3. PORT C:
 * PC4 OUTPUT; LOW ENABLES PA0-PA7 TO HDSP-247X
 * HIGH ENABLES KEYBOARD TO HDSP-247X

LOC	OBJECT	CODE	SOURCE STATEMENTS
000C		PA	EQU 0CH
000D		PB	EQU 0DH
000E		PC	EQU 0EH
000F		CNTRL	EQU 0FH
E000 02	E0	ASCII TEXT	ORG 0E000H DW TEXT 32
E002 00			
E100 00		STAT	ORG 0E100H
E101 00		ADDR	DB 0
E102 00		DATA	DB 0
			DS 32
E400 F3		READ	ORG 0E400H
E401 F5			DI
E402 E5			PUSH PSW
E403 C5			PUSH H
E404 0E 20	E1		PUSH B
E406 21 00	E1		MVI C, 32
E409 DB 0D		LOOP1	LXI H, STAT
E40B 06 00		LOOP2	IN PB
E40D DB 0E			CLEAR INTR
E40F 04			MVI B, 0
E410 1F			IN PC
E411 D2 0D	E4		INR B
E414 3E 0A		LOOP2	RAR
E416 B8			JNC A, 10
E417 DB 0D			CMP B
E419 D2 0B	E4	LOOP1	IN PB
E41C 77		LOOP3	JNC M, A
E41D 23			MOV INX H
E41E DB 0E		LOOP4	IN PC
E420 1F			RAR
E421 D2 1E	E4	LOOP4	JNC A, 10
E424 DB 0D			IN PB
E426 0D			DCR C
E427 C2 1C	E4	LOOP3	JNZ M, A
E42A 77			MOV INX H
E42B C1			POP B
E42C E1			POP H
E42D F1			PSW
E42E FB			RET
E42F C9			
E430 2A 00	E0	LOAD	LHLD ASCII
E433 7E		LOOP5	MOV A, M
E434 FE FF			CPI 0FFH
E436 CA 45	E4		JZ ENDL
E439 D3 0C			OUT PA
E43B 23			OUTPUT TO DISPLAY
E43C DB 0E		LOOP6	INX H
E43E 17			IN PC
E43F D2 3C	E4	LOOP6	RAL
E442 C3 33	E4		JNC LOOP6
E445 23		ENDL	JMP LOOP5
E446 22 00	E0		INX H
E449 C9			SHLD ASCII
E44A 3E A7		START	MVI A, 0A7H
E44C D3 0F			OUT CNTRL
E44E 3E 0C			MVI A, 0CH
E450 D3 0F			CLEAR INTE A
E452 3E 05			OUT CNTRL
E454 D3 0F			MVI A, 05H
			OUT CNTRL
			SET INTE B
* PROCEDURE TO LOAD HDSP-247X SYSTEM			
E456 3E 08			MVI A, 08H
E458 D3 0F			OUT CNTRL
E45A CD 30	E4		ENABLE A SIDE OF MUX
* PROCEDURE TO READ DATA OUT OF HDSP-247X SYSTEM			
E45D 3E 09			MVI A, 09H
E45F D3 0F			OUT CNTRL
E461 FB			ENABLE B SIDE OF MUX
			INT MUST CALL READ

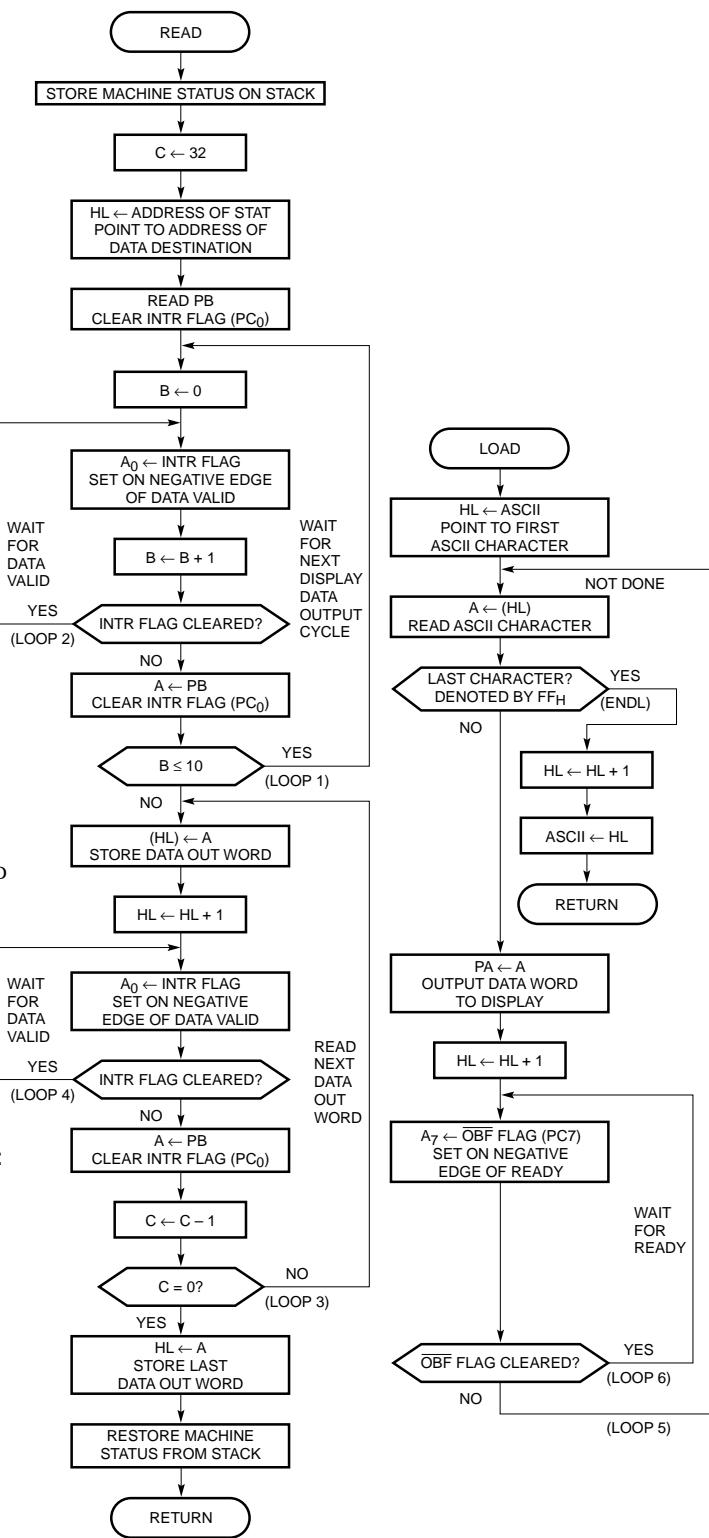


Figure 23. 8080A Microprocessor Program that Interfaces to the Circuit shown in Figure 17.

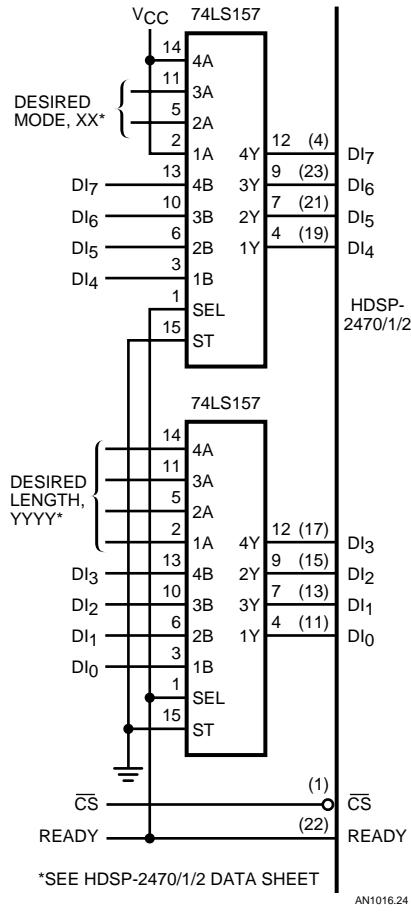


Figure 24. External Circuitry to Load a Control Word into the HDSP-2470/2471/2472 Alphanumeric System upon Request

maximum power dissipation can be reduced to under 1.0 W, while the typical power dissipation can be reduced to 0.60 W. In most indoor ambients, the D.F. can be reduced to 10% for standard red and 5% for GaP displays. Under these conditions the maximum power dissipation is 0.72 W or 0.52 W and the typical power dissipation is 0.43 W or 0.34 W. Thus, in power sensitive applications, GaP displays can be used to conserve power. Turning off V_{CC} during the time the display is blanked can further reduce the power dissipation. In this manner the maximum power dissipation

can be reduced .32 W and the typical power dissipation can be reduced to 0.20 W for the GaP displays.

$$\begin{aligned}
 T_J &= 99^\circ\text{C} + (25^\circ\text{C}/\text{W}) \\
 &\quad (1.12 \text{ W}) \\
 &= 99^\circ\text{C} + 28^\circ\text{C} \\
 &= 127^\circ\text{C}
 \end{aligned} \quad (24)$$

Heat Sinking Considerations

For operation at the maximum temperature of 85°C, it is important that the following criteria be met:

$$a. T_{PIN} \leq 100^\circ\text{C}$$

where T_{PIN} = temperature of hottest pin

$$b. T_J \leq 125^\circ\text{C}$$

The thermal resistance IC junction to case, Θ_{JC} , or IC junction to pin, Θ_{J-PIN} , is shown in Table 2. Using these factors, it is possible to determine the required heat sink power dissipation capability and associated power derating through the following equations:

$$T^* = \Theta_{JA}^* P_D + T_A \quad (21)$$

$$T_J = T^* + \Theta_{J-PIN}^* P_D \quad (22)$$

where

* = Pin or Case

Table 2. Device Thermal Resistance

Device	Θ_{JC}	Θ_{J-PIN}
HDSP-2000 Series	20°C/W	25°C/W
HDSP-2300 Series	7.5°C/W	10°C/W
HDSP-2490 Series	7.5°C/W	13°C/W

For example, given Θ_{PIN-A} of 35°C/W an ambient temperature of 60°C, and the operating conditions shown in equations (13), (14), and (16) the T_{PIN} and T_J for the HDSP-2000 family can be calculated as shown below:

$$\begin{aligned}
 T_{PIN} &= (35^\circ\text{C}/\text{W}) (1.12 \text{ W}) \\
 &\quad + 60^\circ\text{C} \\
 &= 99^\circ\text{C}
 \end{aligned} \quad (23)$$

Heat sink design for the HDSP-2000 family of displays can be accomplished in a variety of ways. For single line applications, a maximum metalized printed circuit board such as shown in Figure 26 can be used. For example, the HDSP-2416/2424/2432/2440 display boards consist of 16, 24, 32 or 40 characters of HDSP-2000 displays mounted on a maximum metalized printed circuit board. The HDSP-2432 printed circuit board is 2.3" x 6.4" and has a Θ_{PIN-A} of about 45°C/W per package for a 1/2 ounce copper clad printed circuit. These display boards are designed for free air operation of 55°C and operation to 70°C with forced air cooling of 150 fpm normal to the rear side of the board, for displays operating at a P_D of 1.00 watt or less.

Heat Sink Design for Operation Above 70°C

A free air operating temperature of 85°C can be achieved by heat sinking the display. Figure 27 depicts a two part heat sink which can be assembled using two different extruded parts. In this design, the vertical fins promote heat transfer due to naturally induced convection. Care should be taken to insure a good thermal path between the two portions of the heat sink. To optimize power handling capability, the heat transfer contact area between the printed circuit board metallization and the heat sink should be maximized. A thermally conductive silicon rubber sheet can be used to insulate the printed circuit board. Heat sink assemblies similar to

Assumptions Used in	Maximum Power Dissipation Operating Conditions (Unless otherwise specified)	Power Dissipation	Maximum Power Dissipation Operating Conditions (Unless otherwise specified)	Power Dissipation
	$V_{CC} = 5.25 \text{ V}$ $V_{COL} = 3.5 \text{ V}$ $n = 20$ $D.F. = .175$ $V_B = \text{logical 0 during } t \text{ (and } T_B)$ $T_B = 0$	1.12 W	$V_{CC} = 5.00 \text{ V}$ $V_{COL} = 3.0 \text{ V}$ $n = 15$ $D.F. = .175$ $V_B = \text{logical 0 during } t \text{ (and } T_B)$ $T_B = 0$.65 W
1. Reduce n	$n = 18$	1.04 W		
2. Reduce n and V_{COL}	$n = 18$ $V_{COL} = 3.0 \text{ V}$.95 W		
3. Reduce V_{COL}	$V_{COL} = 3.0 \text{ V}$	1.02 W	$V_{COL} = 2.4 \text{ V}$.58 W
			$V_{COL} = 2.75 \text{ V}$.62 W
4. Reduce D.F.	$D.F. = .10$.78 W	$D.F. = .10$.47 W
	$D.F. = .05$.55 W	$D.F. = .05$.35 W
5. Reduce V_{COL} and D.F.	$V_{COL} = 3.0 \text{ V}$ $D.F. = .10$.72 W	$V_{COL} = 2.4 \text{ V}$ $D.F. = .10$.43 W
	$V_{COL} = 3.0 \text{ V}$ $D.F. = .05$.52 W	$V_{COL} = 2.75 \text{ V}$ $D.F. = .05$.34 W
6. Reduce D.F. Turn-off V_{CC} during T_B	$D.F. = .10$ $X = .625$.66 W	$D.F. = .10$ $X = .625$.39 W
	$D.F. = .05$ $X = .375$.45 W	$D.F. = .05$ $X = .375$.21 W
7. Reduce V_{COL} , Reduce D.F., Turn-off V_{CC} during T_B	$V_{COL} = 3.0 \text{ V}$ $D.F. = .10$ $X = .625$.60 W	$V_{COL} = 2.4 \text{ V}$ $D.F. = .10$ $X = .625$.34 W
	$V_{COL} = 3.0 \text{ V}$ $D.F. = .05$ $X = .375$.32 W	$V_{COL} = 2.75 \text{ V}$ $D.F. = .05$ $X = .375$.20 W

$$\text{where } x = \left(\frac{t + T}{t + T + T_B} \right)$$

Figure 25. Maximum and Typical Power Dissipation for the HDSP-2000/1/2/3 and HDSP-2300 Alphanumeric Displays

the one shown in Figure 27 typically exhibit a thermal resistance, Θ_{PIN-A} , of 14°C/W per package for a 32 character display.

Copper or aluminum bars mounted underneath the displays can also be used to heat sink the display assembly. Heat generated within the displays is conducted through the ceramic substrate into the bar. The ends of the bar are mounted to a heat sink or to a metal front panel. The bar can be insulated from the pins of the display and the printed circuit board with a thermally conductive silicon rubber sheet. Figure 28 shows a metal plate with slots milled in the plate for each row of displays such that each horizontal row of displays straddles a bar.

A thermal resistance model for this heat sinking technique is shown in Figure 29. This model assumes that all heat generated in the display is generated in the center of each display package and that the ends of the bar are connected to an ideal heat sink. Then the temperature rise of the centermost display in the bar can be calculated as shown below:

$$\begin{aligned} T_C &= 4(\Theta/2) P_D + 3\Theta P_D \\ &\quad + 2\Theta P_D + \Theta P_D + T_A \\ &= 8\Theta P_D + T_A \end{aligned} \quad (25)$$

For display strings of an even number of n displays, the case temperature of the centermost displays can be calculated as

$$T_C = (n^2/8) \Theta P_D + T_A \quad (26)$$

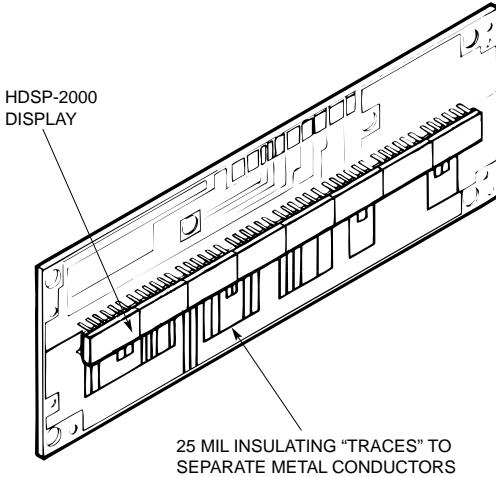


Figure 26. Maximum Metallized Printed Circuit for the Agilent HDSP-2000

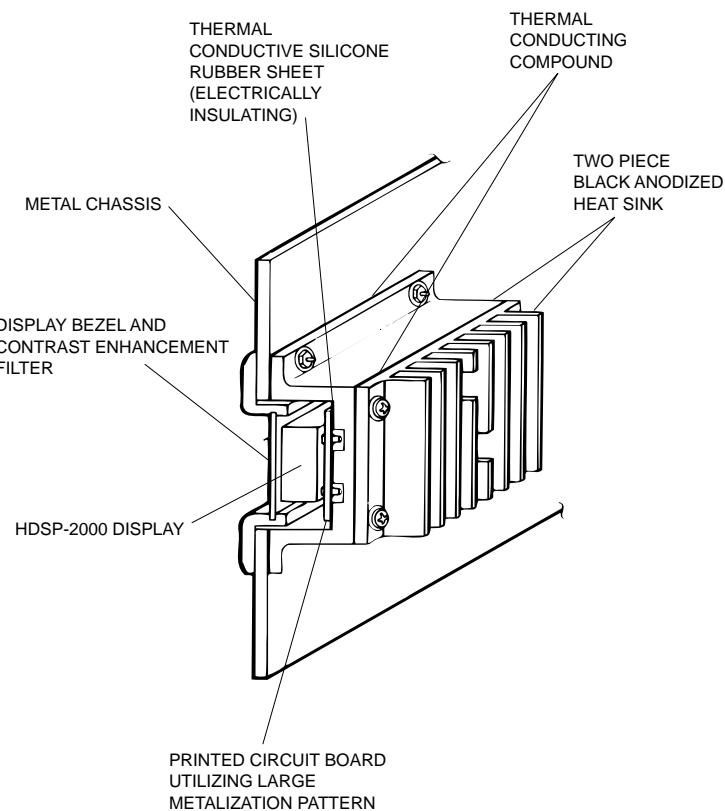


Figure 27. Two-Part Heat Sink for the HDSP-2000

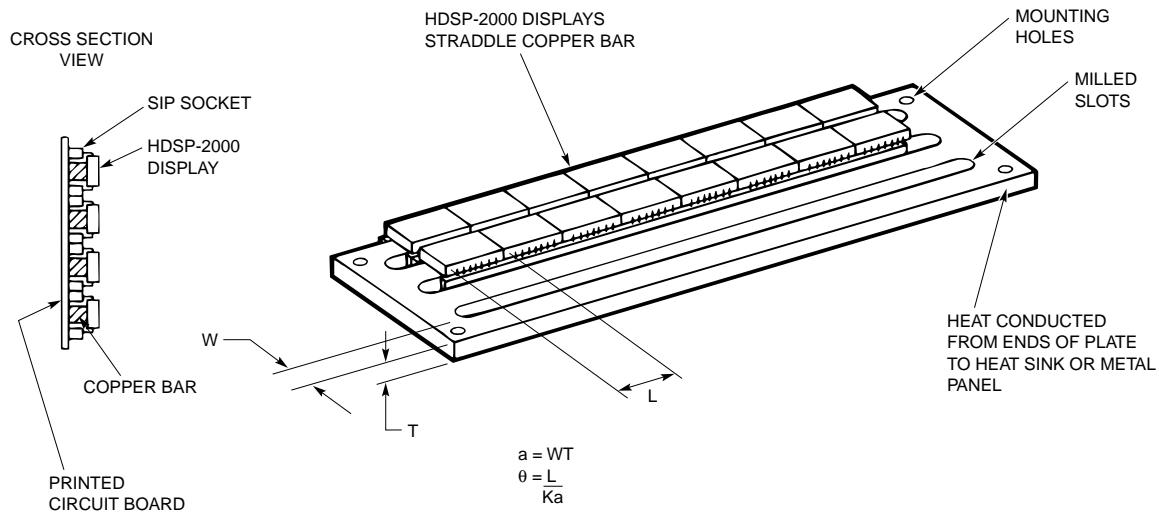


Figure 28. Multiline HDSP-2000 Heat Sink

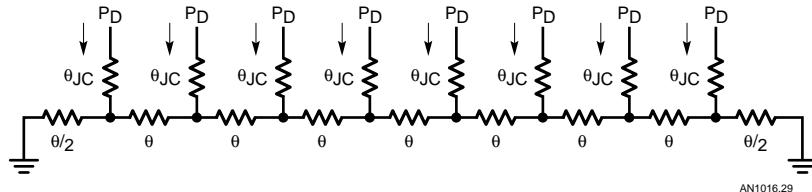


Figure 29. Thermal Resistance Model for Multiline HDSP-2000 Heat Sink

The effectiveness of this type of heatsink can be determined by calculating the thermal resistance of each section of bar under each display

be 6.35 mm (0.25") thick times the row-to-row pin spacing of the display minus 2.54 mm (.10"). Thus, Θ can be calculated as shown below:

$$\Theta = \frac{L}{Ka} \quad (27)$$

where

L = length of bar under each display, mm

K = thermal conductivity of bar, $W/mm^{\circ}C$ ($0.3937 W/mm^{\circ}C$ for copper)

a = cross sectional area of bar, mm^2

If the displays are mounted in a strip socket such as the Robinson Nugent SB-25-100-G socket, then the bar cross sectional area could

The T_C and T_J can be calculated for a 32 character HDSP-2000 display with a copper bar mounted under the row of displays for an ambient temperature of $85^{\circ}C$

HDSP-2000 Family

$$\Theta = \frac{17.8 \text{ mm}}{(0.3937 W / mm^{\circ}C) (6.35 \text{ mm}) (5.08 \text{ mm})} = 1.40^{\circ}C/W \quad (28)$$

HDSP-2300 Family

$$\Theta = \frac{20.3 \text{ mm}}{(0.3937 W / mm^{\circ}C) (6.35 \text{ mm}) (3.81 \text{ mm})} = 2.13^{\circ}C/W \quad (29)$$

HDSP-2490 Family

$$\Theta = \frac{35.6 \text{ mm}}{(0.3937 W / mm^{\circ}C) (6.35 \text{ mm}) (12.7 \text{ mm})} = 1.12^{\circ}C/W \quad (30)$$

and the operating conditions shown in equations (13), (14), (15), and (16):

$$\begin{aligned} T_C &= 8 (1.40^\circ\text{C/W}) \\ &\quad (1.12 \text{ W}) + 85^\circ\text{C} \\ &= 98^\circ\text{C} \end{aligned} \quad (31)$$

Adding in the junction-to-case temperature rise as shown in equation (22), the T_J can be calculated as:

$$\begin{aligned} T_J &= 98^\circ\text{C} + (20^\circ\text{C/W}) \\ &\quad (1.12 \text{ W}) \\ &= 98^\circ\text{C} + 22^\circ\text{C} \\ &= 120^\circ\text{C} \end{aligned} \quad (32)$$

Intensity Control

An important consideration regarding display intensity is the control of the intensity with respect to the ambient lighting level. In dim ambients, a very bright display will produce very rapid viewer fatigue. Conversely, in bright ambient situations, a dim display will be difficult if not im-

possible to read and will also produce viewer fatigue and high error rates. For this reason, control of display intensity with respect to the environment ambient intensity is an important consideration. The HDSP-2000 family of displays is ideally suited for wide ranges of ambient lighting since the intensity of these displays can be varied over a very wide dynamic range. The propagation delay between the V_B input and the time that the LEDs turn on or off is under a microsecond, allowing dynamic variations of over 2000 to 1 in display luminous intensity at a 100 Hz refresh rate.

Figure 30 depicts a scheme which will automatically control display intensity over a range of 10 to 1 as a function of ambient intensity. This circuit utilizes a resettable monostable multivibrator which is triggered by the column enable pulse. The duration of the multivibrator output is controlled by a photoconductor. At the end of a column enable pulse, the multivibrator is reset to insure that column current is off prior to the initiation of a new display shift register loading sequence. The output of this circuit is used to modulate either the V_B inputs of the HDSP-2000 displays or the column enable input circuitry. For maximum reduction in display power, both inputs should be modulated.

In the circuit shown in Figure 30, the photocell may be replaced by a 50 K Ω potentiometer to allow manual control of display intensity.

Figure 31 shows a manually adjustable dimming circuit that provides a very wide range of display intensity. With a 100 Hz

display refresh rate, a 4000 to 1 dynamic range of display intensity can be achieved. The Intersil ICM7555 timer is used as a retriggerable monostable multivibrator. The output of the timer is used to simultaneously pulse width modulate V_B , the display column current, and the display supply current. Initially the 100 pF capacitor is held discharged by the timer. At the negative transition of the trigger input the timer would normally allow the capacitor to charge, however the 2N3906 transistor keeps the capacitor discharged until the trigger input goes high. As soon as the trigger input goes high, the capacitor is charged by a constant current source formed by the RCA CA3084 transistor array. As soon as the voltage across the capacitor reaches 2/3 V_{CC} the output of the timer goes low, and the timer discharges the capacitor. The 2N3906 transistor always discharges the capacitor when the trigger is low, therefore the output of the timer stays high if the voltage across the capacitor never reaches 2/3 V_{CC} . For the values shown, t can be varied exponentially from .5 μs to about 1900 μs . Since Q1 and Q2 are monolithic transistors, t is relatively independent of temperature.

Figure 31 also shows a circuit to switch V_{CC} of the displays off during the time that the display is blanked. When the 2N2219A transistor is off, the LM350 provides a regulated 3 A 5 V output. However, when the 2N2219A transistor is turned on, the output of the LM350 regulator is reduced to 1.2 V. This reduces I_{CC} to under 10 mA per display. Capacitive loading of the regulator should be minimized as much as possible to maximize the switching speed.

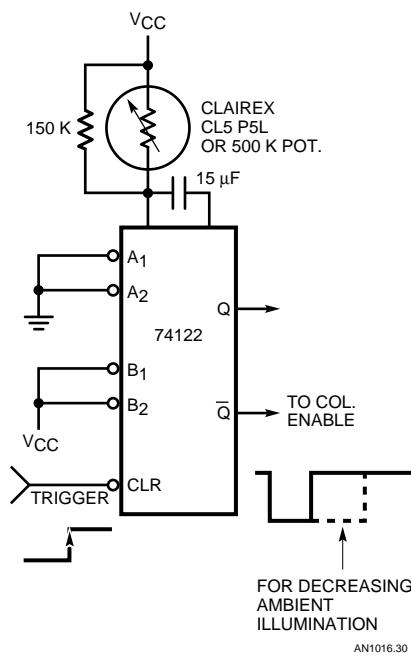


Figure 30. Intensity Modulation Control Using a One Shot Multivibrator

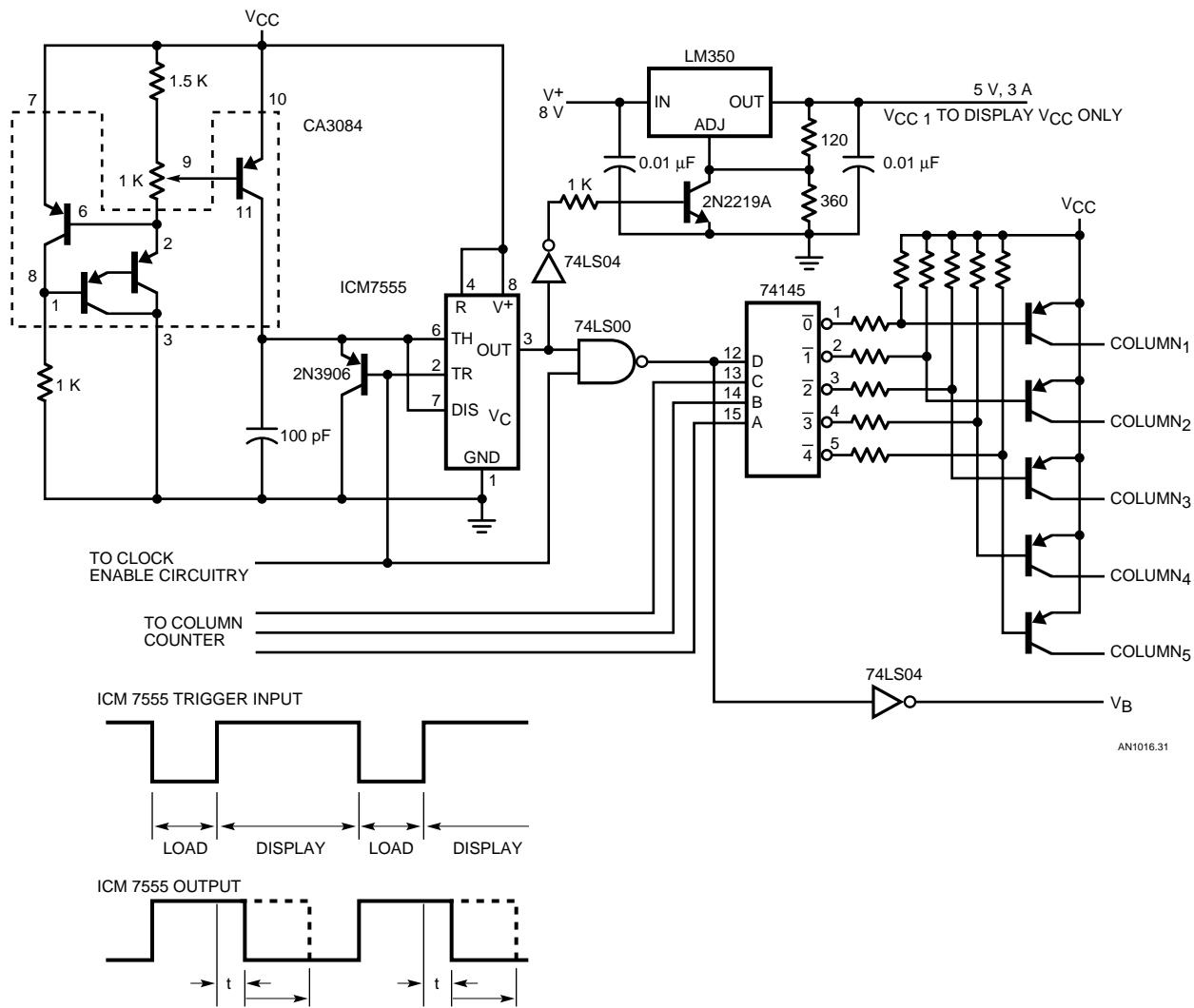


Figure 31. Wide Range Intensity Modulation Control and Power Switching of Display I_{CC} to Conserve Power

The Intensity and Color Matching

The luminous intensity and dominant wavelength of LED displays can vary over a wide range. If there is too great a difference between the luminous intensity or dominant wavelength of adjacent characters in the display string, the display will appear objectionable to the viewer. To solve the problem, all HDSP-2000 displays are categorized for luminous intensity. The category of each display package is indicated by a letter preceding the date code on

the package. When assembling display strings, all packages in the string should have the same intensity category. This will insure satisfactory intensity matching of the characters. All HDSP-2000 family displays are categorized in overlapping intensity categories. All characters of all packages designated to be within a given letter category will fall within an intensity ratio of less than 2:1. For dot matrix displays, a character-to-character intensity ratio of 2:1 is not generally discernible to the human eye.

Since the human eye is very sensitive to variations in dominant wavelength in the yellow and green region, all yellow and green HDSP-2000 family displays are also categorized for dominant wavelength. The dominant wavelength bin for each display package is indicated by a number code following the category letter code on the back of the package. The dominant wavelength bins are 3.5 nm wide for yellow and 4.0 nm wide for green. These dominant wavelength variations are generally not discernible by the human eye.

Display Color	Ambient Lighting		
	Dim	Moderate	Bright
HDSP-2XX0 Standard Red	Homalite H100-1650 3M Panel Film R6510 Panelgraphic Dark Red 63 Ruby Red 60 Chequers Red 118 Rohm & Haas 2423	Homalite H100-1266 Gray H100-1250 Gray H100-1230 Bronze Rohm & Haas 2074 Gray 2370 Bronze	
HDSP-2XX1 (Yellow)	Homalite H100-1726 H100-1720 3M Panel Film A5910 Panelgraphic Yellow 27 Amber 23 Chequers Amber 107	Polaroid HNCP37 3M Light Control Film N00220 Panelgraphic Gray 15 Gray 10 Chequers Gray 105	
HDSP-2XX2 (HER)	Homalite H100-1670 3M Panel Film R6310 Panelgraphic Scarlet Red 65 Chequers Red 112		Polaroid HNCP-10
HDSP-2XX3 (Agilent Green)	Homalite H100-1440 H100-1425 Panelgraphic Green 48 Chequers Green 107		

Contrast Enhancement

Another important consideration for optimum display appearance and readability is the contrast between the display "ON" elements and the background. High contrast can be achieved by placing a filter over the display. The filter, if properly chosen, will transmit the luminance of the light emitting elements while attenuating the luminance of the background.

Filter choice is dependent upon the LED display package, ambient lighting conditions and the desired front panel appearance. For alphanumeric displays in indoor lighting ambients a plastic or glass wavelength filter can be used. In sunlight ambients a neutral density circular polarizer sandwiched between two pieces of optically coated glass is recommended. Figure 32 lists the filter materials recommended for each particular display color. For further information please see Application Note 1015 on Contrast Enhancement for LED Displays.

Figure 32. Contrast Enhancement Filters