



Typical Applications

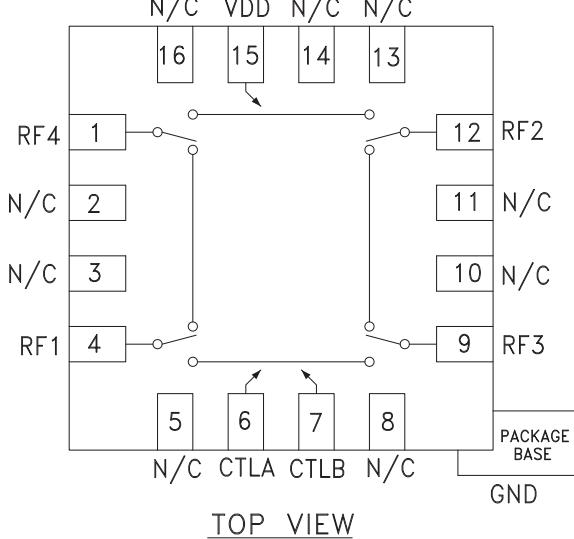
The HMC427LP3 / HMC427LP3E is ideal for:

- Test Instrumentation
- Fiber Optics & Broadband Telecom
- Basestation Infrastructure
- Microwave Radio & VSAT
- Military Radios, Radar, & ECM

Features

- High Isolation: 40 ~ 45 dB thru 6 GHz
- Low Insertion Loss: 1.2 dB@ 6 GHz
- Non-Reflective Design
- 3 x 3 mm SMT Package

Functional Diagram

10
SWITCHES - SMT


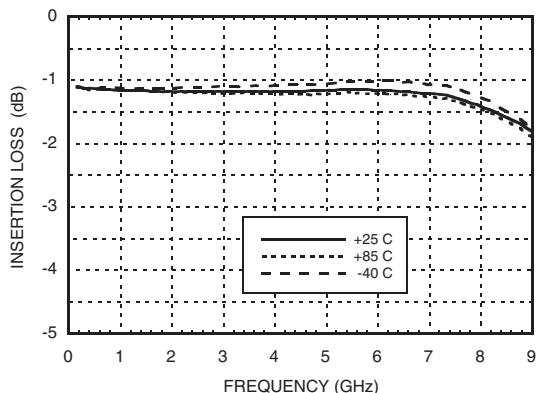
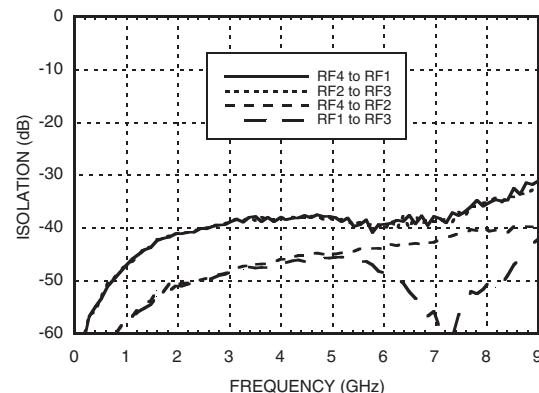
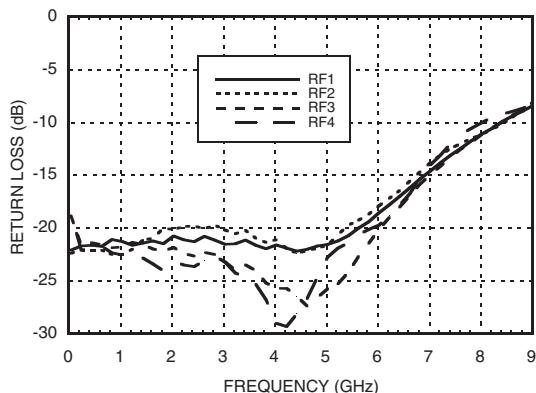
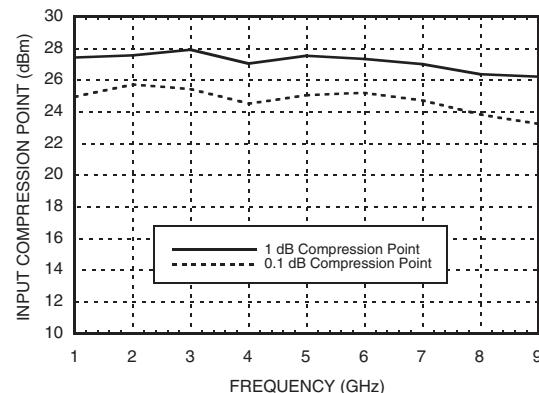
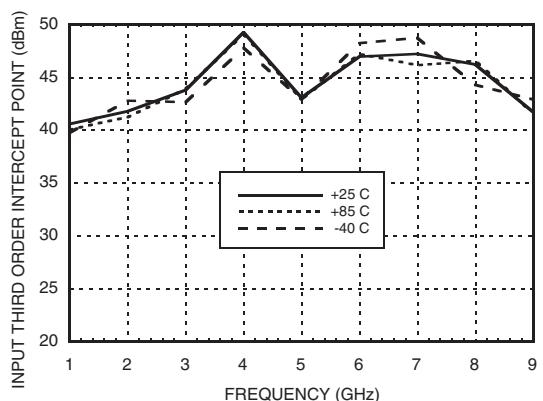
General Description

The HMC427LP3 & HMC427LP3E are low loss broadband positive control transfer switches in leadless surface mount packages. Covering DC to 8 GHz, this switch offers high isolation and low insertion loss. The switch operates using a positive control voltage of 0/+5V and requires a fixed bias of +5V @ < 20 μ A.

* Blocking capacitors are required at ports RF1, 2, 3, & 4. Their value will determine the lowest transmission frequency.

Electrical Specifications, $T_A = +25^\circ C$, With 0/+5V Control, 50 Ohm System

| Parameter | Frequency | Min. | Typ. | Max. | Units |
|--|--|----------------------|----------------------|------------|----------------------|
| Insertion Loss | DC - 6.0 GHz DC - 8.0 GHz | | 1.2 1.6 | 1.6 2.1 | dB dB |
| Isolation | DC - 1.0 GHz DC - 2.0 GHz DC - 6.0 GHz DC - 8.0 GHz | 42 37 33 27 | 48 42 38 32 | | dB dB dB dB |
| Return Loss | DC - 6.0 GHz DC - 8.0 GHz | | 17 15 | | dB dB |
| Input Power for 1 dB Compression | 1.0 - 8.0 GHz | 23 | 26 | | dBm |
| Input Third Order Intercept (Two-Tone Input Power= +7 dBm Each Tone, 1 MHz Tone Separation) | 1.0 - 8.0 GHz | 37 | 43 | | dBm |
| Switching Characteristics tRISE, tFALL (10/90% RF) tON, tOFF (50% CTL to 10/90% RF) | DC - 8.0 GHz | | 2 4 | | ns ns |


Insertion Loss vs. Temperature

Isolation

Return Loss

0.1 and 1 dB Input Compression Point

Input Third Order Intercept Point



Absolute Maximum Ratings

| | |
|-------------------------------|-----------------------|
| Bias Voltage Range (Vdd) | +7.0 Vdc |
| Control Voltage Range (A & B) | -0.5V to Vdd +1.0 Vdc |
| Channel Temperature | 150 °C |
| Thermal Resistance | 130 °C/W |
| Storage Temperature | -65 to +150 °C |
| Operating Temperature | -40 to +85 °C |
| Maximum Input Power | +27 dBm |
| ESD Sensitivity (HBM) | Class 1A |


**ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS**
Note:

DC blocking capacitors are required at ports RF1, 2, 3, & 4. Their value will determine the lowest transmission frequency.

Bias Voltage & Current

| Vdd Range = +5.0 Vdc ± 10 % | | |
|-----------------------------|-----------------|-----------------|
| Vdd (Vdc) | Idd (Typ.) (µA) | Idd (Max.) (µA) |
| +5.0 | 5 | 10 |

Control Voltages

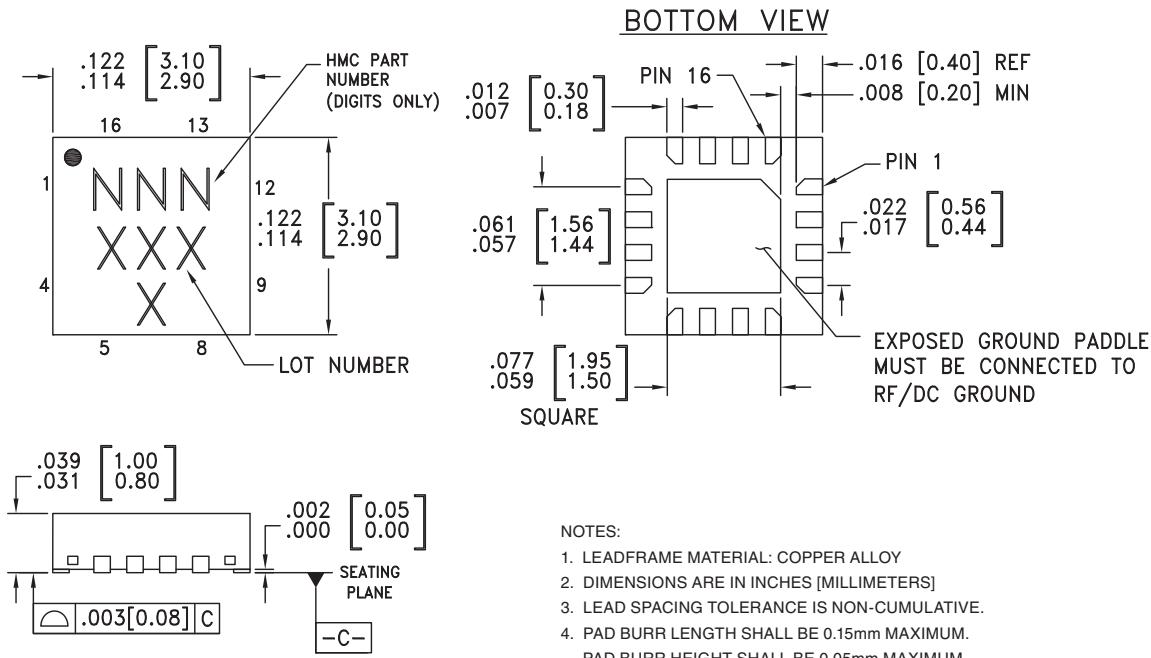
| State | Bias Condition |
|-------|------------------------------|
| Low | 0 to +0.2 Vdc @ 5 µA Typical |
| High | Vdd ± 0.2 Vdc @ 5 µA Typical |

Truth Table

| Control Input | | Signal Path State | | | |
|---------------|------|-------------------|------------|------------|------------|
| A | B | RF4 to RF2 | RF1 to RF3 | RF4 to RF1 | RF2 to RF3 |
| Low | High | On | On | Off | Off |
| High | Low | Off | Off | On | On |



Outline Drawing



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM.
PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE
SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED
LAND PATTERN.

Package Information

| Part Number | Package Body Material | Lead Finish | MSL Rating | Package Marking ^[3] |
|-------------|--|---------------|---------------------|--------------------------------|
| HMC427LP3 | Low Stress Injection Molded Plastic | Sn/Pb Solder | MSL1 ^[1] | 427 XXXX |
| HMC427LP3E | RoHS-compliant Low Stress Injection Molded Plastic | 100% matte Sn | MSL1 ^[2] | 427 XXXX |

[1] Max peak reflow temperature of 235 °C

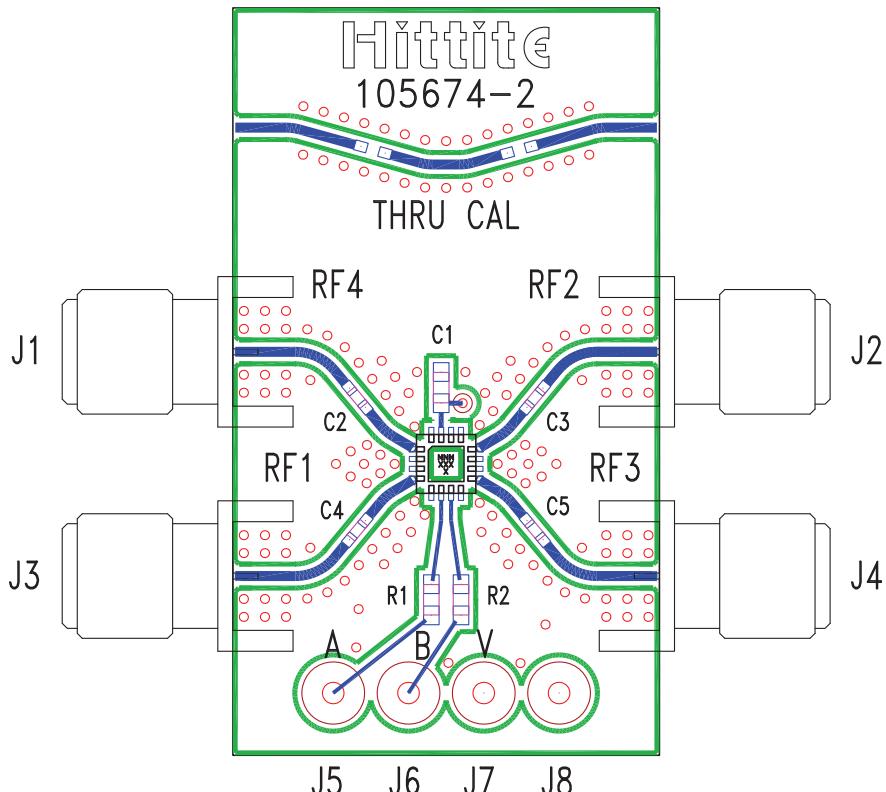
[2] Max peak reflow temperature of 260 °C

[3] 4-Digit lot number XXXX



Pin Descriptions

| Pin Number | Function | Description | Interface Schematic |
|--------------------------------|--------------------|--|---------------------|
| 1, 4, 9, 12 | RF4, RF1, RF3, RF2 | This pin is DC coupled and matched to 50 Ohm. Blocking capacitors are required. | |
| 2, 3, 5, 8, 10, 11, 13, 14, 16 | N/C | This pin should be connected to PCB RF ground to maximize isolation. | |
| | GND | Package bottom has exposed metal paddle that must be connected to PCB RF ground. | |
| 6 | CTRLA | See truth table and control voltage table. | |
| 7 | CTRLB | See truth table and control voltage table. | |
| 15 | VDD | Supply Voltage +5V ± 10%. | |


Evaluation PCB

List of Materials for Evaluation PCB 105672 [1]

| Item | Description |
|---------|--|
| J1 - J4 | PCB Mount SMA RF Connector |
| J5 - J8 | DC Pin |
| C1 | 1000 pF Capacitor, 0603 Pkg. |
| C2 - C5 | 100 pF Capacitor, 0402 Pkg. |
| R1 - R2 | 100 Ohm Resistor, 0603 Pkg. |
| U1 | HMC427LP3 / HMC427LP3E Transfer Switch |
| PCB [2] | 105674 Evaluation PCB |

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should be generated with proper RF circuit design techniques. Signal lines at the RF port should have 50 ohm impedance and the package ground leads and package bottom should be connected directly to the ground plane similar to that shown above. The evaluation circuit board shown above is available from Hittite Microwave Corporation upon request.

Mouser Electronics

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