AN-1363
APPLICATION NOTE

Meeting Biasing Requirements of Externally Biased RF/Microwave Amplifiers with Active Bias Controllers
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INTRODUCTION

Radio frequency (RF) and microwave amplifiers provide their best performance under specific bias conditions. The quiescent current established by the bias point affects critical performance metrics such as linearity and efficiency. While some amplifiers are self biased, many devices require external biasing using multiple supplies that must be sequenced properly for safe operation.

This application note provides an overview of bias sequencing requirements and the effects of using various bias conditions. It presents an elegant solution for biasing amplifiers using active bias controller such as the HMC980, HMC980LP4E, HMC981, HMC981LP3E, HMC920LP5E, and all externally biased RF/microwave amplifiers.

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REVISION HISTORY

7/2016—Revision 0: Initial Version

BIASED AMPLIFIERS

POWER SUPPLY SEQUENCING

Power supply sequencing is critical while operating externally biased amplifiers for the following reasons:

- Failing to follow the proper power supply sequencing compromises the reliability of the device. Exceeding breakdown voltage levels can result in instant failure. Long term reliability degrades when out of bond conditions are repeated multiple times, and the system is stressed. In addition, continually violating the sequencing pattern damages the on-chip protection circuitry and results in long term damage, which can result in a failure in the field operation.

- Optimizing the bias level not only during power up and power down but also during regular operation can improve the performance of the RF amplifier, depending on the configuration and the application requirements. For some applications, changes can be made to the RF performance of the amplifier to comply with different field scenarios. For example, the output power can be increased for wider coverage during rainy weather, or the output power can be reduced during clear weather. The external gate control of the amplifier can implement these arrangements.

Analog Devices, Inc., has a wide selection of RF amplifier types. Many RF amplifiers are based on a depletion mode, pseudo-morphic, high electron mobility transfer (pHEMT) technology. The transistors used in this process typically require supplies for the drain pins and gate pins. This quiescent drain current is a function of the gate voltage. See Figure 1 for the typical IV characteristics of a typical field effect transistor (FET) process.
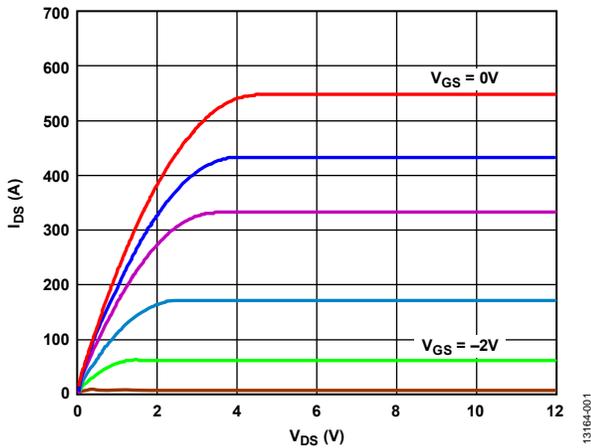
Figure 1. Typical IV Characteristics of a Typical FET Process

As the gate to source voltage (V_{GS}) increases, more electrons enter the channel, resulting in a higher drain to source current (I_{DS}).

Additionally, as the drain to source voltage (V_{DS}) increases, the drain to source current also increases (in the linear region) due to the higher field force pulling the electrons.

In real-world amplifiers, due to effects like channel length modulation, these amplifiers can be broadly categorized into two categories: self biased and externally biased amplifiers.

SELF BIASED AMPLIFIERS

Self biased amplifiers have an internal circuit that sets the optimal bias point suitable for operation. These amplifiers tend to be best suited for broadband, low powered applications. See Figure 2 for a typical pinout of a self biased amplifier.
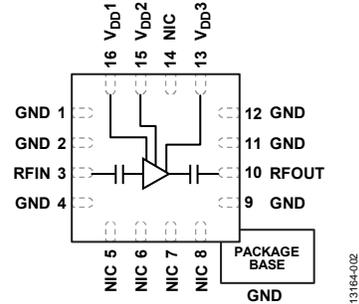
Figure 2. Typical Pinout for a Multistage Self Biased Amplifier with Multiple Bias Pins

While self biased amplifiers are simple to use, they may not provide the best performance because the internal resistive bias circuit cannot fully compensate for lot, device, and temperature variations.

EXTERNALLY BIASED AMPLIFIERS

Externally biased amplifiers tend to provide higher performance than self biased amplifiers under specific bias conditions. The quiescent drain current of the amplifier affects parameters such as power compression point, gain, noise figure, intermodulation products, and efficiency. For these high performance externally biased amplifiers, correctly sequencing the supplies is crucial for safe and optimal performance.

This procedure also applies to other radio frequency integrated circuits (RFICs), such as frequency multipliers, upconverters, and downconverters. These products can require similar biasing techniques. Table 1 lists externally biased RF products from various product families.

Table 1. Externally Biased RF Devices

Device Number	Product Family
HMC1082LP4E	Driver amplifier/medium power amplifier
HMC1049 Bare Die	Low noise amplifier
HMC7357LP5GE	Power amplifier
HMC463	Wideband distributed amplifier
HMC996LP4E	Variable gain amplifier
HMC598	Frequency multiplier chip
HMC1065LP4E	Downconverter
HMC6787ALC5A	Upconverter
HMC871LC5	Optical modulator driver

Figure 3 shows the typical connections for the pins of an externally biased amplifier and the corresponding transistor pins. The pin mapping in Figure 3 is a simplified representation of the amplifier.
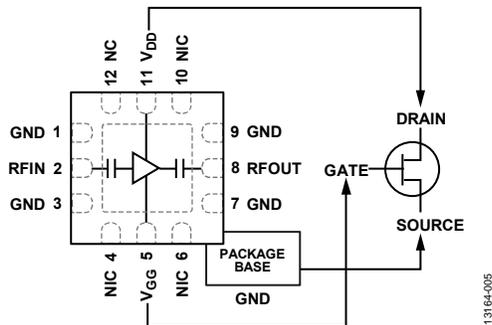

Figure 3. Typical Connections of an Externally Biased Amplifier

Furthermore, many externally biased amplifiers have multiple stages to meet design requirements such as gain, bandwidth, and power. Figure 4 shows a typical block diagram of the HMC1131, which is a multistage externally biased amplifier.
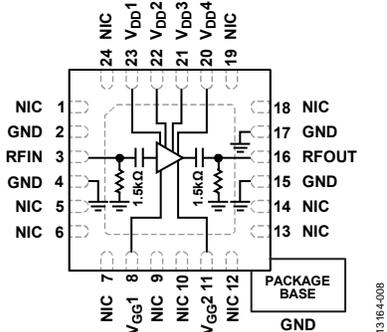

Figure 4. HMC1131 Multistage Externally Biased Amplifier

HMC1131 Biasing and Sequencing Requirements

The HMC1131 is a gallium arsenide (GaAs), pHEMT, monolithic microwave integrated circuit (MMIC), medium power amplifier. It operates from 24 GHz to 35 GHz. The 4-stage design typically provides a 22 dB gain, 23 dBm output power for 1 dB compression (P1dB), and 27 dBm saturated output power (P_{SAT}) under the bias conditions of V_{DD} = 5 V and I_{DQ} = 225 mA, where V_{DD} is the drain bias voltage and I_{DQ} is the quiescent drain current. The electrical specifications table of the HMC1131 data sheet, for the 24 GHz to 27 GHz frequency range, gives this information. Figure 4 shows the pin connections of the HMC1131.

To achieve a target quiescent drain current (I_{DQ}) of 225 mA, set the voltage of the gate bias pins ($V_{GG}1$ and $V_{GG}2$) between 0 V and −2 V. To set that negative voltage without damaging the amplifier, follow the recommended biasing sequence during power up and power down.

The recommended bias sequence during power up for the HMC1131 is the following:

1. Connect to ground.
2. Set $V_{GG}1$ and $V_{GG}2$ to −2 V.
3. Set $V_{DD}1$ through $V_{DD}4$, the drain voltage bias pins, to 5 V.
4. Increase $V_{GG}1$ and $V_{GG}2$ to achieve an I_{DQ} of 225 mA.
5. Apply the RF signal

The recommended bias sequence during power down for the HMC1131 is the following:

1. Turn the RF signal off.
2. Decrease $V_{GG}1$ and $V_{GG}2$ to −2 V to achieve an I_{DQ} of approximately 0 mA.
3. Decrease $V_{DD}1$ through $V_{DD}4$ to 0 V.
4. Increase $V_{GG}1$ and $V_{GG}2$ to 0 V.

When the gate voltage ($V_{GG}x$) is −2 V, the transistors are pinched off. Therefore, I_{DQ} is typically close to zero.

In general, the recommended biasing sequence is similar for most externally biased amplifiers. I_{DQ}, $V_{DD}x$, and $V_{GG}x$ values are different for different devices. For GaAs devices, V_{GG} is generally set to −2 V or −3 V to turn off the amplifier, while that voltage can be −5 V to −8 V for gallium nitride (GaN) amplifiers. Similarly, $V_{DD}x$ can reach 28 V, even 50 V, for GaN devices, while it is usually less than 13 V for GaAs amplifiers.

In general, for multistage amplifiers, the V_{GG} pins are connected and biased together. By following the same procedure, a user can get the typical performance results provided on the data sheet. Operating the amplifier under different bias conditions may provide different performance. For instance, using a different $V_{GG}x$ level for the HMC1131 gate bias pins to obtain various I_{DQ} values changes the RF and dc performance of the amplifier.

Figure 5 shows the P1dB vs. the frequency at various supply currents, and Figure 6 shows the output third order intercept (IP3) performance vs. the frequency at various supply currents for the HMC1131.
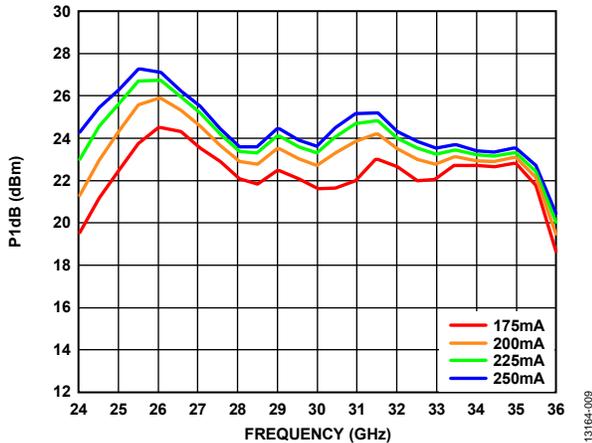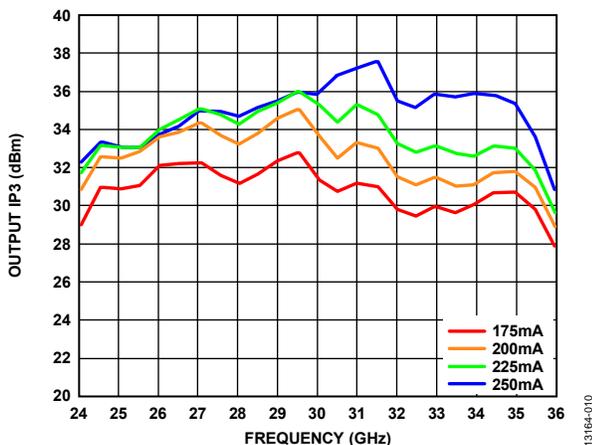
Figure 5. P1dB vs. Frequency at Various Supply Currents

Figure 6. Output IP3 vs. Frequency at Various Supply Currents, P_{OUT}/Tone = 10 dBm

Another option for biasing amplifiers with multiple $V_{GG}x$ pins is to control the gate bias pins independently. This operation mode helps users customize device performance by optimizing specific parameters such as P1dB, IP3, NF, gain, and power consumption.

This flexibility is useful for some applications. If the performance data of an amplifier provided on the data sheet meets some requirements of the application easily, yet misses others by a small margin, testing the performance under different bias conditions can be advantageous without exceeding the absolute maximum ratings given in the data sheet.

Another option for biasing externally biased amplifiers, is setting $V_{GG}x$ for the desired I_{DQ} of 225 mA and using a constant gate voltage during normal operation. In this case, the I_{DD} of the amplifier increases under the RF drive. This behavior is shown in the power compression at 30.5 GHz in the HMC1131 data sheet (see the orange line). The performance of the amplifier with constant gate voltage and with constant I_{DD} can be different.

CASCODE AMPLIFIERS

Analog Devices wideband distributed amplifiers often use a cascode architecture to extend the frequency range. The cascode distributed amplifier uses a fundamental cell of two FETs in series, source to drain. This fundamental cell is then duplicated a number of times. This duplication increases the operation bandwidth. Figure 7 shows a simplified schematic for a fundamental cell.
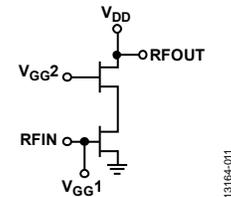
Figure 7. Simplified Fundamental Cascode Cell Schematic

With some exceptions, the cascode wideband amplifiers are externally biased.

The HMC637A is a wideband amplifier that uses cascode topology. The HMC637A is a GaAs, MMIC, metal semiconductor field effect transistor (MESFET) distributed power amplifier that operates between dc and 6 GHz. Figure 8 shows the pin connections for the HMC637A.

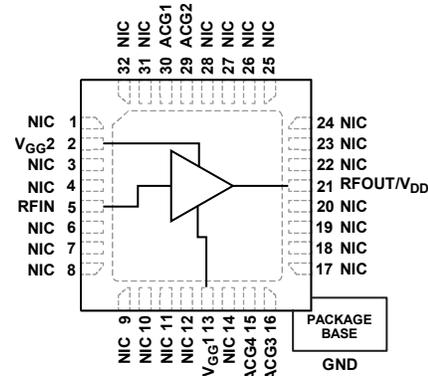*Figure 8. HMC637A Pin Connections*

The amplifier provides 14 dB of gain, 43 dBm of output IP3, and 30.5 dBm of output power at a 1 dB gain compression under the bias conditions of V_{DD} = 12 V, $V_{GG}2$ = 6 V, and I_{DQ} = 400 mA. The electrical specifications table of the HMC637A data sheet provides this information.

To achieve the recommended quiescent drain current of 400 mA, $V_{GG}1$ must be somewhere between 0 to −2 V. To set the desired negative voltage, follow the recommended bias sequence during power up and power down.

The recommended bias sequence for the HMC637A during power up follows:

1. Connect to ground.
2. Set $V_{GG}1$ to −2 V.
3. Set V_{DD} to 12 V.
4. Set $V_{GG}2$ to 6 V ($V_{GG}2$ can be obtained by a resistive divider from V_{DD}).
5. Increase $V_{GG}1$ to achieve a typical quiescent current (I_{DQ}) of 400 mA.
6. Apply the RF signal.

The recommended bias sequence for the HMC637A during power down follows:

1. Turn off the RF signal.
2. Decrease $V_{GG}1$ to −2 V to achieve I_{DQ} = 0 mA.
3. Decrease $V_{GG}2$ to 0 V.
4. Decrease V_{DD} to 0 V.
5. Increase $V_{GG}1$ to 0 V.

USING ACTIVE BIAS CONTROLLERS TO BIAS EXTERNALLY BIASED AMPLIFIERS

There are two major approaches for biasing externally biased amplifiers:

- Constant gate voltage approach. In this approach, the gate voltage value is varied to achieve the desired I_{DQ} value. This gate voltage value is then kept constant during operation, which typically results in a variable drain current (I_{DD}) under the RF drive.
- Constant I_{DD} approach. In this approach, the gate voltage value is varied to achieve the desired I_{DQ} value, then the I_{DD} value of the amplifier is monitored, and the gate voltage value is adjusted constantly to have the same I_{DD} value for different RF drive levels. Active bias controllers keep the I_{DD} of the device under test (DUT) constant.

Another approach, a subset of the constant I_{DD} approach, consists of following the constant I_{DD} approach and switching in between multiple constant I_{DD} levels when necessary due to various field scenarios. For instance, a user can bias a power amplifier stage of a transmitter for high current levels during rainy weather to compensate for the additional rain attenuation. Similarly, a user can bias the same power amplifier for low current levels during clear weather to reduce the power consumption.

In general, Analog Devices RF amplifiers are characterized with a constant gat voltage approach, using bench top power supply units. Therefore, biasing those amplifiers with the constant I_{DD} approach can result in different RF performance than what is given on the amplifier data sheet.

Designing bias circuits for amplifiers to keep the drain current constant and provide necessary sequencing can be cumbersome. Such control circuits are complicated and require not only multiple external components such as low drop out regulators (LDOs), charge pumps, voltage sequencing, and protection circuits, but also calibration cycles. Such implementations occupy a large printed circuit board (PCB) area that is usually much larger than the amplifier itself.

The HMC920LP5E houses all the necessary operation blocks in a compact 5 mm × 5 mm plastic surface-mount technology (SMT) package. By eliminating multiple IC and external component requirements, this compact size results in reduced PCB area compared to the discrete biasing implementations.

Similar to the HMC920LP5E, active bias controllers require less PCB space than discrete transistor solutions. When using the HMC980LP4E, bias sequencing, constant gate voltage adjustment, short-circuit protection, and negative voltage generation features are implemented within 10 mm × 15 mm of PCB space.

The HMC981LP3E, HMC980LP4E, and HMC920LP5E are 3 mm × 3 mm, 4 mm × 4 mm, and 5 mm × 5 mm plastic packaged active bias controllers, respectively. Figure 9 shows the PCB area required for a typical application, including external passive components.
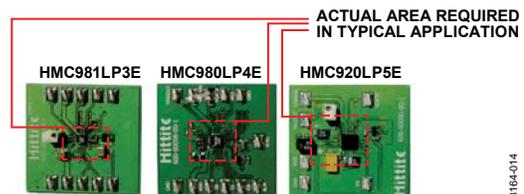

Figure 9. PCB Area Required in Typical Application

The Analog Devices active bias controller family offers some key advantages:

- Internal negative voltage generators generate the negative voltage at the VGATE pin required for externally biased amplifiers. These generators eliminate the need for voltage inverters and reduce the device count, the PCB space, and, as a result, the system cost.
- Continuous internal gate voltage adjustment ensures a constant DUT drain current.
- Bias accuracy improves due to the reduction of device to device variation effects. The optimum gate voltage level required to obtain a desired I_{DD} for different amplifiers with the same device number is different due to device to device variation. Therefore, setting the gate voltage to the same value for separate DUTs results in a different RF performance. Active bias controllers adjust the gate voltage level separately for each individual DUT and reduce the performance difference introduced by device to device variation.

Figure 10 and Figure 11 show this reduction on device to device variation effects.
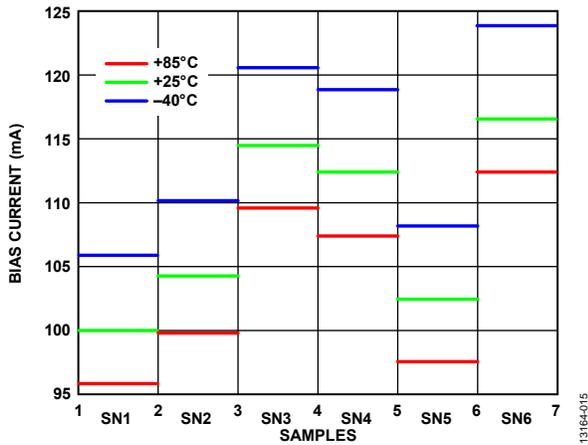

Figure 10. Bias Current Variation of a Typical Amplifier Under Fixed External VGATE Bias
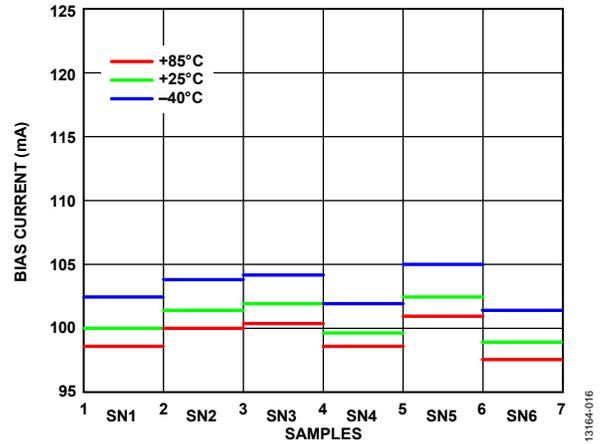

Figure 11. Improved Bias Current Variation of Same Amplifier when Biased with the HMC920LP5E

- Internal bias sequencing circuitry ensures that positive voltages on the VDRAIN pin and the VG2 pin are not supplied to the DUT when the negative VGATE voltage is not present. This feature eliminates the external components used for sequencing during DUT power up and power down.

- Short-circuit protection circuitry disables the VDRAIN pin after the VGATE pin and therefore makes sure that the DUT is safe, even under short circuit conditions.
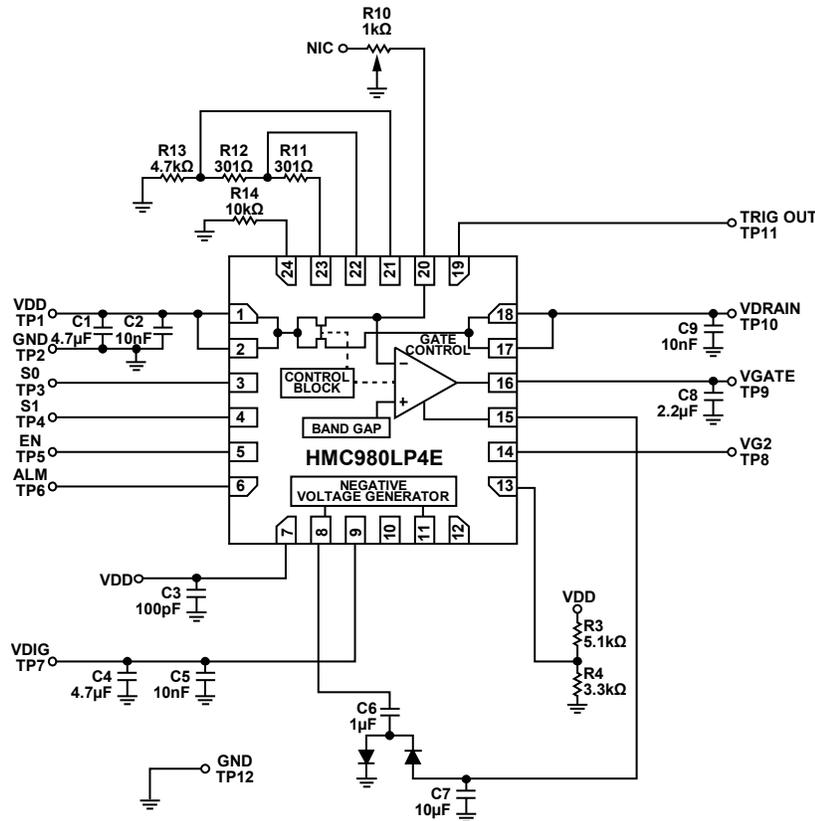
Figure 12. Typical Application Circuit for the HMC980LP4E

Table 2. Selected Features of Active Bias Controllers

Device Number	Supply Range (V)	VDRAIN (V)	IDRAIN (mA)	IGATE (mA)	Over/Under Current Alarm	Short-Circuit Protection	VDRAIN LDO	Negative Voltage Generator
HMC920LP5E	5 to 16.5	3 to 15	0 to 500	−4 to +4	Yes	Yes	Yes	Yes
HMC980LP4E	5 to 16.5	5 to 16.5	50 to 1600	−4 to +4	Yes	Yes	No	Yes
HMC981LP3E	4 to 12	4 to 12	20 to 200	−0.8 to +0.8	No	Yes	No	Yes

With an internal feedback, the automatic gate voltage control achieves a constant quiescent bias current through the amplifier under bias, independent of the temperature and amplifier threshold variations. The quiescent bias current is adjusted with a resistor connected externally. Figure 12 shows the R_{SENSE} resistor (R10) connected to Pin 20 of the HMC980LP4E.

Further details on how to calculate the R_{SENSE} and V_{DD} values can be found on the active bias controller data sheets.

Analog Devices offers three active bias controllers: the HMC920LP5E, HMC980LP4E, and HMC981LP3E. Table 2 details selected features of these active bias controllers.

The HMC980LP4E provides the ability to source high drain currents, while the HMC981LP3E is best suited for devices that require lower drain currents. In addition to the negative voltage generator, the HMC920LP5E integrates a positive voltage regulator, providing the ability to source drain pins.

OPERATING PRINCIPLES

For externally biased amplifiers, Analog Devices data sheets highlight the biasing requirements for V_{GG} and I_{DD} at the bottom of electrical specifications table. For instance, the HMC637A requires its $V_{GG}1$ to be adjusted from −2 V to 0 V to obtain a typical I_{DQ} of 400 mA. However, follow the recommended sequencing during power-up and power-down to avoid damaging the HMC637A.

The HMC980LP4E employs an integrated control circuitry to manage safe power-up and power-down sequencing of the targeted amplifier.

During power up, the VDD and VDIG supplies of the bias controller turn on, and then VNEG generates by the internal negative voltage generator (NVG). VNEG starts to decrease and stops when it reaches its default value (typically −2.46 V). The VGATE output voltage also starts to decrease. Typically, once VNEG = −2.5 V and VGATE = −2.1 V are reached, the VDRAIN output is enabled, and VGATE begins to increase toward 0 V to obtain the desired I_{DD} value for the DUT.

Similar power-down protection circuitry also provides a safe power down for the DUT. During power down, VGATE always shuts down after VDD, even if there is a short circuit on the VDD pins or on the VGG pins of the DUT. This feature introduces advanced protection of the DUT, under excessive DUT I_{DD} current scenarios.
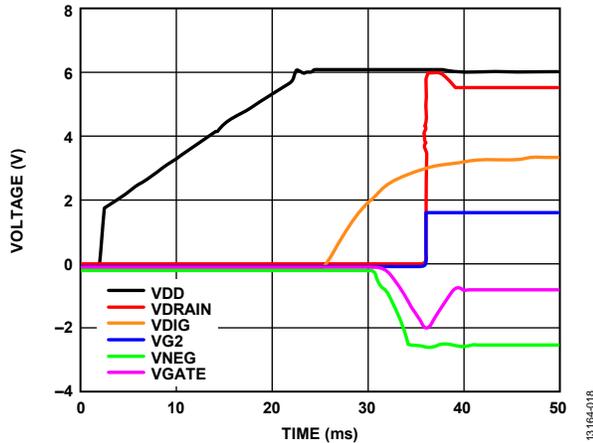

Figure 13. *HMC981LP3E Enabling Sequence for Supply Rails*

ADJUSTING THE DEFAULT VNEG AND VGATE THRESHOLD VALUES

The typical VNEG value is −2.46 V, as seen in Figure 14. Due to the internal logic that exists inside HMC980LP4E, this default value limits the VGATE output voltage swing capabilities of the HMC980LP4E.
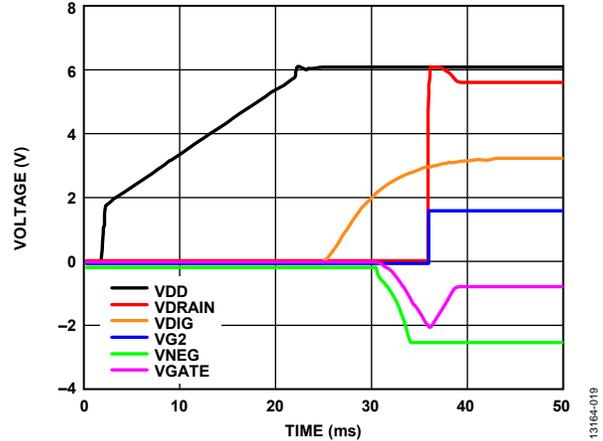

Figure 14. *Default VNEG Value*

With the default configuration, the typical VGATE output swing is in between −2 V and 0 V. However,

- For some DUTs, gate voltages of less than −2 V are necessary.
- Some DUTs have a gate voltage absolute maximum rating (AMR) that is greater than −2.1 V, such as −1.5 V. In such a case, the DUT is expected to have a typical gate voltage higher than the AMR value of VGATE, such as −1 V. During the power up, however, the VGATE output of the HMC980LP4E always reduces to a typical value of −2 V.

Adjusting the default values of VNEG and VGATE by external resistors solves both of these problems. The R5, R6, R7, and R8 resistors shown in Figure 15 are used for this purpose.
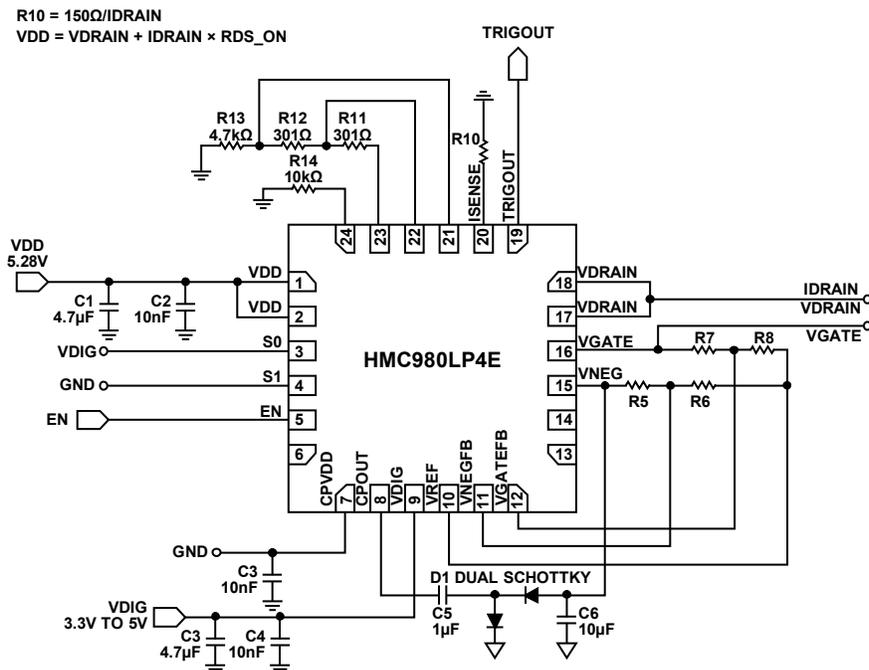

Figure 15. *External Resistors for Adjusting Default VNEG and VGATE Values*

If the desired VNEG < −2.46 V, then R5 (kΩ) = open, and R6 (kΩ) = 50/(50 × (Desired VNEG − 0.815)/(262 × (0.815 − 1.44)) − 1).

If the desired VNEG > −2.46 V, then R5 (kΩ) = 262/(262 × (1.44 − 0.815)/(50 × (0.815 − Desired VNEG)) − 1), and R6 (kΩ) = open.

If the desired VGATE < −2.46 V, then R7 (kΩ) = open, and R8 (kΩ) = 50/(50 × (Desired VGATE − 0.815)/(262 × (0.815 − 1.44)) − 1).

If the desired VGATE > −2.46 V, then R7 (kΩ) = 262/(262 × (1.44 − 0.815)/(50 × (0.815 − Desired VGATE)) − 1), and R8 (kΩ) = open.

During power up, VNEG is enabled if VNEG reaches a default value of −2.46 V; therefore, the VNEG value must be less than the VGATE value.

It is recommended to configure the HMC980LP4E for VNEG values greater than −3.5 V.

For example, if the desired VNEG = −1.5 V and VGATE = −1.3 V, R5 = 631 kΩ, R7 = 477 kΩ, and R6 = R8 = open. In addition, if the desired VNEG = −3.2 V and VGATE = −3 V, R6 = 221 kΩ, R8 = 303 kΩ, and R5 = R7 = open.

REDUCING VGATE RISE TIME

A delay exists between the moment that the enable signal reaches the enable pin of the active bias controller and the moment that the VGATE voltage level at the DUT VGATE input pin settles to the desired value. This delay is due to the combination of the internal propagation delay of the bias controller and the settling time of the VGATE signal. The VGATE settling time is affected by the shunt capacitors used on the connection between the active bias controller VGATE output and the DUT VGATE input pin. The HMC980LP4E typical enable waveform (see Figure 16) shows a VGATE settling time greater than 1 ms.
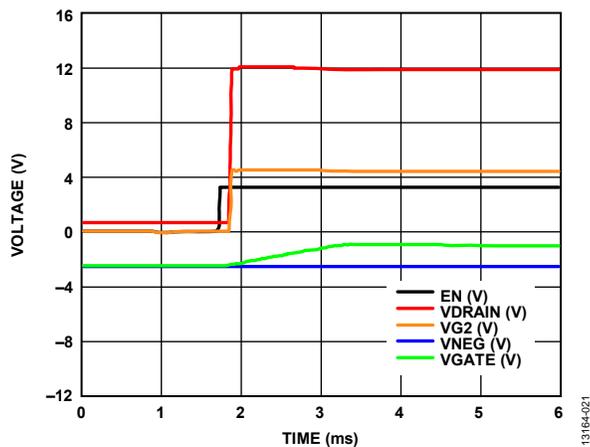
Figure 16. HMC980LP4E Typical Enable Waveform

The external circuit affects the gate rise time but not the propagation delay. Figure 17 shows a typical VGATE connection between the HMC980LP4E and a DUT amplifier. Generally, the shunt capacitor, C1, is used on the VGG pins of the amplifiers, where R1 is usually 0 Ω, that is, not used.
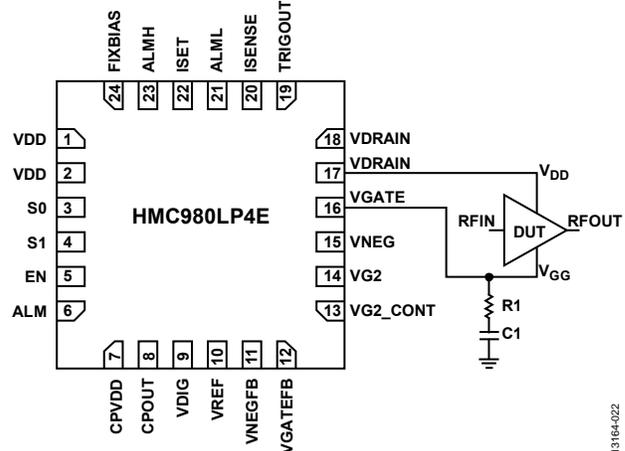
Figure 17. VGATE Connection Circuitry Between the HMC980LP4E and the DUT

When C1 = 10 µF, the typical rise time is greater than 1.5 ms (see Figure 18). Reducing C1 to 1 µF reduces the rise time to 131 µs (see Figure 19).
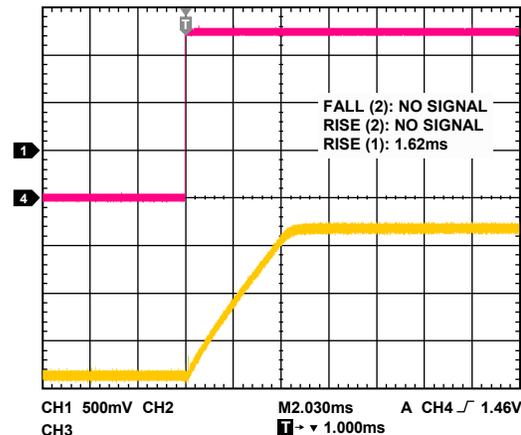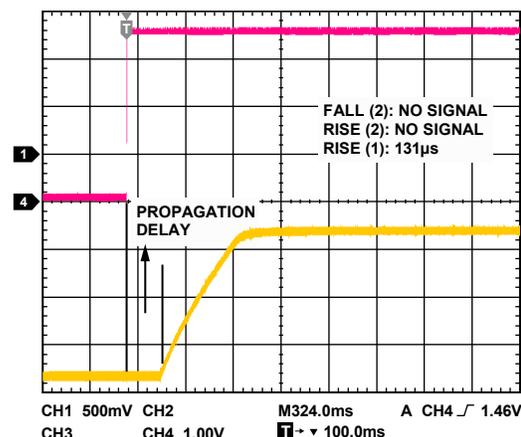
Figure 18. Typical VGATE Rise Time with C1 = 10 µF

Figure 19. Typical VGATE Rise Time with C1 = 1 µF

When C1 = 100 nF, the VGATE rise time is reduced to 15.5 μs, but overshooting introduces ringing (see Figure 20). Adding a series resistor, R1, with a value of 68 Ω to C1 = 100 nF improves the response and keeps the rise time within a similar level (see Figure 21).
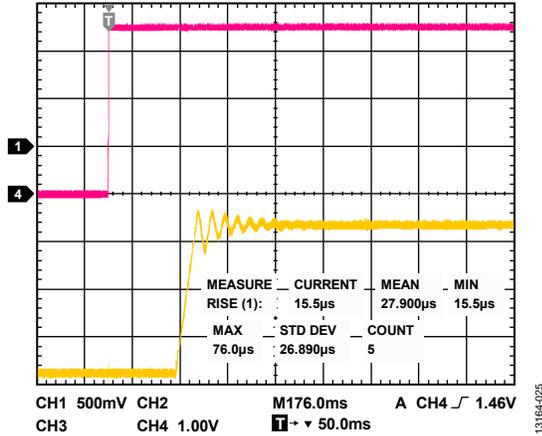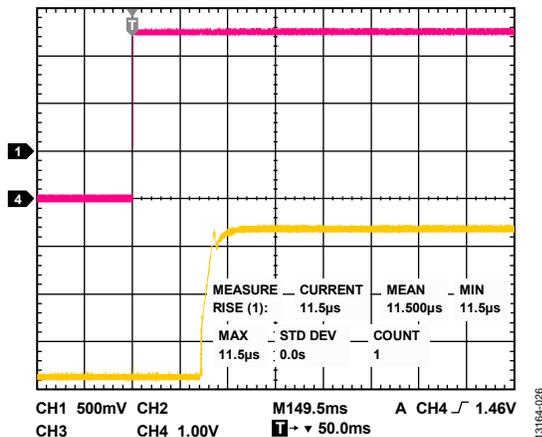

Figure 20. Typical VGATE Rise Time with C1 = 100 nF

Figure 21. Typical VGATE Rise Time with C1 = 100 nF and R1 = 68 Ω

DAISY-CHAIN CONFIGURATION

When multiple active bias controllers bias multiple DUTs, they can be used in a daisy-chain configuration. The TRIGOUT output of the active bias controller generates when the VDRAIN, VG2, and VGATE outputs settle. Using the TRIGOUT signal to enable another bias controller with the enable pin (EN) improves the system safety level. A daisy-chain configuration has many applications, Figure 22 and Figure 23 show two applications. The number of DUT stages and bias controllers can be increased.
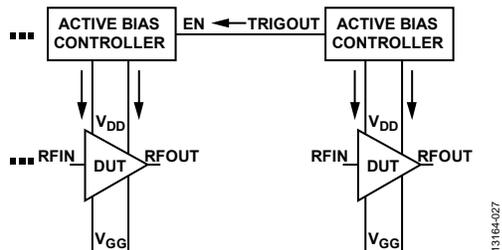
Figure 22. Daisy-Chain Configuration with Two Amplifiers in Cascade Configuration
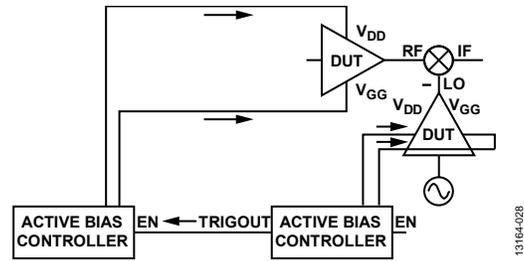
Figure 23. Daisy-Chain Configuration Where DUT Amplifiers Are on Different Signal Paths

Figure 24 shows the VDRAINx and VGATEx responses of two active bias controllers in a daisy-chain configuration, powering two DUTs individually. The second bias controller enables by the trigger signal sourced from the first bias controller. This architecture ensures that the second DUT enables after the first DUT.
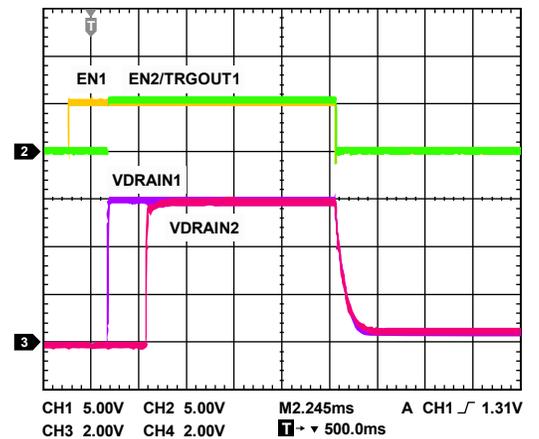
Figure 24. VDRAINx Responses of Two Active Bias Controllers in a Daisy-Chain Configuration, Powering Two DUTs Individually
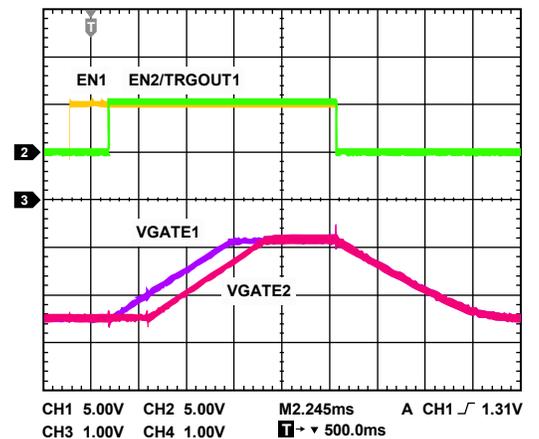
Figure 25. VGATEx Responses of Two Active Bias Controllers in a Daisy-Chain Configuration, Powering Two DUTs Individually

TESTING THE FUNCTIONALITY OF THE ACTIVE BIAS CONTROLLER

The VDRAIN and VGATE outputs of active bias controllers can bias a DUT, such as an FET or an amplifier with external biasing requirements. Once the DUT is connected to the bias controller, the feedback loop is closed and the bias controller becomes operational.

Because the loop does not close, it is not feasible to test the functionality of an active bias controller with a fixed load, like a resistor.

Although testing active bas controllers without a DUT does not provide useful information, perform the following diagnostic checks.

- IDD = 0 mA results in a negligible voltage drop across the V_{DD} input and VDRAIN output; therefore, VDRAIN is almost equal to V_{DD}.
- VNEG is typically −2.46 V.
- VGATE hits a maximum value of VNEG + 4.5 V, which is typically 2.04 V.

For other bias controllers, these values can be extracted from their data sheets.

BIASING MULTIPLE DUTS BY A SINGLE ACTIVE BIAS CONTROLLER

It is possible to bias two or more DUTs by a single active bias controller. To do so, calculate the RSENSE value considering the total drain current of the DUTs.

Note, however, that using this approach limits the benefits that an active bias controller offers for the following reasons:

- An active bias controller is not able to compensate device-to-device gate voltage variation that is common with GaAs devices. As a result, two devices can be biased using one gate voltage, resulting in nonoptimal performance.
- If one of the DUTs draws excessive current due to a short circuit or other terms of failure, the bias controller shuts down all DUTs under bias. Although this does not damage the devices, it compromises system functionality.

SAMPLE ACTIVE BIAS CONTROLER APPLICATION CIRCUITS

Biasing the HMC460LC5 with the HMC981LP3E

To bias the HMC460LC5 with the HMC981LP3E, do the following:

- Set R10 to 426 Ω to set I_{DD} = 75 mA for the HMC981LP3E. A common resistor value of 430 Ω can be used.
- Calculate a V_{DD} value of 8.75 V.
- Use R4 and R6 to ensure that the VGATE voltage is within the Absolute Maximum Ratings section of the HMC981LP3E data sheet. Refer to the Adjusting the Default VNEG and VGATE Threshold Values section for details.
- The shunt V_{GG} capacitor values can be reduced to increase the rise time (see HMC460LC5 in Figure 26). Refer to the Reducing VGATE Rise Time section for further details.

Figure 26. Application Circuit for Biasing the HMC460LC5 with the HMC981LP3E

Biasing the HMC1082LP4E with the HMC980LP4E

To bias the HMC1082LP4E with the HMC980LP4E, do the following:

- Set R10 to 680 Ω to set I_{DD} = 220 mA for the HMC980LP4E
- Calculate a V_{DD} value of 5.62 V.

- Use R5 and R7 to ensure that the VGATE voltage is within the Absolute Maximum Ratings section of the HMC980LP4E data sheet. Refer to the Adjusting the Default VNEG and VGATE Threshold Values section for details.
- The shunt V_{GG} capacitor values can be reduced to increase the rise time (see HMC1082LP4E in Figure 27). Refer to the Reducing VGATE Rise Time section for further details.

Figure 27. Application Circuit for Biasing the HMC1082LP4E with the HMC980LP4E

Biasing the HMC659LC5 with the HMC980LP4E

To bias the HMC659LC5 with the HMC980LP4E, do the following:

- Set R10 to 500 Ω to set I_{DD} = 300 mA for the HMC980LP4E.
- Use a common resistor value of 510 Ω.
- Calculate a V_{DD} value of 8.84 V.
- Use R3 and R4 to set $V_{GG}2$ for the HMC980LP4E.

- Use R5 and R7 to ensure that the VGATE voltage is within the Absolute Maximum Ratings section of the HMC980LP4E data sheet. Refer to the Adjusting the Default VNEG and VGATE Threshold Values section for further details.
- The shunt V_{GGx} capacitors value can be reduced to increase the rise time (see HMC659LC5 in Figure 28). Refer to the Reducing VGATE Rise Time section for further details.

Figure 28. Application Circuit for Biasing the HMC659LC5 with the HMC980LP4E

Biasing the HMC659LC5 with the HMC920LP5E

To bias the HMC659LC5 with the HMC920LP5E, do the following:

- Set R_{SENSE} to 549 Ω to set I_{DD} = 300 mA for the HMC920LP5E.
- Set R8 to 30.9 kΩ to set VDRAIN = 8 V.

- Use R20 and R22 to ensure that the VGATE voltage is within the Absolute Maximum Ratings section of the HMC920LP5E data sheet. Refer to the Adjusting the Default VNEG and VGATE Threshold Values section for details.
- The shunt V_{GGx} capacitor values can be reduced to increase the rise time (see HMC659LC5 in Figure 29). Refer to the Reducing VGATE Rise Time section for further details.

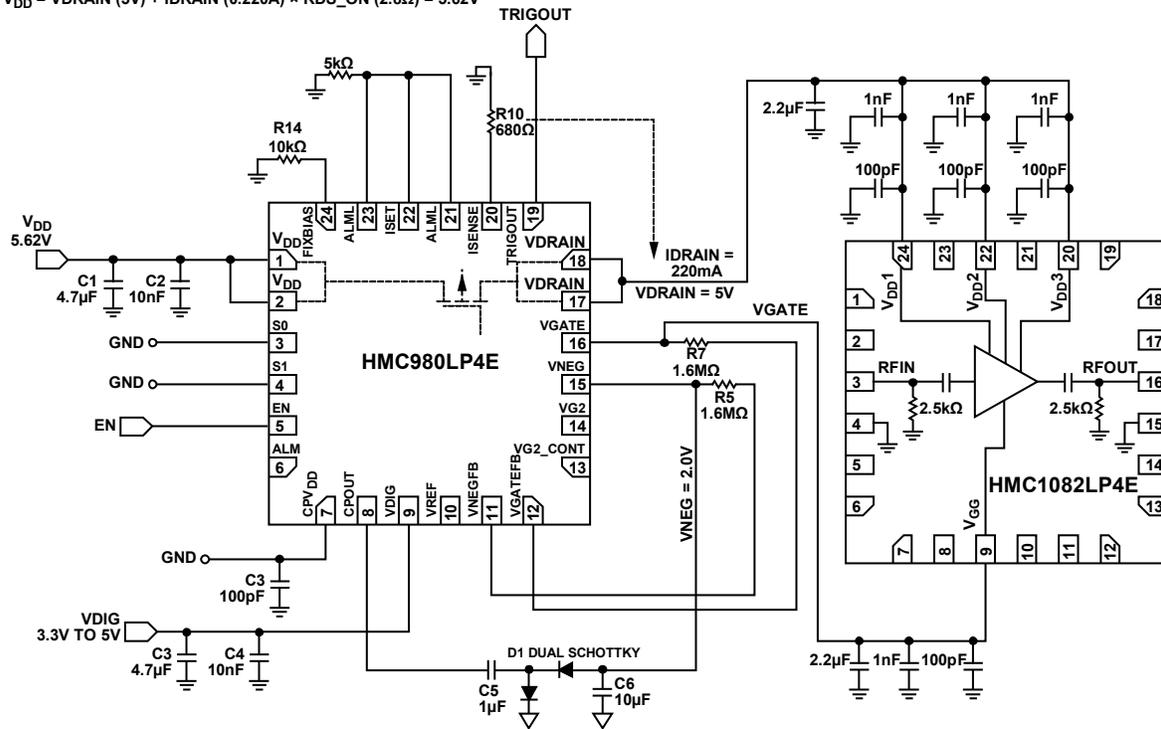*Figure 29. Application Circuit for Biasing the HMC659LC5 with the HMC920LP5E*

CONCLUSION

Follow the recommended biasing sequence for externally biased devices during power-up and power-down to ensure the safety of the device. Operating amplifiers with an active bias controller ensures that the device is sequenced properly and at the desired level, improving overall system performance.

The active bias controller family from Analog Devices can address the biasing requirements of externally biased RF/microwave components, such as FETs, amplifiers, multipliers, optical modulator drivers, and frequency converters. The gate voltages of the DUTs are adjusted with a closed feedback loop for the desired drain current. The sequencing feature of the VGATE, VDRAIN, and VGG2 outputs of the bias controller during power up and power down ensures that the DUT is protected.

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