OFFLINE POWER SUPPLY USING THE FARM AC FRONT-END MODULE

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TPB 107

An autoranging, high density, low profile switching power supply can be realized using Vicor DC-DC converters and an AC front-end module (FARM).

OVERVIEW

In addition to providing transient / surge immunity and EMI filtering, the FARM (Filter / Autoranging Rectifier Module) contains all of the power switching and control circuitry necessary for autoranging rectification, inrush current limiting, and overvoltage protection. This module also provides converter enable and status functions for orderly power up / down control or sequencing. To complete the AC front-end configuration, the user only needs to add hold up capacitors, and a few additional discrete components.

The FARM maintains the DC output bus voltage between 250 and 370 Vdc over the entire input voltage range, which is compatible with Vicor's Maxi, Mini, Micro Series, 300 V input converters as well as VI-26x and VI-J6x DC-DC converters. The FARM automatically switches to the proper bridge or doubler mode depending on the input voltage, eliminating the possibility of damage due to improper line connection. The FARM1xxx is rated at 500 W in the low range (90-132 Vac input), and 750 W in the high range (180-264 Vac input). The FARM2xxx is rated for 750 W and 1000 W for the low and high input ranges respectively. Either of these modules can serve as the AC front-end for any number and combination of compatible converters as long as the maximum power rating is not exceeded.

Strap (ST) Pin.

In addition to input and output power pin connections, it is necessary to connect the Strap pin to the junction of the series hold up capacitors C1, C2 (Figure 1) for proper autoranging operation. Gas tubes across the capacitors provide input transient protection. The bleeder resistors (R1, R2) discharge the hold up capacitors when power is switched off.

Enable (EN) Pin.

The Enable pin (see Figure 2) must be connected to the PC or Gate In pin of all converter modules to disable the converters during power up. Otherwise, the converters would attempt to start while the hold up capacitors were being charged through an unbypassed thermistor. This condition prevents the bus voltage from reaching the thermistor bypass threshold thus disabling the power supply. The Enable output (the drain of an N channel MOSFET) is internally pulled up to 15 V through a 150 k resistor.

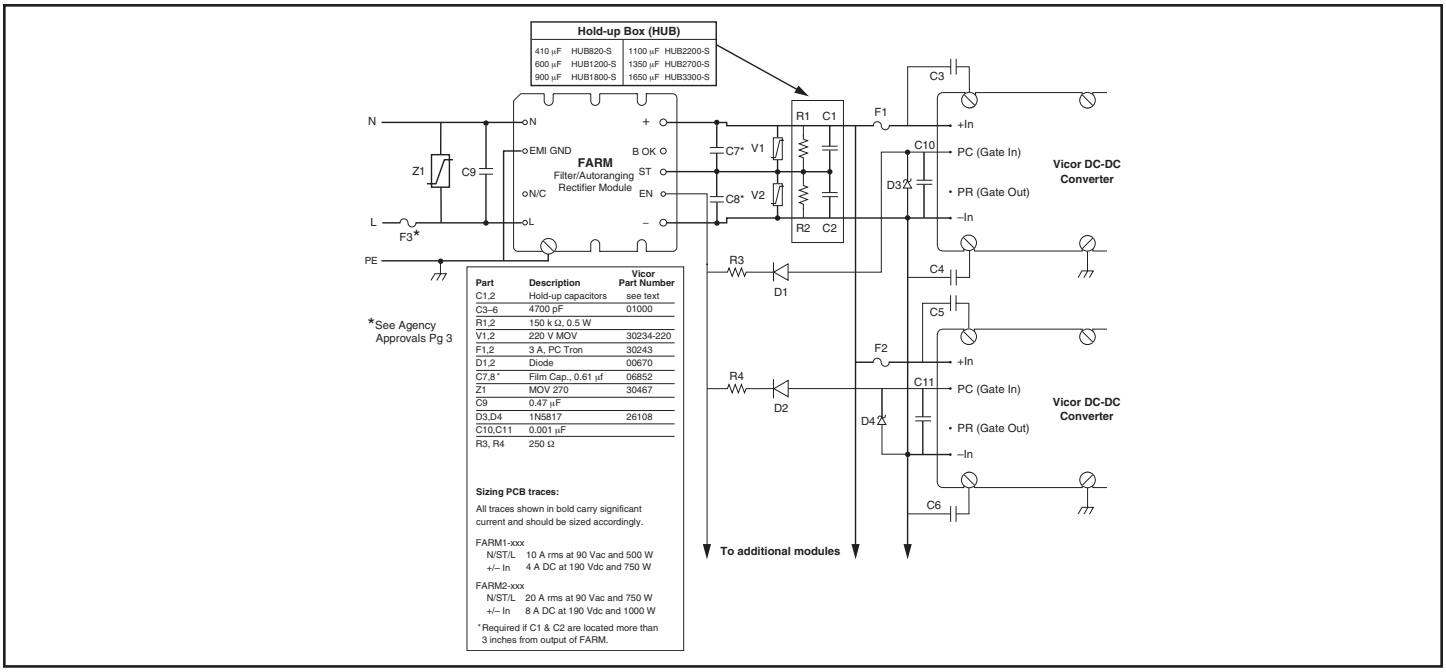

***Figure 1**—Converter connections*

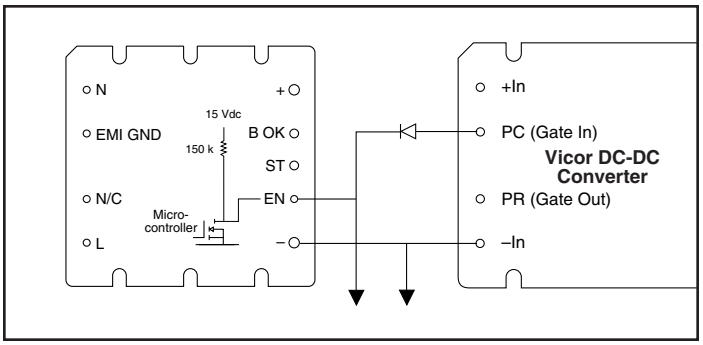

Figure 2*—Enable (EN) function*

A signal diode should be placed close to and in series with the PC (or Gate In) pin of each converter to eliminate the possibility of control interference between converters. The Enable pin switches to the high state (15 V) with respect to the negative output power pin to turn on the converters after the power up inrush is over. The Enable function also provides input overvoltage protection for the converters by turning off the converters if the DC bus voltage exceeds 400 Vdc. The thermistor bypass switch opens if this condition occurs, placing the thermistor in series with the input voltage, which limits input current in case the gas tubes fire. The thermistor bypass switch also opens if a fault or overload reduces the bus voltage to less than 180 Vdc.

Bus-OK (BOK) Pin.

(See Figure 3.) The Bus-OK pin is intended to provide early-warning power fail information and is also referenced to the negative output pin.

CAUTION: There is no input to output isolation in the FARM. It is necessary to monitor Bus-OK via an optoisolator if it is to be used on the secondary (output) side of the converters. A line isolation transformation should be used when performing scope measurements. Scope probes should never be applied simultaneously to the input and output as this will destroy the unit.

Filter.

(See Figure 4.) An integral input filter consists of a common mode choke and Y-rated capacitors (line-ground) plus two X-rated capacitors (line-line). This filter configuration provides sufficient common mode and differential mode insertion loss in the frequency range between 100 kHz and 30 MHz to comply with the Level B conducted emissions limit, as illustrated in Figure 5.

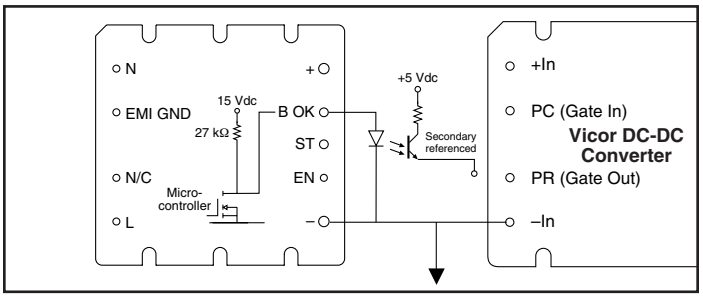

Figure 3*—BUS OK (BOK) isolated power status indicator*

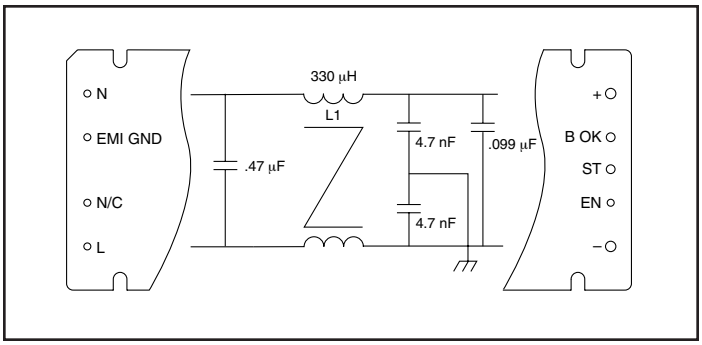

Figure 4*—Internal filter*

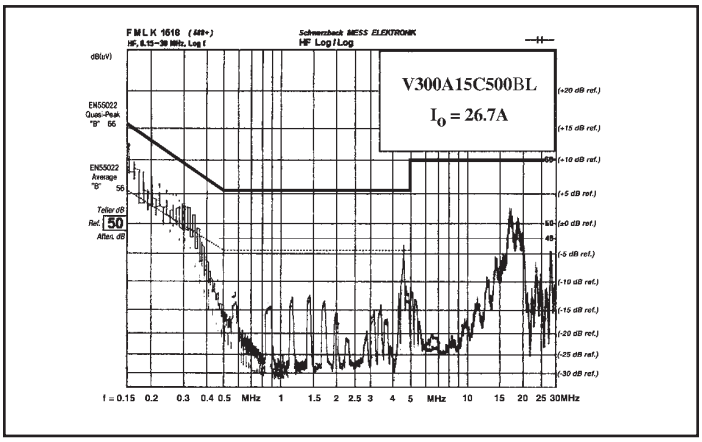

Figure 5*—Conducted emissions (V300A15C500BL)*

FUNCTIONAL DESCRIPTION

Power Up Sequence.

Upon application of input power (see 1.1 of Figure 6), the output bus capacitors begin to charge. The thermistor limits the charge current, and the exponential time constant is determined by the hold up capacitor value and the thermistor cold resistance. The slope (dv/dt) of the capacitor voltage versus time approaches zero as the capacitors become charged to the peak of the AC line voltage.

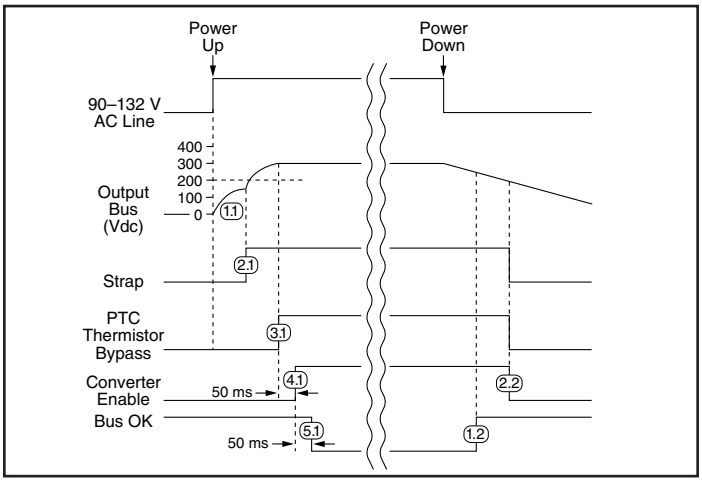

Figure 6*—Timing diagrams: power up / down sequence*

The switch that bypasses the inrush limiting PTC (positive temperature coefficient) thermistor is open when power is applied, as is the switch that engages the strap for voltage doubling (see Figure 7). In addition, the converter modules are disabled via the Enable (EN) line, and Bus-OK (BOK) is high.

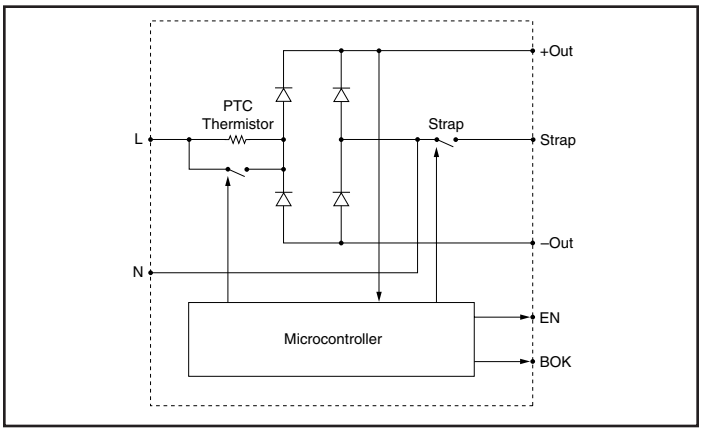

Figure 7*—Functional block diagram: autoranging rectifier*

2.1 If the bus voltage is less than 200 V as the slope nears zero, the voltage doubler is activated, and the bus voltage climbs exponentially to twice the peak line voltage. If the bus voltage is greater than 200 V, the doubler is not activated.

3.1 If the bus voltage is greater than 235 V as the slope approaches zero, the inrush limiting thermistor is bypassed. Below 235 V, it is not bypassed.

4.1 The converters are enabled 50 milliseconds after the thermistor bypass switch is closed.

5.1 Bus-OK is asserted after an additional 50 millisecond delay to allow the converter outputs to settle within specification.

Power Down Sequence.

(See Figure 6.) When input power is turned off or fails, the following sequence occurs as the bus voltage decays:

1.2 Bus-OK is deasserted when the bus voltage falls below 210 Vdc.

2.2 The converters are disabled when the bus voltage falls below 190 Vdc. If power is reapplied after the converters are disabled, the entire sequence is repeated. If a momentary power interruption occurs and power is reestablished before the bus reaches the disable threshold, the power up sequence is not repeated.

DETERMINING REQUIRED HOLD UP CAPACITORS

Hold up capacitor values should be determined according to output bus voltage ripple, power fail hold up time, and ride-through time. (See Figure 8.) Many applications require the power supply to maintain specified output regulation during a momentary power failure of specified duration, i.e., the converters must hold up or ride through such an event while maintaining undisturbed output voltage regulation. Similarly, many of these same systems require notification of an impending power failure in order to allow time to perform an orderly shut down.

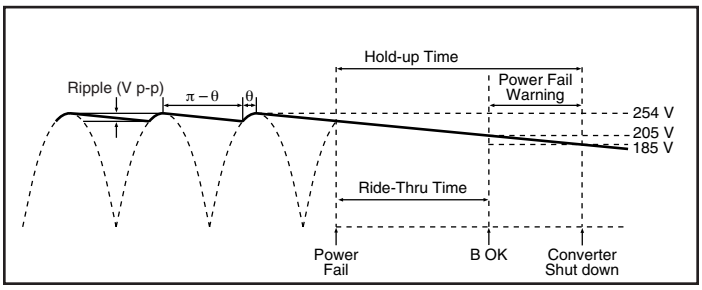

Figure 8*—Hold up time*

The energy stored on a capacitor which has been charged to voltage V is:

$$\varepsilon = 1/2(CV^2) \quad (1)$$

Where: ε = stored energy
C = capacitance
V = voltage across the capacitor

Energy is given up by the capacitors as they are discharged by the converters. The energy expended (the power-time product) is:

$$\varepsilon = P\Delta t = C(V_1^2 - V_2^2)/2 \quad (2)$$

Where: P = operating power
Δt = discharge interval
V_1 = capacitor voltage at the beginning of Δt
V_2 = capacitor voltage at the end of Δt

Rearranging Equation 2 to solve for the required capacitance:

$$C = 2P\Delta t / (V_1^2 - V_2^2) \quad (3)$$

The hold up time (Δt) is defined as the interval between power fail warning (BOK) and converter shut down (EN) as illustrated in Figure 8. The Bus-OK and Enable thresholds are 205 V and 185 V, respectively. A simplified relationship between hold up time, operating power, and bus capacitance is obtained by inserting these constants:

$$C = 2P\Delta t / (205^2 - 185^2)$$
$$C = 2P\Delta t / (7{,}800)$$

It should be noted that the series combination (C1, C2, see Figure 1) requires each capacitor to be twice the calculated value, but the required voltage rating is reduced to 200 V.

Allowable ripple voltage on the bus (or ripple current in the capacitors) may define the capacitance requirement. Consideration should be given to converter ripple rejection

and resulting output ripple voltage. The ripple rejection, R, of Vicor converters is specified as a function of the input / output voltage ratio:

$$R = 30+20\log(V_{IN} / V_{OUT}) \quad (4)$$

For example, a converter whose output is 15 V and nominal input is 300 V will provide 56 dB ripple rejection, i.e., 10 V_{PP} of input ripple will produce 15 V_{PP} of output ripple. Equation 3 is again used to determine the required capacitance. In this case, V_1 and V_2 are the instantaneous values of bus voltage at the peaks and valleys (see Figure 8) of the ripple, respectively. The capacitors must hold up the bus voltage for the time interval (Δt) between peaks of the rectified line as given by:

$$\Delta t = (\pi - \theta) / 2\pi f \quad (5)$$

Where: f = line frequency

θ = rectifier conduction angle

The approximate conduction angle is given by:

$$\theta = \text{Cos}^{-1} V_2 / V_1 \quad (6)$$

Another consideration in hold up capacitor selection is their ripple current rating. The capacitors' rating must be higher than the maximum operating ripple current. The approximate operating ripple current (rms) is given by:

$$I_{RMS} = 2P/Vac \quad (7)$$

Where: P = operating power level

V_{AC} = operating line voltage

Calculated values of bus capacitance for various hold up time, ride-through time, and ripple voltage requirements are given as a function of operating power level in Figures 9, 10, and 11, respectively.

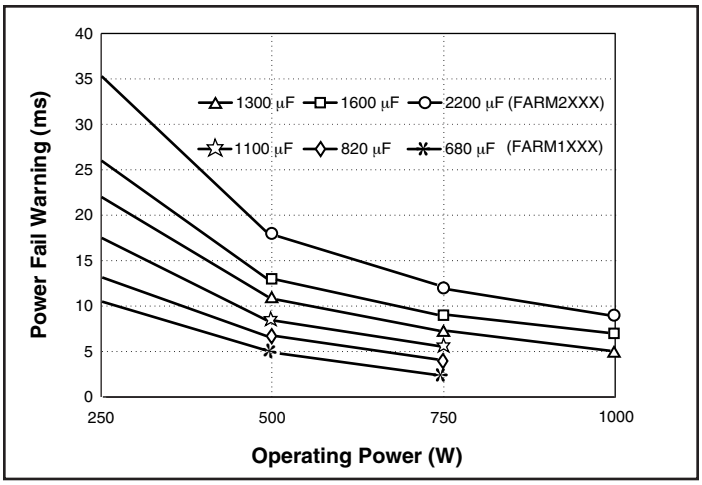

Figure 9*—Hold-up time vs. operating power and total bus capacitance, series combination of C1, C2 (see Fig. 1)*

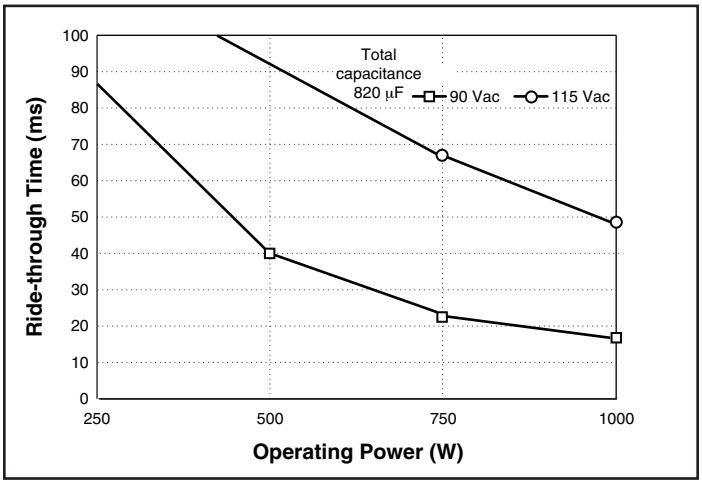

Figure 10*—Ride-through time vs. operating power*

EXAMPLE

In this example, the output required from the DC-DC converter at the point of load is 12 Vdc at 320 W. Therefore, the output power from the FARM would be 375 W (assuming a converter efficiency of 85%). The desired hold up time is 9 ms over an input range of 90 to 264 Vac.

Determining Required Hold up Capacitance.

Figure 9 is used to determine holdup capacitance for a given hold up time and power level, and shows that the total bus capacitance must be at least 820 µF. Since two capacitors are used in series, each capacitor must be at least 1,640 µF. Note that hold-up time is not dependent on line voltage.

Determining Ride-through Time.

Figure 10 illustrates ride-through time as a function of line voltage and output power, and shows that at a nominal line of 90 Vac, ride-through would be 68 ms. Ride-through time is a function of line voltage.

Determining Ripple Voltage on Hold up Capacitors.

Figure 11 is used to determine ripple voltage as a function of operating power and bus capacitance, and shows that the ripple voltage across the holdup capacitors will be 12Vac.

Determining the Ripple on the Output of the DC-DC converter.

Figure 12 is used to determine the ripple rejection of the DC-DC converter and indicates a ripple rejection of approximately 60 dB for a 12 V output. Since the ripple on the bus voltage is 12 Vac and the ripple rejection of the converter is 60 dB, the output ripple of the converter due to ripple on its input (primarily 120 Hz) will be 12 mVpp. Note that Vicor Maxi, Mini, Micro Series converters have greater ripple rejection than either VI-200s or VI-J00s.

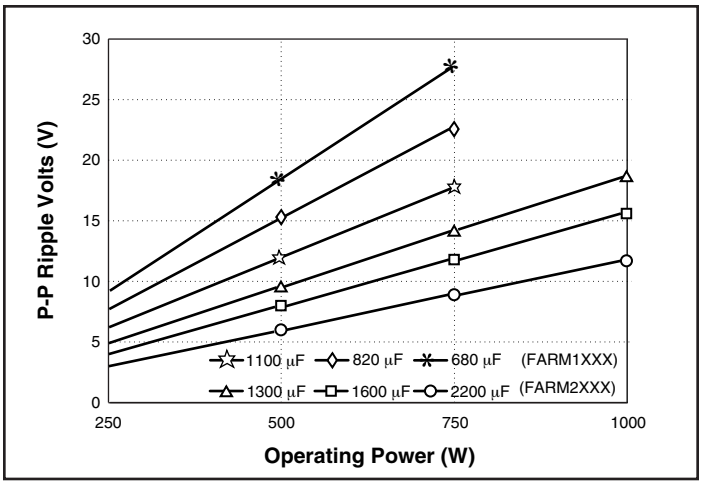

Figure 11—Ripple voltage vs. operating power and bus capacitance, series combination of C1, C2 (see Fig. 1)

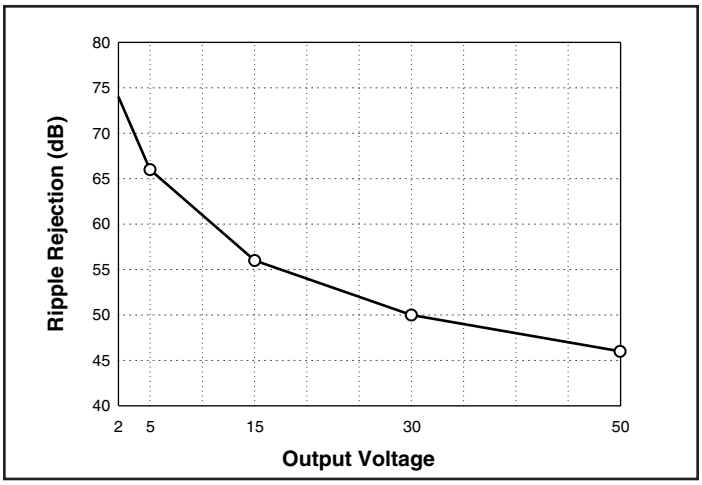

Figure 12—Converter ripple rejection vs. output voltage