

32-Channel Serial to Parallel Converter With Open Drain Outputs

Features

- ▶ Processed with HVCMOS® technology
- ▶ Output voltages to 225V using a ramped supply voltage
- ▶ SINK current minimum 100mA
- ▶ Shift register speed 8.0MHz
- ▶ Strobe and enable inputs
- ▶ CMOS compatible inputs
- ▶ Forward and reverse shifting options
- ▶ Hi-Rel processing available

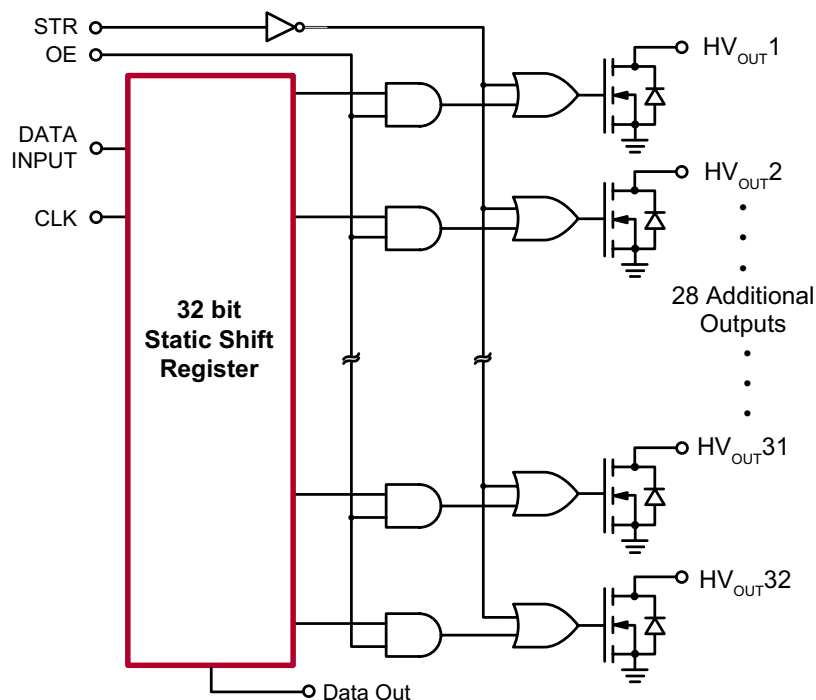
General Description

The HV5122 is a low voltage serial to high voltage parallel converter with open drain outputs. This device has been designed for use as a driver for AC electroluminescent displays. They can also be used in any application requiring multiple output high voltage current sinking capabilities such as driving inkjet and electrostatic print heads, plasma panels, vacuum fluorescent, or large matrix LCD displays.

This device consists of a 32-bit shift register and control logic to perform the Output Enable and all-on functions. Data is shifted through the shift register on the high to low transition of the clock. The HV5122 shifts in the counter-clockwise direction when viewed from the top of the package. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register. Operation of the shift register is not affected by the OE(Output Enable) or the STR(Strobe) inputs.

The HV5122 has been designed to be used in systems which either switch off the high voltage supply before changing the state of the high voltage outputs or which limit the current through each output.

Functional Block Diagram



Ordering Information

Device	Package Options		
	44-Lead Quad Cerpac Chip Carrier .650x.650in body .190in height (max) .050in pitch	44-Lead Quad Plastic Gullwing 10.00x10.00mm body 2.35mm height (max) 0.80mm pitch	44-Lead Quad Plastic Chip Carrier .653x.653in body .180in height (max) .050in pitch
HV5122	HV5122DJ*	HV5122PG-G	HV5122PJ-G



-G indicates package is RoHS compliant ("Green")
* Hi-Rel processing available

Absolute Maximum Ratings

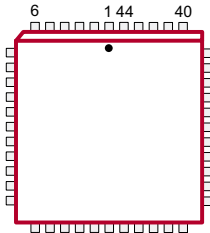
Parameter	Value
Supply voltage, V_{DD}	-0.5V to +15V
Supply voltage, V_{PP}	-0.5V to +250V
Logic input levels	-0.5V to V_{DD} +0.5V
Ground current ¹	1.5A
Continuous total power dissipation ²	
Plastic	1200W
Ceramic	1500W
Operating temperature range	
Plastic	-40°C to +85°C
Ceramic	-55°C to +125°C
Storage temperature range	-65°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

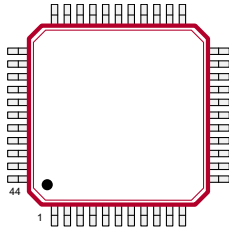
Notes:

- 1. Duty cycle is limited by the total power dissipated in the package.
- 2. For operation above 25°C ambient derate linearly to maximum operating temperature at 20mW/°C for plastic and at 15mW/°C for ceramic.

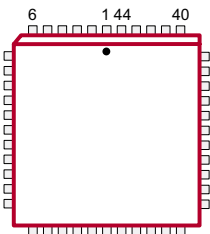
Pin Configurations



44-Lead Quad Cerpac Chip Carrier (DJ)



44-Lead Quad Plastic Gullwing (PG)



44-Lead Quad Plastic Chip Carrier (PJ)

Product Marking

Top Marking



YY = Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID*

Bottom Marking



*May be part of top marking

44-Lead Quad Plastic Chip Carrier (DJ)

Top Marking



YY = Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID*

Bottom Marking



— = "Green" Packaging
*May be part of top marking

44-Lead Quad Plastic Gullwing (PG)

Top Marking



YY = Year Sealed
WW = Week Sealed
L = Lot Number
A = Assembler ID
C = Country of Origin*
— = "Green" Packaging
*May be part of top marking

Bottom Marking



44-Lead Quad Plastic Chip Carrier (PJ)

Packages may or may not include the following marks: Si or

Recommended Operating Conditions

Sym	Parameter		Min	Typ	Max	Units
V _{DD}	Logic voltage supply		10.8	12	13.2	V
HV _{OUT}	High voltage output		-0.3	-	225	V
V _{IH}	High-level input voltage		V _{DD} -2.0	-	V _{DD}	V
V _{IL}	Low-level input voltage		0	-	2.0	V
f _{CLK}	Clock frequency		-	-	8.0	MHz
T _A	Operating free-air temperature	Plastic	-40	-	+85	°C
		Ceramic	-55	-	+125	

Power-Up Sequence

Power-up sequence should be the following:

1. Connect ground
2. Apply V_{DD}
3. Set all inputs to a known state

Power-down sequence should be the reverse of the above.

Electrical Characteristics (Over recommended operating conditions unless otherwise specified)

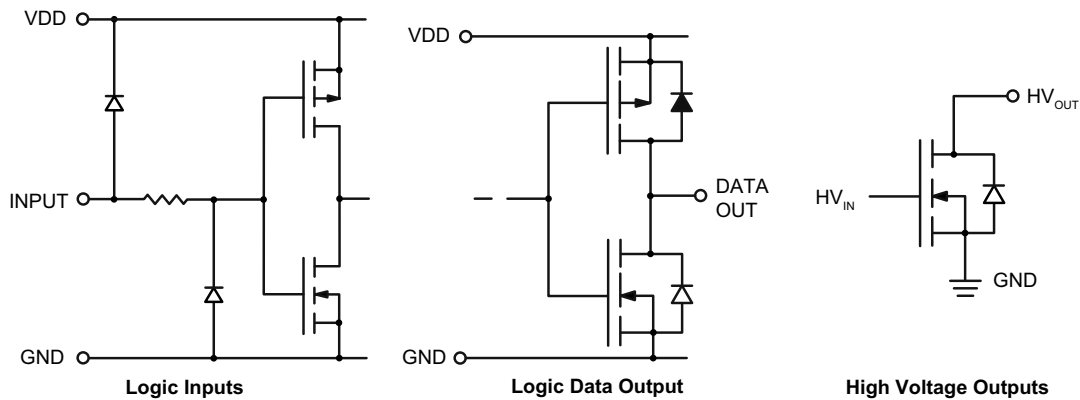
DC Characteristics

Sym	Parameter	Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current	-	15	mA	$f_{CLK} = 8.0\text{MHz}$, $F_{DATA} = 4.0\text{MHz}$
I_{DDQ}	Quiescent V_{DD} supply current	-	100	μA	All $V_{IN} = 0\text{V}$
$I_{O(OFF)}$	Off-state output current	-	10	μA	All outputs high, all SWS parallel
I_{IH}	High level logic input current	-	1.0	μA	$V_{IH} = 12\text{V}$
I_{IL}	Low level logic input current	-	-1.0	μA	$V_{IL} = 0$
V_{OH}	High level output data out	$V_{DD} - 1.0\text{V}$	-	V	$I_{DOUT} = -100\mu\text{A}$
V_{OL}	Low level output voltage	HV_{OUT}	-	V	$I_{HVOUT} = +100\text{mA}$
		Data out	-		$I_{DOUT} = +100\mu\text{A}$
V_{OC}	HV_{OUT} clamp voltage	-	-1.5	V	$I_{OL} = -100\text{mA}$

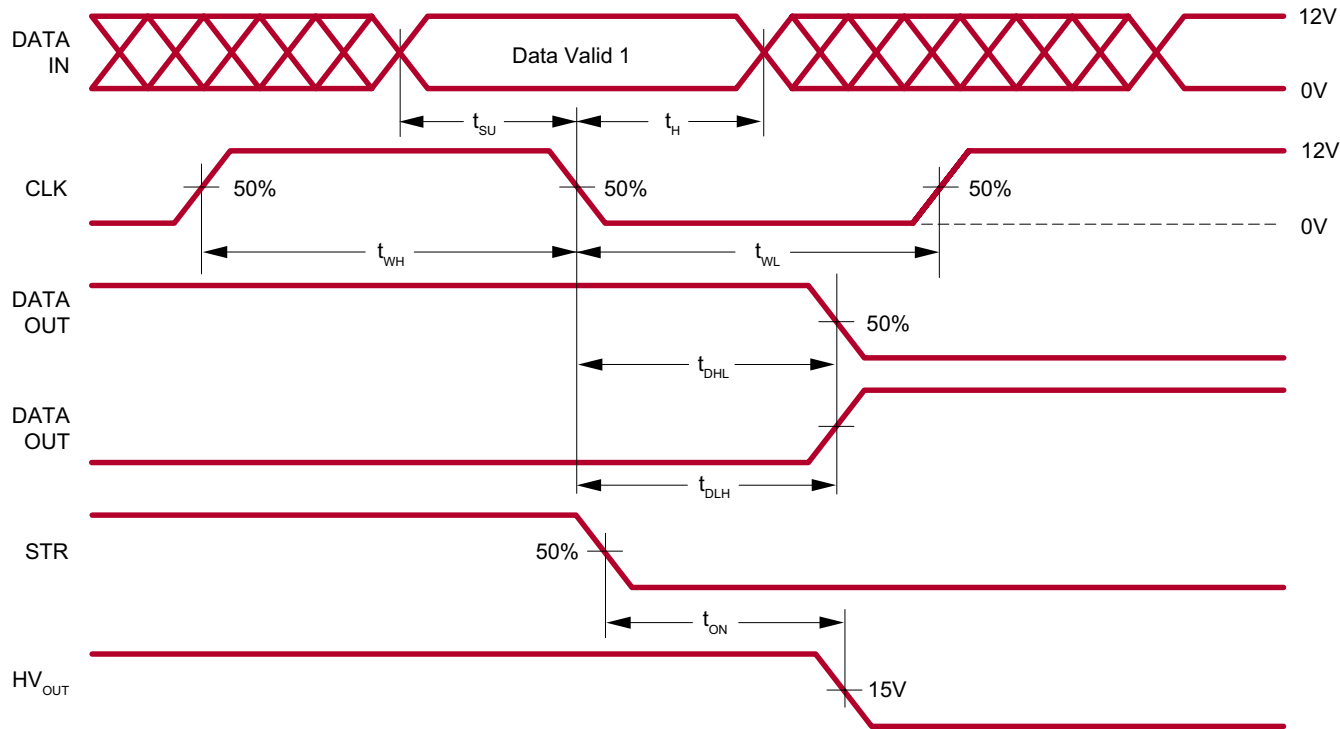
AC Characteristics ($V_{DD} = 12\text{V}$, $T_A = 25^\circ\text{C}$)

Sym	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency	-	8.0	MHz	---
t_W	Clock width, high or low	62	-	ns	---
t_{SU}	Data setup time before CLK falls	25	-	ns	---
t_H	Data hold time after CLK falls	10	-	ns	---
t_{ON}	Turn-on time, HV_{OUT} from strobe	-	500	ns	$R_L = 2.0\text{K}\Omega$ to 200V
t_{DHL}	Data output delay after H to L CLK	-	100	ns	$C_L = 15\text{pF}$
t_{DLH}	Data output delay after L to H CLK	-	100	ns	$C_L = 15\text{pF}$

Input and Output Equivalent Circuits



Switching Waveforms



Function Table

Function	Inputs				Outputs				
	Data In	CLK	OE	STR	Shift Reg		HV Outputs		Data Out
					1	2...32	1	2...32	
All on	X	X	X	L	•	•...•	ON	ON...ON	•
All off	X	X	L	H	•	•...•	OFF	OFF...OFF	•
Load S/R	H OR L	↓	L	H	H or L	•...•	OFF	OFF...OFF	-
Output Enable	X	H OR L	H	H	H or L	•...•	ON or OFF	•...•	•

Notes:
H = high level, L = low level, X = irrelevant, ↓ = high-to-low transition
• = dependent on previous stage's state before the last CLK: High-to-low transition

44-Lead PQFP Pin Assignment (PG)

HV5122PG		
Pin	Function	Description
1	HV _{OUT} 11	High voltage outputs.
2	HV _{OUT} 12	
3	HV _{OUT} 13	
4	HV _{OUT} 14	
5	HV _{OUT} 15	
6	HV _{OUT} 16	
7	HV _{OUT} 17	
8	HV _{OUT} 18	
9	HV _{OUT} 19	
10	HV _{OUT} 20	
11	HV _{OUT} 21	
12	HV _{OUT} 22	
13	HV _{OUT} 23	
14	HV _{OUT} 24	
15	HV _{OUT} 25	
16	HV _{OUT} 26	
17	HV _{OUT} 27	
18	HV _{OUT} 28	
19	HV _{OUT} 29	
20	HV _{OUT} 30	
21	HV _{OUT} 31	
22	HV _{OUT} 32	
23	DATA OUT	Data output for cascading to the data input of the next device.
24	N/C	No connect.
25		
26		
27		
28	OE	Output enable input. When OE is LOW, all HV outputs are forced into a LOW state, regardless of data in each channel. When OE is HIGH, all HV outputs reflect data latched.
29	CLK	Data shift register clock. Input are shifted into the shift register on the positive edge of the clock.
30	GND	Logic and high voltage ground.
31	VDD	Low voltage logic power rail.
32	STR	Strobe.

44-Lead PQFP Pin Assignment (PG) (cont.)

HV5122PG		
Pin	Function	Description
33	DATA IN	Serial data input. Data needs to be present before each rising edge of the clock.
34	N/C	No connect.
35	HV _{OUT} 1	High voltage outputs.
36	HV _{OUT} 2	
37	HV _{OUT} 3	
38	HV _{OUT} 4	
39	HV _{OUT} 5	
40	HV _{OUT} 6	
41	HV _{OUT} 7	
42	HV _{OUT} 8	
43	HV _{OUT} 9	
44	HV _{OUT} 10	

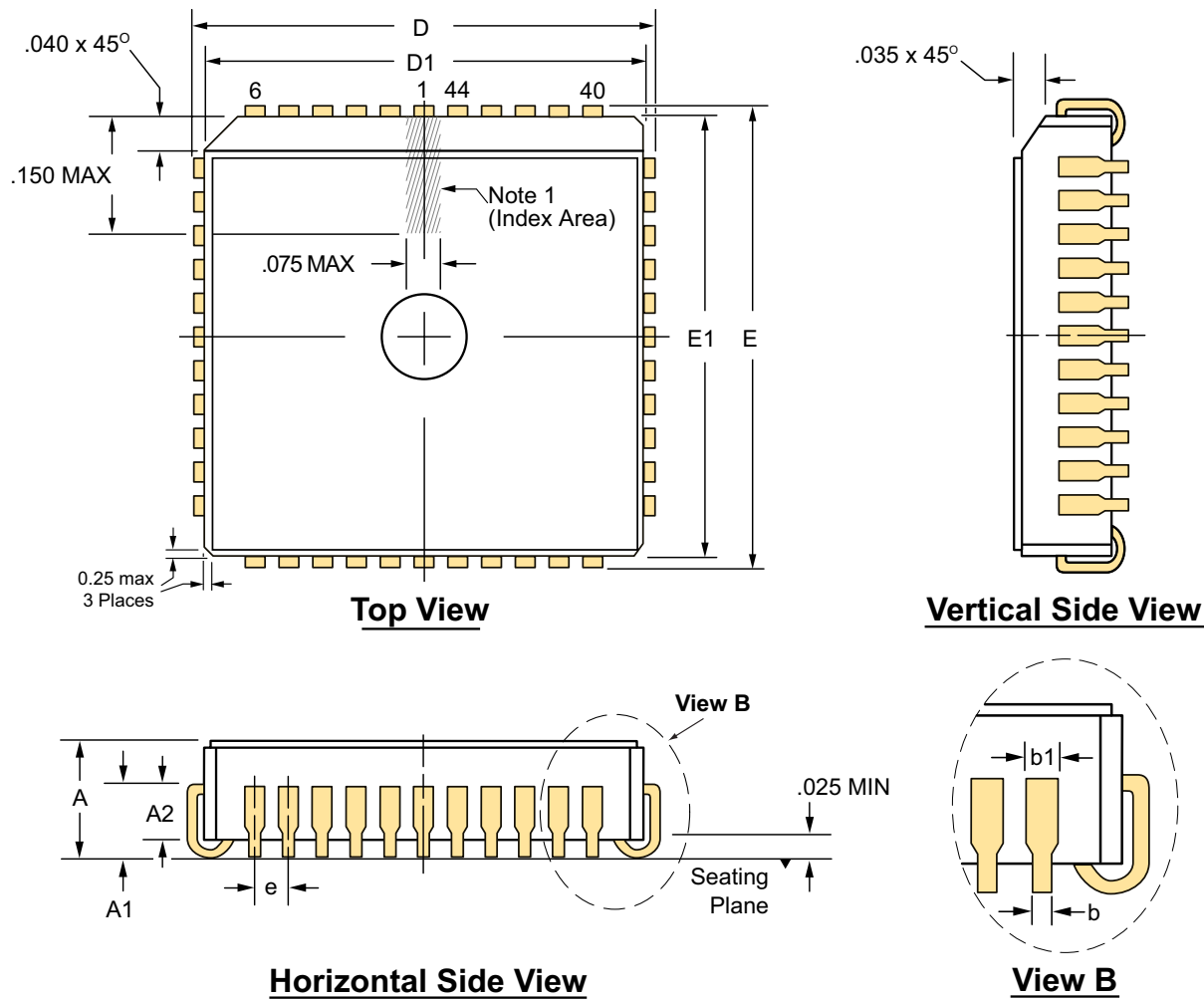
44-Lead PLCC Pin Assignment (DJ/PJ)

HV5122PJ		
Pin	Function	Function
1	HV _{OUT} 16	High voltage outputs
2	HV _{OUT} 17	
3	HV _{OUT} 18	
4	HV _{OUT} 19	
5	HV _{OUT} 20	
6	HV _{OUT} 21	
7	HV _{OUT} 22	
8	HV _{OUT} 23	
9	HV _{OUT} 24	
10	HV _{OUT} 25	
11	HV _{OUT} 26	
12	HV _{OUT} 27	
13	HV _{OUT} 28	
14	HV _{OUT} 29	
15	HV _{OUT} 30	
16	HV _{OUT} 31	
17	HV _{OUT} 32	

44-Lead PLCC Pin Assignment (DJ/PJ) (cont.)

HV5122PJ		
Pin	Function	Function
18	DATA OUT	Data output for cascading to the data input of the next device.
19	N/C	No connect.
20		
21		
22		
23	OE	Output enable input. When OE is LOW, all HV outputs are forced into a LOW state, regardless of data in each channel. When OE is HIGH, all HV outputs reflect data latched.
24	CLK	Data shift register clock. Input are shifted into the shift register on the positive edge of the clock.
25	GND	Logic and high voltage ground.
26	VDD	Low voltage logic power rail.
27	STR	Strobe.
28	DATA IN	Serial data input. Data needs to be present before each rising edge of the clock.
29	N/C	No connect.
30	HV _{OUT} 1	High voltage outputs.
31	HV _{OUT} 2	
32	HV _{OUT} 3	
33	HV _{OUT} 4	
34	HV _{OUT} 5	
35	HV _{OUT} 6	
36	HV _{OUT} 7	
37	HV _{OUT} 8	
38	HV _{OUT} 9	
39	HV _{OUT} 10	
40	HV _{OUT} 11	
41	HV _{OUT} 12	
42	HV _{OUT} 13	
43	HV _{OUT} 14	
44	HV _{OUT} 15	

44-Lead Quad Cerpac Package Outline (DJ)
.650x.650in body, .190in height (max), .050in pitch

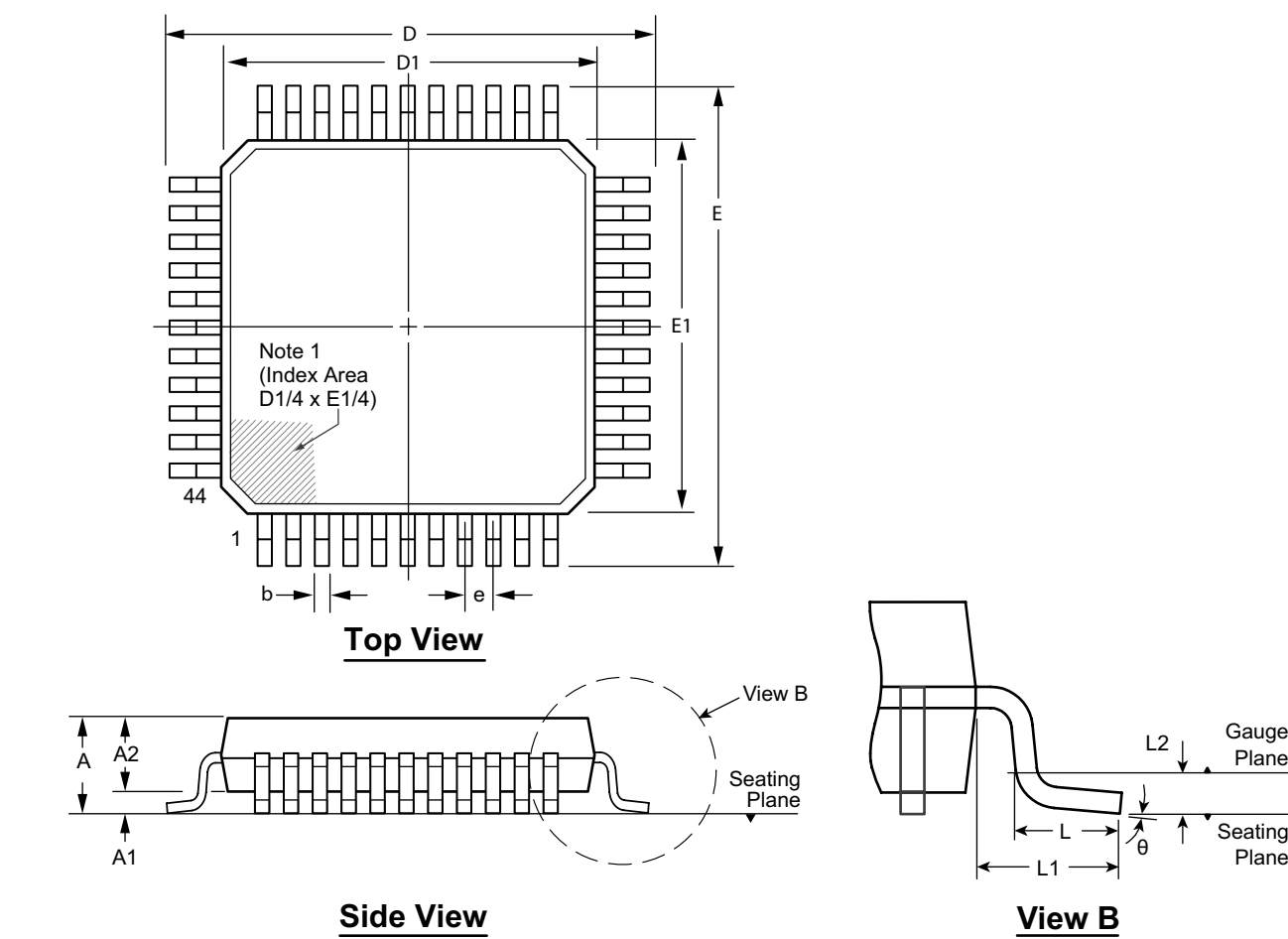


Note:
1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol	A	A1	A2	b	b1	D	D1	E	E1	e
Dimension (inches)	MIN	.155	.090	.060 REF	.017	.026	.685	.630	.685	.050 BSC
	NOM	.172	.100		.019	.029	.690	.650	.690	
	MAX	.190	.120		.021	.032	.695	.665	.695	

JEDEC Registration MO-087, Variation AB, Issue B, August, 1991.
Drawings not to scale.
Supertex Doc. #: DSPD-44CERPACDJ, Version D090808.

44-Lead PQFP Package Outline (PG)
10.00x10.00mm body, 2.35mm height (max), 0.80mm pitch



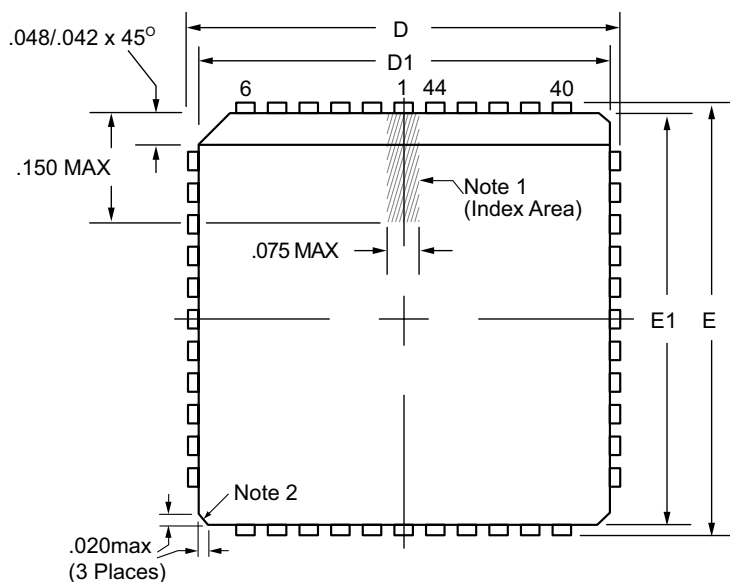
Note:
1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ
Dimension (mm)	MIN	1.95*	0.00	1.95	0.30	13.65*	9.80*	13.65*	9.80*	0.80 BSC	0.73	1.95 REF	0.25 BSC	0°
	NOM	-	-	2.00	-	13.90	10.00	13.90	10.00		0.88			3.5°
	MAX	2.35	0.25	2.10	0.45	14.15*	10.20*	14.15*	10.20*		1.03			7°

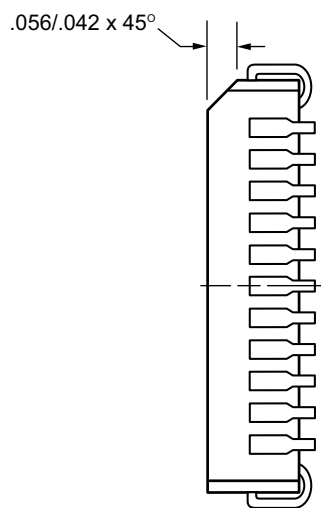
JEDEC Registration MO-112, Variation AA-2, Issue B, Sep. 1995.
* This dimension is not specified in the JEDEC drawing.
Drawings not to scale.
Supertex Doc. #: DSPD-44PQFPPG, Version C041309.

44-Lead PLCC Package Outline (PJ)

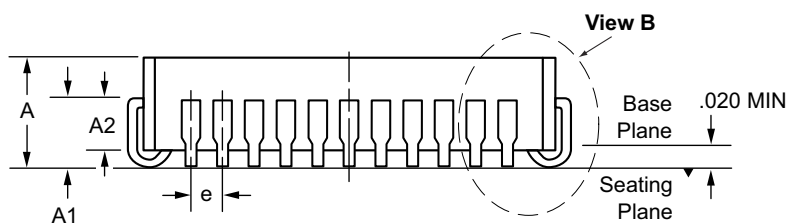
.653x.653in body, .180in height (max), .050in pitch



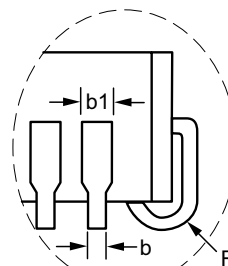
Top View



Vertical Side View



Horizontal Side View



View B

Notes:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Actual shape of this feature may vary.

Symbol		A	A1	A2	b	b1	D	D1	E	E1	e	R
Dimension (inches)	MIN	.165	.090	.062	.013	.026	.685	.650	.685	.650	.050 BSC	.025
	NOM	.172	.105	-	-	-	.690	.653	.690	.653		.035
	MAX	.180	.120	.083	.021	.036 [†]	.695	.656	.695	.656		.045

JEDEC Registration MS-018, Variation AC, Issue A, June, 1993.

[†] This dimension differs from the JEDEC drawing.

Drawings not to scale.

Supertex Doc. #: DSPD-44PLCCPJ, Version F031111.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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