# 32-Channel Vacuum-Fluorescent Display Driver

## Features

- 32 output lines
- 90V output swing
- Active pull-down
- Latches on all outputs
- Up to 6.0MHz @ $V_{DD}$ = 5.0V
- -40°C to +85°C operation

## Applications

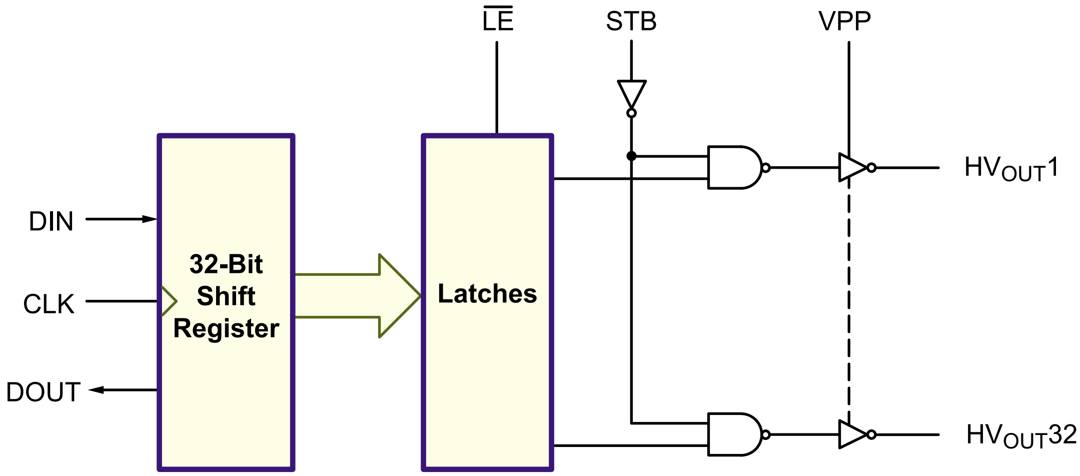
- Vacuum flourescent displays
- DC plasma displays

## General Description

The HV518 is designed for vacuum fluorescent or DC plasma applications, where it can serve as a segment, digit or matrix display driver. Each device has 32 outputs, 32 latches and a 32-bit cascadable shift register.

Serial data enters the shift register on the LOW-to-HIGH transition of the clock input. With latch enable ($\overline{LE}$) HIGH, parallel data is transferred to the output buffers through a 32-bit latch. When $\overline{LE}$ is low the data is stored in the latch. When STROBE is LOW, all outputs are enabled; if STROBE is HIGH, all outputs are LOW.

## Block Diagram

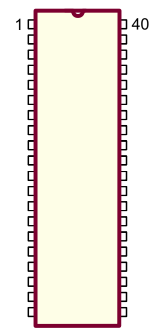


## Ordering Information

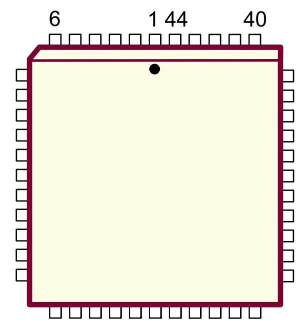
| Device | Package Options | |
|---|---|---|
| | **40-Lead PDIP**<br>*1.980x.600in body (max)*<br>*.250in height (max)*<br>*.100in pitch* | **44-Lead PLCC**<br>*.653x.653in body*<br>*.180in height (max)*<br>*.050in pitch* |
| HV518 | HV518P-G | HV518PJ-G |

*-G indicates package is RoHS compliant ('Green')*

## Pin Configurations




**40-Lead PDIP (P)**
***(top view)***




**44-Lead PLCC (PJ)**
***(top view)***

## Absolute Maximum Ratings

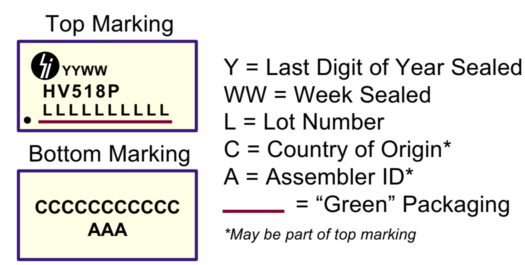
| Parameter | Value |
|---|---|
| Supply voltage, $V_{DD}$ | -0.5V to +6.0V |
| Supply voltage, $V_{PP}$ | -0.5V to +90V |
| Logic input levels | -0.5V to $V_{DD}$ +0.5V |
| Continuous total power dissipation[1,2] | 1200mW |
| Operating temperature | -40°C to +85°C |
| Storage temperature | -65°C to +150°C |
| Soldering temperature[3] | 260°C |

*Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to GND.*

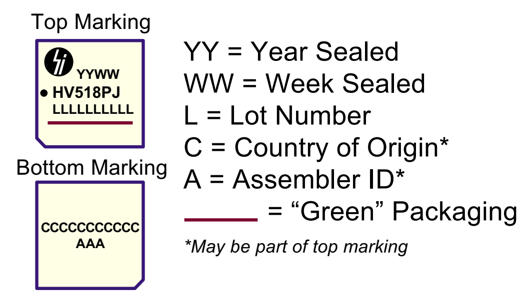
***Notes:***

1. *Duty cycle is limited by the total power dissipated in the package.*
2. *For operation above 25°C ambient, derate linearly to 85°C at 20mW/°C.*
3. *Distance of 1.6mm from case for 10 seconds.*

## Product Markings




**40-Lead PDIP (P)**




**44-Lead PLCC (PJ)**

## Recommended Operating Conditions *($T_A$ = 25°C, unless otherwise noted)*

| Sym | Parameter | Min | Max | Unit | Conditions |
|---|---|---|---|---|---|
| $V_{DD}$ | Logic supply voltage | 4.5 | 5.5 | V | --- |
| $V_{PP}$ | High voltage supply | 8.0 | 80 | V | --- |
| $V_{IH}$ | High-level input voltage | 3.5 | - | V | $V_{DD}$ = 4.5V, See Figure 1 |
| $V_{IL}$ | Low-level input voltage | - | 1.0 | V | $V_{DD}$ = 4.5V, See Figure 1 |
| $I_{OH}$ | High-level output current | -25 | - | mA | --- |
| $I_{OL}$ | Low-level output current | - | 2.0 | mA | --- |
| $f_{CLK}$ | Clock frequency | - | 6.0 | MHz | $V_{DD}$ = 4.5V, See Figure 1 |
| $t_{w(CKH)}$ | Pulse duration, clock high | 83 | - | ns | $V_{DD}$ = 4.5V |
| $t_{w(CKL)}$ | Pulse duration, clock low | 83 | - | ns | $V_{DD}$ = 4.5V |
| $t_{su}$ | Setup time, data before clock | 75 | - | ns | $V_{DD}$ = 4.5V |
| $t_h$ | Hold time, data after clock | 75 | - | ns | $V_{DD}$ = 4.5V |
| $T_A$ | Operating ambient temperature | -40 | 85 | °C | --- |

## Electrical Characteristics *(over recommended ranges of operating ambient temperature unless otherwise noted.)*

| Sym | Parameter | | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply current | | - | - | 10 | mA | $V_{DD}$ = 5.0V, $f_{CH}$ = 6.0 MHz |
| $I_{DDQ}$ | Quiescent supply current | | - | - | 0.5 | mA | $V_{DD}$ = 5.5V, $V_{IN}$ = 0V |
| $I_{PP}$ | Supply current | | - | - | 12 | mA | Outputs high, $T_A$ = -40$^O$ |
| | | | - | 7.0 | 10 | mA | Outputs high, $T_A$ = 0 to +85$^O$ |
| | | | - | - | 500 | µA | Outputs low |
| $V_{OH}$ | $HV_{IN}$ operating current | HV output | 70 | - | - | V | $I_{OH}$ = -25mA |
| | | Serial output | 4.5 | 4.9 | 5.0 | | $V_{DD}$ = 5.0V, $I_{OH}$ = -20µA |
| $V_{OL}$ | $LV_{IN}$ operating current | HV output | - | - | 5.0 | V | $I_{OL}$ = 1.0mA |
| | | Serial output | - | 0.06 | 0.8 | | $I_{OL}$ = 20µA |
| $I_{IH}$ | Logic input current high | | - | 0.1 | 1.0 | µA | $V_{IH}$ = $V_{DD}$ |
| $I_{IL}$ | Logic input current low | | - | -0.1 | -1.0 | µA | $V_{IL}$ = 0V |

***Note:***
*The total number of ON outputs times the duty cycle must not exceed the allowable package power disspation.*

## Switching Characteristics *($V_{PP}$ = 80V, $C_L$ = 50pF, $T_A$ = 25°C, unless otherwise noted)*

| Sym | Parameter | | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| $t_d$ | Delay time, clock to data output | | - | - | 600 | ns | $C_L$ = 15pF, See Figure 2 |
| $t_{DHL}$ | Delay time, high-to-low-level, HV output | From latch enable | - | - | 1.5 | µs | $V_{DD}$ = 4.5V, See Figure 3 |
| | | From strobe | - | - | 1.0 | | $V_{DD}$ = 4.5V, See Figure 4 |
| $t_{DLH}$ | Delay time, low-to-high-level, HV output | From latch enable | - | - | 1.5 | µs | $V_{DD}$ = 4.5V, See Figure 3 |
| | | From strobe | - | - | 1.0 | | $V_{DD}$ = 4.5V, See Figure 4 |
| $t_{THL}$ | Transition time, high-to-low-level, HV output | | - | - | 3.0 | µs | $V_{DD}$ = 4.5V, See Figure 4 |
| $t_{TLH}$ | Transition time, low-to-high-level, HV output | | - | - | 2.5 | µs | $V_{DD}$ = 4.5V, See Figure 4 |

## Power-Up/ Power-Down Sequences

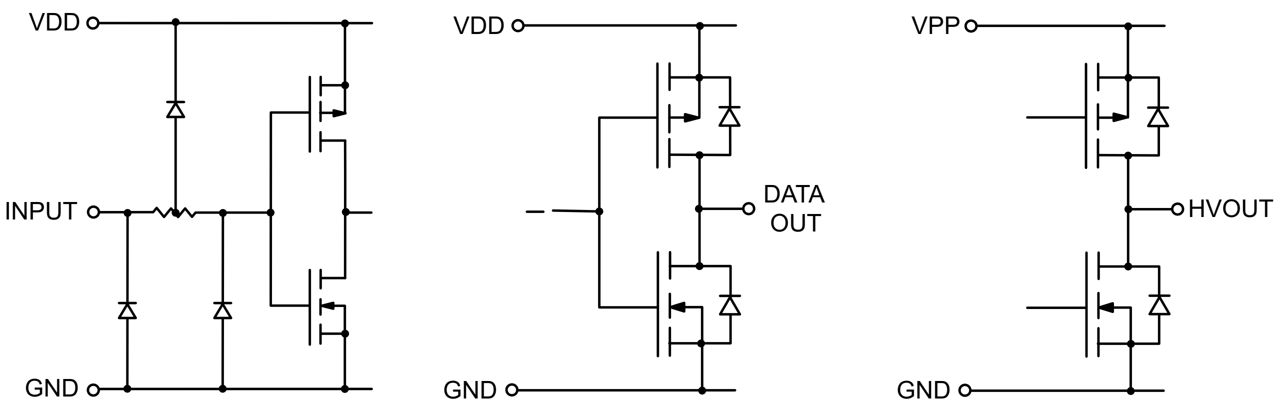
***Power-up sequence should be the following:***

1. Connect ground.
2. Apply $V_{DD}$.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply $V_{PP}$.

*The $V_{PP}$ should not drop below $V_{DD}$ or float during operation.*

***Power-down sequence should be the reverse of the above.***

## Input and Output Equivalent Circuits




## Parameter Measurement Information

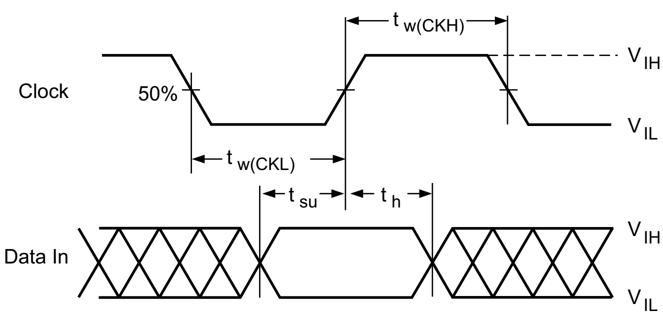



**Figure 1:** Input Timing Voltage Waveforms

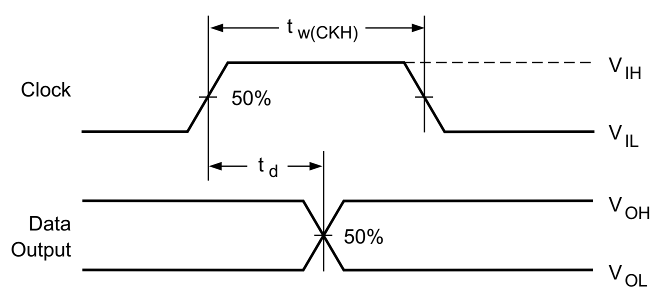



**Figure 2**

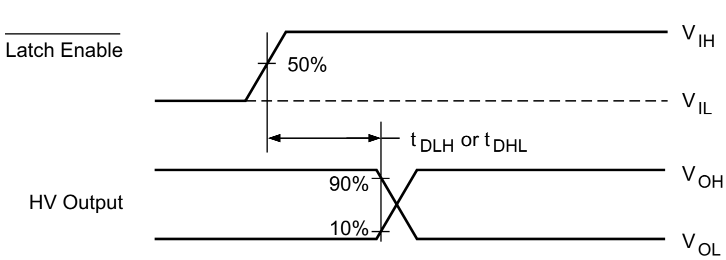



**Figure 3**

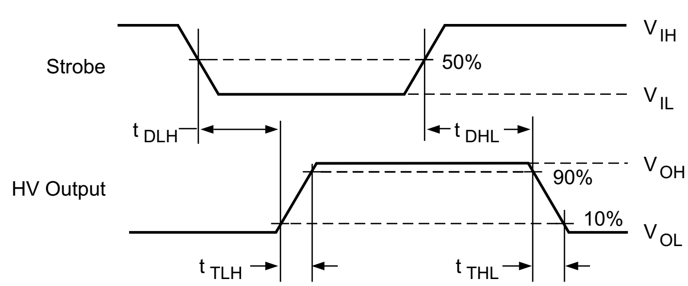



**Figure 4:** Switching-Time Voltage Waveforms

***Note:***

*For testing purposes, all input pulses have maximum rise and fall times of 30 nsec.*

## Truth Tables

### Input

| Data In | CLK | Data Out |
|---|---|---|
| H | ↑ | H |
| L | ↑ | L |
| X | No Change | * |

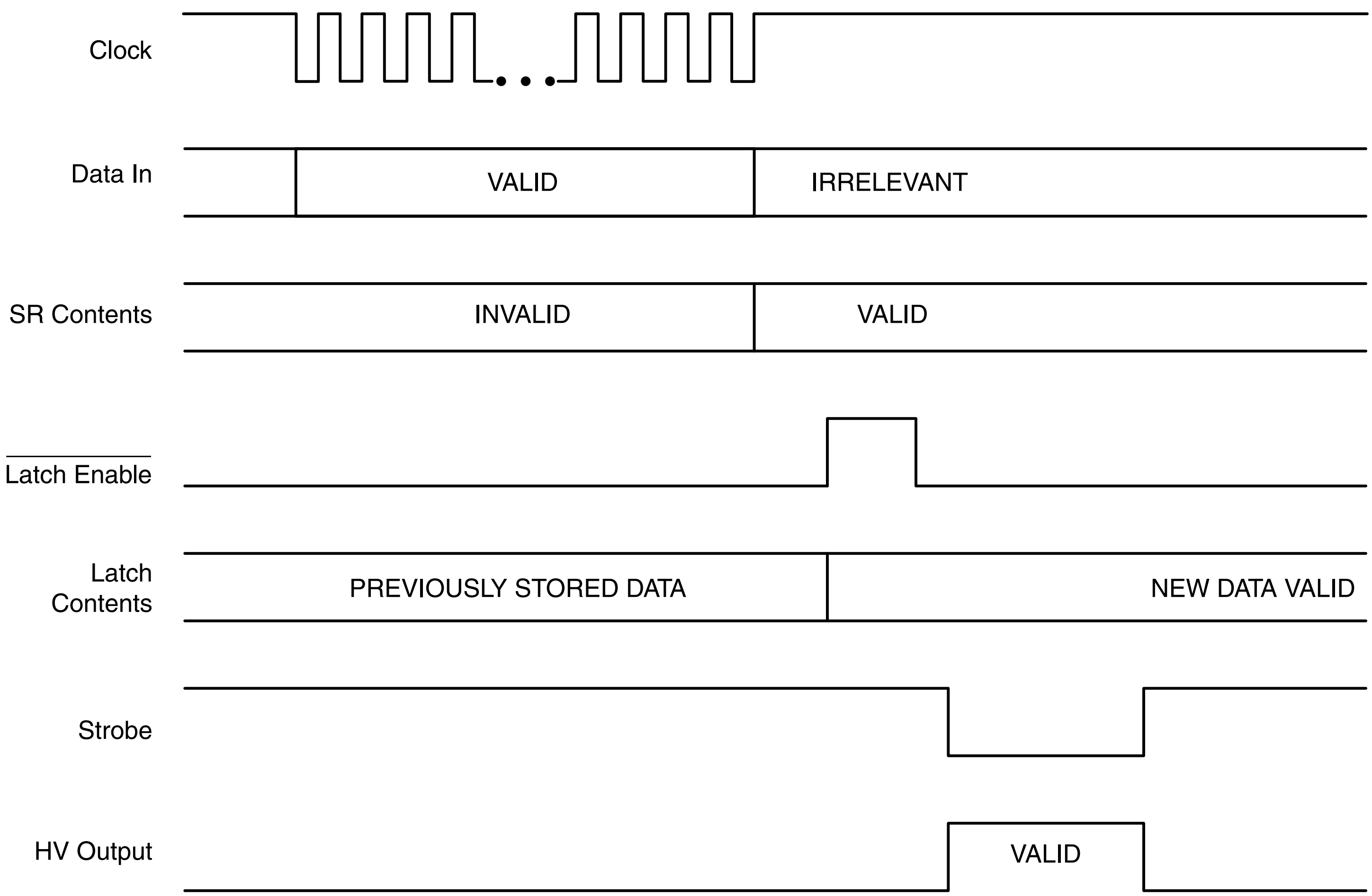
* Previous state.

### Output

| Data In | $\overline{LE}$ | STB | HV Outputs |
|---|---|---|---|
| X | X | H | All Low |
| H | H | L | High |
| L | H | L | Low |
| X | L | L | * |

* Previous state.

## Typical Operating Sequence



## Pin Descriptions

### 40-Lead PDIP (P)

| Pin # | Function |
|---|---|
| 1 | VPP |
| 2 | SERIAL OUT |
| 3 | $HV_{OUT}32$ |
| 4 | $HV_{OUT}31$ |
| 5 | $HV_{OUT}30$ |
| 6 | $HV_{OUT}29$ |
| 7 | $HV_{OUT}28$ |
| 8 | $HV_{OUT}27$ |
| 9 | $HV_{OUT}26$ |
| 10 | $HV_{OUT}25$ |
| 11 | $HV_{OUT}24$ |
| 12 | $HV_{OUT}23$ |
| 13 | $HV_{OUT}22$ |
| 14 | $HV_{OUT}21$ |

| Pin # | Function |
|---|---|
| 15 | $HV_{OUT}20$ |
| 16 | $HV_{OUT}19$ |
| 17 | $HV_{OUT}18$ |
| 18 | $HV_{OUT}17$ |
| 19 | STROBE |
| 20 | GND |
| 21 | CLOCK |
| 22 | $\overline{LE}$ |
| 23 | $HV_{OUT}16$ |
| 24 | $HV_{OUT}15$ |
| 25 | $HV_{OUT}14$ |
| 26 | $HV_{OUT}13$ |
| 27 | $HV_{OUT}12$ |
| 28 | $HV_{OUT}11$ |

| Pin # | Function |
|---|---|
| 29 | $HV_{OUT}10$ |
| 30 | $HV_{OUT}9$ |
| 31 | $HV_{OUT}8$ |
| 32 | $HV_{OUT}7$ |
| 33 | $HV_{OUT}6$ |
| 34 | $HV_{OUT}5$ |
| 35 | $HV_{OUT}4$ |
| 36 | $HV_{OUT}3$ |
| 37 | $HV_{OUT}2$ |
| 38 | $HV_{OUT}1$ |
| 39 | DATA IN |
| 40 | VDD |

### 44-Lead PLCC (PJ)

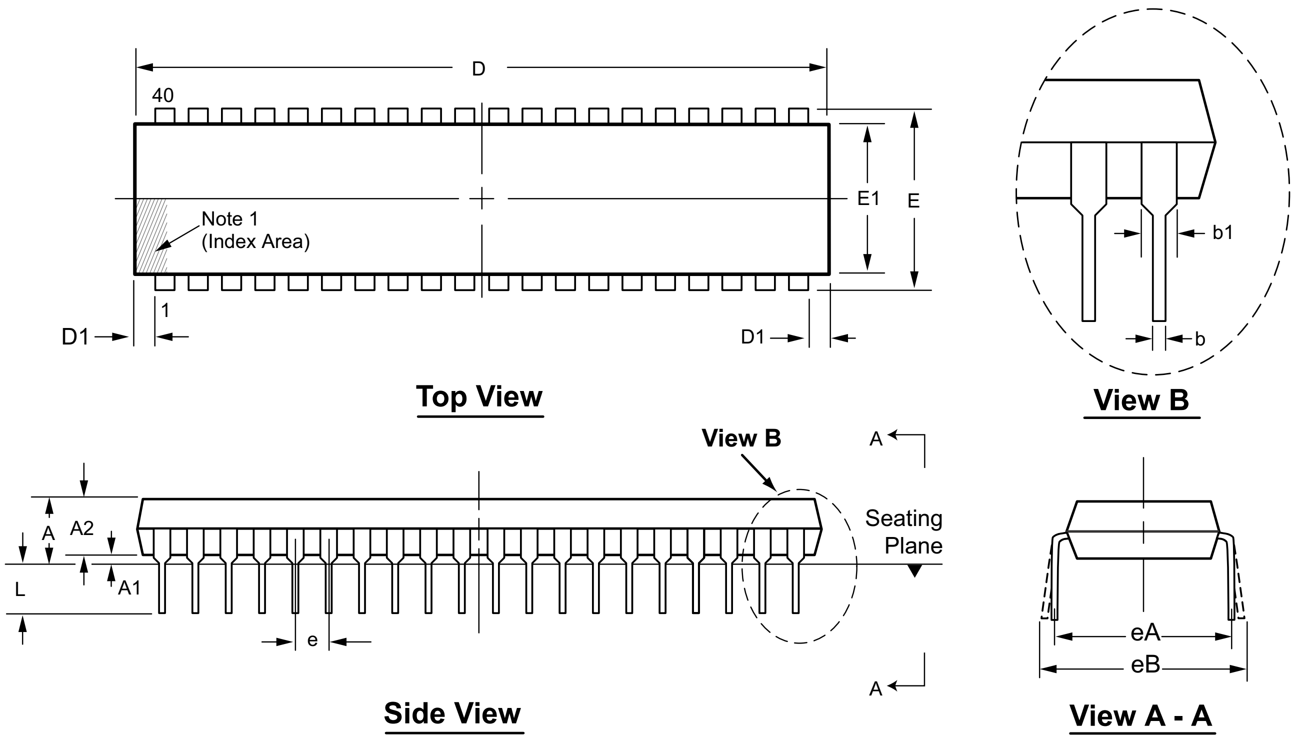
| Pin # | Function |
|---|---|
| 1 | VPP |
| 2 | SERIAL OUT |
| 3 | $HV_{OUT}32$ |
| 4 | $HV_{OUT}31$ |
| 5 | $HV_{OUT}30$ |
| 6 | NC |
| 7 | $HV_{OUT}29$ |
| 8 | $HV_{OUT}28$ |
| 9 | $HV_{OUT}27$ |
| 10 | $HV_{OUT}26$ |
| 11 | $HV_{OUT}25$ |
| 12 | $HV_{OUT}24$ |
| 13 | $HV_{OUT}23$ |
| 14 | $HV_{OUT}22$ |
| 15 | $HV_{OUT}21$ |

| Pin # | Function |
|---|---|
| 16 | $HV_{OUT}20$ |
| 17 | $HV_{OUT}19$ |
| 18 | N/C |
| 19 | $HV_{OUT}18$ |
| 20 | $HV_{OUT}17$ |
| 21 | STROBE |
| 22 | GND |
| 23 | CLOCK |
| 24 | $\overline{LE}$ |
| 25 | $HV_{OUT}16$ |
| 26 | $HV_{OUT}15$ |
| 27 | $HV_{OUT}14$ |
| 28 | N/C |
| 29 | N/C |
| 30 | $HV_{OUT}13$ |

| Pin # | Function |
|---|---|
| 31 | $HV_{OUT}12$ |
| 32 | $HV_{OUT}11$ |
| 33 | $HV_{OUT}10$ |
| 34 | $HV_{OUT}9$ |
| 35 | $HV_{OUT}8$ |
| 36 | $HV_{OUT}7$ |
| 37 | $HV_{OUT}6$ |
| 38 | $HV_{OUT}5$ |
| 39 | $HV_{OUT}4$ |
| 40 | $HV_{OUT}3$ |
| 41 | $HV_{OUT}2$ |
| 42 | $HV_{OUT}1$ |
| 43 | DATA IN |
| 44 | VDD |

# 40-Lead PDIP (.600in Row Spacing) Package Outline (P)

### *2.095x.580in body (max), .250in height (max), .100in pitch*



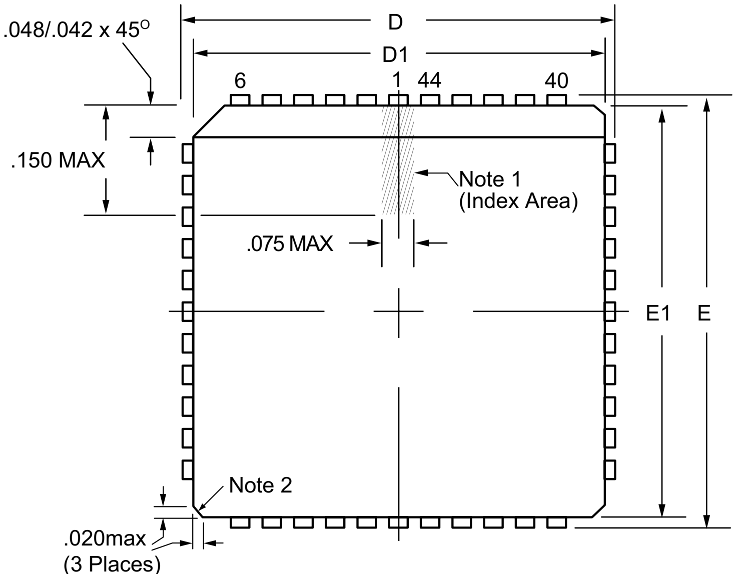

***Note:***

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 Identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

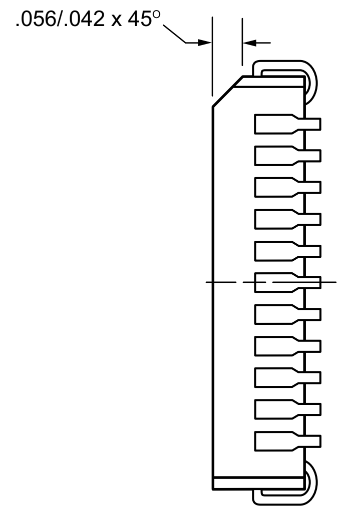
| Symbol | | A | A1 | A2 | b | b1 | D | D1 | E | E1 | e | eA | eB | L |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Dimension (inches) | MIN | .140* | .015 | .125 | .014 | .030 | 1.980 | .065† | .590† | .485 | .100 BSC | .600 BSC | .600* | .115 |
| | NOM | - | - | - | - | - | - | - | - | - | | | - | - |
| | MAX | .250 | .055* | .195 | .023† | .070 | 2.095 | .085* | .625 | .580 | | | .700 | .200 |

*JEDEC Registration MS-011, Variation AC, Issue B, June, 1988.*
* *This dimension is not specified in the original JEDEC drawing. The value listed is for reference only.*
† *This dimension is a non-JEDEC dimension.*
***Drawings not to scale.***
***Supertex Doc. #:** DSPD-40DIPP, Version B090608.*

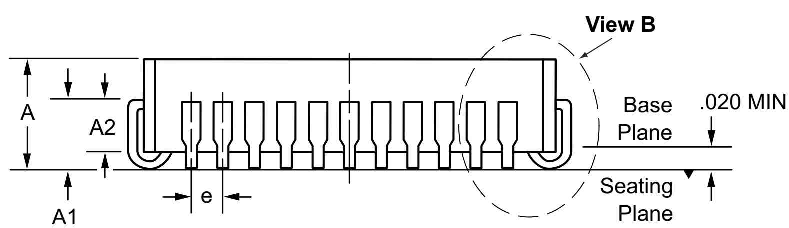
# 44-Lead PLCC Package Outline (PJ)
## *.653x.653in body, .180in height (max), .050in pitch*



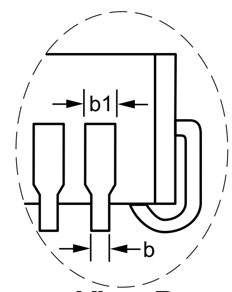

**Top View**




**Vertical Side View**




**Horizontal Side View**




**View B**

***Notes:***
1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Actual shape of this feature may vary.*

| Symbol | | A | A1 | A2 | b | b1 | D | D1 | E | E1 | e |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Dimension (inches) | MIN | .165 | .090 | .062 | .013 | .026 | .685 | .650 | .685 | .650 | .050 BSC |
| | NOM | .172 | .105 | - | - | - | .690 | .653 | .690 | .653 | |
| | MAX | .180 | .120 | .083 | .021 | .036† | .695 | .656 | .695 | .656 | |

*JEDEC Registration MS-018, Variation AC, Issue A, June, 1993.*
*† This dimension is a non-JEDEC dimension.*
***Drawings not to scale.***
***Supertex Doc. #:** DSPD-44PLCCPJ, Version D092408.*

*(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)*



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