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UniIC

4Gb DDR3(L) X16 SDRAM

EU RoHS Compliant Products

Data Sheet

Rev. F

Revision History		
Date	**Revision**	**Subjects (major changes since last revision)**
2013/09/01	A	Initial Release
2016/03/01	B	Change to UniIC Format
2016/04/26	C	Combine DDR3(1.5V) and DDR3L(1.35V)
2016/12/20	D	Add the “I” grade products
2017/04/11	E	Add the component HXB(I)15H4G160AF–11M
2017/08/08	F	1. Update the IDD； 2. Update the Interface Capacitance

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1 Overview

This chapter gives an overview of the 4Gbit DDR3(L) SDRAM component product and describes its main characteristics.

1.1 Features

The 4Gbit DDR3(L) SDRAM offers the following key features:

- VDD, VDDQ= 1.283V to 1.45V(Backward compatible for VDD, VDDQ=1.5 V ± 0.075V)
- Data rate : 800Mbps/1066Mbps/1333Mbps/1600Mbps/1866Mbps
- SDRAM configurations with ×16 data in/outputs
- Page Size: 2 KByte page size
  Row address: A0 to A14
  Column address: A0 to A9
- Asynchronous /RESET
- Auto-Precharge operation for read and write commands
- Refresh, Self-Refresh and power saving Power-down modes; Auto Self-refresh (ASR) and Partial array self refresh (PASR)
- Average Refresh Period 7.8 µs at a T_{OPER} up to 85 °C, 3.9 µs up to 95 °C
- Operating temperature range:
  Comercial: 0- 95 °C
  Industrial:-40-95°C
- Data mask function for write operation
- Commands can be entered on each positive clock edge
- Data and data mask are referenced to both edges of a differential data strobe pair (double data rate)
- CAS latency (CL): 5, 6, 7, 8, 9 ,10 ,11,13
- Posted CAS with programmable additive latency (AL = 0, CL–1 and CL–2) for improved command, address and data bus efficiency
- Read Latency RL = AL + CL
- Programmable CAS Write Latency (CWL) per operating frequency: 5,6,7,8,9
- Write Latency WL = AL + CWL
- Burst length 8 (BL8) and burst chop 4(BC4) modes: fixed via mode register (MRS) or selectable On-The-Fly (OTF)
- Programmable read burst ordering: interleaved or sequential
- Multi-purpose register (MPR) for readout of non-memory related information
- System level timing calibration support via write leveling and MPR read pattern
- Differential clock inputs (CK and /CK)
- Bi-directional, differential data strobe pair (DQS AND /DQS) is transmitted / received with data. Edge aligned with read data and center-aligned with write data
- DLL aligns transmitted read data and strobe pair transition with clock
- Programmable on-die termination (ODT) for data, data mask and differential strobe pairs
- Dynamic ODT mode for improved signal integrity and pre-selectable termination impedances during writes
- ZQ Calibration for output driver and on-die termination using external reference resistor to ground
- Driver strength : RZQ/7, RZQ/6 (RZQ = 240 Ω)
- Lead and halogen free packages: 96 ball (PG-TFBGA-96)
- Interface: SSTL_15

1.2 Product List

Table 1 shows all possible products within the 4Gbit DDR3(L) SDRAM component generation. Availability depends on application needs. For UniICpart number nomenclature see **Chapter 6**.

TABLE 1
Ordering Information for 4Gbit DDR3(L) Components

UniIC Part Number	Max. Clock frequency	CAS-RCD-RP latencies	Speed Sort Name	Package
4G bit DDR3 SDRAM Components in × 16 Organization (256 Mbit × 16)				
HXB(I)15H4G160AF–25E	400 MHz	6–6–6	DDR3–800E	PG-TFBGA-96
HXB(I)15H4G160AF–19F	533 MHz	7–7–7	DDR3–1066F	PG-TFBGA-96
HXB(I)15H4G160AF–15H	667 MHz	9–9–9	DDR3–1333H	PG-TFBGA-96
HXB(I)15H4G160AF–13K	800 MHz	11-11-11	DDR3–1600K	PG-TFBGA-96
HXB(I)15H4G160AF–11M	933 MHz	13-13-13	DDR3–1866M	PG-TFBGA-96
4G bit DDR3L SDRAM Components in × 16 Organization (256 Mbit × 16)				
HXB(I)13H4G160AF–15H	667 MHz	9–9–9	DDR3L–1333H	PG-TFBGA-96
HXB(I)13H4G160AF–13K(T)	800 MHz	11-11-11	DDR3L–1600K	PG-TFBGA-96

1.3 DDR3(L) SDRAM Addressing

TABLE 2
4Gbit DDR3(L) SDRAM Addressing

Configuration	**256Mb × 16**	**Note**
Internal Organization	8 banks × 32M bits × 16	
Number of Banks	8	
Bank Address	BA[2:0]	
Row Address	A[14:0]	
Column Address	A[9:0]	
Page Size	2KB	1)
Auto-Precharge	A10 | AP	
Burst length on-the-fly bit	A12 | /BC	

1) Page size is the number of bytes of data delivered from the array to the internal sense amplifiers when an ACTIVE command is registered. Page size is per memory bank and calculated as follows: Page Size = $2^{COLBITS} \times ORG/8$, where COLBITS is the number of column address bits and ORG is the number of DQ bits for a given SDRAM configuration (×4, ×8 or ×16).

1.4 Package Ballout

Figure 1 show the ballouts for DDR3(L) SDRAM components. See **Chapter 6** for package outlines.

1.4.1 Ballout for 256 Mb ×16 Components

FIGURE 1
Ballout for 256 Mb ×16 Components (PG-TFBGA-96)

	1	2	3	4	5	6	7	8	9	
A	V_{DDQ}	DQU5	DQU7				DQU4	V_{DDQ}	V_{SS}	**A**
B	V_{SSQ}	V_{DD}	V_{SS}				$\overline{\text{DQSU}}$	DQU6	V_{SSQ}	**B**
C	V_{DDQ}	DQU3	DQU1				DQSU	DQU2	V_{DDQ}	**C**
D	V_{SSQ}	V_{DDQ}	DMU				DQU0	V_{SSQ}	V_{DD}	**D**
E	V_{SS}	V_{SSQ}	DQL0				DML	V_{SSQ}	V_{DDQ}	**E**
F	V_{DDQ}	DQL2	DQSL				DQL1	DQL3	V_{SSQ}	**F**
G	V_{SSQ}	DQL6	$\overline{\text{DQSL}}$				V_{DD}	V_{SS}	V_{SSQ}	**G**
H	V_{REFDQ}	V_{DDQ}	DQL4				DQL7	DQL5	V_{DDQ}	**H**
J	NC	V_{SS}	$\overline{\text{RAS}}$				CK	V_{SS}	NC	**J**
K	ODT	V_{DD}	$\overline{\text{CAS}}$				$\overline{\text{CK}}$	V_{DD}	CKE	**K**
L	NC	$\overline{\text{CS}}$	$\overline{\text{WE}}$				A10/AP	ZQ	NC	**L**
M	V_{SS}	BA0	BA2				NC	V_{REFCA}	V_{SS}	**M**
N	V_{DD}	A3	A0				A12/$\overline{\text{BC}}$	BA1	V_{DD}	**N**
P	V_{SS}	A5	A2				A1	A4	V_{SS}	**P**
R	V_{DD}	A7	A9				A11	A6	V_{DD}	**R**
T	V_{SS}	$\overline{\text{RESET}}$	A13				A14	A8	V_{SS}	**T**

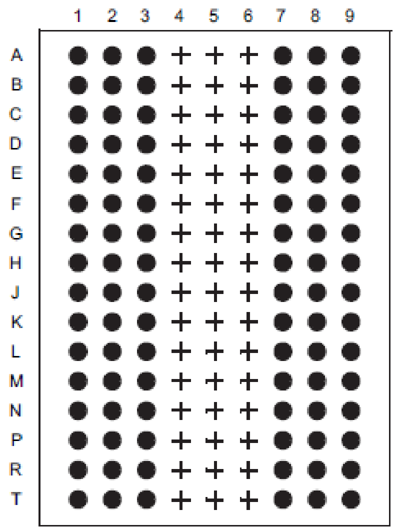
Ball Locations (x16)

● Populated ball

+ Ball not populated

Top view

(See the balls through the package)



1.5 Input / Output Signal Functional Description

TABLE 3
Input / Output Signal Functional Description

Symbol	Type	Function
CK, /CK	Input	**Clock:** CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK.
CKE	Input	**Clock Enable:** CKE High activates, and CKE Low deactivates internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (active row in any bank). CKE is asynchronous for Self-Refresh exit. After V_{REFCA} and V_{REFDQ} have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained High throughout read and write accesses. Input buffers, excluding CK, /CK, ODT, CKE and /RESET are disabled during Power-down. Input buffers, excluding CKE and RESET are disabled during self refresh.
/CS	Input	**Chip Select:** All commands are masked when /CS is registered High. /CS provides for external Rank selection on systems with multiple ranks. /CS is considered part of the command code.
/RAS, /CAS, /WE	Input	**Command Inputs: /**RAS, /CAS and /WE (along with /CS) define the command being entered.
ODT	Input	**On-Die Termination:** ODT (registered High) enables termination resistance internal to the DDR3(L) SDRAM. When enabled, ODT is only applied to each DQ, DQS, /DQS and DM signal for ×8 configurations. The ODT signal will be ignored if the Mode Register MR1 is programmed to disable ODT and during Self Refresh.
DM (DMU), (DML)	Input	**Input Data Mask :** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS.
BA0 - BA2	Input	**Bank Address Inputs:** Define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a mode register set cycle.
A0 - A14	Input	**Address Inputs:** Provides the row address for Active commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12 | /BC have additional functions, see below). The address inputs also provide the op-code during Mode Register Set commands. For numbers of addresses used on this assembly see **Table 2**.

Symbol	Type	Function
A10 | AP	Input	**Auto-Precharge:** A10 | AP is sampled during Read/Write commands to determine whether Auto-Precharge should be performed to the accessed bank after the Read/Write operation. (High: Auto-Precharge, Low: no Auto-Precharge). A10 | AP is sampled during Precharge command to determine whether the Precharge applies to one bank (A10 Low) or all banks (A10 High). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 | /BC	Input	**Burst Chop:** A12 | /BC is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (High: no burst chop, Low: burst chopped). See **"Command Truth Table" on Page 9** for details.
DQ	Input/ Output	**Data Input/Output:** Bi-directional data bus.
DQSL,/DQSL DQSU, /DQSU	Input/ Output	**Data Strobe:** Output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQSL and DQSU are paired with differential signals /DQSL and /DQSU, respectively, to provide differential pair signaling to the system during reads and writes. DDR3(L) SDRAM supports differential data strobe only and does not support single-ended.
/RESET	Input	**Active Low Asynchronous Reset:** Reset is active when /RESET is Low, and inactive when /RESET is High. /RESET must be High during normal operation. /RESET is a CMOS rail to rail signal with DC High and Low are 80% and 20% of V_{DD}, /RESET active is destructive to data contents.
NC	—	**No Connect:** no internal electrical connection is present
V_{DDQ}	Supply	**DQ Power Supply:** 1.283V to 1.45V or 1.5 V ± 0.075V
V_{SSQ}	Supply	**DQ Ground**
V_{DD}	Supply	**Power Supply:** 1.283V to 1.45V or 1.5 V ± 0.075V
V_{SS}	Supply	**Ground**
V_{REFDQ}	Supply	**Reference Voltage for DQ**
V_{REFCA}	Supply	**Reference Voltage for Command and Address inputs**
ZQ	Supply	Reference ball for ZQ calibration

Note: Input only pins (BA0-BA2, A0-A14, /RAS, /CAS, /WE, /CS, CKE, ODT, and /RESET) do not supply termination

2 Functional Description

2.1 Truth Tables

The truth tables list the input signal values at a given clock edge which represent a command or state transition expected to be executed by the DDR3(L) SDRAM. **Table 4** lists all valid commands to the DDR3(L) SDRAM. For a detailed description of the various power mode entries and exits please refer to **Table 5**. In addition, the DM functionality is described in **Table 6**.

TABLE 4
Command Truth Table

Function	Abbreviation	CKE		CS	RAS	CAS	WE	BA0 - BA2	A13 - A14	A12 / BC	A10 / AP	A0 - A9,A11	Notes
		Previous Cycle	Current Cycle										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	V	7,9,12
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	7,8,9,12
				L	H	H	H	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	
Precharge all Banks	PREA	H	H	L	L	H	L	V	V	V	H	V	
Bank Activate	ACT	H	H	L	L	H	H	BA	Row Address (RA)				
Write (Fixed BL8 or BL4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Write (BL4, on the Fly)	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	
Write with Auto Precharge (Fixed BL8 or BL4)	WRA	H	H	L	H	L	L	BA	RFU	V	H	CA	
Write with Auto Precharge (BL4, on the Fly)	WRAS4	H	H	L	H	L	L	BA	RFU	L	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	L	L	BA	RFU	H	H	CA	
Read (Fixed BL8 or BL4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	
Read (BL4, on the Fly)	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	
Read with Auto Precharge (Fixed BL8 or BL4)	RDA	H	H	L	H	L	H	BA	RFU	V	H	CA	
Read with Auto Precharge (BL4, on the Fly)	RDAS4	H	H	L	H	L	H	BA	RFU	L	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	L	H	BA	RFU	H	H	CA	
No Operation	NOP	H	H	L	H	H	H	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	11
ZQ calibration Long	ZQCL	H	H	L	H	H	L	X	X	X	H	X	
ZQ calibration Short	ZQCS	H	H	L	H	H	L	X	X	X	L	X	
Power Down Entry	PDE	H	L	L	H	H	H	V	V	V	V	V	6,12
				H	X	X	X	X	X	X	X	X	
Power Down Exit	PDX	L	H	L	H	H	H	V	V	V	V	V	6,12
				H	X	X	X	X	X	X	X	X	

Note :

1. All DDR3(L) SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock. The MSB of BA, RA, and CA are device density and configuration dependant
2. RESET is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.
3. Bank addresses (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register
4. “V” means “H or L (but a defined logic level)” and “X” means either “defined or undefined (like floating) logic level”
5. Burst reads or writes cannot be terminated or interrupted and Fixed/on the fly BL will be defined by MRS
6. The Power Down Mode does not perform any refresh operations.
7. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
8. Self refresh exit is asynchronous.
9. V_{REF}(Both V_{REFDQ} and V_{REFCA}) must be maintained during Self Refresh operation.
10. The No Operation command (NOP) should be used in cases when the DDR3(L) SDRAM is in an idle or a wait state. The purpose of the No Operation command (NOP) is to prevent the DDR3(L) SDRAM from registering any unwanted commands between operations. A No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.
11. The Deselect command performs the same function as a No Operation command.
12. Refer to the CKE Truth Table for more detail with CKE transition

TABLE 5

Clock Enable (CKE) Truth Table for Synchronous Transitions

Current State [1]	**CKE(N-1)**[2]	**CKE(N)**[2]	**Command (N)**[3]	**Action (N)**[3]	**Note**
	Previous Cycle	**Current Cycle**	**/RAS, /CAS, /WE, /CS**		
Power Down	L	L	X	Maintain Power Down	4)5)6)7)8)9)
	L	H	DES or NOP	Power Down Exit	4)5)6)7)8)10)
Self Refresh	L	L	X	Maintain Self Refresh	4)5)6)7)9)11)
	L	H	DES or NOP	Self Refresh Exit	4)5)6)7)11)12)13)
Bank(s) Active	H	L	DES or NOP	Active Power Down Entry	4)5)6)7)8)10)14)
Reading	H	L	DES or NOP	Power Down Entry	4)5)6)7)8)10)14)15)
Writing	H	L	DES or NOP	Power Down Entry	4)5)6)7)8)10)14)15)
Precharging	H	L	DES or NOP	Power Down Entry	4)5)6)7)8)10)14)15)
Refreshing	H	L	DES or NOP	Precharge Power Down Entry	4)5)6)7)10)
All Banks Idle	H	L	DES or NOP	Precharge Power Down Entry	4)5)6)7)10)8)14)16)
	H	L	REF	Self Refresh Entry	4)5)6)7)14)16)17)
Any other state	Refer to **“Command Truth Table” on Page 9** for more detail with all command signals				4)5)6)7)18)

1) Current state is defined as the state of the DDR3(L) SDRAM immediately prior to clock edge N.
2) CKE(N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
3) COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N),ODT is not included here.
4) All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5) The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
6) CKE must be registered with the same value on $t_{CKE.MIN}$ consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the $t_{CKE.MIN}$ clocks of registeration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of $t_{IS} + t_{CKE.MIN} + t_{IH}$.
7) DES and NOP are defined in **“Command Truth Table” on Page 9**.
8) The Power Down does not perform any refresh operations
9) X means Don’t care (including floating around V_{REFCA}) in Self Refresh and Power Down. It also applies to address pins.
10) Valid commands for Power Down Entry and Exit are NOP and DES only
11) V_{REF} (both V_{REFCA} and V_{REFDQ}) must be maintained during Self Refresh operation.
12) On Self Refresh Exit DES or NOP commands must be issued on every clock edge occurring during the t_{XS} period. Read, or ODT commands may be issued only after t_{XSDLL} is satisfied.
13) Valid commands for Self Refresh Exit are NOP and DES only.
14) Self Refresh can not be entered while Read or Write operations are in progress.
15) If all banks are closed at the conclusion of a read, write or precharge command then Precharge Power-down is entered, otherwise Active Power-down is entered.

16) ‘Idle state’ is defined as all banks are closed (t_{RP}, t_{DAL}, etc. satisfied), no data bursts are in progress, CKE is High, and all timings from previous operations are satisfied (t_{MRD}, t_{MOD}, t_{RFC}, $t_{ZQ.INIT}$, $t_{ZQ.OPER}$, t_{ZQCS}, etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied (t_{XS}, t_{XP}, t_{XPDLL}, etc.).
17) Self Refresh mode can only be entered from the All Banks Idle state.
18) Must be a legal command as defined in **“Command Truth Table” on Page 9**.

TABLE 6
Data Mask (DM) Truth Table

Name (Function)	**DM**	**DQs**
Write Enable	L	Valid
Write Inhibit	H	X

2.2 Mode Register 0 (MR0)

The mode register MR0 stores the data for controlling various operating modes of DDR3(L) SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, WR (write recovery time for auto-precharge) and DLL control for precharge Power-Down, which includes various vendor specific options to make DDR3(L) SDRAM useful for various applications. The mode register is written by asserting Low on /CS, /RAS, /CAS, /WE, BA0, BA1, and BA2, while controlling the states of address pins according to **Table 7**.

BA2	BA1	BA0	A14~A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	**0**	**0**	**0**$^{1)}$	**PPD**	**WR**			**DLL**	**TM**	**CL**			**RBT**	**CL**	**BL**	

TABLE 7
MR0 Mode register Definition (BA[2:0]=000B)

Field	**Bits**$^{1)}$	**Description**
BL	A[1:0]	**Burst Length (BL) and Control Method** Number of sequential bits per DQ related to one Read/Write command. 00_B **BL8MRS** mode with fixed burst length of 8. A12 | /BC at Read or Write command time is Don't care at read or write command time. 01_B **BLOTF** on-the-fly (OTF) enabled using A12 | /BC at Read or Write command time. When A12 | /BC is High during Read or Write command time a burst length of 8 is selected (BL8OTF mode). When A12 | /BC is Low, a burst chop of 4 is selected (BC4OTF mode). Auto-Precharge can be enabled or disabled. 10_B **BC4MRS** mode with fixed burst chop of 4 with $t_{CCD} = 4 \times n_{CK}$. A12 | /BC is Don't care at Read or Write command time. 11_B **TBD** Reserved
RBT	A3	**Read Burst Type** 0_B Nibble Sequential 1_B Interleaved
CL	A[6:4,2]	**CAS Latency (CL)** CAS Latency is the delay, in clock cycles, between the internal Read command and the availability of the first bit of output data. *Note: For more information on the supported CL and AL settings based on the operating clock frequency, refer to **"Speed Bins" on Page 32**.* *Note: All other bit combinations are reserved.* 0000_B RESERVED 0010_B 5 0100_B 6 0110_B 7 1000_B 8 1010_B 9 1100_B 10 1110_B 11

Field	**Bits**[1]	**Description**
TM	A7	**Test Mode** The normal operating mode is selected by MR0(bit A7 = 0) and all other bits set to the desired values shown in this table. Programming bit A7 to a 1 places the DDR3(L) SDRAM into a test mode that is only used by the SDRAM manufacturer and should NOT be used. No operations or functionality is guaranteed if A7 = 1. 0_B Normal Mode 1_B Vendor specific test mode
DLLres	A8	**DLL Reset** The internal DLL Reset bit is self-clearing, meaning it returns back to the value of 0 after the DLL reset function has been issued. Once the DLL is enabled, a subsequent DLL Reset should be applied. Any time the DLL reset function is used, t_{DLLK} must be met before any functions that require the DLL can be used (i.e. Read commands or synchronous ODT operations). 0_B No DLL Reset 1_B DLL Reset triggered
WR	A[11:9]	**Write Recovery for Auto-Precharge** Number of clock cycles for write recovery during Auto-Precharge. WR_{MIN} in clock cycles is calculated by dividing $t_{WR.MIN}$ (in ns) by the actual $t_{CK.AVG}$ (in ns) and rounding up to the next integer: WR.MIN [n_{CK}] = Roundup($t_{WR.MIN}$[ns] / $t_{CK.AVG}$[ns]). The WR value in the mode register must be programmed to be equal or larger than WR.MIN. The resulting WR value is also used with t_{RP} to determine t_{DAL}. Since WR of 9 and 11 is not implemented in DDR3(L) and the above formula results in these values, higher values have to be programmed. 000_B Reserved 001_B 5 010_B 6 011_B 7 100_B 8 101_B 10 110_B 12 111_B Reserved
PPD	A12	**Precharge Power-Down DLL Control** Active Power-Down will always be with DLL-on. Bit A12 will have no effect in this case. For Precharge Power-Down, bit A12 in MR0 is used to select the DLL usage as shown below. 0_B **Slow Exit.** DLL is frozen during precharge Power-down.Read and synchronous ODT commands are only allowed after t_{XPDLL}. 1_B **Fast Exit.** DLL remains on during precharge Power-down.Any command can be applied after t_{XP}, provided that other timing parameters are satisfied.

1) A13, A14 - even if not available on a specific device - must be programmed to 0_B.

2.3 Mode Register 1 (MR1)

The Mode Register MR1 stores the data for enabling or disabling the DLL, output driver strength, R_{TT}_Nom impedance, additive latency (AL), Write leveling enable and Qoff (output disable). The Mode Register MR1 is written by asserting Low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, High on BA0 and Low on BA1and BA2, while controlling the states of address pins according to **Table 8**.

BA2	BA1	BA0	A14~ A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	**0**	**1**	**0**$^{1)}$	**Qoff**	**0**	**0**	**RTT_ nom**	**0**	**Level**	**RTT_ nom**	**DIC**	**AL**		**RTT_ nom**	**DIC**	**DLL**

TABLE 8
MR1 Mode Register Definition (BA[2:0]=001B)

Field	**Bits**$^{1)}$	**Description**
DLLdis	A0	**DLL Disable** The DLL must be enabled for normal operation. DLL enable is required during power up initialization, after reset and upon returning to normal operation after having the DLL disabled. During normal operation (DLL-on) with MR1(A0 = 0), the DLL is automatically disabled when entering Self-Refresh operation and is automatically re-enabled and reset upon exit of Self-Refresh operation. Any time the DLL is enabled, a DLL reset must be issued afterwards. Any time the DLL is reset, t_{DLLK} clock cycles must occur before a Read or synchronous ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the t_{DQSCK}, t_{AON}, t_{AOF} or t_{ADC} parameters. During t_{DLLK}, CKE must continuously be registered high. DDR3(L) SDRAM does not require DLL for any Write operation. 0_B DLL is enabled 1_B DLL is disabled
DIC	A[5, 1]	**Output Driver Impedance Control** *Note: All other bit combinations are reserved.* 00: RZQ/6 01_B Nominal Drive Strength RON34 = RQZ/7 (nominal 34.3 Ω, with nominal RZQ = 240 Ω)
R_{TT_NOM}	A[9, 6, 2]	**Nominal Termination Resistance of ODT** **Notes** 1. *If R_{TT_NOM} is used during Writes, only the values $R_{ZQ}/2$, $R_{ZQ}/4$ and $R_{ZQ}/6$ are allowed.* 2. *In Write leveling Mode (MR1[bit7] = 1) with MR1[bit12] = 1, all R_{TT}_Nom settings are allowed; in Write Leveling Mode (MR1[bit7] = 1) with MR1[bit12] = 0, only R_{TT_NOM} settings of $R_{ZQ}/2$, $R_{ZQ}/4$ and $R_{ZQ}/6$ are allowed.* 3. *All other bit combinations are reserved.* 000_B ODT disabled, R_{TT_NOM} = off, Dynamic ODT mode disabled 001_B RTT60 = RZQ / 4 (nominal 60 Ω with nominal RZQ = 240 Ω) 010_B RTT120 = RZQ / 2 (nominal 120 Ω with nominal RZQ = 240 Ω 011_B RTT40 = RZQ / 6 (nominal 40 Ω with nominal RZQ = 240 Ω) 100_B RTT20 = RZQ / 12 (nominal 20 Ω with nominal RZQ = 240 Ω) 101_B RTT30 = RZQ / 8 (nominal 30 Ω with nominal RZQ = 240 Ω)

Field	Bits[1]	Description
AL	A[4, 3]	**Additive Latency (AL)** Any read or write command is held for the time of Additive Latency (AL) before it is issued as internal read or write command. **Notes** *1. AL has a value of CL - 1 or CL - 2 as per the CL value programmed in the MR0 register.* 00_B AL = 0 (AL disabled) 01_B AL = CL - 1 10_B AL = CL - 2 11_B Reserved
Write Leveling enable	A7	**Write Leveling Mode** 0_B **Write Leveling Mode** Disabled, Normal operation mode 1_B **Write Leveling Mode** Enabled
TDQS enable	A11	0: Disabled 1: Enabled
Qoff	A12	**Output Disable** Under normal operation, the SDRAM outputs are enabled during read operation and write leveling for driving data (Qoff bit in the MR1 is set to 0_B). When the Qoff bit is set to 1_B, the SDRAM outputs (DQ, DQS, /DQS) will be disabled - also during write leveling. Disabling the SDRAM outputs allows users to run write leveling on multiple ranks and to measure I_{DD} currents during Read operations, without including the output. 0_B Output buffer enabled 1_B Output buffer disabled

1) A13, A14 - even if not available on a specific device - must be programmed to 0_B.

2.4 Mode Register 2 (MR2)

The Mode Register MR2 stores the data for controlling refresh related features, R_{TT_WR} impedance, and CAS write latency. The Mode Register MR2 is written by asserting Low on CS, RAS, CAS, WE, High on BA1 and Low on BA0 and BA2, while controlling the states of address signals according to **Table 9**.

BA2	BA1	BA0	A14~A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	**1**	**0**	**0** 1)	**0**	**0**	**Rtt_WR**		**0**	**SRT**	**ASR**	**CWL**			**PASR**		

TABLE 9
MR2 Mode Register Definition (BA[2:0]=010B)

Field	**Bits** 1)	**Description**
PASR	A[2:0]	**Partial Array Self Refresh (PASR)** If PASR (Partial Array Self Refresh) is enabled, data located in areas of the array beyond the specified self refresh location may get lost if self refresh is entered. During non-self-refresh operation, data integrity will be maintained if t_{REFI} conditions are met. 000_B Full array (Banks 000_B - 111_B) 001_B Half Array(Banks 000_B - 011_B) 010_B Quarter Array(Banks 000_B - 001_B) 011_B 1/8th array (Banks 000_B) 100_B 3/4 array(Banks 010_B - 111_B) 101_B Half array(Banks 100_B - 111_B) 110_B Quarter array(Banks 110_B - 111_B) 111_B 1/8th array(Banks 111_B)
CWL	A[5:3]	**CAS Write Latency (CWL)** Number of clock cycles from internal write command to first write data in. *Note: All other bit combinations are reserved.* 000_B 5 (3.3 ns $\geq t_{CK.AVG} \geq$ 2.5 ns) 001_B 6 (2.5 ns > $t_{CK.AVG} \geq$ 1.875 ns) 010_B 7 (1.875 ns > $t_{CK.AVG} \geq$ 1.5 ns) 011_B 8 (1.5 ns > $t_{CK.AVG} \geq$ 1.25 ns) *Note: Besides CWL limitations on $t_{CK.AVG}$, there are also $t_{AA.MIN/MAX}$ restrictions that need to be observed. For details, please refer to **Chapter 4.1**, **Speed Bins**.*
RFU	A6	**0: Manual SR reference (SRT)** **1: ASR enable (Optional)**.

Field	Bits[1]	Description
SRT	A7	**Self-Refresh Temperature Range (SRT)** The SRT bit must be programmed to indicate T_{OPER} during subsequent self refresh operation. 0_B Normal operating temperature range 1_B Extended operating temperature range
$R_{\mathrm{TT\_WR}}$	A[10:9]	**Dynamic ODT mode and $R_{\mathrm{TT\_WR}}$ Pre-selection** **Notes** 1. *All other bit combinations are reserved.* 2. *The R_{TT_WR} value can be applied during writes even when R_{TT_NOM} is disabled. During write leveling, Dynamic ODT is not available.* 00_B Dynamic ODT mode disabled 01_B Dynamic ODT mode enabled with $R_{\mathrm{TT\_WR}}$ = RZQ/4 = 60 Ω 10_B Dynamic ODT mode enabled with $R_{\mathrm{TT\_WR}}$ = RZQ/2 = 120Ω

[1] A13, A14 - even if not available on a specific device - must be programmed to 0_B.

2.5 Mode Register 3 (MR3)

The Mode Register MR3 controls Multi purpose registers and optional On-die thermal sensor (ODTS) feature. The Mode Register MR3 is written by asserting Low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, High on BA1 and BA0, and Low on BA2 while controlling the states of address signals according to **Table 10**.

BA2	BA1	BA0	A14~A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	**1**	**1**	**0**[1]	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**MPR**	**MPR loc**	

TABLE 10
MR3 Mode Register Definition (BA[2:0]=011B)

Field	Bits[1]	Description
MPR loc	A[1:0]	**Multi Purpose Register Location** 00_B Pre-defined data pattern for read synchronization 01_B RFU 10_B RFU 11_B ODTS On-Die Thermal sensor readout (optional)
MPR	A2	**Multi Purpose Register Enable** *Note: When MPR is disabled, MR3 A[1:0] will be ignored.* 0_B MPR disabled, normal memory operation 1_B Dataflow from the Multi Purpose register MPR

1) A13, A14 - even if not available on a specific device - must be programmed to 0_B.

2.6 Burst Order

Accesses within a given burst may be interleaved or nibble sequential depending on the programmed bit A3 in the mode register MR0.

Regarding read commands, the lower 3 column address bits CA[2:0] at read command time determine the start address for the read burst.

Regarding write commands, the burst order is always fixed. For writes with a burst length of 8, the inputs on the lower 3 column address bits CA[2:0] are ignored during the write command. For writes with a burst being chopped to 4, the input on column address 2 (CA[2]) determines if the lower or upper four burst bits are selected. In this case, the inputs on the lower 2 column address bits CA[1:0] are ignored during the write command. The following table shows burst order versus burst start address for reads and writes of bursts of 8 as well as of bursts of 4 operation (burst chop).

TABLE 11
Bit Order during Burst

Burst Length	Command	Column Address 2:0			Interleaved Burst Sequence								Nibble Sequential Burst Sequence								Note
					Bit Order within Burst								Bit Order within Burst								
		CA2	CA1	CA0	1.	2.	3.	4.	5.	6.	7.	8.	1.	2.	3.	4.	5.	6.	7.	8.	
8	READ	0	0	0	**0**	1	2	3	**4**	5	6	7	**0**	1	2	3	**4**	5	6	7	1)
		0	0	1	**1**	0	3	2	**5**	4	7	6	**1**	2	3	0	**5**	6	7	4	1)
		0	1	0	**2**	3	0	1	**6**	7	4	5	**2**	3	0	1	**6**	7	4	5	1)
		0	1	1	**3**	2	1	0	**7**	6	5	4	**3**	0	1	2	**7**	4	5	6	1)
		1	0	0	**4**	5	6	7	**0**	1	2	3	**4**	5	6	7	**0**	1	2	3	1)
		1	0	1	**5**	4	7	6	**1**	0	3	2	**5**	6	7	4	**1**	2	3	0	1)
		1	1	0	**6**	7	4	5	**2**	3	0	1	**6**	7	4	5	**2**	3	0	1	1)
		1	1	1	**7**	6	5	4	**3**	2	1	0	**7**	4	5	6	**3**	0	1	2	1)
	WRITE	V	V	V	**0**	1	2	3	**4**	5	6	7	**0**	1	2	3	**4**	5	6	7	1)2)
4 (Burst Chop Mode)	READ	0	0	0	**0**	1	2	3	**T**	T	T	T	**0**	1	2	3	**T**	T	T	T	1)3)4)
		0	0	1	**1**	0	3	2	**T**	T	T	T	**1**	2	3	0	**T**	T	T	T	1)3)4)
		0	1	0	**2**	3	0	1	**T**	T	T	T	**2**	3	0	1	**T**	T	T	T	1)3)4)
		0	1	1	**3**	2	1	0	**T**	T	T	T	**3**	0	1	2	**T**	T	T	T	1)3)4)
		1	0	0	**4**	5	6	7	**T**	T	T	T	**4**	5	6	7	**T**	T	T	T	1)3)4)
		1	0	1	**5**	4	7	6	**T**	T	T	T	**5**	6	7	4	**T**	T	T	T	1)3)4)
		1	1	0	**6**	7	4	5	**T**	T	T	T	**6**	7	4	5	**T**	T	T	T	1)3)4)
		1	1	1	**7**	6	5	4	**T**	T	T	T	**7**	4	5	6	**T**	T	T	T	1)3)4)
	WRITE	0	V	V	**0**	1	2	3	**X**	X	X	X	**0**	1	2	3	**X**	X	X	X	1)2)4)5)
		1	V	V	**4**	5	6	7	**X**	X	X	X	**4**	5	6	7	**X**	X	X	X	1)2)4)5)

1) 0...7 bit number is value of CA[2:0] that causes this bit to be the first read during a burst.
2) V: a valid logic level (0 or 1), but respective buffer input ignores level on input pins.
3) T: output drivers for data and strobe are in high impedance.
4) In case of BC4MRS (burst length being fixed to 4 by MR0 setting), the internal write operation starts two clock cycles earlier than for the BL8 modes. This means that the starting point for t_{WR} and t_{WTR} will be pulled in by two clocks. In case of BC4OTF mode (burst length being selected on-the-fly via A12 | /BC), the internal write operation starts at the same point in time as a burst of 8 write operation. This means that during on-the-fly control, the starting point for t_{WR} and t_{WTR} will not be pulled in by two clocks.
5) X: Don’t Care

3 Operating Conditions and Interface Specification

3.1 Absolute Maximum Ratings

TABLE 12
Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Note
		Min.	Max.		
Voltage on V_{DD} ball relative to V_{SS}	V_{DD}	–0.4	+1.975	V	1)2)
Voltage on V_{DDQ} ball relative to V_{SS}	V_{DDQ}	–0.4	+1.975	V	1)2)
Voltage on any ball relative to V_{SS}	V_{IN}, V_{OUT}	–0.4	+1.975	V	1)
Storage Temperature	T_{STG}	–55	+100	°C	1)3)

1) Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2) V_{DD} and V_{DDQ} must be within 300mV of each other at all times. V_{REFDQ} and V_{REFCA} must not be greater than 0.6 x V_{DDQ}. When V_{DD} and V_{DDQ} are less than 500 mV, V_{REFDQ} and V_{REFCA} may be equal or less than 300 mV.

3) Storage Temperature is the case surface temperature on the center/top side of the SDRAM. For the measurement conditions, please refer to JESD51-2 standard.

3.2 Operating Conditions

TABLE 13
SDRAM Component Operating Temperature Range

Parameter	Symbol	Rating		Unit	Note
		Min.	Max.		
Normal Operating Temperature Range	T_{OPER}	0	85	°C	1)2)3)
Extended Temperature Range		85	95	°C	1)3)4)
Industrial Temperature		-40	95	°C	1)3)4)

1) Operating Temperature T_{OPER} is the case surface temperature on the center / top side of the SDRAM. For measurement conditions, please refer to the industry standard document JESD51-2.

2) The Normal Temperature Range specifies the temperatures where all SDRAM specification will be supported.

3) During operation, the SDRAM operating temperature must be maintained above 0 °C under all operating conditions. Either the device operating temperature rating or the optional ODTS MPR Readout function (See Chapter 2.18, On-Die Thermal Sensor (ODTS)) may be used to set an appropriate refresh rate and/or to monitor the maximum operating temperature. When using the optional ODTS MPR Readout function, the actual device operating temperature may be higher than the T_{OPER} rating that applies for the Normal or Extended Temperature Ranges. For example, T_{CASE} may be above 85 °C when the ODTS indicates that 1X refresh is supported.

4) Some application require operation of the DRAM in the Extended Temperature Range between 85 ℃ and 95 ℃ operating temperature. Full specifications are provided in this range, but the following additional conditions apply:
a) Refresh commands have to be doubled in frequency, therefore reducing the Refresh interval t_{REFI} to 3.9 µs.
b) If Self-Refresh operation is required in the Extended Temperature Range, than it is mandatory to use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0_B and MR2 A7 = 1_B) . For SDRAM operations on DIMM module refer to DIMM module data sheets and SPD bytes for Extended Temperature and Auto Self-Refresh option availability.

TABLE 14
DC Operating Conditions

Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Note**
Supply Voltage	V_{DD}	1.283	1.35	1.45	V	1)2)
		1.425	1.5	1.575	V	1)2)
Supply Voltage for Output	V_{DDQ}	1.283	1.35	1.45	V	1)2)
		1.425	1.5	1.575	V	1)2)
Reference Voltage for DQ, DM inputs	$V_{REFDQ.DC}$	0.49 x V_{DD}	0.5 x V_{DD}	0.51 x V_{DD}	V	3)4)
Reference Voltage for ADD, CMD inputs	$V_{REFCA.DC}$	0.49 x V_{DD}	0.5 x V_{DD}	0.51 x V_{DD}	V	3)4)
External Calibration Resistor connected from ZQ ball to ground	R_{ZQ}	237.6	240.0	242.4	Ω	5)

1) V_{DDQ} tracks with V_{DD}. AC parameters are measured with V_{DD} and V_{DDQ} tied together
2) Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
3) The ac peak noise on V_{REF} may not allow V_{REF} to deviate from $V_{REF.DC}$ by more than ±1% V_{DD} (for reference: approx. ± 15 mV).
4) For reference: approx. $V_{DD}/2 \pm 15$ mV.
5) The external calibration resistor R_{ZQ} can be time-shared among DRAMs in multi-rank DIMMs.

TABLE 15
Input and Output Leakage Currents

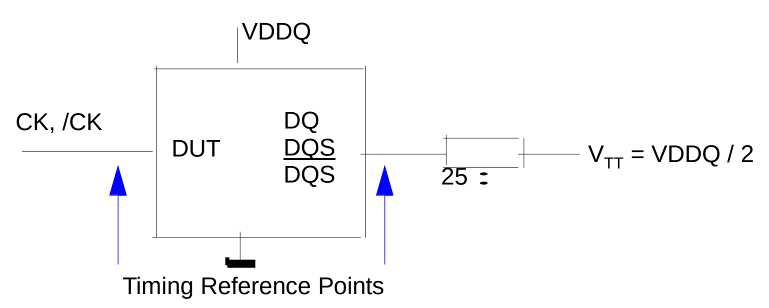
Parameter	**Symbol**	**Condition**	**Rating**		**Unit**	**Note**
			Min.	**Max.**		
Input Leakage Current	I_{IL}	Any input 0 V < V_{IN} < V_{DD}	–2	+2	µA	1)2)
Output Leakage Current	I_{OL}	0V < V_{OUT} < V_{DDQ}	–5	+5	µA	2)3)

1) All other pins not under test = 0 V.
2) Values are shown per ball.
3) DQ's, DQS, /DQS and ODT are disabled.

3.3 Interface Test Conditions

Figure 2 represents the effective reference load of 25 Ω used in defining the relevant timing parameters of the device as well as for output slew rate measurements. It is not intended as either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

FIGURE 2
Reference Load for AC Timings and Output Slew Rates



The Timing Reference Points are the idealized input and output nodes / terminals on the outside of the packaged SDRAM device as they would appear in a schematic or an IBIS model.

The output timing reference voltage level for single ended signals is the cross point with $V_{TT.}$

The output timing reference voltage level for differential signals is the cross point of the true (e.g. DQS) and the complement (e.g. /DQS) signal.

3.4 Voltage Levels

3.4.1 DC and AC Logic Input Levels

Single-Ended Signals

Table 16 shows the input levels for single-ended input signals.

TABLE 16
DC and AC Input Levels for Single-Ended Command, Address and Control Signals

Parameter	Symbol	DDR3(L)-800, 1066; -1333,1600,1866		Unit	Note
		Min.	Max.		
DC input logic high	$V_{IH.CA.DC}$	$V_{REF} + 0.100$	V_{DD}	V	1)
DC input logic low	$V_{IL.CA.DC}$	V_{SS}	$V_{REF} - 0.100$	V	1)
AC input logic high	$V_{IH.CA.AC}$	$V_{REF} + 0.175$	See 2)	V	1)
AC input logic low	$V_{IL.CA.AC}$	See 2)	$V_{REF} - 0.175$	V	1)

1) For input only pins except RESET: $V_{REF} = V_{REF.CA}$
2) See **Chapter 3.9**, **Overshoot and Undershoot Specification**.

TABLE 17
DC and AC Input Levels for Single-Ended DQ and DM Signals

Parameter	Symbol	DDR3(L)-800, 1066,		DDR3(L)-1333,1600 , -1866		Unit	Note
		Min.	Max.	Min.	Max.		
DC input logic high	$V_{IH.DQ.DC}$	$V_{REF} + 0.100$	V_{DD}	$V_{REF} + 0.100$	V_{DD}	V	1)
DC input logic low	$V_{IL.DQ.DC}$	V_{SS}	$V_{REF} - 0.100$	V_{SS}	$V_{REF} - 0.100$	V	1)
AC input logic high	$V_{IH.DQ.AC}$	$V_{REF} + 0.175$	See 2)	--	--	V	1) 3)
AC input logic low	$V_{IL.DQ.AC}$	See 2)	$V_{REF} - 0.175$	--	--	V	1) 3)

1) For DQ and DM: $V_{REF} = V_{REFDQ}$, for input only signals except RESET: $V_{REF} = V_{REFCA}$
2) See **Chapter 3.9**, **Overshoot and Undershoot Specification**.
3) Single ended swing requirement for DQS, /DQS is 350 mV (peak to peak). Differential swing requirement for DQS, /DQS is 700 mV (peak to peak).

Differential Swing Requirement for Differential Signals

Table 18 shows the input levels for differential input signals.

TABLE 18
Differential swing requirement for clock (CK - /CK) and strobe (DQS - /DQS)

Parameter	Symbol	DDR3(L)–800, -1066,–1333, -1600,–1866		Unit	Note
		Min.	Max.		
Differential input high	$V_{IH.DIFF}$	+0.200(+0.18)	See 1)	V	2)
Differential input low	$V_{IL.DIFF}$	See1)	–0.200(-0.18)	V	2)
Differential input high AC	$V_{IH.DIFF.AC}$	2 x ($V_{IH.AC}$ - V_{REF}) 3)	See 1)	V	4)
Differential input low AC	$V_{IL.DIFF.AC}$	See 1)	2 x (V_{REF} - $V_{IL.AC}$) 5)	V	4)

1) These values are not defined, however they single-ended signals CK, /CK, DQS, /DQS need to be within the respective limits ($V_{IH.DC.MAX}$, $V_{IL.DC.MIN}$) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to **Chapter 3.9** .

2) Used to define a differential signal slew-rate.

3) Clock: use $V_{IH.CA.AC}$ for $V_{IH.AC}$. Strobe: use $V_{IH.DQ.AC}$ for $V_{IH.AC}$.

4) For CK - /CK use V_{IH} /$V_{IL.AC}$ of ADD/CMD and V_{REFCA}; for DQS - /DQS use V_{IH} /$V_{IL.AC}$ of DQs and V_{REFDQ}; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.

5) Clock: use $V_{IL.CA.AC}$ for $V_{IL.AC}$. Strobe: use $V_{IL.DQ.AC}$ for $V_{IL.AC}$.

TABLE 19
Allowed Time Before Ringback (t_{DVAC}) for CK - /CK and DQS - /DQS

Slew Rate [V/ns]	t_{DVAC} [ps] @ $\lvert V_{IH/IL.DIFF.AC}\rvert$ = 350mV		t_{DVAC} [ps] @ $\lvert V_{IH/IL.DIFF.AC}\rvert$ = 300mV	
	Min.	Max.	Min.	Max.
> 4.0	75	—	175	—
4.0	57	—	170	—
3.0	50	—	167	—
2.0	38	—	163	—
1.8	34	—	162	—
1.6	29	—	161	—
1.4	22	—	159	—
1.2	13	—	155	—
1.0	0	—	150	—
<1.0	0	—	150	—

Single-Ended Requirements for Differential Signals

Each individual component of a differential signal (CK, DQS, /CK, /DQS,) has also to comply with certain requirements for single-ended signals.

CK and /CK have to approximately reach $V_{SEH.MIN}$ / $V_{SEL.MAX}$ (approximately equal to the ac-levels ($V_{IH.AC}$ / $V_{IL.AC}$) for ADD/CMD signals) in every half-cycle.

DQS, /DQS have to reach $V_{SEH.MIN}$ / $V_{SEL.MAX}$ (approximately the ac-levels ($V_{IH.AC}$ / $V_{IL.AC}$) for DQ signals) in every half-cycle preceeding and following a valid transition.

Note that the applicable ac-levels for ADD/CMD and DQs might be different per speed-bin etc. E.g. if $V_{IH150.AC}$ / $V_{IL150.AC}$ is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK and /CK.

Note that while ADD/CMD and DQ signal requirements are with respect to V_{ref}, the single-ended components of differential signals have a requirement with respect to $V_{DD}/2$; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time.

For single-ended components of differential signals the requirement to reach $V_{SEL.MAX}$, $V_{SEH.MIN}$ has no bearing on timing, but adds a restriction on the common mode charateristics of these signals.

TABLE 20
Each Single-Ended Levels for CK, DQS, /DQS, /CK,

Parameter	**Symbol**	**DDR3(L)–800,-1066-,–1333,-1600,–1866**		**Unit**	**Note**
		Min.	**Max.**		
Single-ended highlevel for strobes	V_{SEH}	(VDD/2) + 0.175	NOTE 3	V	1,2
Single-ended high-level for CK,/ CK	V_{SEH}	(VDD/2) + 0.175	NOTE 3	V	
Single-ended low-level for strobes	V_{SEL}	NOTE 3	(VDD/2) + 0.175	V	
Single-ended low-level for CK, /CK	V_{SEL}	NOTE 3	(VDD/2) + 0.175	V	

Note: 1. For CK, CK use VIH/VIL(AC) of address/command; for strobes (DQS, DQS) use VIH/VIL(AC) of DQs.
2. VIH(AC)/VIL(AC) for DQs is based on VREFDQ; VIH(AC)/VIL(AC) for address/command is based on VREFCA; if a reduced AC-high or AC-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however the single-ended components of differential signals CK, CK, DQS, DQS need to be within the respective limits (VIH(DC) max, VIL(DC) min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot specifications”.

TABLE 21
Cross Point Voltage for Differential Input Signals (CK, DQS)

Symbol	**Parameter**	**DDR3(L)–800,-1066-,–1333,-1600,–1866**		**Unit**	**Note**
		Min.	**Max.**		
V_{IX}	Differential Input Cross Point Voltage relative to $V_{DD}/2$ for CK - $\overline{\text{CK}}$	–175(–150)	175(150)	mV	1
V_{IX}	Differential Input Cross Point Voltage relative to $V_{DD}/2$ for $\overline{\text{DQS}}$ -DQS	–150	150	mV	

1) Extended range for V_{IX} is only allowed for clock and if single-ended clock input signals CK and /CK are monotonic, have a single-ended swing V_{SEL}/V_{SEH} (see **Single-Ended Requirements for Differential Signals**) of at least $V_{DD}/2$ +/-250 mV and if the differential slew rate of CK - /CK is larger than 3 V/ns.

3.4.2 DC and AC Output Measurements Levels

TABLE 22
DC and AC Output Levels for Single-Ended Signals

Parameter	**Symbol**	**Value**	**Unit**	**Note**
DC output high measurement level (for output impedance measurement)	$V_{OH.DC}$	0.8 x V_{DDQ}	V	
DC output mid measurement level (for output impedance measurement)	$V_{OM.DC}$	0.5 x V_{DDQ}	V	
DC output low measurement level (for output impedance measurement)	$V_{OL.DC}$	0.2 x V_{DDQ}	V	

Parameter	Symbol	Value	Unit	Note
AC output high measurement level (for output slew rate)	$V_{OH.AC}$	V_{TT} + 0.1 x V_{DDQ}	V	1)
AC output low measurement level (for output slew rate)	$V_{OL.AC}$	V_{TT} - 0.1 x V_{DDQ}	V	1)

1) Background: the swing of ± 0.1 x V_{DDQ} is based on approximately 50% of the static differential output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to V_{TT} = V_{DDQ} / 2.

TABLE 23
AC Output Levels for Differential Signals

Parameter	Symbol	Value		Unit	Note
		Min.	Max.		
AC differential output high measurement level (for output slew rate)	$V_{OH.DIFF.AC}$	+0.2 x V_{DDQ}		V	1)
AC differential output low measurement level (for output slew rate)	$V_{OL.DIFF.AC}$	–0.2 x V_{DDQ}		V	1)
Deviation of the output cross point voltage from the termination voltage	V_{OX}	-100	100	mV	2)

1) Background: the swing of ± 0.2 x V_{DDQ} is based on approximately 50% of the static differential output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to V_{TT} =V_{DDQ} / 2 at each of the differential outputs.
2) With an effective test load of 25 Ω to V_{TT} = V_{DDQ}/2 at each of the differential outputs (see chapter **Chapter 3.3**, **Interface Test Conditions**).

3.5 Output Slew Rates

TABLE 24
Output Slew Rates

Parameter	Symbol	DDR3(L)–800,-1066-,–1333,-1600,–1866		Unit	Note
		Min.	Max.		
Single-ended Output Slew Rate	SRQse	2.5(1.75)	5(5)	V / ns	1)2)
Differential Output Slew Rate	SRQdiff	5(3.5)	10(12)	V / ns	

1) For R_{ON} = R_{ZQ}/7 settings only.
2) Background for Symbol Nomenclature: SR: Slew Rate; Q: Query Output; se: single-ended; diff: differential

3.6 ODT DC Impedance and Mid-Level Characteristics

Table 25 provides the ODT DC impedance and mid-level characteristics.

TABLE 25
ODT DC Impedance and Mid-Level Characteristics

Symbol	Description	V_{OUT} Condition	Min.	Nom.	Max.	Unit	Note
R_{TT120}	R_{TT} effective = 120 Ω	$V_{IL.AC}$ and $V_{IH.AC}$	0.9	1.0	1.6	$R_{ZQ}/2$	1)2)3)4)
R_{TT60}	R_{TT} effective = 60 Ω		0.9	1.0	1.6	$R_{ZQ}/4$	1)2)3)4)
R_{TT40}	R_{TT} effective = 40 Ω		0.9	1.0	1.6	$R_{ZQ}/6$	1)2)3)4)
R_{TT30}	R_{TT} effective = 30 Ω		0.9	1.0	1.6	$R_{ZQ}/8$	1)2)3)4)
R_{TT20}	R_{TT} effective = 20 Ω		0.9	1.0	1.6	$R_{ZQ}/12$	1)2)3)4)
ΔV_M	Deviation of V_M with respect to V_{DDQ} / 2	floating	–5	—	+5	%	1)2)3)4)5)

1) With R_{ZQ} = 240 Ω.
2) Measurement definition for R_{TT} : Apply $V_{IH.AC}$ and $V_{IL.AC}$ to test ball separately, then measure current I ($V_{IH.AC}$) and I ($V_{IL.AC}$) respectively. $R_{TT} = [V_{IH.AC} - V_{IL.AC}] / [I (V_{IH.AC}) - I (V_{IL.AC})]$
3) The tolerance limits are specified after calibration with stable voltage and temperature. For the behaviour of the tolerance limits if temperature or voltage changes after calibration, see the **ODT DC Impedance Sensitivity on Temperature and Voltage Drifts**.
4) The tolerance limits are specified under the condition that $V_{DDQ} = V_{DD}$ and that $V_{SSQ} = V_{SS}$.
5) Measurement Definition for ΔV_M: Measure voltage (V_M) at test ball (midpoint) with no load: $\Delta V_M = (2 \times V_M / V_{DDQ} - 1) \times 100\%$

3.7 ODT DC Impedance Sensitivity on Temperature and Voltage Drifts

If temperature and/or voltage change after calibration, the tolerance limits widen for R_{TT} according to the following tables. The following definitions are used:

$\Delta T = T - T$ (at calibration)

$\Delta V = V_{DDQ} - V_{DDQ}$ (at calibration)

$V_{DD} = V_{DDQ}$

TABLE 26
ODT DC Impedance after proper IO Calibration and Voltage/Temperature Drift

Symbol	Value		Unit	Note
	Min.	Max.		
R_{TT}	0.9 - dR_{TT}dT x |ΔT| - dR_{TT}dV x |ΔV|	1.6 + dR_{TT}dT x |ΔT| + dR_{TT}dV x |ΔV|	R_{ZQ} / $TISF_{RTT}$	1)

1) $TISF_{RTT}$: Termination Impedance Scaling Factor for R_{TT}:
$TISF_{RTT}$ = 12 for R_{TT020}
$TISF_{RTT}$ = 8 for R_{TT030}
$TISF_{RTT}$ = 6 for R_{TT040}
$TISF_{RTT}$ = 4 for R_{TT060}
$TISF_{RTT}$ = 2 for R_{TT120}

TABLE 27
OTD DC Impedance Sensitivity Parameters

Symbol	Value		Unit	Note
	Min.	Max.		
dR_{TT}dT	0	1.5	%/°C	1)
dR_{TT}dV	0	0.15	%/mV	

1) These parameters may not be subject to production test. They are verified by design and characterization.

3.8 Interface Capacitance

Definition and values for interface capacitances are provided in the following table.

TABLE 28
Interface Capacitance Values

Parameter	Symbol	DDR3(L)–800		DDR3(L)–1066		DDR3(L)–1333		DDR3(L)–1600		DDR3(L)–1866		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
1.35V													
Input/Output Capacitance (DQ,DM,DQS,/DQQS)	C_{IO}	1.5	2.5	1.5	2.5	1.5	2.3	1.2	2.3	TBD	TBD	pF	1,2,3
Input Capacitance (CK and /CK)	C_{CK}	0.8	1.6	0.8	1.6	0.8	1.4	0.8	1.4	0.8	1.3	pF	2,3
Input Capacitance Delta (CK and /CK)	C_{DCK}	0	0.15	0	0.15	0	0.15	0	0.15	0	0.15	pF	2,3,4
Input/Output Capacitance delta (DQS and /DQS)	C_{DDQS}	0	0.2	0	0.2	0	0.15	0	0.15	0	0.15	pF	2,3,5
Input Capacitance (All other input-only pins)	C_{I}	0.75	1.3	0.75	1.3	0.75	1.3	0.75	1.3	TBD	TBD	pF	2,3,6
Input Capacitance delta (All control input-only pins)	C_{DI_CTRL}	–0.5	0.3	–0.5	0.3	–0.4	0.2	–0.4	0.2	–0.4	0.2	pF	2,3,7,8
Input Capacitance delta (All ADD and CMD input-only pins)	$C_{DI\_ADD\_CMD}$	–0.5	0.5	–0.5	0.5	–0.4	0.4	–0.4	0.4	–0.4	0.4	pF	2,3,9,10
Input/Output Capacitance delta (DQ,DM,DQS,/DQQS)	C_{DIO}	–0.5	0.3	–0.5	0.3	–0.5	0.3	–0.5	0.3	–0.5	0.3	pF	2,3,11
Input/output capacitance of ZQ pin	C_{ZQ}	–	3	–	3	–	3	–	3	–	3	pF	2,3,12
1.5V													
Input/Output Capacitance (DQ,DM,DQS,/DQQS)	C_{IO}	1.4	3.0	1.4	2.7	1.4	2.5	1.4	2.3	1.4	2.2	pF	1,2,3
Input Capacitance (CK and /CK)	C_{CK}	0.8	1.6	0.8	1.6	0.8	1.4	0.8	1.4	0.8	1.3	pF	2,3
Input Capacitance Delta (CK and /CK)	C_{DCK}	0	0.15	0	0.15	0	0.15	0	0.15	0	0.15	pF	2,3,4
Input/Output Capacitance delta (DQS and /DQS)	C_{DDQS}	0	0.2	0	0.2	0	0.15	0	0.15	0	0.15	pF	2,3,5
Input Capacitance (CK and /CK) (All other input-only pins)	C_{I}	0.75	1.4	0.75	1.35	0.75	1.3	0.75	1.3	0.75	1.2	pF	2,3,6
Input Capacitance delta (All control input-only pins)	C_{DI_CTRL}	-0.5	0.3	-0.5	0.3	-0.4	0.2	-0.4	0.2	-0.4	0.2	pF	2,3,7,8
Input Capacitance delta (All ADD and CMD input-only pins)	$C_{DI\_ADD\_CMD}$	–0.5	0.5	–0.5	0.5	–0.4	0.4	–0.4	0.4	–0.4	0.4	pF	2,3,9,10

Input/Output Capacitance delta (DQ,DM,DQS,/DQQS)	C_{DIO}	-0.5	0.3	-0.5	0.3	-0.5	0.3	-0.5	0.3	-0.5	0.3	pF	2,3,11
Input/output capacitance of ZQ pin	C_{ZQ}	–	3	–	3	–	3	–	3	–	3	pF	2,3,12

1) Although the DM signal has different function, the loading matches DQ and DQS
2) This parameter is not subject to production test. It is verified by design and characterization. Capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ} applied and all other balls floating (except the ball under test, CKE, /RESET and ODT as necessary). $V_{DD} = V_{DDQ}$ = 1.35V/1.5 V, $V_{BIAS} = V_{DD}/2$ and on-die termination off
3) This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
4) Absolute value of $C_{CK} - C_{CK\#}$
5) Absolute value of $C_{IO.DQS} - C_{IO.DQS\#}$
6) C_I applies to ODT, /CS, CKE, A[15:0], BA[2:0], /RAS, /CAS, /WE
7) C_{DI_CTRL} applies to ODT, /CS and CKE
8) $C_{DI\_CTRL} = C_{I.CTRL} - 0.5 \times (C_{I.CK} + C_{I.CK\#})$
9) $C_{DI\_ADD\_CMD}$ applies to A[15:0], BA[2:0], /RAS, /CAS and /WE
10) $C_{DI\_ADD\_CMD} = C_{I.ADD,CMD} - 0.5 \times (C_{I.CK} + C_{I.CK\#})$
11) $C_{DIO} = C_{IO.DQ,DM} - 0.5 \times (C_{IO.DQS} + C_{IO.DQS\#})$
12) Maximum external load capacitance on ZQ signal: 5 pF

3.9 Overshoot and Undershoot Specification

TABLE 29
AC Overshoot / Undershoot Specification for Address and Control Signals

Parameter	DDR3(L) –800	DDR3(L) –1066	DDR3(L) –1333	DDR3(L) –1600	DDR3(L) –1866	Unit	Note
Maximum peak amplitude allowed for overshoot area	0.4	0.4	0.4	0.4	0.4	V	1)
Maximum peak amplitude allowed for undershoot area	0.4	0.4	0.4	0.4	0.4	V	1)
Maximum overshoot area above V_{DD}	0.67	0.5	0.4	0.33	0.28	V × ns	1)
Maximum undershoot area below V_{SS}	0.67	0.5	0.4	0.33	0.28	V × ns	1)

1) Applies for the following signals: A[15:0], BA[3:0], /CS, /RAS, /CAS, /WE, CKE and ODT

FIGURE 3
AC Overshoot / Undershoot Definitions for Address and Control Signals

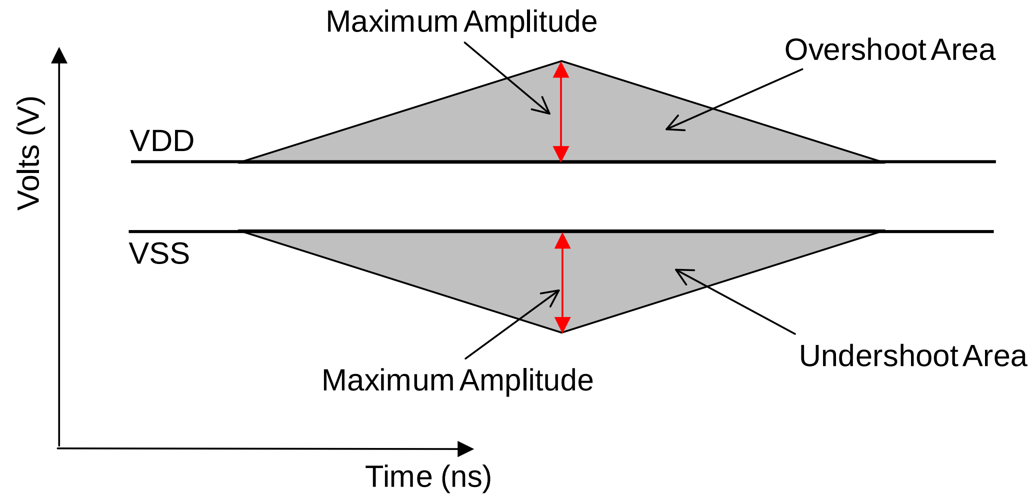
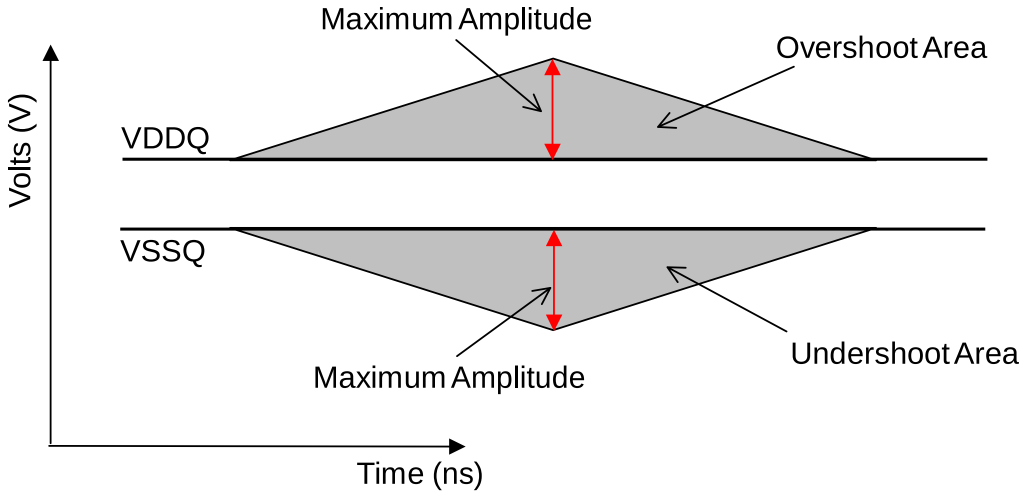


TABLE 30
AC Overshoot / Undershoot Specification for Clock, Data, Strobe and Mask Signals

Parameter	DDR3(L) –800	DDR3(L) –1066	DDR3(L) –1333	DDR3(L) –1600	DDR3(L) –1866	Unit	Note
Maximum peak amplitude allowed for overshoot area	0.4	0.4	0.4	0.4	0.4	V	1)
Maximum peak amplitude allowed for undershoot area	0.4	0.4	0.4	0.4	0.4	V	1)
Maximum overshoot area above V_{DDQ}	0.25	0.19	0.15	0.13	0.11	V × ns	1)
Maximum undershoot area below V_{SSQ}	0.25	0.19	0.15	0.13	0.11	V × ns	1)

1) Applies for CK, /CK, DQ, DQS, /DQS & DM

FIGURE 4
AC Overshoot / Undershoot Definitions for Clock, Data, Strobe and Mask Signals



4 Speed Bins, AC Timing and IDD

The following AC timings are provided with CK AND /CK and DQS AND /DQS differential slew rate of 2.0 V/ns. Timings are further provided for calibrated OCD drive strength under the “Reference Load for Timing Measurements” according to **Chapter 3.3** only.

The CK AND /CK input reference level (for timing referenced to CK AND /CK) is the point at which CK and /CK cross. The DQS AND /DQS reference level (for timing referenced to DQS AND /DQS) is the point at which DQS and /DQS cross. The output timing reference voltage level is V_{TT}.

4.1 Speed Bins

The following tables show DDR3(L) speed bins and relevant timing parameters. Other timing parameters are provided in the following chapter. For availability and ordering information of products for a specific speed bin, please see **Table 1**.

The absolute specification for all speed bins is T_{OPER} and V_{DD} = V_{DDQ} = 1.283V to 1.45V or 1.5 V ± 0.075V. In addition the following general notes apply.

General Notes for Speed Bins:

- The CL setting and CWL setting result in $t_{CK.AVG.MIN}$ and $t_{CK.AVG.MAX}$ requirements. When making a selection of $t_{CK.AVG}$, both need to be fulfiled: Requirements from CL setting as well as requirements from CWL setting
- $t_{CK.AVG.MIN}$ limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller industry standard $t_{CK.AVG}$ value (2.5, 1.875, 1.5) when calculating CL [nCK] = t_{AA} [ns] / $t_{CK.AVG}$ [ns], rounding up to the next ‘Supported CL’
- $t_{CK.AVG.MAX}$ limits: Calculate $t_{CK.AVG}$ = $t_{AA.MAX}$ / CLSELECTED and round the resulting $t_{CK.AVG}$ down to the next valid speed bin limit (i.e. 3.3 ns or 2.5 ns or 1.875 ns or 1.25 ns). This result is $t_{CK.AVG.MAX}$ corresponding to CLSELECTED ‘Reserved’ settings are not allowed. User must program a different value
- Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the tables which are not subject to Production Tests but verified by Design/Characterization
- Any DDR3(L)-1333 speed bin also supports functional operation at lower frequencies as shown in the tables which are not subject to Production Tests but verified by Design/Characterization
- Any DDR3(L)-1600 speed bin also supports functional operation at lower frequencies as shown in the tables which are not subject to Production Tests but verified by Design/Characterization

TABLE 31
DDR3-800 Speed Bins

Speed Bin				DDR3(L)-800		Unit	Notes
CL-nRCD-nRP				**6-6-6**			
Parameter			**Symbol**	**Min**	**Max**		
Internal read command to first data			tAA	15	20	ns	
Active to read or write delay time			tRCD	15	-	ns	
Precharge command period			tRP	15	-	ns	
Active to active/auto-refresh command time			tRC	52.5	-	ns	
Active to precharge command period			tRAS	37.5	9 * tREFI	ns	8
Average Clock Cycle Time	CL = 5	CWL = 5	tCK(avg)	3.0	3.3	ns	1,2,3,4
	CL = 6	CWL = 5	tCK(avg)	2.5	3.3	ns	1,2,3
Supported CL setting				5, 6		nCK	
Supported CWL setting				5		nCK	

TABLE 32
DDR3-1066 Speed Bins

Speed Bin				DDR3(L)-1066		Unit	Notes
CL-nRCD-nRP				**7-7-7**			
Parameter			**Symbol**	**Min**	**Max**		
Internal read command to first data			tAA	13.125	20	ns	
Active to read or write delay time			tRCD	13.125	-	ns	
Precharge command period			tRP	13.125	-	ns	
Active to active/auto-refresh command time			tRC	50.625	-	ns	
Active to precharge command period			tRAS	37.5	9 * tREFI	ns	8
Average Clock Cycle Time	CL = 5	CWL = 5	tCK(avg)	3.0	3.3	ns	1,2,3,5
		CWL = 6	tCK(avg)	Reserved	Reserved	ns	4
	CL = 6	CWL = 5	tCK(avg)	2.5	3.3	ns	1,2,3,5
		CWL = 6	tCK(avg)	Reserved	Reserved	ns	4
	CL = 7	CWL = 5	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 6	tCK(avg)	1.875	< 2.5	ns	1,2,3
	CL = 8	CWL = 5	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 6	tCK(avg)	1.875	< 2.5	ns	1,2,3
Supported CL setting				5, 6, 7, 8		nCK	
Supported CWL setting				5, 6		nCK	

TABLE 33
DDR3(L)-1333 Speed Bins

Speed Bin				DDR3(L)-1333		Unit	Notes
CL-nRCD-nRP				**9-9-9**			
Parameter			**Symbol**	**Min**	**Max**		
Internal read command to first data			tAA	13.5 (13.125)	20	ns	9
Active to read or write delay time			tRCD	13.5 (13.125)	-	ns	9
Precharge command period			tRP	13.5 (13.125)	-	ns	9
Active to active/auto-refresh command time			tRC	49.5 (49.125)	-	ns	9
Active to precharge command period			tRAS	36	9 * tREFI	ns	8
Average Clock Cycle Time	CL = 5	CWL = 5	tCK(avg)	3.0	3.3	ns	1,2,3,6
		CWL = 6,7	tCK(avg)	Reserved	Reserved	ns	4
	CL = 6	CWL = 5	tCK(avg)	2.5	3.3	ns	1,2,3,6
		CWL = 6	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 7	tCK(avg)	Reserved	Reserved	ns	4
	CL = 7	CWL = 5	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 6	tCK(avg)	1.875	< 2.5	ns	1,2,3,6
		CWL = 7	tCK(avg)	Reserved	Reserved	ns	4
	CL = 8	CWL = 5	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 6	tCK(avg)	1.875	< 2.5	ns	1,2,3,6
		CWL = 7	tCK(avg)	Reserved	Reserved	ns	4
	CL = 9	CWL = 5, 6	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 7	tCK(avg)	1.5	< 1.875	ns	1,2,3
	CL = 10	CWL = 5, 6	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 7	tCK(avg)	1.5	< 1.875	ns	1,2,3
Supported CL setting				5, 6, 7, 8, 9, 10		nCK	
Supported CWL setting				5, 6, 7		nCK	

TABLE 34
DDR3(L)-1600 Speed Bins

Speed Bin				**DDR3(L)-1600**		**Unit**	**Notes**
CL-nRCD-nRP				**11-11-11**			
Parameter			**Symbol**	**Min**	**Max**		
Internal read command to first data			tAA	13.75 (13.125)	20	ns	9
Active to read or write delay time			tRCD	13.75 (13.125)	-	ns	9
Precharge command period			tRP	13.75 (13.125)	-	ns	9
Active to active/auto-refresh command time			tRC	48.75 (48.125)	-	ns	9
Active to precharge command period			tRAS	35	9 * tREFI	ns	8
Average Clock Cycle Time	CL = 5	CWL = 5	tCK(avg)	3.0	3.3	ns	1,2,3,7
		CWL = 6,7	tCK(avg)	Reserved	Reserved	ns	4
	CL = 6	CWL = 5	tCK(avg)	2.5	3.3	ns	1,2,3,7
		CWL = 6	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 7	tCK(avg)	Reserved	Reserved	ns	4
	CL = 7	CWL = 5	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 6	tCK(avg)	1.875	< 2.5	ns	1,2,3,7
		CWL = 7	tCK(avg)	Reserved	Reserved	ns	4
	CL = 8	CWL = 5	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 6	tCK(avg)	1.875	< 2.5	ns	1,2,3,7
		CWL = 7	tCK(avg)	Reserved	Reserved	ns	4
	CL = 9	CWL = 5, 6	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 7	tCK(avg)	1.5	< 1.875	ns	1,2,3,7
	CL = 10	CWL = 5, 6	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 7	tCK(avg)	1.5	< 1.875	ns	1,2,3,7
		CWL = 8	tCK(avg)	Reserved	Reserved	ns	4
	CL = 11	CWL = 5, 6,7	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 8	tCK(avg)	1.25	< 1.5	ns	1,2,3
Supported CL setting				5, 6, 7, 8, 9, 10,11		nCK	
Supported CWL setting				5, 6, 7, 8		nCK	

TABLE 35
DDR3-1866 Speed Bins

Speed Bin				DDR3(L)-1866		Unit	Notes
CL-nRCD-nRP				13-13-13			
Parameter			Symbol	Min	Max		
Internal read command to first data			tAA	13.91 (13.125)	20	ns	11
Active to read or write delay time			tRCD	13.91 (13.125)	-	ns	11
Precharge command period			tRP	13.91 (13.125)	-	ns	11
Active to active/auto-refresh command time			tRC	47.91 (47.125)	-	ns	11
Active to precharge command period			tRAS	34	9 * tREFI	ns	9
Average Clock Cycle Time	CL = 5	CWL = 5	tCK(avg)	3.0	3.3	ns	1,2,3,8
		CWL = 6,7	tCK(avg)	Reserved	Reserved	ns	4
	CL = 6	CWL = 5	tCK(avg)	2.5	3.3	ns	1,2,3,8
		CWL = 6	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 7	tCK(avg)	Reserved	Reserved	ns	4
	CL = 7	CWL = 5	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 6	tCK(avg)	1.875	2.5	ns	1,2,3,8
		CWL = 7	tCK(avg)	Reserved	Reserved	ns	1,2,3,8
	CL = 8	CWL = 5	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 6	tCK(avg)	1.875	2.5	ns	1,2,3,8
		CWL = 7	tCK(avg)	Reserved	Reserved	ns	4
	CL = 9	CWL = 5, 6	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 7	tCK(avg)	1.5	1.875	ns	1,2,3,8
	CL = 10	CWL = 5, 6	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 7	tCK(avg)	1.5	1.875	ns	1,2,3,8
		CWL = 8	tCK(avg)	Reserved	Reserved	ns	4
	CL = 11	CWL = 5, 6,7	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 8	tCK(avg)	1.25	1.5	ns	1,2,3,8
	CL = 12	CWL = 5, 6,7,8	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 9	tCK(avg)	Reserved	Reserved	ns	4
	CL = 13	CWL = 5, 6,7,8	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 9	tCK(avg)	1.07	1.25	ns	1,2,3
Supported CL setting				5, 6, 7, 8, 9, 10,11,13		nCK	
Supported CWL setting				5, 6, 7, 8, 9		nCK	

NOTE :

1. The CL setting and CWL setting result in tCK(avg) Min and tCK(avg) Max requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(avg) Min limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(avg) value (2.5, 1.875, 1.5, or 1.25 ns) when calculating CL [nCK] = tAA [ns] / tCK(avg) [ns], rounding up to the next "Supported CL".
3. tCK(avg) Max limits: Calculate tCK(avg) = tAA Max / CL Selected and round the resulting tCK(avg) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.25 ns). This result is tCK(avg) Max corresponding to CL selected.
4. "Reserved" settings are not allowed. User must program a different value.
5. Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to production tests but verified by design/characterization.
6. Any DDR3(L)-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to production tests but verified by design/characterization.
7. Any DDR3(L)-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to production tests but verified by design/characterization.
8. tREFI depends on operating case temperature (Tc).
9. For devices supporting optional downshift to CL=7 and CL=9, tAA/tRCD/tRP min must be 13.125 ns or lower. SPD settings must be programmed to match. For example, DDR3-1333(CL9) devices supporting downshift to DDR3-1066(CL7) should program 13.125 ns in SPD bytes for tAAmin (Byte 16), tRCDmin (Byte 18), and tRPmin (Byte 20). DDR3-1600(CL11) devices supporting downshift to DDR3-1333(CL9) or DDR3-1066(CL7) should program 13.125 ns in SPD bytes for tAAmin (Byte16), tRCDmin (Byte 18), and tRPmin (Byte 20). DDR3-1600 devices supporting down binning to DDR3-1333 or DDR3-1066 should program 13.125ns in SPD byte for tAAmin (Byte 16), tRCDmin (Byte 18) and tRPmin(Byte 20). Once tRP (Byte 20) is programmed to 13.125ns, tRCmin (Byte 21,23) also should be programmed accod- ingly. For example, 49.125ns, (tRASmin + tRPmin = 36ns + 13.125ns) for DDR3-1333 and 48.125ns (tRASmin + tRPmin = 35ns + 13.125ns) for DDR3-1600.

4.2 AC Timing Characteristics

(VDD = 1.283V to 1.45V or 1.5 V ± 0.075V; VDDQ = 1.283V to 1.45V or 1.5 V ± 0.075V)

TABLE 36

AC Timing parameters

Parameter	Symbol	DDR3(L)-800		DDR3(L)-1066		Unit	Note
		Min	Max	Min	Max		
Average clock cycle time	t_{CK}(avg)	Please refer Speed Bins				ps	
Minimum clock cycle time (DLL-off mode)	t_{CK} (DLL-off)	8	-	8	-	ns	6
Average CK high level width	t_{CH}(avg)	0.47	0.53	0.47	0.53	t_{CK}(avg)	
Average CK low level width	t_{CL}(avg)	0.47	0.53	0.47	0.53	t_{CK}(avg)	
Active Bank A to Active Bank B command period	t_{RRD}	10	-	10	-	ns	
		4	-	4	-	nCK	
Four activate window	t_{FAW}	50	-	50	-	ns	
Address and Control input hold time (VIH/VIL (DC100) levels)	t_{IH}(base) DC100	275	-	200	-	ps	16
Address and Control input setup time (VIH/VIL (AC175) levels)	t_{IS}(base) AC175	200	-	125	-	ps	16
Address and Control input setup time (VIH/VIL (AC150) levels)	t_{IS}(base) AC150	350	-	275	-	ps	16,24
DQ and DM input hold time (VIH/VIL (DC100) levels)	t_{DH}(base) DC100	150	-	100	-	ps	17
DQ and DM input setup time (VIH/VIL (AC175) levels)	t_{DS}(base) AC175	75	-	25	-	ps	17
DQ and DM input setup time (VIH/VIL (AC150) levels)	t_{DS}(base) AC150	125	-	75	-	ps	17
Control and Address Input pulse width for each input	t_{IPW}	900	-	780	-	ps	25
DQ and DM Input pulse width for each input	t_{DIPW}	600	-	490	-	ps	25
DQ high impedance time	t_{HZ}(DQ)	-	400	-	300	ps	13,14
DQ low impedance time	t_{LZ}(DQ)	-800	400	-600	300	ps	13,14
DQS, DQS high impedance time (RL + BL/2 reference)	t_{HZ}(DQS)	-	400	-	300	ps	13,14
DQS, DQS low impedance time (RL - 1 reference)	t_{LZ}(DQS)	-800	400	-600	300	ps	13,14
DQS, DQS to DQ Skew, per group, per access	t_{DQSQ}	-	200	-	150	ps	12,13
CAS to CAS command delay	t_{CCD}	4	-	4	-	nCK	
DQ output hold time from DQS, DQS	t_{QH}	0.38	-	0.38	-	t_{CK}(avg)	12,13
DQS, DQS rising edge output access time from rising CK, CK	t_{DQSCK}	-400	400	-300	300	ps	12,13
DQS latching rising transitions to associated clock edges	t_{DQSS}	-0.25	0.25	-0.25	0.25	t_{CK}(avg)	
DQS falling edge hold time from rising CK	t_{DSH}	0.2	-	0.2	-	t_{CK}(avg)	29

Parameter	Symbol	DDR3(L)-800		DDR3(L)-1066		Unit	Note
		Min	Max	Min	Max		
DQS falling edge setup time to rising CK	t_{DSS}	0.2	-	0.2	-	t_{CK}(avg)	29
DQS input high pulse width	t_{DQSH}	0.45	0.55	0.45	0.55	t_{CK}(avg)	27,28
DQS input low pulse width	t_{DQSL}	0.45	0.55	0.45	0.55	t_{CK}(avg)	26,28
DQS output high time	t_{QSH}	0.38	-	0.38	-	t_{CK}(avg)	12,13
DQS output low time	t_{QSL}	0.38	-	0.38	-	t_{CK}(avg)	12,13
Mode register set command cycle time	t_{MRD}	4	-	4	-	nCK	
Mode register set command update delay	t_{MOD}	15	-	15	-	ns	
		12	-	12	-	nCK	
Read preamble time	t_{RPRE}	0.9	-	0.9	-	t_{CK}(avg)	13,19
Read postamble time	t_{RPST}	0.3	-	0.3	-	t_{CK}(avg)	11,13
Write preamble time	t_{WPRE}	0.9	-	0.9	-	t_{CK}(avg)	1
Write postamble time	t_{WPST}	0.3	-	0.3	-	t_{CK}(avg)	1
Write recovery time	t_{WR}	15	-	15	-	ns	
Auto precharge write recovery + Precharge time	t_{DAL}(min)	WR + roundup [tRP / tCK(avg)]				nCK	
Multi-purpose register recovery time	t_{MPRR}	1	-	1	-	nCK	22
Internal write to read command delay	t_{WTR}	7.5	-	7.5	-	ns	18
		4	-	4	-	nCK	18
Internal read to precharge command delay	t_{RTP}	7.5	-	7.5	-	ns	
		4	-	4	-	nCK	
Minimum CKE low width for Self-refresh entry to exit timing	t_{CKESR}	t_{CKE}(min) +1nCK	-	t_{CKE}(min) +1nCK	-		
Valid clock requirement after Self-refresh entry or Power-down entry	t_{CKSRE}	10	-	10	-	ns	
		5	-	5	-	nCK	
Valid clock requirement before Self-refresh exit or Power-down exit	t_{CKSRX}	10	-	10	-	ns	
		5	-	5	-	nCK	
Exit Self-refresh to commands not requiring a locked DLL	t_{XS}	t_{RFC}(min) +10	-	t_{RFC}(min) +10	-	ns	
		5	-	5	-	nCK	
Exit Self-refresh to commands requiring a locked DLL	t_{XSDLL}	t_{DLLK} (min)	-	t_{DLLK} (min)	-	nCK	
Auto-refresh to Active/Auto-refresh command time	t_{RFC}	260	-	260	-	ns	
Average Periodic Refresh Interval 0°C ≤ Tc ≤ +85°C	t_{REFI}	-	7.8	-	7.8	µs	
Average Periodic Refresh Interval +85°C < Tc ≤ +95°C	t_{REFI}	-	3.9	-	3.9	µs	
CKE minimum high and low pulse width	t_{CKE}	7.5	-	5.625	-	ns	
		3	-	3	-	nCK	

Parameter	Symbol	DDR3(L)-800		DDR3(L)-1066		Unit	Note
		Min	Max	Min	Max		
Exit reset from CKE high to a valid command	t_{XPR}	t_{RFC}(min) +10	-	t_{RFC}(min) +10	-	ns	
		5	-	5	-	nCK	
DLL locking time	t_{DLLK}	512	-	512	-	nCK	
Power-down entry to exit time	t_{PD}	t_{CKE}(min)	9*t_{REFI}	t_{CKE}(min)	9*t_{REFI}		15
Exit precharge power-down with DLL frozen to commands requiring a locked DLL	t_{XPDLL}	24	-	24	-	ns	2
		10	-	10	-	nCK	2
Exit power-down with DLL on to any valid command; Exit precharge power-down with DLL frozen to commands not requiring a locked DLL	t_{XP}	7.5	-	7.5	-	ns	
		3	-	3	-	nCK	
Command pass disable delay	t_{CPDED}	1	-	1	-	nCK	
Timing of ACT command to Power-down entry	$t_{ACTPDEN}$	1	-	1	-	nCK	20
Timing of PRE command to Power-down entry	t_{PRPDEN}	1	-	1	-	nCK	20
Timing of RD/RDA command to Power-down entry	t_{RDPDEN}	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power-down entry (BL8OTF, BL8MRS, BL4OTF)	t_{WRPDEN} (min)	WL + 4 + [tWR/tCK(avg)]				nCK	9
Timing of WR command to Power-down entry (BC4MRS)	t_{WRPDEN} (min)	WL + 2 + [tWR/tCK(avg)]				nCK	9
Timing of WRA command to Power-down entry (BL8OTF, BL8MRS, BL4OTF)	tWRAPDEN	WL+4 +WR+1	-	WL+4 +WR+1	-	nCK	10
Timing of WRA command to Power-down entry (BC4MRS)	tWRAPDEN	WL+2 +WR+1	-	WL+2 +WR+1	-	nCK	10
Timing of REF command to Power-down entry	$t_{REFPDEN}$	1	-	1	-	nCK	20,21
Timing of MRS command to Power-down entry	tMRSPDEN	t_{MOD} (min)	-	t_{MOD} (min)	-		
RTT turn-on	t_{AON}	-400	400	-300	300	ps	7
Asynchronous RTT turn-on delay (Power-down with DLL frozen)	t_{AONPD}	2	8.5	2	8.5	ns	
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	0.3	0.7	tCK(avg)	8
Asynchronous RTT turn-off delay (Power-down with DLL frozen)	t_{AOFPD}	2	8.5	2	8.5	ns	
ODT high time without write command or with write command and BC4	ODTH4	4	-	4	-	nCK	
ODT high time with Write command and BL8	ODTH8	6	-	6	-	nCK	
RTT dynamic change skew	t_{ADC}	0.3	0.7	0.3	0.7	t_{CK}(avg)	
Power-up and reset calibration time	t_{ZQinit}	512	-	512	-	nCK	

Parameter	Symbol	DDR3(L)-800		DDR3(L)-1066		Unit	Note
		Min	Max	Min	Max		
Normal operation full calibration time	t_{ZQoper}	256	-	256	-	nCK	
Normal operation short calibration time	t_{ZQCS}	64	-	64	-	nCK	23
First DQS pulse rising edge after write leveling mode is programmed	t_{WLMRD}	40	-	40	-	nCK	3
DQS, DQS delay after write leveling mode is pro-grammed	$t_{WLDQSEN}$	25	-	25	-	nCK	3
Write leveling setup time from rising CK, CK crossing to rising DQS, DQS crossing	t_{WLS}	325	-	245	-	ps	
Write leveling hold time from rising DQS, DQS crossing to rising CK, CK crossing	t_{WLH}	325	-	245	-	ps	
Write leveling output delay	t_{WLO}	0	9	0	9	ns	
Write leveling output error	t_{WLOE}	0	2	0	2	ns	
Absolute clock period	t_{CK}(abs)	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	ps	
Absolute clock high pulse width	t_{CH}(abs)	0.43	-	0.43	-	t_{CK}(avg)	30
Absolute clock low pulse width	t_{CL}(abs)	0.43	-	0.43	-	t_{CK}(avg)	31
Clock period jitter	t_{JIT}(per)	-100	100	-90	90	ps	
Clock period jitter during DLL locking period	t_{JIT}(per,lck)	-90	90	-80	80	ps	
Cycle to cycle period jitter	t_{JIT}(cc)	-	200	-	180	ps	
Cycle to cycle period jitter during DLL locking period	t_{JIT}(cc,lck)	-	180	-	160	ps	
Cumulative error across 2 cycles	t_{ERR}(2per)	-147	147	-132	132	ps	
Cumulative error across 3 cycles	t_{ERR}(3per)	-175	175	-157	157	ps	
Cumulative error across 4 cycles	t_{ERR}(4per)	-194	194	-175	175	ps	
Cumulative error across 5 cycles	t_{ERR}(5per)	-209	209	-188	188	ps	
Cumulative error across 6 cycles	t_{ERR}(6per)	-222	222	-200	200	ps	
Cumulative error across 7 cycles	t_{ERR}(7per)	-232	232	-209	209	ps	
Cumulative error across 8 cycles	t_{ERR}(8per)	-241	241	-217	217	ps	
Cumulative error across 9 cycles	t_{ERR}(9per)	-249	249	-224	224	ps	
Cumulative error across 10 cycles	t_{ERR}(10per)	-257	257	-231	231	ps	
Cumulative error across 11 cycles	t_{ERR}(11per)	-263	263	-237	237	ps	
Cumulative error across 12 cycles	t_{ERR}(12per)	-269	269	-242	242	ps	
Cumulative error across n = 13,14,...49,50 cycles	tERR(nper)	t_{ERR}(nper)min = (1 + 0.68ln(n))*t_{JIT}(per)min t_{ERR}(nper)max = (1 + 0.68ln(n))*t_{JIT}(per)max				ps	32

Parameter	Symbol	DDR3(L)-1333		DDR3(L)-1600		Unit	Note
		Min	Max	Min	Max		
Average clock cycle time	t_{CK}(avg)	Please refer Speed Bins				ps	
Minimum clock cycle time (DLL-off mode)	t_{CK} (DLL-off)	8	-	8	-	ns	6
Average CK high level width	t_{CH}(avg)	0.47	0.53	0.47	0.53	t_{CK}(avg)	
Average CK low level width	t_{CL}(avg)	0.47	0.53	0.47	0.53	t_{CK}(avg)	
Active Bank A to Active Bank B command period	t_{RRD}	7.5	-	7.5	-	ns	
		4	-	4	-	nCK	
Four activate window	t_{FAW}	45	-	40	-	ns	
Address and Control input hold time (VIH/VIL (DC100) levels)	t_{IH}(base) DC100	140	-	120	-	ps	16
Address and Control input setup time (VIH/VIL (AC175) levels)	t_{IS}(base) AC175	65	-	45	-	ps	16
Address and Control input setup time (VIH/VIL (AC150) levels)	t_{IS}(base) AC150	190	-	170	-	ps	16,24
DQ and DM input hold time (VIH/VIL (DC100) levels)	t_{DH}(base) DC100	65	-	45	-	ps	17
DQ and DM input setup time (VIH/VIL (AC175) levels)	t_{DS}(base) AC175	-	-	-	-	ps	17
DQ and DM input setup time (VIH/VIL (AC150) levels)	t_{DS}(base) AC150	30	-	10	-	ps	17
Control and Address Input pulse width for each input	t_{IPW}	620	-	560	-	ps	25
DQ and DM Input pulse width for each input	t_{DIPW}	400	-	360	-	ps	25
DQ high impedance time	t_{HZ}(DQ)	-	250	-	225	ps	13,14
DQ low impedance time	t_{LZ}(DQ)	-500	250	-450	225	ps	13,14
DQS, DQS high impedance time (RL + BL/2 reference)	t_{HZ}(DQS)	-	250	-	225	ps	13,14
DQS, DQS low impedance time (RL - 1 reference)	t_{LZ}(DQS)	-500	250	-450	225	ps	13,14
DQS, DQS to DQ Skew, per group, per access	t_{DQSQ}	-	125	-	100	ps	12,13
CAS to CAS command delay	t_{CCD}	4	-	4	-	nCK	
DQ output hold time from DQS, DQS	t_{QH}	0.38	-	0.38	-	t_{CK}(avg)	12,13
DQS, DQS rising edge output access time from rising CK, CK	t_{DQSCK}	-255	255	-225	225	ps	12,13
DQS latching rising transitions to associated clock edges	tDQSS	-0.25	0.25	-0.27	0.27	tCK(avg)	
DQS falling edge hold time from rising CK	tDSH	0.2	-	0.18	-	tCK(avg)	29
DQS falling edge setup time to rising CK	tDSS	0.2	-	0.18	-	tCK(avg)	29

Parameter	Symbol	DDR3(L)-1333		DDR3(L)-1600		Unit	Note
		Min	**Max**	**Min**	**Max**		
DQS input high pulse width	t_{DQSH}	0.45	0.55	0.45	0.55	t_{CK}(avg)	27,28
DQS input low pulse width	t_{DQSL}	0.45	0.55	0.45	0.55	t_{CK}(avg)	26,28
DQS output high time	t_{QSH}	0.40	-	0.40	-	t_{CK}(avg)	12,13
DQS output low time	t_{QSL}	0.40	-	0.40	-	t_{CK}(avg)	12,13
Mode register set command cycle time	t_{MRD}	4	-	4	-	nCK	
Mode register set command update delay	t_{MOD}	15	-	15	-	ns	
		12	-	12	-	nCK	
Read preamble time	t_{RPRE}	0.9	-	0.9	-	t_{CK}(avg)	13,19
Read postamble time	t_{RPST}	0.3	-	0.3	-	t_{CK}(avg)	11,13
Write preamble time	t_{WPRE}	0.9	-	0.9	-	t_{CK}(avg)	1
Write postamble time	t_{WPST}	0.3	-	0.3	-	t_{CK}(avg)	1
Write recovery time	t_{WR}	15	-	15	-	ns	
Auto precharge write recovery + Precharge time	t_{DAL}(min)	WR + roundup [tRP / tCK(avg)]				nCK	
Multi-purpose register recovery time	t_{MPRR}	1	-	1	-	nCK	22
Internal write to read command delay	t_{WTR}	7.5	-	7.5	-	ns	18
		4	-	4	-	nCK	18
Internal read to precharge command delay	t_{RTP}	7.5	-	7.5	-	ns	
		4	-	4	-	nCK	
Minimum CKE low width for Self-refresh entry to exit timing	tCKESR	t_{CKE}(min) +1nCK	-	t_{CKE}(min) +1nCK	-		
Valid clock requirement after Self-refresh entry or Power-down entry	t_{CKSRE}	10	-	10	-	ns	
		5	-	5	-	nCK	
Valid clock requirement before Self-refresh exit or Power-down exit	t_{CKSRX}	10	-	10	-	ns	
		5	-	5	-	nCK	
Exit Self-refresh to commands not requiring a locked DLL	t_{XS}	t_{RFC}(min) +10	-	t_{RFC}(min) +10	-	ns	
		5	-	5	-	nCK	
Exit Self-refresh to commands requiring a locked DLL	t_{XSDLL}	t_{DLLK} (min)	-	t_{DLLK} (min)	-	nCK	
Auto-refresh to Active/Auto-refresh command time	t_{RFC}	260	-	260	-	ns	
Average Periodic Refresh Interval 0°C ≤ Tc ≤ +85°C	t_{REFI}	-	7.8	-	7.8	µs	
Average Periodic Refresh Interval +85°C < Tc ≤ +95°C	t_{REFI}	-	3.9	-	3.9	µs	
CKE minimum high and low pulse width	t_{CKE}	5.625	-	5	-	ns	
		3	-	3	-	nCK	
Exit reset from CKE high to a valid command	t_{XPR}	t_{RFC}(min) +10	-	t_{RFC}(min) +10	-	ns	
		5	-	5	-	nCK	
DLL locking time	t_{DLLK}	512	-	512	-	nCK	

Parameter	Symbol	DDR3(L)-1333		DDR3(L)-1600		Unit	Note
		Min	Max	Min	Max		
Power-down entry to exit time	t_{PD}	t_{CKE}(min)	9*t_{REFI}	t_{CKE}(min)	9*t_{REFI}		15
Exit precharge power-down with DLL frozen to commands requiring a locked DLL	t_{XPDLL}	24	-	24	-	ns	2
		10	-	10	-	nCK	2
Exit power-down with DLL on to any valid command; Exit precharge power-down with DLL frozen to commands not requiring a locked DLL	t_{XP}	6	-	6	-	ns	
		3	-	3	-	nCK	
Command pass disable delay	t_{CPDED}	1	-	1	-	nCK	
Timing of ACT command to Power-down entry	$t_{ACTPDEN}$	1	-	1	-	nCK	20
Timing of PRE command to Power-down entry	t_{PRPDEN}	1	-	1	-	nCK	20
Timing of RD/RDA command to Power-down entry	t_{RDPDEN}	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power-down entry (BL8OTF, BL8MRS, BL4OTF)	t_{WRPDEN} (min)	WL + 4 + [tWR/tCK(avg)]				nCK	9
Timing of WR command to Power-down entry (BC4MRS)	t_{WRPDEN} (min)	WL + 2 + [tWR/tCK(avg)]				nCK	9
Timing of WRA command to Power-down entry (BL8OTF, BL8MRS, BL4OTF)	tWRAPDEN	WL+4 +WR+1	-	WL+4 +WR+1	-	nCK	10
Timing of WRA command to Power-down entry (BC4MRS)	tWRAPDEN	WL+2 +WR+1	-	WL+2 +WR+1	-	nCK	10
Timing of REF command to Power-down entry	$t_{REFPDEN}$	1	-	1	-	nCK	20,21
Timing of MRS command to Power-down entry	tMRSPDEN	t_{MOD} (min)	-	t_{MOD} (min)	-		
RTT turn-on	t_{AON}	-250	250	-225	225	ps	7
Asynchronous RTT turn-on delay (Power-down with DLL frozen)	t_{AONPD}	2	8.5	2	8.5	ns	
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	0.3	0.7	tCK(avg)	8
Asynchronous RTT turn-off delay (Power-down with DLL frozen)	t_{AOFPD}	2	8.5	2	8.5	ns	
ODT high time without write command or with write command and BC4	ODTH4	4	-	4	-	nCK	
ODT high time with Write command and BL8	ODTH8	6	-	6	-	nCK	
RTT dynamic change skew	t_{ADC}	0.3	0.7	0.3	0.7	t_{CK}(avg)	
Power-up and reset calibration time	t_{ZQinit}	512	-	512	-	nCK	
Normal operation full calibration time	t_{ZQoper}	256	-	256	-	nCK	
Normal operation short calibration time	t_{ZQCS}	64	-	64	-	nCK	23
First DQS pulse rising edge after write leveling mode is programmed	t_{WLMRD}	40	-	40	-	nCK	3

Parameter	Symbol	DDR3(L)-1333		DDR3(L)-1600		Unit	Note
		Min	Max	Min	Max		
DQS, DQS delay after write leveling mode is pro-grammed	$t_{WLDQSEN}$	25	-	25	-	nCK	3
Write leveling setup time from rising CK, CK crossing to rising DQS, DQS crossing	t_{WLS}	195	-	165	-	ps	
Write leveling hold time from rising DQS, DQS crossing to rising CK, CK crossing	t_{WLH}	195	-	165	-	ps	
Write leveling output delay	t_{WLO}	0	9	0	7.5	ns	
Write leveling output error	t_{WLOE}	0	2	0	2	ns	
Absolute clock period	t_{CK}(abs)	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	ps	
Absolute clock high pulse width	t_{CH}(abs)	0.43	-	0.43	-	t_{CK}(avg)	30
Absolute clock low pulse width	t_{CL}(abs)	0.43	-	0.43	-	t_{CK}(avg)	31
Clock period jitter	t_{JIT}(per)	-80	80	-70	70	ps	
Clock period jitter during DLL locking period	t_{JIT}(per,lck)	-70	70	-60	60	ps	
Cycle to cycle period jitter	t_{JIT}(cc)	-	160	-	140	ps	
Cycle to cycle period jitter during DLL locking period	t_{JIT}(cc,lck)	-	140	-	120	ps	
Cumulative error across 2 cycles	t_{ERR}(2per)	-118	118	-103	103	ps	
Cumulative error across 3 cycles	t_{ERR}(3per)	-140	140	-122	122	ps	
Cumulative error across 4 cycles	t_{ERR}(4per)	-155	155	-136	136	ps	
Cumulative error across 5 cycles	t_{ERR}(5per)	-168	168	-147	147	ps	
Cumulative error across 6 cycles	t_{ERR}(6per)	-177	177	-155	155	ps	
Cumulative error across 7 cycles	t_{ERR}(7per)	-186	186	-163	163	ps	
Cumulative error across 8 cycles	t_{ERR}(8per)	-193	193	-169	169	ps	
Cumulative error across 9 cycles	t_{ERR}(9per)	-200	200	-175	175	ps	
Cumulative error across 10 cycles	t_{ERR}(10per)	-205	205	-180	180	ps	
Cumulative error across 11 cycles	t_{ERR}(11per)	-210	210	-184	184	ps	
Cumulative error across 12 cycles	t_{ERR}(12per)	-215	215	-188	188	ps	
Cumulative error across n = 13,14,...49,50 cycles	tERR(nper)	t_{ERR}(nper)min = (1 + 0.68ln(n))*t_{JIT}(per)min t_{ERR}(nper)max = (1 + 0.68ln(n))*t_{JIT}(per)max				ps	32

		DDR3(L)-1866					
Parameter	**Symbol**	**Min**	**Max**			**Unit**	**Note**
Average clock cycle time	t_{CK}(avg)	Please refer Speed Bins				ps	
Minimum clock cycle time (DLL-off mode)	t_{CK} (DLL-off)	8	-			ns	6
Average CK high level width	t_{CH}(avg)	0.47	0.53			t_{CK}(avg)	
Average CK low level width	t_{CL}(avg)	0.47	0.53			t_{CK}(avg)	
Active Bank A to Active Bank B command period	t_{RRD}	6	-			ns	
		4	-			nCK	
Four activate window	t_{FAW}	35	-			ns	
Address and Control input hold time (VIH/VIL (DC100) levels)	t_{IH}(base) DC100	100	-			ps	16
Address and Control input setup time (VIH/VIL (AC125) levels)	t_{IS}(base) AC125	150	-			ps	16
Address and Control input setup time (VIH/VIL (AC135) levels)	t_{IS}(base) AC135	65	-			ps	16
DQ and DM input hold time (VIH/VIL (DC100) levels)	t_{DH}(base) DC100	70	-			ps	17
DQ and DM input setup time (VIH/VIL (AC135) levels)	t_{DS}(base) AC135	68	-			ps	17
Control and Address Input pulse width for each input	t_{IPW}	535	-			ps	25
DQ and DM Input pulse width for each input	t_{DIPW}	320	-			ps	25
DQ high impedance time	t_{HZ}(DQ)	-	195			ps	13,14
DQ low impedance time	t_{LZ}(DQ)	-390	195			ps	13,14
DQS, DQS high impedance time (RL + BL/2 reference)	t_{HZ}(DQS)	-	195			ps	13,14
DQS, DQS low impedance time (RL - 1 reference)	t_{LZ}(DQS)	-390	195			ps	13,14
DQS, DQS to DQ Skew, per group, per access	t_{DQSQ}	-	85			ps	12,13
CAS to CAS command delay	t_{CCD}	4	-			nCK	
DQ output hold time from DQS, DQS	t_{QH}	0.38	-			t_{CK}(avg)	12,13
DQS, DQS rising edge output access time from rising CK, CK	t_{DQSCK}	-195	195			ps	12,13
DQS latching rising transitions to associated clock edges	tDQSS	-0.27	0.27			tCK(avg)	
DQS falling edge hold time from rising CK	tDSH	0.18	-			tCK(avg)	29
DQS falling edge setup time to rising CK	tDSS	0.18	-			tCK(avg)	29
DQS input high pulse width	t_{DQSH}	0.45	0.55			t_{CK}(avg)	27,28

Parameter	Symbol	DDR3(L)-1866				Unit	Note
		Min	Max				
DQS input low pulse width	t_{DQSL}	0.45	0.55			t_{CK}(avg)	26,28
DQS output high time	t_{QSH}	0.40	-			t_{CK}(avg)	12,13
DQS output low time	t_{QSL}	0.40	-			t_{CK}(avg)	12,13
Mode register set command cycle time	t_{MRD}	4	-			nCK	
Mode register set command update delay	t_{MOD}	15	-			ns	
		12	-			nCK	
Read preamble time	t_{RPRE}	0.9	-			t_{CK}(avg)	13,19
Read postamble time	t_{RPST}	0.3	-			t_{CK}(avg)	11,13
Write preamble time	t_{WPRE}	0.9	-			t_{CK}(avg)	1
Write postamble time	t_{WPST}	0.3	-			t_{CK}(avg)	1
Write recovery time	t_{WR}	15	-			ns	
Auto precharge write recovery + Precharge time	t_{DAL}(min)	WR + roundup [tRP / tCK(avg)]				nCK	
Multi-purpose register recovery time	t_{MPRR}	1	-			nCK	22
Internal write to read command delay	t_{WTR}	7.5	-			ns	18
		4	-			nCK	18
Internal read to precharge command delay	t_{RTP}	7.5	-			ns	
		4	-			nCK	
Minimum CKE low width for Self-refresh entry to exit timing	tCKESR	t_{CKE}(min) +1nCK	-				
Valid clock requirement after Self-refresh entry or Power-down entry	t_{CKSRE}	10	-			ns	
		5	-			nCK	
Valid clock requirement before Self-refresh exit or Power-down exit	t_{CKSRX}	10	-			ns	
		5	-			nCK	
Exit Self-refresh to commands not requiring a locked DLL	t_{XS}	t_{RFC}(min) +10	-			ns	
		5	-			nCK	
Exit Self-refresh to commands requiring a locked DLL	t_{XSDLL}	t_{DLLK} (min)	-			nCK	
Auto-refresh to Active/Auto-refresh command time	t_{RFC}	260	-			ns	
Average Periodic Refresh Interval 0°C $\leq$ Tc $\leq$ +85°C	t_{REFI}	-	7.8			µs	
Average Periodic Refresh Interval +85°C < Tc $\leq$ +95°C	t_{REFI}	-	3.9			µs	
CKE minimum high and low pulse width	t_{CKE}	5	-			ns	
		3	-			nCK	
Exit reset from CKE high to a valid command	t_{XPR}	t_{RFC}(min) +10	-			ns	
		5	-			nCK	

Parameter	Symbol	DDR3(L)-1866				Unit	Note
		Min	Max				
DLL locking time	t_{DLLK}	512	-			nCK	
Power-down entry to exit time	t_{PD}	t_{CKE}(min)	9*t_{REFI}				15
Exit precharge power-down with DLL frozen to commands requiring a locked DLL	t_{XPDLL}	24	-			ns	2
		10	-			nCK	2
Exit power-down with DLL on to any valid command; Exit precharge power-down with DLL frozen to commands not requiring a locked DLL	t_{XP}	6	-			ns	
		3	-			nCK	
Command pass disable delay	t_{CPDED}	2	-			nCK	
Timing of ACT command to Power-down entry	$t_{ACTPDEN}$	1	-			nCK	20
Timing of PRE command to Power-down entry	t_{PRPDEN}	1	-			nCK	20
Timing of RD/RDA command to Power-down entry	t_{RDPDEN}	RL+4+1	-			nCK	
Timing of WR command to Power-down entry (BL8OTF, BL8MRS, BL4OTF)	t_{WRPDEN} (min)	WL + 4 + [tWR/tCK(avg)]				nCK	9
Timing of WR command to Power-down entry (BC4MRS)	t_{WRPDEN} (min)	WL + 2 + [tWR/tCK(avg)]				nCK	9
Timing of WRA command to Power-down entry (BL8OTF, BL8MRS, BL4OTF)	tWRAPDEN	WL+4 +WR+1	-			nCK	10
Timing of WRA command to Power-down entry (BC4MRS)	tWRAPDEN	WL+2 +WR+1	-			nCK	10
Timing of REF command to Power-down entry	$t_{REFPDEN}$	1	-			nCK	20,21
Timing of MRS command to Power-down entry	tMRSPDEN	t_{MOD} (min)	-				
RTT turn-on	t_{AON}	-195	195			ps	7
Asynchronous RTT turn-on delay (Power-down with DLL frozen)	t_{AONPD}	2	8.5			ns	
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7			tCK(avg)	8
Asynchronous RTT turn-off delay (Power-down with DLL frozen)	t_{AOFPD}	2	8.5			ns	
ODT high time without write command or with write command and BC4	ODTH4	4	-			nCK	
ODT high time with Write command and BL8	ODTH8	6	-			nCK	
RTT dynamic change skew	t_{ADC}	0.3	0.7			t_{CK}(avg)	
Power-up and reset calibration time	t_{ZQinit}	512	-			nCK	
Normal operation full calibration time	t_{ZQoper}	256	-			nCK	
Normal operation short calibration time	t_{ZQCS}	64	-			nCK	23

Parameter	Symbol	DDR3(L)-1866				Unit	Note
		Min	Max				
First DQS pulse rising edge after write leveling mode is programmed	t_{WLMRD}	40	-			nCK	3
DQS, DQS delay after write leveling mode is pro-grammed	$t_{WLDQSEN}$	25	-			nCK	3
Write leveling setup time from rising CK, CK crossing to rising DQS, DQS crossing	t_{WLS}	140	-			ps	
Write leveling hold time from rising DQS, DQS crossing to rising CK, CK crossing	t_{WLH}	140	-			ps	
Write leveling output delay	t_{WLO}	0	7.5			ns	
Write leveling output error	t_{WLOE}	0	2			ns	
Absolute clock period	t_{CK}(abs)	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max			ps	
Absolute clock high pulse width	t_{CH}(abs)	0.43	-			t_{CK}(avg)	30
Absolute clock low pulse width	t_{CL}(abs)	0.43	-			t_{CK}(avg)	31
Clock period jitter	t_{JIT}(per)	-60	60			ps	
Clock period jitter during DLL locking period	t_{JIT}(per,lck)	-50	50			ps	
Cycle to cycle period jitter	t_{JIT}(cc)	-	120			ps	
Cycle to cycle period jitter during DLL locking period	t_{JIT}(cc,lck)	-	100			ps	
Cumulative error across 2 cycles	t_{ERR}(2per)	-88	88			ps	
Cumulative error across 3 cycles	t_{ERR}(3per)	-105	105			ps	
Cumulative error across 4 cycles	t_{ERR}(4per)	-117	117			ps	
Cumulative error across 5 cycles	t_{ERR}(5per)	-126	126			ps	
Cumulative error across 6 cycles	t_{ERR}(6per)	-133	133			ps	
Cumulative error across 7 cycles	t_{ERR}(7per)	-139	139			ps	
Cumulative error across 8 cycles	t_{ERR}(8per)	-145	145			ps	
Cumulative error across 9 cycles	t_{ERR}(9per)	-150	150			ps	
Cumulative error across 10 cycles	t_{ERR}(10per)	-154	154			ps	
Cumulative error across 11 cycles	t_{ERR}(11per)	-158	158			ps	
Cumulative error across 12 cycles	t_{ERR}(12per)	-161	161			ps	
Cumulative error across n = 13,14,...49,50 cycles	tERR(nper)	t_{ERR}(nper)min = (1 + 0.68ln(n))*t_{JIT}(per)min t_{ERR}(nper)max = (1 + 0.68ln(n))*t_{JIT}(per)max				ps	32

Notes for AC Electrical Characteristics

NOTE :

1. Actual value dependant upon measurement level definitions which are TBD.
2. Commands requiring a locked DLL are: READ (and READA) and synchronous ODT commands.
3. The max values are system dependent.
4. WR as programmed in mode register.
5. Value must be rounded-up to next higher integer value.
6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, tREFI.
7. ODT turn on time (min.) is when the device leaves high impedance and ODT resistance begins to turn on.

ODT turn on time (max.) is when the ODT resistance is fully on. Both are measured from ODTLon.

8. ODT turn-off time (min.) is when the device starts to turn-off ODT resistance. ODT turn-off time (max.) is when the bus is in high impedance. Both are measured from ODTLoff.

9. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR / tCK to the next integer.
10. WR in clock cycles as programmed in MR0.
11. The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side.
12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by TBD.
13. Value is only valid for RON34.
14. Single ended signal parameter. Refer to the section of tLZ(DQS), tLZ(DQ), tHZ(DQS), tHZ(DQ) Notes for definition and measurement method.
15. tREFI depends on operating case temperature (Tc).
16. tIS(base) and tIH(base) values are for 1V/ns command/addresss single-ended slew rate and 2V/ns CK, /CK differential slew rate, Note for DQ and DM signals, VREF(DC) = VREFDQ(DC). For input only pins except /RESET, VREF(DC) = VREFCA(DC). See Address / Command Setup, Hold and Derating section.
17. tDS(base) and tDH(base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, /DQS differential slew rate. Note for DQ and DM signals,VREF(DC)= VREFDQ(DC). For input only pins except RESET, VREF(DC) = VREFCA(DC). See Data Setup, Hold and and Slew Rate Derating section.
18. Start of internal write transaction is defined as follows ;

For BL8 (fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL. For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL.

For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.

19. The maximum read preamble is bound by tLZDQS(min) on the left side and tDQSCK(max) on the right side.
20. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operation.
21. Although CKE is allowed to be registered LOW after a REFRESH command once tREFPDEN(min) is satisfied, there are cases where additional time such as tXPDLL(min) is also required.
22. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
23. One ZQCS command can effectively correct a minimum of 0.5 % (ZQCorrection) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the “Output Driver Voltage and Temperature Sensitivity” and “ODT Voltage and Temperature Sensitivity” tables. The appropriate interval between ZQCS commands can be determined from these tables and other application specific parameters.

One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{\text{ZQCorrection}}{(\text{TSens} \times \text{Tdriftrate}) + (\text{VSens} \times \text{Vdriftrate})}$$

where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.

24. The tIS(base) AC150 specifications are adjusted from the tIS(base) specification by adding an additional 100 ps of derating to accommodate for the lower alternate threshold of 150 mV and another 25 ps to account for the earlier reference point [(175 mv - 150 mV) / 1 V/ns].
25. Pulse width of a input signal is defined as the width between the first crossing of VREF(DC) and the consecutive crossing of VREF(DC).
26. tDQSL describes the instantaneous differential input low pulse width on DQS - /DQS, as measured from one falling edge to the next consecutive rising edge.
27. tDQSH describes the instantaneous differential input high pulse width on DQS - /DQS, as measured from one rising edge to the next consecutive falling edge.

28. tDQSH,act + tDQSL,act = 1 tCK,act ; with tXYZ,act being the actual measured value of the respective timing parameter in the application.
29. tDSH,act + tDSS,act = 1 tCK,act ; with tXYZ,act being the actual measured value of the respective timing parameter in the application.
30. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
31. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
32. n = from 13 cycles to 50 cycles. This row defines 38 parameters.

4.3 IDD Specification

(VDD = 1.283V to 1.45V or 1.5 V ± 0.075V; VDDQ =1.283V to 1.45V or 1.5 V ± 0.075V)

TABLE 37
IDD Specification

Conditions	Symbol	Data rate (Mbps)	IDD max. 1.5V	IDD max. 1.35V	Unit
Operating One Bank Active-Precharge Current; CKE: High; External clock: On; tCK, nRC, nRAS, CL: see timing used table; BL: 8; AL: 0; CS: High between ACT and PRE; Command, Address: partially toggling; Data IO: FLOATING; DM:stable at 0; Bank Activity: Cycling with one bank active at a time; Output Buffer and RTT: Enabled in Mode Regis- ters; ODT Signal: stable at 0	IDD0	1866 1600 1333 1066 800	60 55 50 45 40	60 55 50 45 40	mA
Operating One Bank Active-Read-Precharge Current; CKE: High; External clock On; tCK, nRC, nRAS, nRCD, CL: see timing used table; BL: 81; AL: 0; CS: Hig between ACT, RD and PRE; Command, Address, Data IO: partially toggling DM:stable at 0; Bank Activ- ity: Cycling with one bank active at a time; Output Buffe and RTT: Enabled in Mode Reg- isters; ODT Signal: stable at 0	IDD1	1866 1600 1333 1066 800	80 75 70 65 60	80 75 70 65 60	mA
Precharge Power-Down Current Slow Exit; CKE: Low; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; CS: stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: En- abled in Mode Registers; ODT Signal: stable at 0; Pre-charge Power Down Mode: Slow Exit	IDD2P0	1866 1600 1333 1066 800	12 12 12 12 12	12 12 12 12 12	mA
Precharge Power-Down Current Fast Exit; CKE: Low; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; CS: stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: En- abled in Mode Registers; ODT Signal: stable at 0; Pre-charge Power Down Mode: Fast Exit	IDD2P1	1866 1600 1333 1066 800	19 18 17 16 15	19 18 17 16 15	mA
Precharge Standby Current; CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; CS: stable at 1; Command, Address: partially toggling; Data IO: FLOATING; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: En- abled in Mode Registers; ODT Signal: stable at 0	IDD2N	1866 1600 1333 1066 800	25 25 25 25 25	25 25 25 25 25	mA
Precharge Standby ODT Current; CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; CS: stable at 1; Command, Address: partially toggling; Data IO: FLOATING; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: En- abled in Mode Registers; ODT Signal: toggling	IDD2NT	1866 1600 1333 1066 800	30 30 30 30 30	30 30 30 30 30	mA
Precharge Quiet Standby Current; CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; CS: stable at 1; Command, Address: stable at 0; Data IO: FLOATING DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled i Mode Reg- isters; ODT Signal: stable at 0	IDD2Q	1866 1600 1333 1066 800	25 25 25 25 25	25 25 25 25 25	mA
Active Power-Down Current; CKE: Low; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; CS: stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD3P	1866 1600 1333 1066 800	22 22 22 22 22	22 22 22 22 22	mA

Conditions	Symbol	Data rate (Mbps)	IDD max. 1.5V	IDD max. 1.35V	Unit
Active Standby Current; CKE: High; External clock: On; tCK, CL: see timing used table;BL: 8; AL: 0; CS: stable at 1; Command, Address: partially toggling; Data IO: FLOATING;DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD3N	1866 1600 1333 1066 800	34 32 30 28 26	34 32 30 28 26	mA
Operating Burst Read Current; CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; CS: High between RD; Command, Address: par-tially toggling; Data IO: seamless read data burst with different data between one burst and the next one; DM:stable at 0; Bank Activity: all banks open, RD commands cycling through banks:0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD4R	1866 1600 1333 1066 800	150 135 120 105 90	150 135 120 105 90	mA
Operating Burst Write Current; CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; CS: High between WR; Command, Address: par-tially toggling; Data IO: seamless write data burst with different data between one burst and the next one; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at HIGH	IDD4W	1866 1600 1333 1066 800	165 150 135 120 105	165 150 135 120 105	mA
Burst Refresh Current; CKE: High; External clock: On; tCK, CL, nRFC: see timing used table; BL: 8; AL: 0; CS: High between REF; Command, Address: partially toggling; Data IO: FLOATING; DM:stable at 0; Bank Activity: REF command every nRFC; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD5B	1866 1600 1333 1066 800	160 160 160 160 160	160 160 160 160 160	mA
Self Refresh Current: Normal Temperature Range; TCASE: 0- 85°C; Auto Self-Re-fresh (ASR): Disabled; Self-Refresh Temperature Range (SRT): Normal; CKE: Low; Ex-ternal clock: Off; CK and CK: LOW; CL: see timing used table; BL: 8; AL: 0; CS,Command, Address, Data IO: FLOATING; DM: stable at 0; Bank Activity: Self-Refresh op-eration; Output Buffer and RTT: Enabled in Mode Registers; ODT signal: FLOATING	IDD6	1866 1600 1333 1066 800	12	12	mA
Self Refresh Current: Extended Temperature Range; TCASE: 0- 95°C; Auto Self-Re-fresh (ASR): Disabled; Self-Refresh Temperature Range (SRT): Extended; CKE: Low; Ex-ternal clock: Off; CK and CK: LOW; CL: see timing used table; BL: 8; AL: 0; CS, Command, Address, Data IO: FLOATING; DM: stable at 0; Bank Activity: Extended Tem-perature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers;ODT Signal: FLOATING	IDD6ET	1866 1600 1333 1066 800	17	17	mA
Operating Bank Interleave Read Current; CKE: High; External clock: On; tCK, nRC,nRAS, nRCD, nRRD, nFAW, CL: see timing used table; BL: 8; AL: CL-1; CS: High be-tween ACT and RDA; Command, Address: partially toggling; Data IO: read data burstswith different data between one burst and the next one; DM: stable at 0; Bank Activity: twotimes interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD7	1866 1600 1333 1066 800	215 195 175 155 135	215 195 175 155 135	mA
RESET Low Current; RESET: Low; External clock: off; CK and CK: LOW; CKE: FLOAT-ING; CS, Command, Address, Data IO: FLOATING; ODT Signal : FLOATING	IDD8	1866 1600 1333 1066 800	12	12	mA

NOTE :

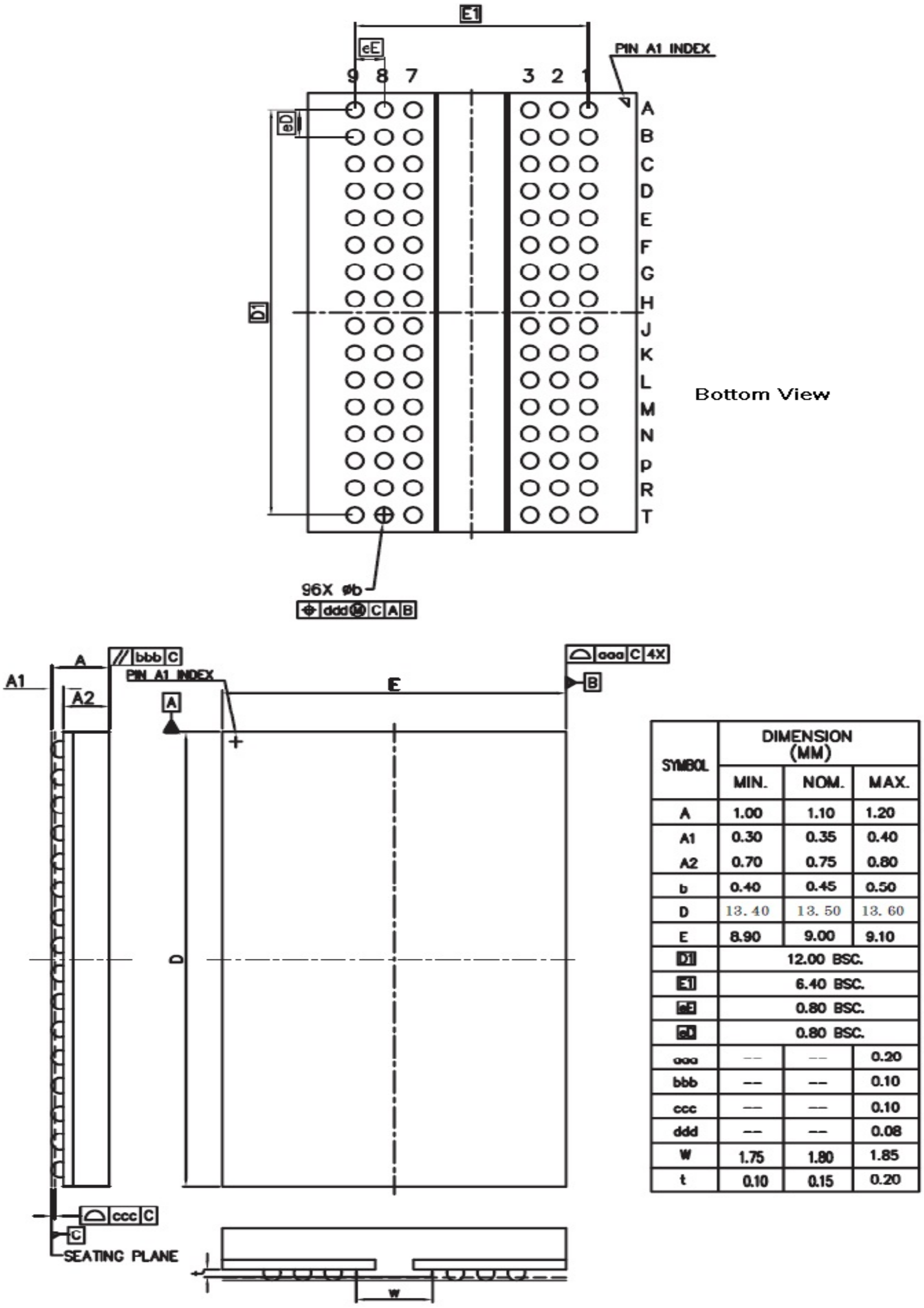
1) Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B

2) Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT_Nom enable: set MR1 A[9,6,2] = 011B; RTT_Wr enable: set MR2 A[10,9] = 10B

5 Package Outlines

Figure 5 reflects the current status of the outline dimensions of the DDR3(L) packages for 4Gbit components x16 configuration. For functional description of each ball see **Chapter 1.4**.

FIGURE 5
Package outline



SYMBOL	DIMENSION (MM)		
	MIN.	NOM.	MAX.
A	1.00	1.10	1.20
A1	0.30	0.35	0.40
A2	0.70	0.75	0.80
b	0.40	0.45	0.50
D	13.40	13.50	13.60
E	8.90	9.00	9.10
D1	12.00 BSC.		
E1	6.40 BSC.		
eE	0.80 BSC.		
eD	0.80 BSC.		
aaa	--	--	0.20
bbb	--	--	0.10
ccc	--	--	0.10
ddd	--	--	0.08
W	1.75	1.80	1.85
t	0.10	0.15	0.20

6 Product Type Nomenclature

For reference the UniIC SDRAM component nomenclature is enclosed in this chapter.

TABLE 38
Examples for Nomenclature Fields

Example for	Field Number									
	1	2	3	4	5	6	7	8	9	10
DDR3(L) DRAM	HXB	15	H	4G	16	0	A	F	–	13K

TABLE 39
DDR3 (L) Memory Components

Field	Description	Values	Coding
1	UniIC Component Prefix	HXB	Memory components, standard temperature range (0°C – +95 °C)
		HXI	Memory components, industrial temperature range (-40°C – +95 °C)
2	Interface Voltage [V]	18	SSTL_18, + 1.8 V (± 0.1 V)
		15	SSTL_15, + 1.5 V (± 0.1 V)
		13	VDD, VDDQ= 1.283V to 1.45V ;Typical:1.35V
3	DRAM Technology	H	DDR3 (L)
4	Component Density [Mbit]	32	32 Mbit
		64	64 Mbit
		128	128 Mbit
		256	256 Mbit
		512	512 Mbit
		1G	1 Gbit
		2G	2 Gbit
		4G	4 Gbit
5	Number of I/Os	40	× 4
		80	× 8
		16	× 16
6	Product Variant	0 .. 9	–
7	Die Revision	A	First
		B	Second
		C	Third
8	Package, Lead-Free Status	C	FBGA, lead-containing
		F	FBGA, lead-free
9	Power	–	Standard power product
		L	Low power product

Field	Description	Values	Coding
10	Speed Grade	19F	CL–tRCD–tRP = 7–7–7
		19G	CL–tRCD–tRP = 8–8–8
		15G	CL–tRCD–tRP = 8–8–8
		15H	CL–tRCD–tRP = 9–9–9
		13K	CL–tRCD–tRP = 11–11–11
		11M	CL–tRCD–tRP = 13–13–13

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