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SONET/SDH Framer  
with Integrated Ser/Des CRU

**Databook**

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IBM Microelectronics Division  
1580 Route 52, Bldg. 504  
Hopewell Junction, NY 12533-6351

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**IBM SONET/SDH Framer****Features**

- Integrated clock recovery and synthesis for four OC-3c/STM-1 signals or one OC-12/OC-12c/STM-4/STM-4c signal
- OC-12/STM-4 or quad OC-3c/STM-1 framing and performance monitoring
- Expansion port for OC-48/STM-16 operation
- Complete Transport/Section Overhead processing and generation conforming to Bellcore and ITU-T standards
- Complete Path Overhead processing and generation for one STS-12c/STM-4c signal or for four STS-3c/STM-1 signals for ATM/PPP
- VC-4 cross-connect, APS for ATM/PPP payloads using the UTOPIA port(s)
- Cell or frame delineation function for four 155 Mb/s signals or one (concatenated or unconcatenated) 622 Mb/s signal
- "PPP" octet stuffing and mapping per RFC1662 and RFC1619 for four 155 Mb/s signals or one unconcatenated multi-PHY 622 Mb/s signal or one concatenated single-PHY 622 Mb/s signal
- One UTOPIA L2+ (cell/frame) 16-bit interface at 50 MHz or two UTOPIA L1 8-bit at 25 MHz
- Quad byte-parallel Telecom Bus at 19.44 MHz
- Access to Line or Section DCC via a port
- Ring port for USHR/P support
- Selectable Intel®/Motorola-compatible microprocessor interface
- Boundary scan capability (IEEE 1149.1)
- 0.35 micron CMOS technology
- Single +3.3 V, ±5% power supply
- 5 V tolerant input/output interfaces (except to line)
- Approx. 4.1 W typ. (four 155 Mb/s interfaces), approx. 3.3 W typ. (one interface at 622 Mb/s)
- 474-pin ceramic ball grid array package initially
- Plastic ball grid array package in future
- SONET/SDH add/drop or higher-order terminal multiplexers
- Transport of ATM/PPP or VT/TU payloads over SONET/SDH
- Transmission of E1/DS1, E3/DS3 or E4 over SONET/SDH
- ATM switches

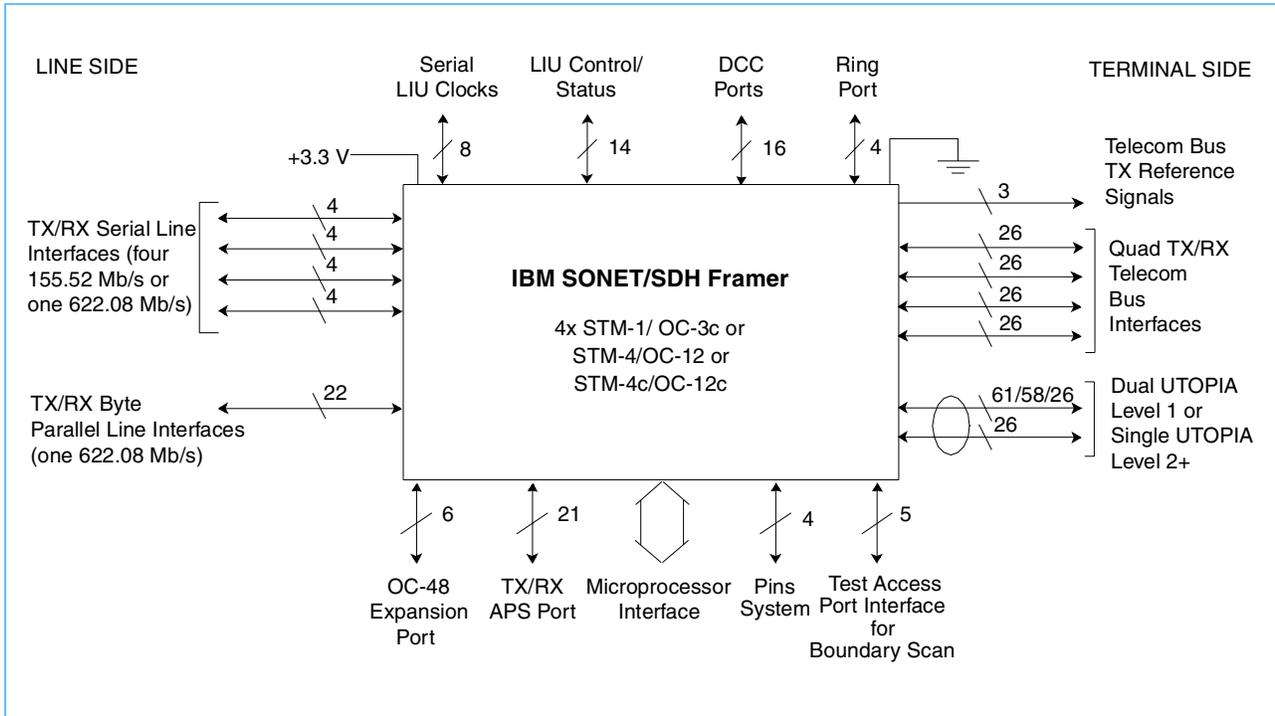
**Description**

IBM3009K2672 is a highly integrated SONET/SDH terminator device designed for ATM cell, frame, higher-order multiplexing, and transmission applications. The primary applications of the SONET/SDH framer are transport of ATM/PPP payloads over SONET/SDH, higher-order muxes, and add/drop muxes. A single IBM SONET/SDH framer can terminate four individual STS-3c or STM-1 lines or a single OC-12/12c or STM-4/4c line. Each SONET/SDH terminator has an associated line interface block that performs clock synthesis and clock recovery for four 155.52 Mb/s signals or single 622.08 Mb/s serial operation. A parallel line interface port and an expansion port allow four SONET/SDH framers to operate in unison for OC-48/STM-16 applications.

The SONET/SDH framer can terminate ATM payloads from any of the above signals into either a single 16-bit or 8-bit UTOPIA Level 2 PHY interface, or two 8-bit UTOPIA Level 1 PHY interfaces. PPP payloads are terminated into a 16-bit wide UTOPIA Level 2+ interface. STM (VT/TU) payloads can be terminated into four 8-bit wide Telecom Bus interfaces. When terminating concatenated payloads, the four Telecom Bus interfaces act in concert as a single 32-bit wide Telecom Bus interface. Single-device APS switching or 1:N APS between multiple SONET/SDH framers is also provided for ATM and PPP payloads.

**IBM SONET/SDH Framer**

**Interface Signals**



**Ordering Information**

| Part Number  | Description  |
|--------------|--|
| IBM3009K2672 | 474-pin Ceramic Ball Grid Array package with Direct Lid Attach |

**Conventions and Notation**

Throughout this document, SDH and SONET terminology are used interchangeably when describing portions of the payload or overhead of a SONET/SDH frame. SDH terminology provides more “granularity” for describing parts of a frame and hence is used more often.

The use of overbars, for example  $\overline{\text{DDEL\_OUT}}$ , designates signals that are active low.

Notation for bit encoding is as follows:

- Hexadecimal values are followed by H. For example: 0B00 H.
- Binary values in text are either spelled out (zero and one) or appear in quotation marks followed by b. For example: ‘10101’b.
- Binary values in the Default and Description columns of the register sections have no special marking, but are isolated from text as in this example:  
 0: No action on read access  
 1: Auto-reset interrupt request register upon read access

## Standards Compliance

Standards documents applicable to the functions of the SONET/SDH framer are listed in the table below. The addresses and other contact information for the organizations that publish them are listed in Standards Documentation Sources on page 277. Throughout this databook, references to these documents show the document number in brackets, e.g. [G.703].

| Document Number | Description   |
|-----------------|---|
| I.361           | ITU-T, Integrated Services Digital Network (ISDN) - Overall Network Aspects and Functions, (11/95)                            |
| I.432.1         | ITU-T, B-ISDN User-Network Interface - Physical Layer Specification: General Characteristics, (08/96)                         |
| G.707           | ITU-T, Network Node Interface for the Synchronous Digital Hierarchy, (03/96)  |
| G.781           | ITU-T, Structure of Recommendations on Equipment for the Synchronous Digital Hierarchy (SDH), (11/92)                         |
| G.782           | ITU-T, Types and Characteristics of Synchronous Digital Hierarchy (SDH) Equipment, (01/94)                                    |
| G.783           | ITU-T, Characteristics of Synchronous Digital Hierarchy (SDH) Equipment Functional Blocks, (04/97)                            |
| G.803           | ITU-T, Architectures of Transport Networks Based on the Synchronous Digital Hierarchy (SDH), (03/93)                          |
| GR-253          | Bellcore, GR-253-CORE, Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria, Issue 2, (12/95)       |
| GR-499          | Bellcore, GR-499-CORE, Transport Systems Generic Requirements (TSGR): Common Requirements, Issue 1, (December 1995)           |
| TR-NWT-000496   | Bellcore, TR-NWT-000496, SONET Add-Drop Multiplex Equipment (SONET ADM) Generic Criteria, Issue 3, (May 1992)                 |
| UL1             | ATM Forum, UTOPIA - An ATM PHY Interface Specification, Level 1, Version 2.01, (03/94)  |
| UL2v1           | ATM Forum, UTOPIA Level 2, Version 1.0, (06/95)   |
| RFC1662         | IETF, PPP in HDLC-like Framing, (07/94)   |
| RFC1619         | IETF, PPP Over SONET/SDH, (05/94)   |
| T1.105-1995     | ANSI, Synchronous Optical Network (SONET) - Basic Description including Multiplex Structure, Rates, and Formats, (1995)       |
| T1X1.5/97-127   | ANSI, Contribution to the T1 Standards Project, Enabling Transparency for the PPP over SONET/SDH Mapping, (12/97)             |
| T1X1.5/97-129   | ANSI, Contribution to the T1 Standards Project, Scramblers for PPP over SONET/SDH: Consideration and Analysis, (12/97)        |
| ISO13239.2      | ISO/IEC, Draft Information Technology - Telecommunications and information exchange between systems - HDLC procedures, (1996) |
| IEEE 1149.1     | IEEE Standard Access Port and Boundary Scan Architecture (1990, supplement a 1993, and supplement b 1994)                     |

## Overview

The SONET/SDH framer is a highly integrated SONET/SDH terminator device designed for transmission, cell, and frame applications. It contains four independent SONET/SDH terminators, which can either terminate ATM/PPP payloads into a UTOPIA Level 2 PHY or Level 2+ interface, or two Level 1 PHY interfaces, or it can interface the SONET/SDH frames to four Telecom Bus interfaces. It is a 3.3 V device with 5 V tolerant inputs and outputs for its Non-Line Interface signals. Several other interfaces are provided to facilitate DCC channel connection to an external HDLC controller, APS, ring operation, and OC-48/STM-16 operation. The IBM SONET/SDH framer is being provided initially in a 474-pin ceramic ball grid array package, but a plastic ball grid array package is planned for future manufacture.

The four SONET/SDH terminators can be configured for operation as either:

- Four individual terminators for STM-1 or STS-3c applications.
- A 4:1 MUX/DEMUX for STM-4 or STS-12 applications.
- A single STM-4c or STS-12c terminator.
- An STM-16/STS-48 interface where four SONET/SDH framers are connected in parallel. An external MUX/DEMUX device is required for this function.

Each SONET/SDH terminator has a Line Interface Unit (LIU) block associated with it that performs clock synthesis and clock recovery for 155.52 Mb/s serial operation. The first LIU block can also perform clock synthesis and clock recovery for 622.08 Mb/s serial operation. When STM-16/OC-48 operation is enabled, the external MUX/DEMUX is required to perform the clock recovery/synthesis. In this case the 8-bit parallel SONET/SDH Line interface will be used at 77.76 MHz.

The Line interfaces are connected to corresponding SONET/SDH Frame Handler (SFH) blocks. These blocks provide the Regenerator Section Overhead (RSOH) and Multiplex Section Overhead (MSOH) functions, i.e. TOH functions. All receive and transmit RSOH, MSOH, and Path Overhead (POH) bytes are stored in the on-chip RAM from where they can be observed/transmitted and also accessed via the microprocessor interface. The four SFH blocks can operate independently for STM-1/STS-3c applications or can operate together for STM-4/STS-12<sup>1</sup> or STM-4c/STS-12c applications. For STM-16/STS-48 applications, an OC-48/STM-16 Expansion Port is provided for synchronizing operation between multiple SONET/SDH framers. Four individual interfaces are provided for each DCC svhannel (regenerator or multiplex section) for connection to an external HDLC controller. The DCC bytes can optionally be inserted via the microprocessor interface. A Ring Port is provided that is used to communicate Line FEBE and RDI, K1 and K2 bytes plus associated alarms (and, when ATM or PPP processing is performed, K3 byte and associated indications as well as path FEBE and RDI information) between SONET/SDH framers. The SFHs can interface to either the external Telecom Bus interfaces or the ATM/PPP blocks.

The SONET/SDH framer has four individual and independent Telecom Bus interfaces which provide an alternative interface to the UTOPIA Level 2+ style interface. The Telecom Bus interface is a byte-wide interface with control signals for identification of the VC-4 and TOH time slots as well as the location of the J0 and J1 bytes. There is one Telecom Bus interface associated with each SFH. However, as is the case with the SFHs, the four Telecom Bus interfaces can operate in concert with each other as one 32-bit wide Telecom Bus interface when STM-4c/STS-12c frames are being processed. The SONET/SDH framer is not restricted to ATM or PPP in "HDLC-like framing" payloads due to the general nature of the Telecom Bus interface. However, when the Telecom Bus interface is used, the SONET/SDH framer does not provide POH processing. Transmit retiming is programmable on a per Telecom Bus basis. Receive retiming is not available. For devices where transmit retiming is not used, a reference clock and frame signal are provided by the SONET/SDH framer to

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1. Already for STM-4 operation, the OFPs have to jointly calculate the B1 and perform frame scrambling over the entire frame. STM-4c, in addition, requires joint B3 calculation, etc.

be used by external devices that are supplying data to the transmit Telecom Bus interfaces. Failure input and outputs are provided for each Telecom Bus interface. In the receive direction, these pins signal to a downstream device that conditions for generating Path AIS have been detected by the SONET/SDH framer. In the transmit direction, these pins signal to the SONET/SDH framer to generate Path AIS in the transmit direction.

There are four individual ATM/PPP Handler blocks. These process the ATM/PPP data and interface to the Transmit APS Cross Connect (TACC) and Receive APS Cross Connect (RACC) blocks. When processing ATM Cells or PPP data, each ATM/PPP block provides a four-cell deep FIFO for clock separation in each direction. Cell rate decoupling is also performed where idle or unassigned cells can be generated. The header and payload bytes of the idle or unassigned cells in the transmit direction can be programmed via the microprocessor interface. A  $1+X^{43}$  polynomial payload scrambler/descrambler function can be enabled via a global control bit for PPP operation. The scrambler/descrambler is always activated when ATM processing is performed.

When the ATM/PPP Handler blocks are processing PPP data, they perform octet stuffing of flag characters (7E Hex) and control escape characters (7D Hex) in the transmit direction, and in the receive direction all control escape characters are destuffed. These blocks can optionally perform 16-bit or 32-bit FCS generation/calculations as selected via global control bits. Frame delimiting and inter-frame flag fill are provided in the transmit direction. An optional  $1+X^{43}$  polynomial scrambler/descrambler function can be enabled via a global control bit. Also a transparent mode of operation is possible, for applications where the PPP in "HDLC-like framing" processing is performed external to the SONET/SDH framer. Registers for programming maximum and minimum allowable received frame lengths are provided. Received frames that exceed the maximum programmed frame length are always discarded. Received frames that are below the minimum programmed frame length may optionally be discarded.

The ATM/PPP Handlers can work individually or in concert with each other depending upon the type of payload being processed. If four individual STM-1/STS-3c frames are being processed, such as in the case of STM-4/STS-12 or four individual 155 Mb/s streams, then the ATM/PPP blocks work individually. If a STM-4c/STS-12c is being processed, then all four ATM/PPP blocks work in parallel. The ATM/PPP blocks interface to the TACC and RACC (transmit and receive APS Cross Connect) blocks.

APS functions are facilitated via an APS interface and the TACC/RACC blocks. These blocks consist of two 5 x 5 cross-connects and two bidirectional APS interfaces, one for transmit and one for receive. The 5 x 5 cross connects handle the data from the four receive/transmit macros plus the receive/transmit APS interface. If a single SONET/SDH framer is used, 1:1, 1:2, and 1:3 APS is supported. If more than one SONET/SDH framer is used, such as in a multiple STM-1/STS-3c situation, a 1:N (N = 1 - 14) protection scheme can be achieved, provided that the two bidirectional APS interfaces are used. The APS function is not available when the Telecom Bus interface is used, or when concatenated payloads such as AU-4-4c are being processed.

The UTOPIA Level 2+ block interfaces to the four ATM/PPP Handler macros. ATM cells and PPP in "HDLC-like framing" are handled by this block. For ATM cells, the UTOPIA Level 2+ block can provide either two 8-bit transmit/receive UTOPIA Level 1 PHY interfaces, or a 16-bit transmit/receive UTOPIA Level 2 PHY interface. Only cell level handshaking is provided. For UTOPIA Level 2+ MPHY operation, 5-bit address registers allow addresses to be assigned to the four individual ATM/PPP Handler macros. For PPP operation, the UTOPIA Level 2+ interface is used with some additional handshaking signals to provide a 16-bit MPHY interface for passing PPP data in the form of programmable-size chunks. Chunk sizes can be programmed to be either 16, 32, 48, or 64 bytes in length. Indications for aborted frames and FCS errors are also provided. As is the case for ATM operation, 5-bit address registers allow addresses to be assigned to the four individual ATM/PPP Handler macros. The UTOPIA Level 1 interfaces can be operated at frequencies up to 25 MHz, while the UTOPIA Level 2 interface can be operated up to 50 MHz.

## IBM SONET/SDH Framer

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Two loopbacks are supported in the transmit direction and one is supported in the receive direction for ATM/PPP payloads. All of the loopbacks occur at the TCS (Transmission Convergence Sublayer) Function Boundaries of the ATM/PPP Handler. The first transmit loopback is at the ATM Cell Buffer (ACB) interface with the ATM/PPP Handler. As soon as the ACB is not empty, the ACB contents are read and provided to the receive direction. The second transmit loopback is at the output of the ATM/PPP Handler before the SFH. The transmit cell stream at the output of the ATM/PPP Handler is looped back to the receive side of the ATM/PPP Handler. This cell stream can contain idle/unassigned cells. Each of the transmit loopbacks has two modes. With the first mode, just the loopback is performed and data is not forwarded to the next processing step in addition to being looped back. The second loopback mode allows data to be forwarded to the next processing step. The receive loopback causes receive data provided by the SFH to be looped back towards the transmit direction. There are two modes for the receive loopbacks: one for loopback only (i.e., no data is passed to the ATM/PPP Handlers), and one where data is also passed to the ATM/PPP Handler.

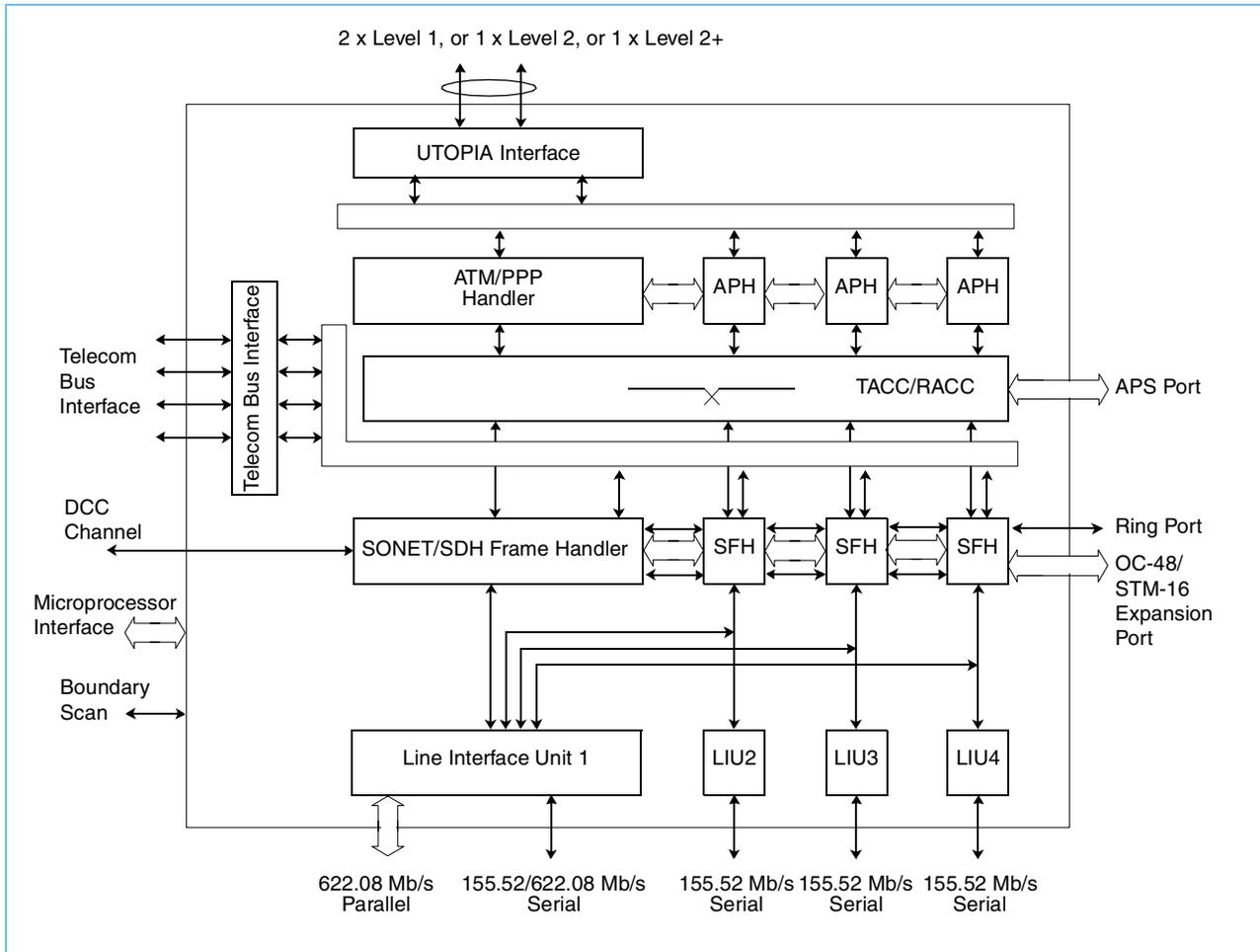
The SONET/SDH framer provides a microprocessor interface that can be selected to be compatible with the Motorola 68360 processor bus type interface (QUICC bus type), or the Intel style bus. The interface can be selected to be either synchronous or asynchronous. The synchronous interface can be run with a maximum clock frequency of 33.3 MHz, while the asynchronous interface can be run with a 50 MHz clock. Polling or interrupt support, and latching of critical events, are provided to accelerate interrupt processing and reduce the burden on the microprocessor. Alarm masks are provided to enable or disable interrupts. Overflow and programmable threshold interrupts are provided on certain counters. An integrated watchdog timer is provided with a programmable period to force microprocessor accesses to terminate when a timeout occurs. Access to the various configuration registers, counters, and the control and status registers is provided via this microprocessor interface.

There are many features included in the SONET/SDH framer that make it well suited for higher-order multiplex applications. The integrated APS Cross Connect Circuit reduces external part counts. In STS-48/STM-16 applications, the SONET/SDH framer can support multiplexing of STM-4, STM-4c, STS-12, or STS-12c frames. Telecom Bus, Dual UTOPIA Level 1 and UTOPIA Level 2 interfaces add a high degree of flexibility for connecting to ATM or PPP terminating/switching equipment or other path terminating equipment. On-chip clock recovery and synthesis for the serial 155 Mb/s or 622 Mb/s interfaces eliminates the need for additional external clock recovery circuitry. The high degree of integration of complex functional blocks into a single device with glueless device-to-device communication for multi-device applications makes possible reduced design and debug time and shorter time to market.

The Boundary Scan Port includes a five-pin TAP (Test Access Port) that conforms to the IEEE 1149.1-1994 standard. This TAP provides external boundary scan to read and write the SONET/SDH framer input and output pins from the TAP for circuit board and component testing.

## Block Diagram and Block Descriptions

### High Level Block Diagram



The previous diagram shows the principal blocks of the SONET/SDH framer. These blocks and other functional units are listed below.

- Four LIU blocks.
- Four SFH blocks, which consist of the sub-blocks SDB (SONET/SDH Data Buffer) and transmit/receive OFP (Overhead Frame Processor). These sub-blocks are not shown in 1:4 Protection with One SONET/SDH Framer: Normal Operation on page 10.
- Four ATM/PPP Handler (APH) blocks, which consist of the sub-blocks: ACB (ATM Cell / PPP Chunk Buffer) and ACH (ATM Cell Handler / PPP Handler), which performs HDLC-like encapsulation. These sub-blocks are not shown in 1:4 Protection with One SONET/SDH Framer: Normal Operation on page 10.
- Transmit/receive APS Cross-Connect (TACC/RACC) block, which is actually a part of the ACH block within the APH. It is shown separately in the block diagram to illustrate its functional relationship to the other blocks.
- UTOPIA interface block, which contains the ACI sub-block.
- Transmit/receive Telecom Bus interface block.
- Transmit/receive DCC Port (included in SFH block).

## IBM SONET/SDH Framer

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- Microprocessor interface.
- Transmit/receive Ring Port (included in SFH block).
- OC-48/STM-16 Expansion Port (included in SFH block).
- Boundary Scan Port.

The SONET/SDH framer can extract ATM/PPP traffic from up to four individual STM-1/STS-3c streams or a single STM-4/4c or STS-12/12c stream and supply them to its receive UTOPIA Level 2 or Level 2+ interface. Conversely, the SONET/SDH framer can accept ATM/PPP traffic on its transmit UTOPIA Level 2 or Level 2+ interface and map the ATM/PPP streams into up to four individual STM-1/STS-3c streams or a single STM-4/4c or STS-12/12c. Other payloads can be handled via the transmit and receive Telecom Bus interfaces.

A high level discussion of the features of the various blocks is given below.

### Line Interface and General Data Flow

The Line interface section of the SONET/SDH framer performs the adaptation between the external SONET/SDH signals and the internal SFH macros.

There are four individual transmit paths that each can handle a single STM-1/STS-3c. Apart from the line interface, the transmit paths are identical and each is composed of the following macros: UTOPIA or Telecom Bus interface, APH, TACC, SFH, and LIU. There are four separate Telecom Bus interfaces, each capable of handling one STM-1/STS-3c stream. Each Telecom Bus has an 8-bit data path with control signals for identifying the VC-4/SPE, and certain overhead bytes.

The macros contained in the four transmit data paths can operate in parallel as one composite macro to support STM-4/4c or STS-12/12c traffic. The four transmit Telecom Bus interfaces can also operate in parallel as one composite Telecom Bus with a 32-bit data path.

The transmit line interface of the SONET/SDH framer consists of four LIUs and a byte-parallel interface. All four LIUs provide clock synthesis for 155.52 Mb/s serial operation with the added feature that LIU #1 can also perform clock synthesis for 622.08 Mb/s serial operation. A byte-parallel interface is provided in LIU #1 for 622.08 Mb/s operation, but no clock synthesis is provided.

Several options are available. If four individual STM-1/STS-3c streams are desired, the four transmit paths act independently and four 155.52 Mb/s streams are provided. If an STM-4/STS-12 signal is desired, the four individual payloads (AU-4/STS-3c SPE) signals are byte-interleaved with TOH (MS and RS) added and scrambled to form a 622.08 Mb/s serial or byte-parallel stream. However, each of the four transmit paths is processing an AU-4/STS-3c SPE. When a STM-4c/STS-12c signal is to be transmitted, the peer macros in the four transmit paths operate together as one large macro. In this case, if the Telecom Bus is used, the four transmit Telecom Bus interfaces act as one large Telecom Bus with a 32-bit wide datapath.

Clock synthesis, as mentioned above, is provided in the transmit direction for the serial interfaces for sourcing data at the serial transmit outputs. One reference clock with selectable frequencies of 19.44 MHz, 38.88 MHz, 77.76 MHz, or 155.52 MHz is used to provide the timebase for all four transmit SONET/SDH streams. However, if the byte-parallel interface is used (for STM-16/OC-48 applications), the external MUX/DEMUX will have to provide a byte clock to the SONET/SDH framer and perform the clock synthesis function. Scrambling is still performed.

The process of extracting data in the receive direction is similar to that in the transmit direction, but the flow is in the opposite direction.

There are four individual receive paths that each can handle a single STM-1/STS-3c. Apart from the line inter-

face, the receive paths are identical and each is composed of the following macros: UTOPIA or Telecom Bus interface, APH, RACC, SFH, and LIU. There are four separate Telecom Bus interfaces each capable of handling one STM-1/STS-3c stream. Each Telecom Bus has an 8-bit data path with control signals for identifying the VC-4/SPE, and certain overhead bytes.

The macros contained in the four receive data paths can operate in parallel as one composite macro to support STM-4/4c or STS-12/12c traffic. The four receive Telecom Bus interfaces can also operate in parallel as one composite Telecom Bus with a 32-bit data path.

The receive Line interface of the SONET/SDH framer consists of four LIUs and a byte-parallel interface. All four LIUs provide clock recovery for 155.52 Mb/s serial operation with the added feature that LIU #1 can also perform clock recovery for 622.08 Mb/s serial operation. A byte-parallel interface is provided in LIU #1 for 622.08 Mb/s operation, but no clock recovery is provided.

The receive Line interface of the SONET/SDH framer provides several options. If four individual STM-1/STS-3c streams are to be processed, the four receive paths act independently and four 155.52 Mb/s streams can be input to the SONET/SDH framer. If an STM-4/STS-12 signal is to be processed, the four individual payloads are byte de-muxed from the applied 622.08 Mb/s serial or byte-parallel stream and are descrambled as appropriate. However, each of the four receive paths is processing a single payload stream. When a STM-4c/STS-12c signal is to be processed, the peer macros in the four receive paths operate together as one large macro. In this case, if the Telecom Bus were being used, the four receive Telecom Bus interfaces would act as one large Telecom Bus with a 32-bit wide datapath.

As mentioned above, clock recovery is provided in the receive direction for the serial interfaces. However, if the byte-parallel interface is used, an external OC-48/STM-16 MUX/DEMUX will have to provide a byte clock to the SONET/SDH framer and perform the clock recovery function. Additionally, byte alignment will need to be performed by the external OC-48/STM-16 MUX/DEMUX.

## **SDB - SONET/SDH Data Buffer**

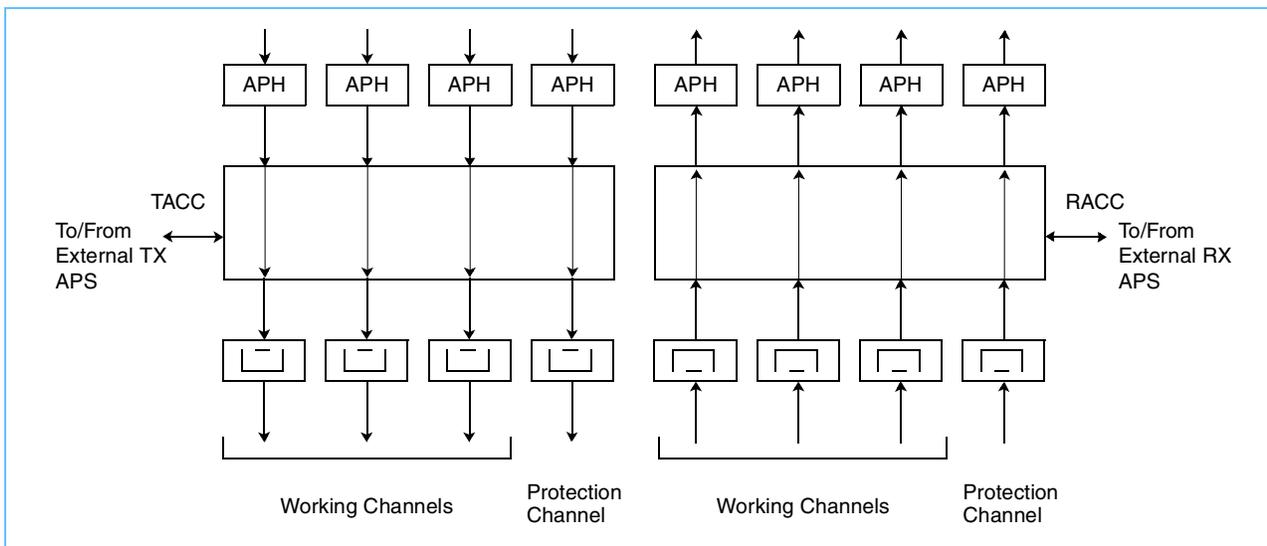
The SDB buffers consist of 63-byte deep FIFOs in the transmit direction and 7-byte deep FIFOs in the receive direction. There is one SDB per SFH macro. The purpose of the SDB is to facilitate the transfer of data between the APH and the SFH blocks, which operate off of different clock islands.

## **RACC and TACC - Receive/Transmit APS Cross Connect**

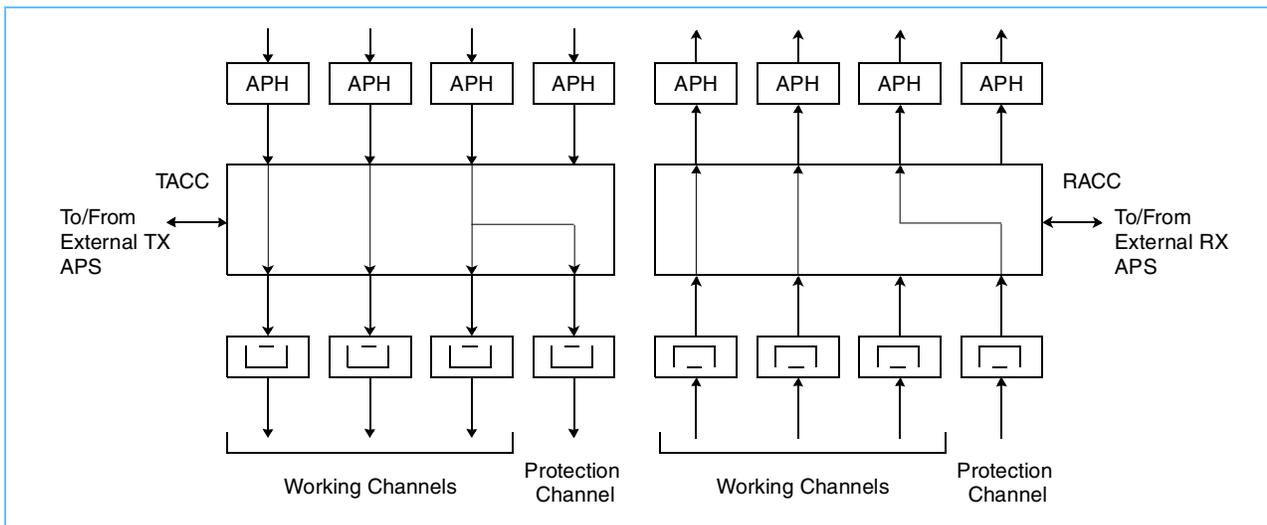
The TACC and RACC blocks consist of two separate 5 x 5 cross connects and two separate byte-wide bidirectional APS interfaces. Switching is supported by the RACC while bridging and switching are supported by the TACC. Command of the switching and bridging is accomplished through two microprocessor-accessible control registers. Upon power-up, each APH macro is bridged to its corresponding SFH. When a switch is performed, the output of the SFH (which is typically a C-4 signal) is switched. In single device operation, there can be three working channels and one protection channel. If a failure occurs on one of the working channels, the TACC is configured to bridge the output of the APH macro for the failing line over to the protection channel's SFH. The RACC is configured to switch the output of the SFH of the protection channel over to the APH of the working channel. This operation is shown in the two figures on page 10.

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**1:4 Protection with One SONET/SDH Framer: Normal Operation**



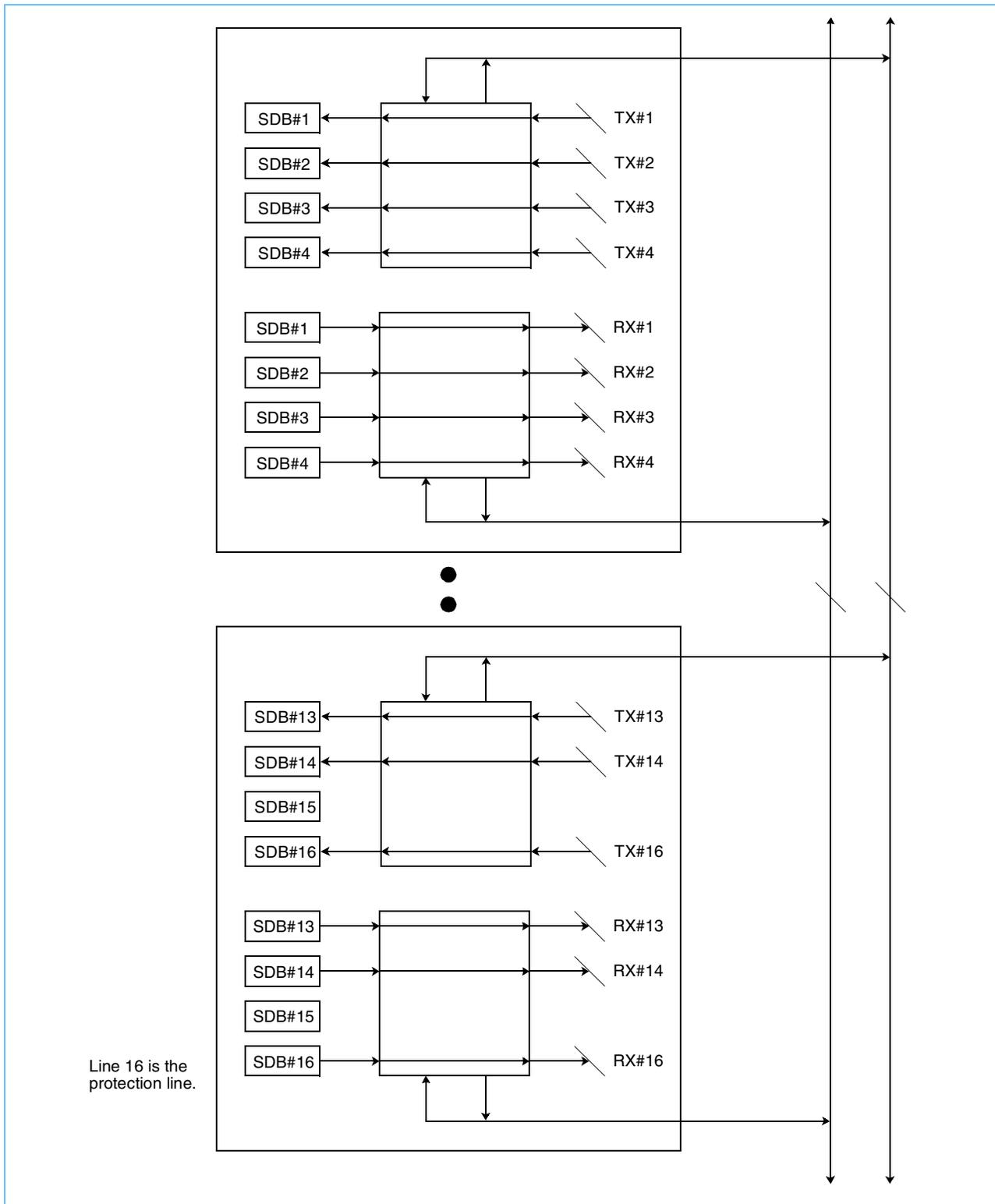
**1:4 Protection with One SONET/SDH Framer: Switch and Bridge to Protection Channel**



As shown in the previous figures, the External Transmit and Receive APS interfaces do not need to be used for the 1:4 protection scheme. However, if multiple SONET/SDH framers are used, then the External Transmit APS interfaces of the SONET/SDH framers can be connected together and, similarly, the External Receive APS interfaces of the SONET/SDH framers can be connected together. In this way a 1:N protection scheme can be achieved. N can range from 1-14 depending on the number of SONET/SDH framers used. The next two figures show a 1:N APS scheme when there is no failure and when there is a failure.

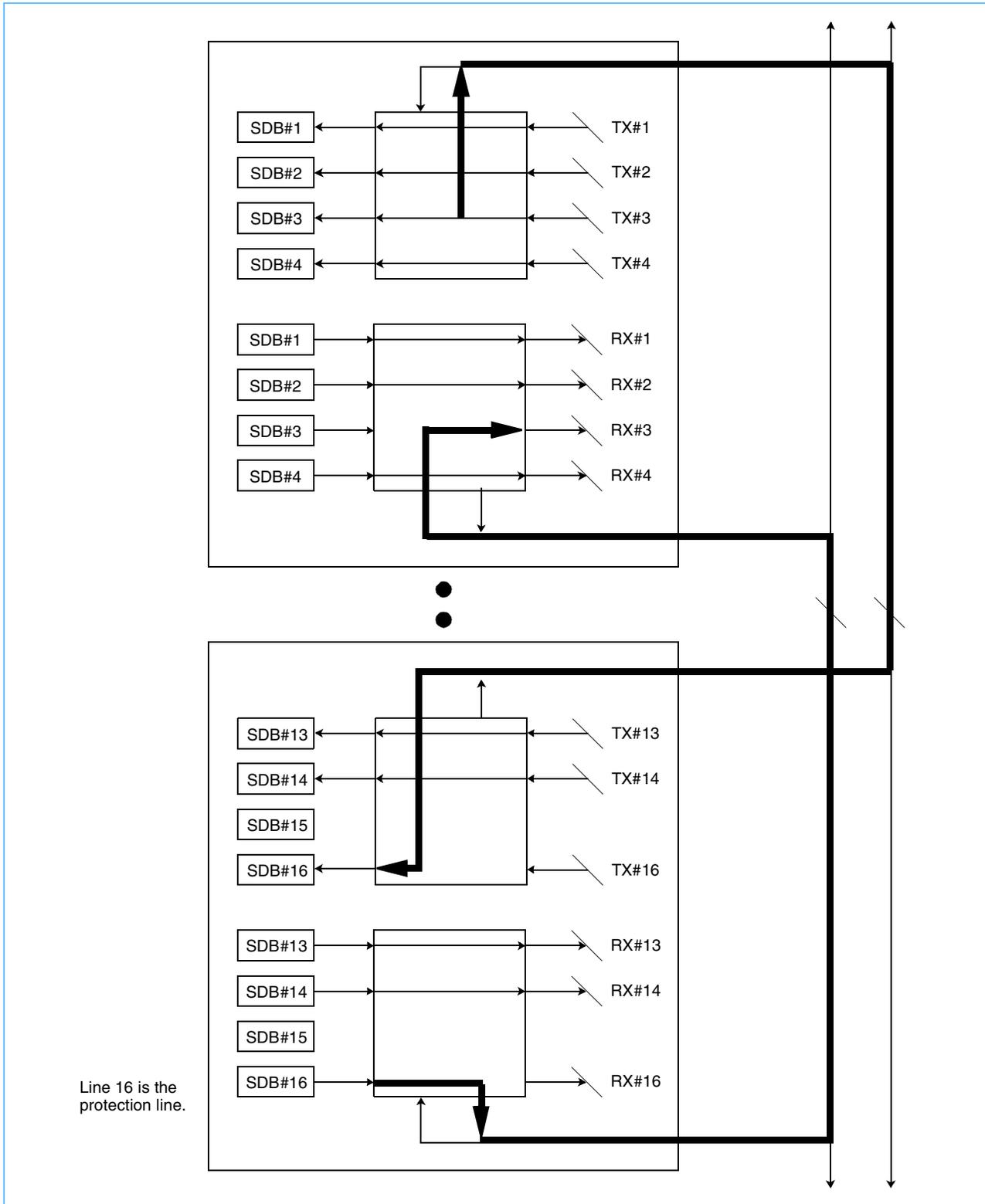
The APS functionality is not active when STM-4c or STS-12C payloads are being processed or when the Telecom Bus interface is being used. Only when ATM and PPP data in 4 x STM-1/STS-3c are processed can the TACC and RACC be used, since the external APS port can handle data from only one STM-1/STS-3c stream at a time. However, the TACC/RACC are still operational in STM-4 and STS-12 modes, but only one C-4 can be switched/bridged.

1:N APS Scheme - No Failure, Protection Line Inactive

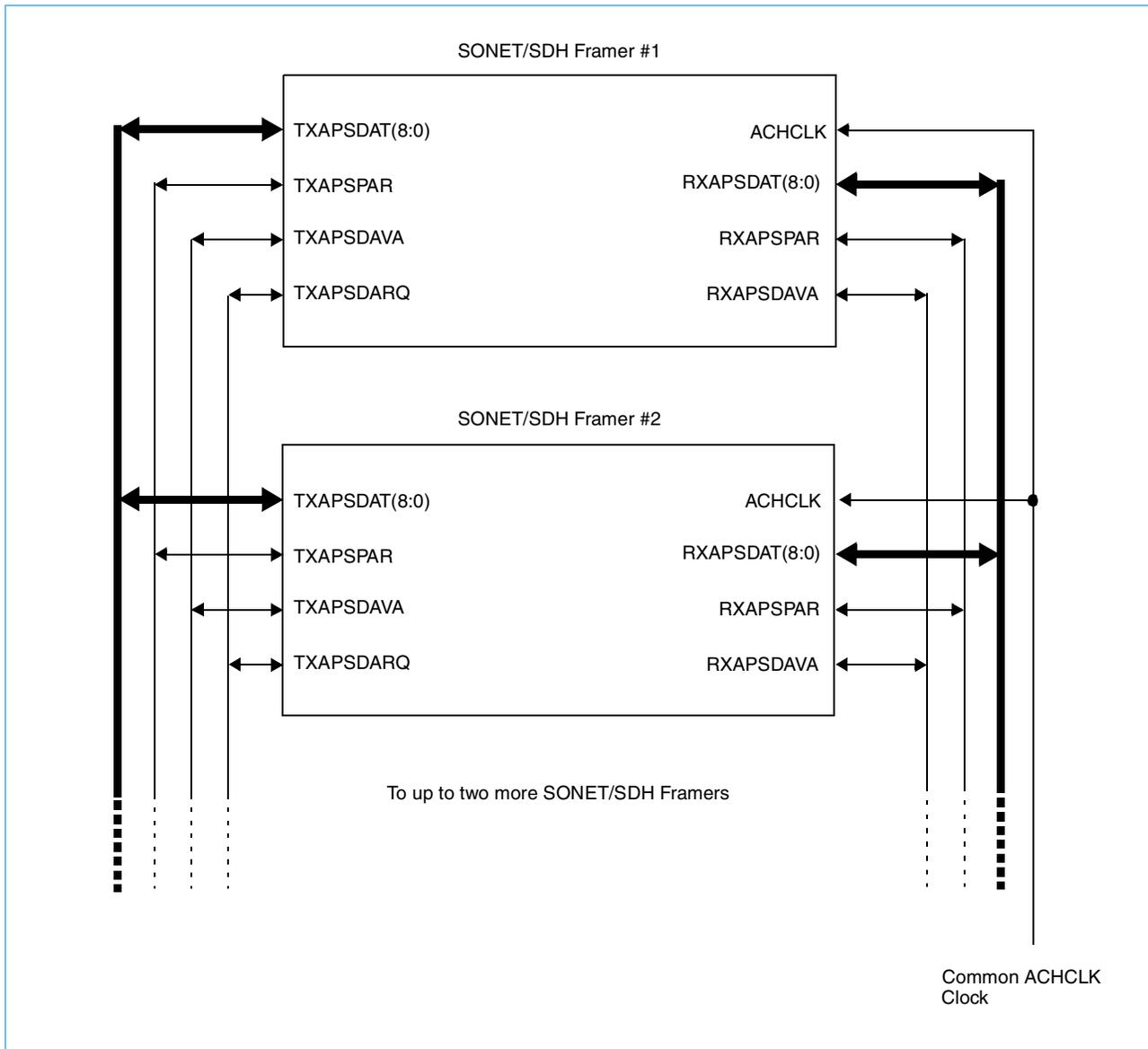


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1:N APS Scheme - Failure, Protection Line Active



### APS Interface Connection for Multi-Device Operation



The previous figure shows how the APS interfaces between SONET/SDH framers should be connected. It should be noted that a common ACHCLK clock is required for all SONET/SDH framers. The skew between the ACHCLK clocks should be taken into consideration to ensure set-up and hold times are met at the interfaces that are inputs. In multi-device operation where the SONET/SDH framers have different transmit reference clocks, pointer processing will need to be turned on and pointer adjustments in the transmit direction will occur. Pointer processing does not need to be enabled if all of the SONET/SDH framers have the same transmit reference clock.

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### APH - ATM/PPP Handler

The ATM/PPP Handler is designed to process either four individual 155.52 Mb/s ATM or PPP streams (i.e., STM-4/STS-12 or 4 x STM-1/STS-3c) or one single 622.08 Mb/s ATM or PPP stream (i.e., STM-4c/STS-12c). It should be noted that an STM-4/STS-12 looks like four individual STM-1/STS-3c streams to the APH macros.

When processing PPP Frame payloads, this macro performs the functions indicated in RFC1619 and RFC1662 for octet synchronous mapping of PPP into HDLC-Like Framing for transmission over SONET/SDH. In addition to those functions, the APH block formats the PPP Frame payloads for insertion into the ACB as well as accepting PPP Frame payloads from the ACB. An optional self-synchronous scrambler/descrambler with polynomial  $1+X^{43}$  is provided for scrambling the HDLC-Like frame stream. PPP Frame data which is leaving the APH in the transmit direction or entering the APH in the receive direction can be scrambled/descrambled under software control.

The APH macro can also perform the TCS Functionality for ATM Cell payloads such as HEC generation/verification, cell scrambling/descrambling, as well as HEC-based Cell Delineation.

### ACB - ATM Cell Buffer

The ACB is a FIFO, four ATM cells deep, that is between the UTOPIA interface and the APH macros. This buffer is used to accrue/accept complete cells/chunks in ATM/PPP processing mode. This is because the SONET/SDH framer is a PHY layer device and only does cell/chunk level handshaking for ATM/PPP applications. When an STM-4c or STS-12c is processed, the ACB macros work in parallel to create one large FIFO in the transmit direction and one large FIFO in the receive direction.

### UTOPIA Interface

Some additional but brief comments on the interface are provided for ATM and PPP mode operation. The “+” in UTOPIA LEVEL 2+ indicates that the SONET/SDH framer uses the UTOPIA interface with some added signals and modifications for transferring PPP data between the SONET/SDH framer and a PPP processing device, which will be called the “ATM Emulation Layer”.

It should be noted that, since the SONET/SDH framer is a PHY layer device, no switching is performed. There exists the option of having two 8-bit UTOPIA level 1 interfaces. These interfaces are compliant with [UL1]. When they are used, only two STM-1/STS-3c streams can be terminated. These streams can either be individual 155.52 Mb/s streams or they can be contained in an STM-4/STS-12. If the need exists for processing more than two AU-4/STS-3c SPE or an STM-4c/STS-12c stream, then the UTOPIA level 2 interface option should be selected. The UTOPIA level 2 interface is compliant with [UL2v1]. When the UTOPIA level 2 interface is selected, up to four STM-1/STS-3c streams can be processed in a single SONET/SDH framer. Each of the four sets of transmit and receive APH macros are considered to be a PHY. There are 8 registers in the SONET/SDH framer (1 for each transmit and receive APH macro) that are used to define a unique 5-bit address to each of the PHYs. When processing an STM-4c/STS-12c stream, the UTOPIA Level 2 interface is also used. In this case, all of the transmit macros operate in parallel and all of the receive macros operate in parallel to form two large macros, or PHYs, capable of processing the STM-4c/STS-12c payloads. Furthermore, the transmit and receive address pins of the UTOPIA Level 2 interface should be strapped low to support the single large PHY.

When the SONET/SDH framer is configured to process PPP payloads, the UTOPIA Level 2+ features are called into play. The UTOPIA Level 2+ interface is a Multi-PHY (MPHY) interface with the following signals that are shared with their UTOPIA counterparts:

- TXUCLK1 - transmit clock input.
- TXUADDR(4:0) - 5-bit transmit MPHY address input.
- TXCLAV(0) - transmit chunk available output signal. There are three other CLAV signals for multi-PHY ATM applications.
- TXSOC - transmit start of chunk input signal.
- TXUDATA(15:0) - transmit data input.
- $\overline{\text{TXENB}}$  - transmit enable input. This signal is active low.
- TXPRTY - transmit parity input.
- RXUCLK1 - receive clock input.
- RXUADD(4:0) - 5-bit receive MPHY address input.
- RXCLAV(0) - receive chunk available output signal. There are three other CLAV signals for multi-PHY ATM applications.
- RXSOC - receive start of chunk input signal.
- RXUDATA(15:0) - receive data output.
- $\overline{\text{RXENB}}$  - receive enable input. This signal is active low.
- RXPRTY - receive parity output.

A number of additional signals are provided for frame delineation purposes:

- TXEOF1 - transmit End-of- Frame input.
- TXSOFI - transmit Start-of-Frame input.
- TXABTO - transmit abort output.
- TXMSI - transmit most significant byte input.
- RXEOF0 - receive End-of- Frame output.
- RXSOFO - receive Start-of-Frame output.
- RXABTO - receive abort output.
- RXMSO - receive most significant byte output.
- RXFCSEO - receive FCS error output. (Both abort and FCS indications can optionally be provided as outputs on this pin.)

Only multi-PHY handshaking is supported when processing PPP Payloads. The UTOPIA Level 2+ behaves the same whether STM-4/STM-1/STS-12/STS-3c streams are being processed or STM-4c/STS-12c streams are being processed. The receive and transmit macros operate in parallel as one large PHY to process the STM-4c/STS-12c streams. As is the case for ATM when STM-4c/STS-12c streams are being processed, the external transmit and receive address pins should be set to low.

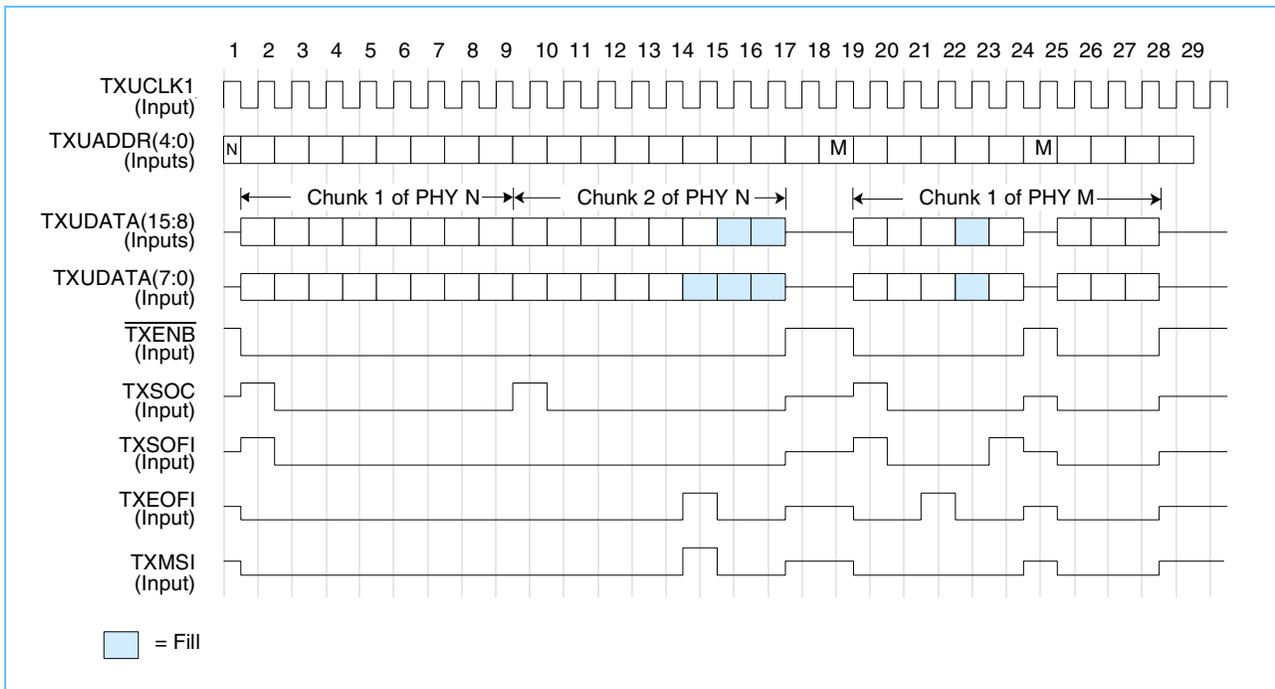
Operation of the UTOPIA Level 2+ interface is very similar to that of multi-PHY UTOPIA. Polling and selection of PHYs are performed in exactly the same way as described in [UL2v1]. Chunks of frame data are passed across the data buses. The chunk is analogous to the ATM cell. The TXSOC and RXSOC signals are analogous to the start-of-cell signal. TX/RXCLAV(0) is analogous to the cell available signal. TXPRTY and RXPRTY are the parity signals. Since PPP frames are of variable size they may or may not fit into a single chunk transfer. The additional signals as listed above help to facilitate frame delineation.

The format of the data on TXUDATA(0-15) depends on the setting of control bits. If the SONET/SDH framer is set to calculate and insert 16-bit or 32-bit FCS, TXUDATA(15:0) contains only raw frame data and intra-chunk fill. The SONET/SDH framer will calculate the FCS and append it to the frame data, insert frame delimiting flags, and stuff the control escape and flag characters between the frame delimiting flags on a frame by frame basis. These operations are described in sections 3.1 and 4.2 of [RFC1662]. Inter-frame flags are inserted as needed. The data can then be optionally scrambled before it is inserted into the SONET/SDH frame. The SONET/SDH framer can be programmed to have a minimum of either 1 or 2 flags in between frames. If trans-

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parent mode is selected, the SONET/SDH framer will take the TXUDATA(15:0) data and insert each entire chunk into the transmit SONET/SDH frame without modification or the data can be optionally scrambled. The TXSOFI, TXEOFI and TXMSI pins are not used when the SONET/SDH framer is in transparent mode and should be tied low. If the SONET/SDH framer is set to not perform any FCS processing it will just take the TXUDATA(15:0) chunk data and insert frame delimiting flags around the frames and stuff the control escape and flag characters between the frame delimiting flags per [RFC1662]. As in the other cases, the data can optionally be scrambled. When FCS processing is disabled, it is expected that the TXUDATA(15:0) will contain the appropriate FCS.

**Transmit UTOPIA Level 2+ Interface Operation for Non-Transparent Mode (16-Byte Chunks)**



The previous figure shows the transfer of frames across the transmit UTOPIA Level 2+ interface. The TXABTO, TXCLAV(0), and TXPRTY signals are omitted to avoid clutter. The polling and selection of PHYs is identical to that in the ATM mode operation, which is also described in [UL2v1]. The TXUADDR(4:0), TXENB, TXCLAV(0), TXSOC and TXPRTY signals therefore behave the same as their ATM counterparts, with the exception that TXCLAV(0) indicates that the SONET/SDH framer can accept at least a complete chunk of data. As stated earlier, a chunk is analogous to a cell. Chunk size is programmable to be either 16, 32, 48, or 64 bytes. Transmit UTOPIA Level 2+ Interface Operation for Non-Transparent Mode (16-Byte Chunks) on page 16 shows the transfer of a 27-byte block of frame data using two back-to-back chunks over PHY N, a 6-byte block of frame data over PHY M, and the start of another block of frame data also over PHY M. The chunk size shown is 16 bytes. PHY N is selected on clock edge 1. TXENB is used to indicate valid data and control signals at the interface. On clock edge 2, TXSOC is sampled as a '1', thus indicating the start of a chunk. Also, on clock edge 2, TXSOFI is sampled high, which indicates the start of a new block of frame data. The block of frame data for PHY N is transferred from clock edge 2 to clock edge 15. The end of this block of frame data is indicated by the TXEOFI signal asserted high. The TXMSI signal is asserted with the TXEOFI signal to indicate that the last byte of the frame is in the Most Significant Byte (MSB) position of that word. The Least Significant Byte (LSB) of that word contains fill. Since there is no more frame data to transfer across PHY N, 2 fill words are added to round out Chunk 2 of PHY N. Fill is data that is used to fill up empty locations in the data stream not occupied by frame data. This fill is either discarded or converted into inter-frame flags (7E H) by the SONET/SDH framer. Another block of frame data is transferred across PHY M on

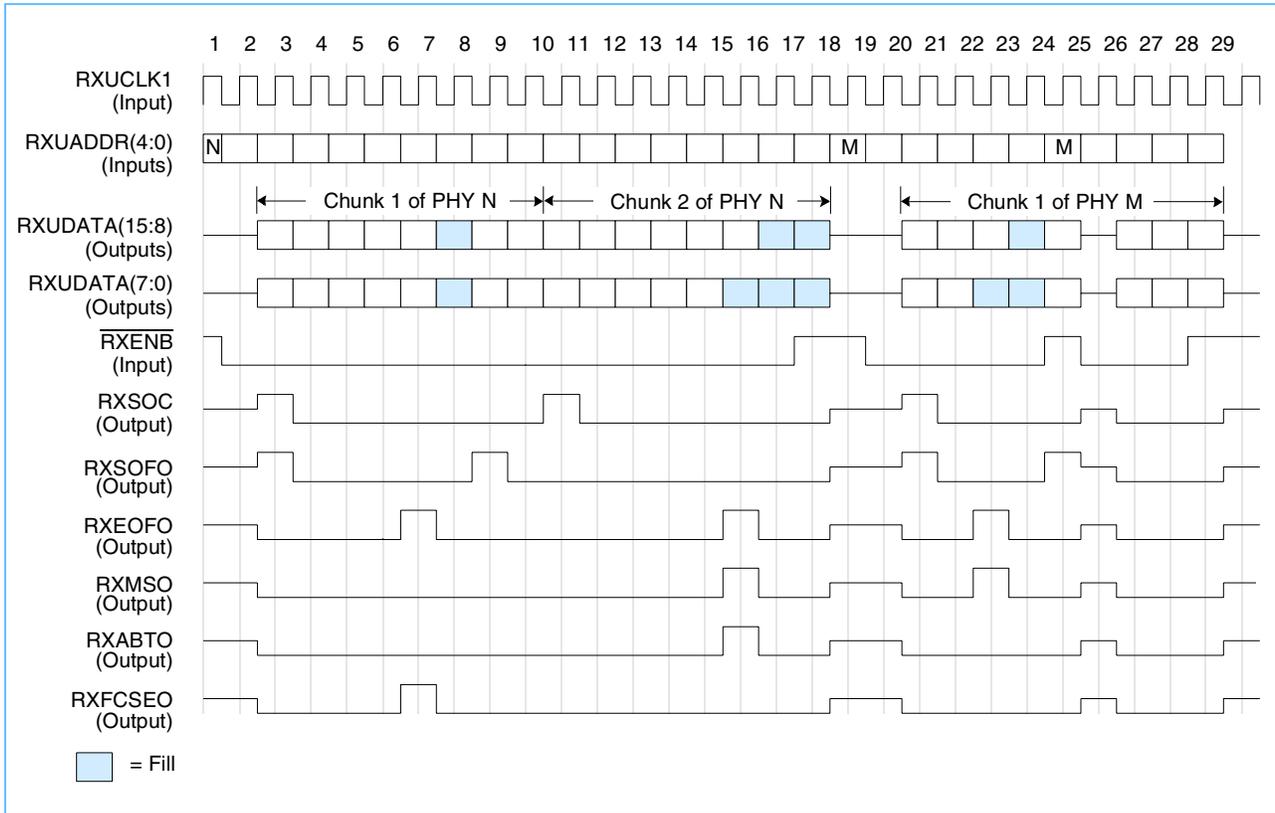
clock edges 20-22. The TXMSI signal is sampled low on clock edge 22, while TXEOF1 is sampled high. This means that the last byte of the block of frame data is in the LSB of that word. A word of fill is present in clock edge 23. There can be any number of fill words between frames in a chunk. However, a frame must always start on the MSB of a word. Furthermore, if a block of frame data ended in a chunk being transferred across PHY X, and that chunk ended before another block of frame data started, then the start of the next block of frame data across PHY X must start in the first word of the next chunk transferred across PHY X. A new block of frame data begins transfer across PHY M on clock edge 24.

**Note:** The TXABTO pin indicates when a transmit FIFO has underflowed during the middle of the transfer of the “HDLC-like” frame. In MPHY mode, if a transmit ACB FIFO underflow occurs in a PHY, say PHY N, while PHY M is being accessed, the TXABTO indication for PHY N will not be output until PHY N is selected. When an abort condition occurs, a 7D7E H sequence is inserted at the point in the broken frame where the FIFO underflow occurred. The rest of the frame data after the FIFO underflow occurred is ignored. If a transmit FIFO underflow occurs when a frame is not being transferred, then flags (7E H) are inserted into the data stream until a new frame is transmitted.

The format of the data on RXUDATA(15:0), and the control signals used, vary with the mode as selected by control bits. In transparent mode, the data in the SONET/SDH payload is extracted and optionally descrambled and output on the RXUDATA(15:0) bus. In transparent mode, only chunks are passed across the interface; FCS processing and frame delineation are not performed. Therefore, the RXSOFO, RXEFOF, RXMSO, and RXFCSEO pins are not used for frame delineation purposes. However, the RXABTO, RXMSO, RXSOFO, and RXEFOF signals are used in conjunction with each other to indicate receive ACB FIFO overflow, illegal sequence detection, and for signaling recovery from reset. They also indicate when the PPP block is initially enabled. RXCLAV(0) functions normally as a chunk available / valid data and controls indication. If no FCS processing is selected (as opposed to transparent mode), the destuffed frame data is output on the data bus minus the frame delimiting and inter-frame flags. It should be noted that, if an FCS is present in the frame, it is also output on the data bus. The control signals function normally with the exception that the RXFCSEO signal is not operational. If 16-bit or 32-bit FCS processing is selected, the destuffed frame data is output on the data bus minus the frame delimiting and inter-frame flags. The FCS is not discarded and is output on the data bus. RXSOFO and RXEFOF are used to indicate the start and end of a frame, respectively. RXMSO is asserted with RXEFOF to indicate that the end of the frame is in the MSB of the current word.

IBM SONET/SDH Framer

Receive UTOPIA Level 2+ Interface Operation for Non-Transparent Mode (16-Byte Chunks)



The previous figure shows the transfer of frames across the receive UTOPIA Level 2+ interface. The RXCLAV(0), and RXPRTY signals are omitted to avoid clutter. The polling and selection of PHYs is identical to that in the ATM mode operation which is also described in [UL2v1]. Therefore, RXUADDR(4:0),  $\overline{RXENB}$ , RXCLAV(0), RXSOC and RXPRTY behave in the same way as their ATM counterparts, but with the exception that RXCLAV(0) indicates that the SONET/SDH framer has at least a complete chunk of data to transfer. As stated earlier, a chunk is analogous to a cell. Chunk size is programmable to be either 16, 32, 48, or 64 bytes. The figure shows the transfer of two blocks of frame data as back to back chunks across PHY N and one complete block and a partial block of frame data across PHY M. The chunk size in this case is 16 bytes. The first block of frame data transferred across PHY N on clock edges 3-7 had an FCS error, which is flagged at the end of the frame data by the RXEFOFO and RXFCSEO signals being asserted. The second block of frame data being transferred across PHY N starts in chunk 1 of PHY N but is aborted in chunk 2 of PHY N. All aborts are signaled by the simultaneous assertion of the RXEFOFO, RXMSO, and RXABTO signals (if the FCSABT control bit is 0) or the simultaneous assertion of the RXEFOFO, RXMSO, and RXFCSEO signals (if the FCSABT control bit is 1). The abort could have occurred due to any of the conditions listed below:

1. Receive FIFO overflow.
2. An illegal sequence (7D7E H) was detected in the data stream.
3. A frame was received that was below the minimum frame length as defined by the MINFL(6:0) bits when DMINF is set to '1'.
4. A frame was received that equaled or exceeded the maximum frame length defined by the MAXFL(15:0) bits.

**Note:** When FCSABT is set to '0', the RXABTO pin indicates detection of one of the abort conditions listed previously. In MPHY mode, if an abort condition is detected in a PHY, say PHY N, while PHY M is being accessed, the RXABTO indication for PHY N will not be output until PHY N is selected. When an abort condition occurs, the rest of the received frame is ignored and used to fill up the chunk until the end of the chunk is reached or until a new frame is received. When FCSABT is set to '1', the RXABTO pin is forced low and the RXFCSEO pin is used to indicate both FCS errors and aborts. The abort signalling described above is the same except that the abort is signalled on the RXFCSEO pin.

Another block of frame data is transferred across PHY M on clock edges 21-23. The RXMSO signal is asserted with the RXEFO coincident with clock edge 23 to indicate that the last byte of the block of frame data is in the LSB of that word. A word of fill is present in clock edge 24. There can be any number of fill words between frames in a chunk. Since the SONET/SDH framer only transfers complete chunks, fill is added to a chunk after the end of a frame to fill out the chunk in lieu of frame data as shown in Receive UTOPIA Level 2+ Interface Operation for Non-Transparent Mode (16-Byte Chunks) on page 18. That is, after the end of a frame, fill is inserted into the chunk until either new frame data is received or until the end of the chunk occurs. A chunk will never start with fill. If a block of frame data ended in a chunk that was being transferred across PHY X, and that chunk ended before another block of frame data started, then the start of the next block of frame data across PHY X will start in the first word of the next chunk transferred across PHY X.

If an abort occurs, the rest of the aborted frame data will be used as fill. This fill will only be used to fill the current chunk until a new frame is received. If the end of the chunk occurs before a new frame is received, the rest of the data will be discarded and the next chunk transferred across that PHY will contain the next received frame. A frame always starts on the MSB of a word.

## Telecom Bus Interface

The SONET/SDH framer contains four full duplex Telecom Bus interfaces, numbered 1 through 4, one Telecom Bus for each STM-1/STS-3c in 4 x STM-1/STS-3c mode, or one Telecom Bus for each AU-4 that may be contained in an STM-4/STS-12 signal. When STM-4c or STS-12c payloads are processed, the four Telecom Bus interfaces act in unison as a 32-bit wide Telecom interface.

**Note:** POH processing is not performed when the SONET/SDH framer is operating in Telecom Bus mode. All POH in the transmit direction are derived from what is input at the transmit Telecom Bus inputs. All POH at the receive Telecom Bus interface are derived directly from the line.

In the transmit direction, the Telecom Bus interface supports either the AU-4 or VC-4 formats on a per Telecom Bus basis. When the AU-4 format is selected, the device driving the transmit Telecom Bus must supply the H1 and H2 pointer bytes. The SONET/SDH framer will use all of the H1 and H2 pointer bytes supplied to it and pass them on to the transmit line. It should be noted that there are 6 bytes (3 H1 and 3 H2) that must be supplied. When the VC-4 format is selected, the SONET/SDH framer performs pointer retiming where it calculates and inserts a pointer value into the outgoing SDH Frame. In the receive direction, the entire received payload is passed, unmodified, to the receive Telecom Bus. Therefore, in 4 x STM-1/STS-3c mode, each STM-1/STS-3c frame is passed to its corresponding Telecom Bus interface. In STM-4/STS-12 mode, all of the data from column 1 in the received frame is passed to receive Telecom Bus #1, all of the data from column 2 in the received frame is passed to receive Telecom Bus #2, etc. In STM-4c/STS-12c mode the same principle of operation applies as in the case of the STM-4/STS-12 mode, except that the RXTB#SPE, C1J1, and FAIL outputs have identical signals on them, where # = 1, 2, 3, 4.

The SONET/SDH framer's Telecom Bus interface supports the following features:

- Option to enable/disable parity checking.
- Option to select if parity is calculated/checked over data only or data and SPE and C1J1 and FAIL signals.

## IBM SONET/SDH Framer

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- Option to select if odd or even parity is used.
- An 8-kHz transmit frame pulse and complementary transmit reference clock outputs are provided to synchronize transmit data into the SONET/SDH framer. These pulses are also available when the UTOPIA or UTOPIA Level 2+ interfaces are used.
- Retiming option can be activated on any transmit Telecom Bus (1-4) on a per Telecom Bus basis.
- Supports connections to mapper devices for TDM applications.

### Transmit Telecom Bus

There are four transmit Telecom Bus interfaces, numbered 1 - 4, allowing the back-to-back connection of SONET/SDH framers (if retiming is turned on), or connections to mapper devices.

Each transmit Telecom Bus interface of the SONET/SDH framer consists of the following inputs: 8-bit data bus (TXTB#DATA(7:0)), clock (TXTB#CLK), SPE indication (TXTB#SPE), C1J1 indication (TXTB#C1J1), parity (TXTB#PAR), and a failure indication (TXTB#FAIL). The SONET/SDH framer also provides a common set of reference timebase signals for synchronizing the data input to each of the Telecom Bus ports for the cases where transmit retiming is not enabled. This reference timebase interface consists of the following outputs: a Transmit Reference Clock and its complement (TXCCLK and  $\overline{\text{TXCCLK}}$ ) and a Transmit Reference Frame Pulse (TXCFRM).

All of the Telecom Bus ports operate at 19.44 MHz. Furthermore, the option to support either a VC-4 (Transmit Retiming On) or AU-4 (Transmit Retiming Off) format is provided via the GContTx#(1:0) (#=1-4) control bits in the GContTx register. Retiming of the transmit Telecom Bus signal is performed when the VC-4 signal format is selected. Retiming is the process of calculating the pointer value based on the phase difference of the input VC-4 and the output frame. That is, pointer adjustments are allowed to occur to compensate for the phase changes between the input VC-4 signal and the phase of the transmit SONET/SDH frame that may occur due to clock offsets.

Transmit retiming is enabled on a per Telecom Bus basis by setting the corresponding GContTx#(1:0) bits to VC-4 mode. When transmit retiming is enabled on a particular Telecom Bus, its transmit signals (clock, data, SPE, etc.) only need to be synchronous to its TXTB#CLK and not to the TXCCLK signal. The J1 and C1 pulses in the TXTB#C1J1 signal are mandatory for the Telecom Bus channels where transmit retiming is enabled. The SONET/SDH framer will calculate a pointer and insert it into the outgoing SDH stream. The SONET/SDH framer will cause pointer adjustments to occur to compensate for the difference in the frequencies between the TXTB#CLK and TXCCLK clocks. Furthermore, the SONET/SDH framer can accept pointer adjustments on its transmit Telecom Bus input and still perform retiming in an error-free fashion.

When transmit retiming is disabled, the transmit Telecom Bus device that is providing data to the SONET/SDH framer must supply an AU-4, that is a VC-4 with valid payload pointer bytes including concatenation indication bytes as applicable.

When the SONET/SDH framer is processing an STM-4c/STS-12c signal, all four Telecom Bus ports operate in parallel as one 32-bit wide Telecom Bus. All input signals must be driven (i.e., all clock, all SPE, all C1J1, etc.). In this case the transmit Telecom Bus data needs to be double word aligned. The receive Telecom Bus data is provided double word aligned.

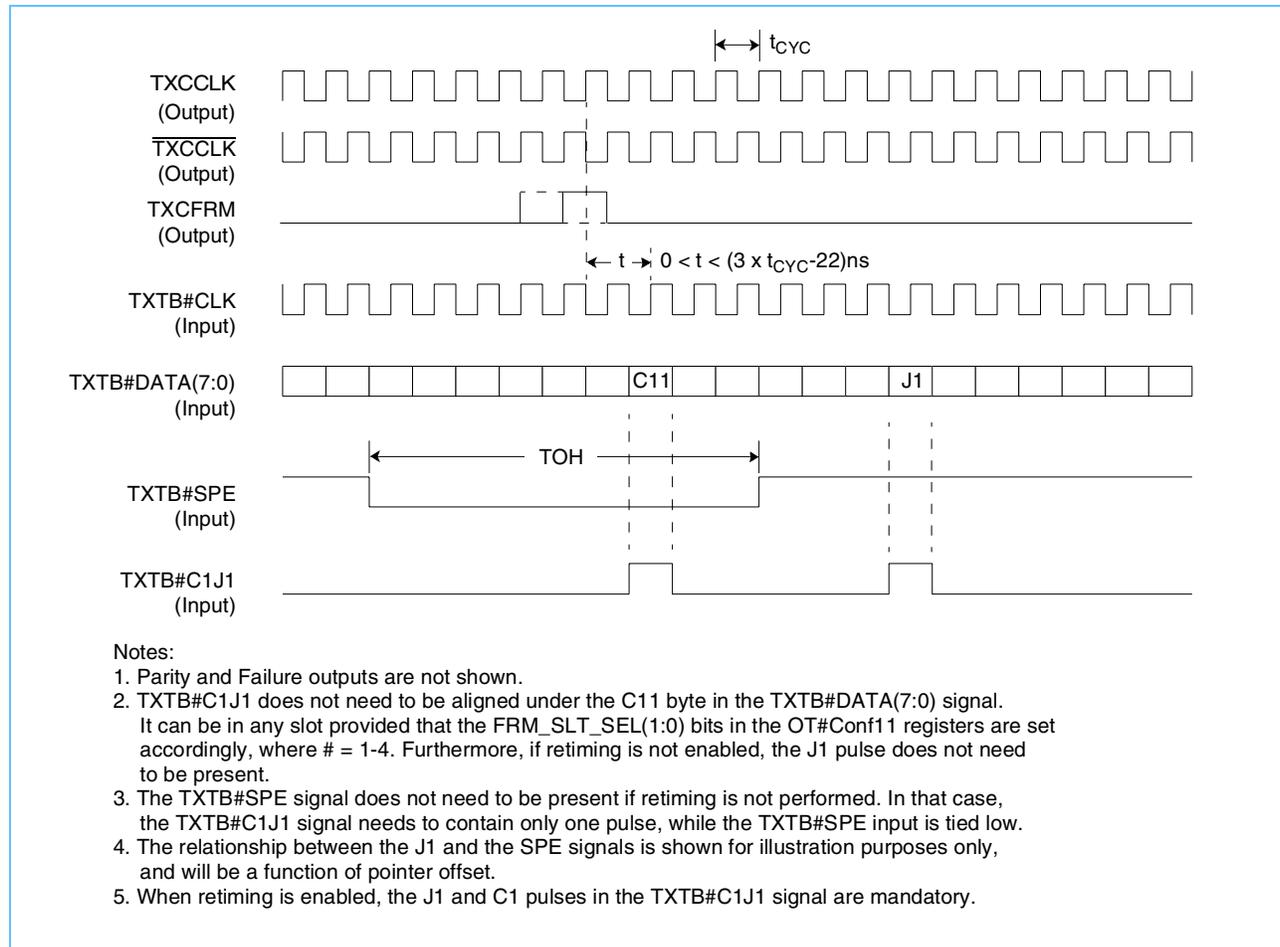
The Telecom Bus interface signals, TXCCLK and  $\overline{\text{TXCCLK}}$ , are provided as a reference clock for devices to put data out onto the Telecom Bus ports of the SONET/SDH framer. These signals have a frequency of 19.44 MHz. If transmit retiming is not selected via the GContTx#(1:0) control bits, one of these clocks must be used to source the data to be transmitted on the appropriate Telecom Bus.

An 8-kHz pulse (TXCFRM) is output on the falling edge of TXCCLK once every frame period and is one TXC-

CLK clock cycle wide. It is used to synchronize the data arriving at the TXTB#DATA(7:0) inputs of the SONET/SDH framer if transmit retiming is not performed. Functional Relationship of the Transmit Telecom Bus Signals shows the relationship between the Input Telecom Bus Data and the TXCFRM signal. The EFRM control bit enables the TXCFRM pulse to come out one cycle earlier to allow more time for the device(s) transmitting on the Telecom Bus to supply the C11 byte (the old numbering scheme is used throughout; this is the J0 byte in the new numbering scheme).

### Functional Relationship of the Transmit Telecom Bus Signals

Transmit retiming is not performed. Subframe 1 is shown.



The transmit Telecom Bus clock input (TXTB#CLK where # = 1-4) is used to clock the transmit Telecom Bus input signals into the SONET/SDH framer. It must be frequency synchronous with the TXCCLK clock if transmit retiming is not performed. Also, no phase relationship is required between TXCCLK and the TXTB#CLK clocks. It should be noted that when an STM-4c/STS-12c payload is being processed, so that the four transmit Telecom Bus interfaces act as a single 32-bit wide interface, all four TXTB#CLK inputs must all be identical.

Each Telecom Bus port has an 8-bit wide data bus that accepts byte-aligned data from the transmitting Telecom Bus device. The data on this bus must have proper alignment with respect to the transmit reference frame pulse TXCFRM if transmit retiming is not performed. Functional Relationship of the Transmit Telecom Bus Signals on page 21 shows the required alignment when transmit retiming is not performed. Note that the TXTB#CLK signal must be frequency synchronous with TXCCLK if transmit retiming is not performed. How-

## IBM SONET/SDH Framer

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ever, any phase relationship may exist between TXCCLK and TXTB#CLK, as long as the C11 byte is clocked into the SONET/SDH framer by the TXTB#CLK signal no later than  $3 \times 51.44 - 22$  ns after the occurrence of the rising edge of TXCCLK that is coincident with TXCFRM being high as shown by the parameter in Functional Relationship of the Transmit Telecom Bus Signals on page 21.

Control bit EFRM allows the TXCFRM pulse to come out one cycle earlier as indicated by the dashed line in Functional Relationship of the Transmit Telecom Bus Signals on page 21. This will allow an extra clock cycle for a device on the Telecom Bus to put out its C11 byte if need be. It is extremely important to note that the C11 byte must be clocked into the SONET/SDH framer within the window defined by Functional Relationship of the Transmit Telecom Bus Signals on page 21 regardless of whether or not the TXCFRM pulse comes out one cycle earlier (i.e., the window is always measured with respect to the normal position of TXCFRM when the EFRM control bit is set to '0').

The TXTB#DATA(7:0) stream must contain valid Pointer Bytes (including concatenation indication) when the SONET/SDH framer is not performing transmit retiming. All other TOH bytes are overwritten by the SONET/SDH framer. The device transmitting on the Telecom Bus must also supply the POH regardless of whether retiming is enabled or not. The SONET/SDH framer will not perform any transmit POH processing while in the Telecom Bus mode of operation. Even if ring port operation is enabled while in Telecom Bus mode, the SONET/SDH framer will ignore POH information from the mating SONET/SDH framer.

It should be noted that when an STM-4c/STS-12c payload is being processed, so that the four transmit Telecom Bus interfaces act as a single 32-bit wide interface, the TXTB1DATA(7:0) contains the MSB of the 32-bit double word of data, i.e., TXTB1DATA(7) is the first bit transmitted while TXTB4DATA(0) is the last bit transmitted.

While transmit retiming is disabled, and the TXTB#SPE input is low, the corresponding C1 pulse in the TXTB#C1J1 signal is used as a slot identifier rather than a C1 byte identifier. A set of control bits FRM\_SLT\_SEL(1:0) in the OT#Conf11 registers are used to tell the SONET/SDH framer which slot the C1 pulse is located in. Functional Relationship of the Transmit Telecom Bus Signals on page 21 shows an example. When transmit retiming is enabled, the pulses on the TXTB#C1J1 signal pin must be both present and coincident with the C11 and J1 bytes in the TXTB#DATA(7:0) signal. It should be noted that when an STM-4c/STS-12c payload is being processed, so that the four transmit Telecom Bus interfaces act as a single 32-bit wide interface, all four TXTB#C1J1 inputs must be identical.

The transmit Telecom Bus SPE input (TXTB#SPE, #=1-4) should be low during TOH time slots and should be high during SPE time slots in each subframe. This includes cases where pointer adjustments are performed and the VC-4 needs to be adjusted about the H3 bytes. For example, the H3 bytes become payload bytes during the frame in which a pointer decrement occurs; therefore, the TXTB#SPE signal should be high coincident with the H3 bytes. Also, in the frame where a pointer increment occurs, the three bytes after the H3 bytes become stuff, therefore the TXTB#SPE signal must be low for those bytes. The TXTB#SPE signal can be tied low if no retiming is done **and** the TXTB#C1J1 signal has only one pulse. It should be noted that when an STM-4c/STS-12c payload is being processed, so that the four transmit Telecom Bus interfaces act as a single 32-bit wide interface, all four TXTB#SPE inputs must be identical.

The Telecom Bus checks the value of the transmit Telecom Bus parity input (TXTB#PAR) against an internally calculated value. The parity calculations that the SONET/SDH framer performs can be configured on a per Telecom Bus basis through the use of the PAR\_EVEN, PAR\_EN, and PAR\_FULL control bits in the OT#Conf11 registers. If the TXTB#PAR signal indicates a different value than the SONET/SDH framer expects, the SONET/SDH framer will indicate an alarm through the PAR\_ERR event bits in the OT#IRQ2 registers. Interrupt mask bits for the PAR\_ERR event bits are provided in the OT#M\_IRQ2 registers. The PAR\_ERR interrupt mask bits will enable an interrupt request to be generated if its corresponding PAR\_ERR event bit is set. The parity is checked on a per Telecom Bus basis regardless of whether or not the Telecom Bus interfaces work individually or as a single bus.

The transmit Telecom Bus failure input (TXTB#FAIL) is generated by the transmit Telecom Bus device to the SONET/SDH framer to tell the SONET/SDH framer to generate AIS-P in the STM-1/STS-3c for which the alarm occurs, regardless of whether retiming is turned on or off. This pin has an internal pull-up resistor to allow automatic AIS generation if a board failure occurs. If this pin is not used it should be tied to ground. It should be noted that when an STM-4c/STS-12c payload is being processed, so that the four transmit Telecom Bus interfaces act as a single 32-bit wide interface, that all four TXTB#FAIL inputs must be activated simultaneously.

### Receive Telecom Bus

There are four receive Telecom Bus interfaces, numbered 1-4, allowing the back-to-back connection of SONET/SDH framers (if retiming is enabled in the transmit direction), or connections to mapper devices.

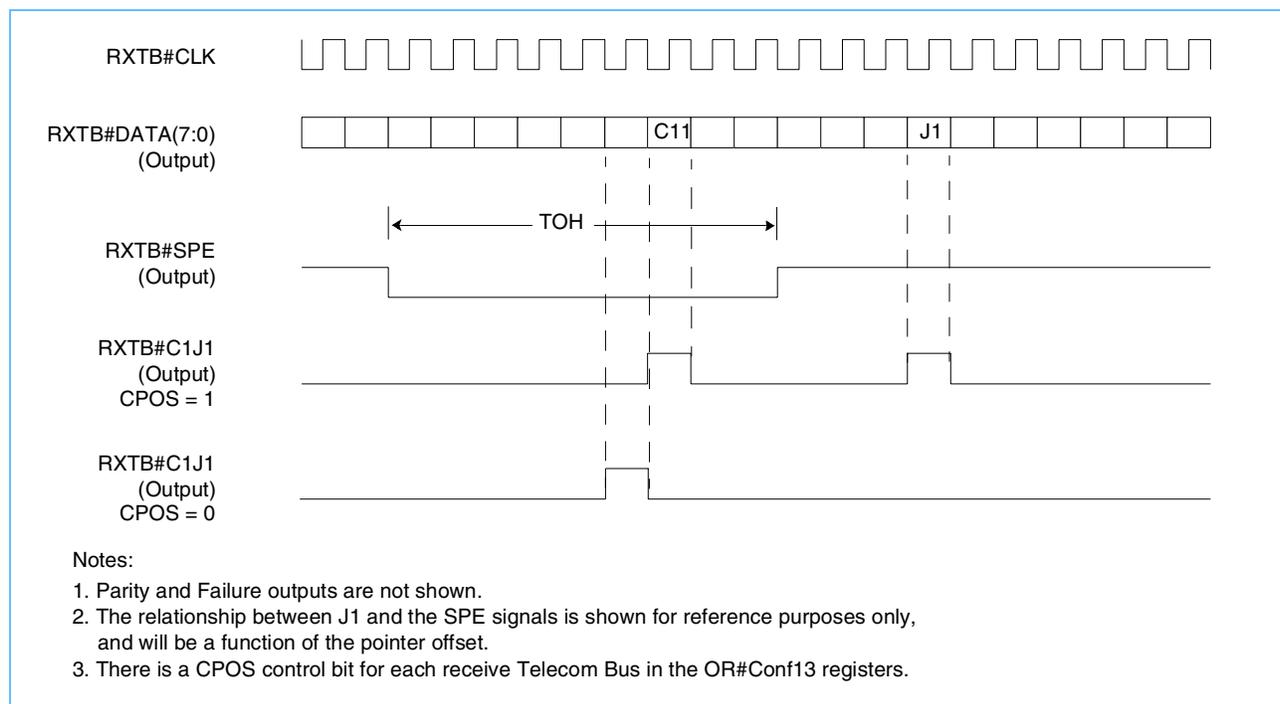
Each receive Telecom Bus interface of the SONET/SDH framer consists of the following outputs: 8-bit data bus (RXTB#DATA(7:0)), clock (RXTB#CLK), SPE indication (RXTB#SPE), C1J1 indication (RXTB#C1J1), parity (RXTB#PAR), and a failure indication (RXTB#FAIL), where # = 1-4. All of the receive Telecom Bus ports operate at 19.44 MHz.

When an STM-4c or STS-12c is processed, the four receive Telecom Buses operate in unison as one Telecom Bus interface. The C1J1, SPE, clock, and FAILURE outputs are identical. RXTB1DATA(7) is the MSB and is the first bit received, while RXTB4DATA(0) is the LSB and is the last bit received.

The subsections that follow summarize the functionality of the receive Telecom Bus interface signals.

The receive Telecom Bus clock output (RXTB#CLK, where # = 1-4) is used to clock out the receive Telecom Bus output signals from the SONET/SDH framer. The clock edge on which the Telecom Bus signals are clocked out is programmable on a per Telecom Bus basis via the CKINV# control bits. See Functional Relationship of the Receive Telecom Bus Signals.

### Functional Relationship of the Receive Telecom Bus Signals Subframe 1 is shown



## IBM SONET/SDH Framer

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Each receive Telecom Bus port has an 8-bit wide data bus that outputs the STM-1/STS-3c # data from the 622.08 Mb/s or 155.52 Mb/s line input to receive Telecom Bus #. The receive Telecom Bus data is byte-aligned and the entire payload, including TOH and POH, is passed through the SONET/SDH framer.

When processing an STM-4c/STS-12c, the four receive Telecom Buses act as a single Telecom Bus, where RXTB1DATA(7) is the MSB and is the first bit received, while RXTB4DATA(0) is the LSB and is the last bit received.

The receive Telecom Bus C1J1 output (RXTB#C1J1) can be programmed to provide two different types of indications, on a per Telecom Bus basis, depending on the setting of the CPOS control bits in the OR#Conf13 registers. When CPOS is set to '1', the corresponding RXTB#C1J1 signal provides two pulses. One pulse is coincident with the C11 byte (RXTB#C1J1 is high and RXTB#SPE is low) and the other is coincident with the J1 byte (RXTB#C1J1 is high and RXTB#SPE is high). The J1 pulse will track the J1 byte position as the SONET/SDH framer receives pointer adjustments. When CPOS is set to '0', the J1 pulse is eliminated and the C1 pulse is coincident with the A2<sub>3</sub> byte.

For all subframes, the receive Telecom Bus SPE output (RXTB#SPE, #=1-4) is low during the TOH byte times in the RXTB#DATA(7:0) stream and is high during the SPE byte times. This includes cases where pointer adjustments are performed and the SPE needs to be adjusted about the H3 bytes. For example, the H3 bytes are payload bytes during the frame in which a pointer decrement occurs; therefore, the RXTB#SPE signal will be high coincident with the H3 bytes for that frame. Also, in the frame where a pointer increment occurs, the three bytes after the H3 bytes become stuff, therefore the RXTB#SPE signal will be low for those bytes.

The parity checking that the SONET/SDH framer performs can be configured on a per Telecom Bus basis through the use of the PAR\_EVEN and PAR\_FULL control bits in the OR#Conf13 registers. Parity is calculated on a per Telecom Bus basis regardless of whether the interfaces work individually or as a single bus.

The receive Telecom Bus failure output (RXTB#FAIL) is generated by SONET/SDH framer in response to an alarm condition that will cause AIS-P to be generated downstream, to tell the downstream device to generate AIS-P in the STM-1/STS-3c in which the alarm occurred. The RXTB#FAIL output will remain active for the duration of the alarm condition that causes it to become set.

### Ring Port

A Ring Port, also known as an AIP (Alarm Indication Port), is provided on the SONET/SDH framer for ring applications where line and path information need to be passed between SONET/SDH framers. The following line and path information are exchanged:

- Path RDI and FEBE.
- Line RDI and FEBE.
- Debounced K1 byte.
- Debounced K2 byte and New APS Indication.
- Debounced K3 byte and New K3 byte indication.

See Operation on page 88 for a detailed description of the Ring Port.

### DCC Port

There are four transmit DCC Ports and four receive DCC Ports. Each port consists of a clock output and a corresponding data input for transmit and a corresponding output for receive. The Line DCC bytes D1-D3 or the MS DCC D4-D12 can be processed by these ports via software control. Optionally, the DCC bytes can be transmitted/received from the on-chip RAM.

## OC-48/STM-16 Expansion Port

An interesting feature of the IBM SONET/SDH framer is that it can be combined with three other SONET/SDH framers to form an STS-48 or STM-16 signal that consists of either 4 x STM-4, 4 x STM-4c, 4 x STS-12, or 4 x STS-12c. The parallel line interfaces are used in this application. A MUX/DEMUX device that performs clock recovery and synthesis is needed to interface the OC-48 or STM-16 serial stream to the SONET/SDH framers. Operation on page 88 contains details for connecting four SONET/SDH framers together for OC-48/STM-16 applications.

## Microprocessor Interface

The SONET/SDH framer has a built-in processor interface which is compatible with the Motorola 68360 processor bus and is adaptable to be compatible with the Intel-type processor bus. Interrupt capability is provided via an interrupt pin and interrupt mask bits. Access to the various configuration registers, counters, control, and status registers is provided via this interface.

There are four operating modes available:

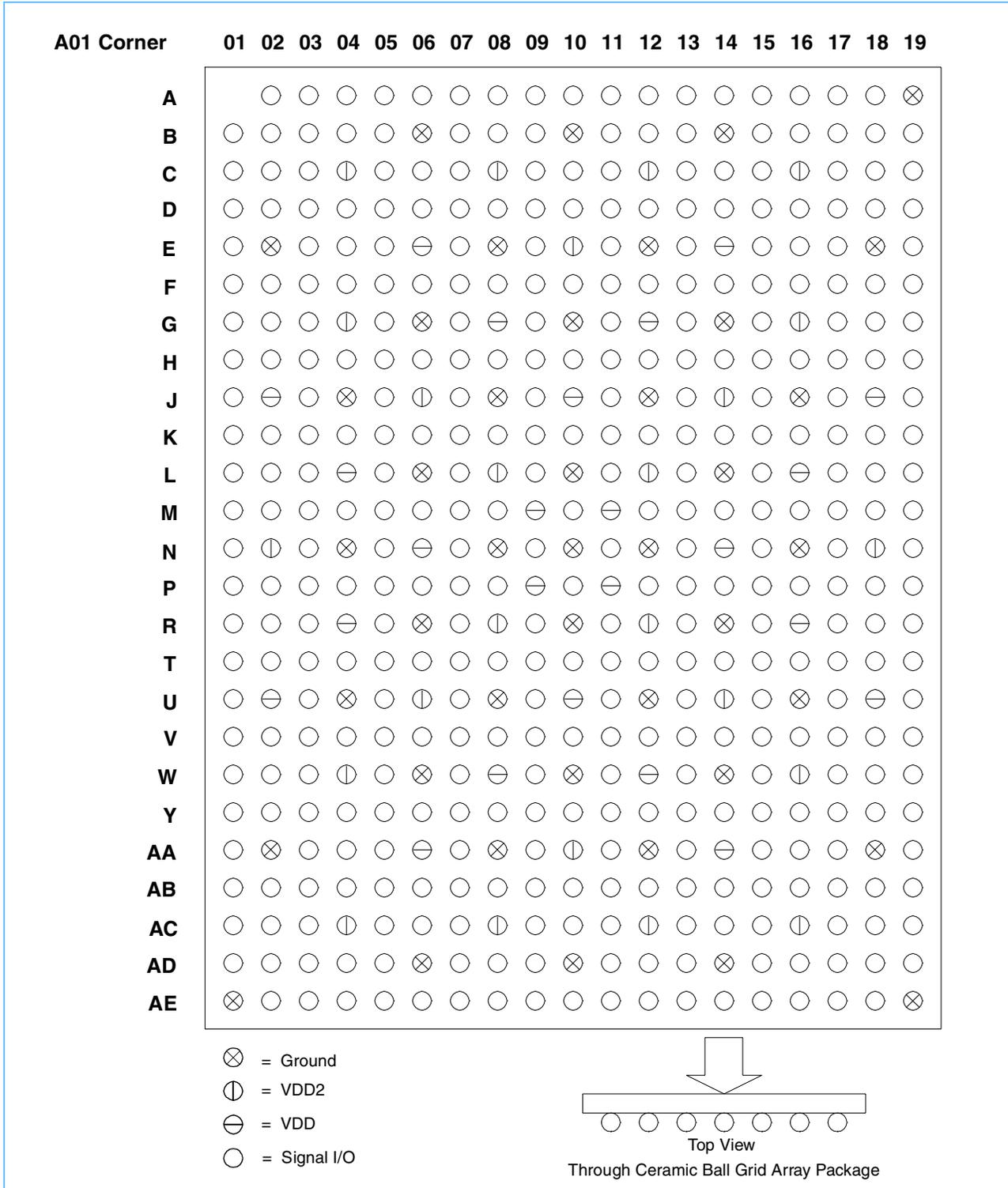
- Motorola synchronous
- Intel synchronous
- Motorola asynchronous
- Intel asynchronous

## Boundary Scan

The Boundary Scan Port includes a five-pin TAP that conforms to the IEEE 1149.1-1994 standard. This TAP provides external boundary scan to read and write the SONET/SDH framer input and output pins from the TAP for board and component testing.

# Pin Information

## Pinout



**JTAG / LSSD / Analog Test Interface Pin Descriptions** (Sheet 1 of 2)

| Name                | Pin No. | I/O | Type      | Description   |
|---------------------|---------|-----|-----------|---|
| LSSD_A              | A13     | I   |           | <b>LSSD Test A clock:</b> Used for factory test of the device. This input is connected to a pull-up resistor in the chip. It should be left unconnected.  |
| LSSD_B              | A11     | I   |           | <b>LSSD Test B clock:</b> Used for factory test of the device. This input is connected to a pull-up resistor in the chip. It should be left unconnected.  |
| LSSD_C              | A07     | I   |           | <b>LSSD Test C clock:</b> Used for factory test of the device. This input is connected to a pull-up resistor in the chip. It should be left unconnected.  |
| SIM_ECL             | C13     | I   |           | <b>LSSD Test ECL clock:</b> Used for factory test of the device. This input is connected to a pull-up resistor in the chip. It should be left unconnected.  |
| TESTGRAC            | V19     | I   |           | <b>LSSD Reset GRA-C clock:</b> Used for factory test of the device. This input is connected to a pull-up resistor in the chip. It should be left unconnected.   |
| $\overline{RI}$     | H17     | I   |           | <b>Receiver Inhibit:</b><br>a) Inhibits all non-test input buffers and forces internal signals connected to them to known values.<br>b) Disables any pull-up resistors to enable IDDQ testing.<br>This input <b>must</b> be tied high.  |
| $\overline{DI1}$    | V01     | I   |           | <b>Driver Inhibit, non-test:</b> Inhibits all non-test output buffers. This input is connected to a pull-up resistor in the chip. It should be left unconnected.  |
| $\overline{DI2}$    | V03     | I   |           | <b>Driver Inhibit, test:</b> Inhibits all test output buffers. This input is connected to a pull-up resistor in the chip. It should be left unconnected.  |
| $\overline{LT}$     | M05     | I   |           | <b>Leakage Test:</b> Disables on-chip circuits that draw direct current, enabling IDDQ measurements to be made. This input is connected to a pull-up resistor in the chip. It should be left unconnected.   |
| $\overline{FRESET}$ | E13     | I   | LVTTL-5sp | <b>Chip Reset:</b> The use of this pin at power-up is <b>mandatory</b> . Holding this pin low causes all the registers in the device to be reset and, provided that TRST is low, the following output drivers to be driven high-Z: TXPDAT1(7:0), TXDCLKT, RXDCLKT1-4, OOF1, all UTOPIA and Telecom Bus outputs, microprocessor interface outputs, all APS interface signals, all Expansion interface outputs, all Ring Port outputs, and the ALARM4(4:0) outputs.<br>The minimum reset pulse width is 10 microseconds. The power and the GPPCLK clock input must be stable during the low to high transition of this pin. The reset pulse applied to this pin should have a rise time less than or equal to 5 ns. |
| TEST_MODE           | E11     | I   |           | <b>LSSD Test Enable:</b> This input is connected to an internal pull-down resistor on the chip. It should be left unconnected.  |
| IOTEST              | T15     | I   |           | <b>LSSD TAP IO Test:</b> Overrides TAP controller and allows the I/O pins to be observed and controlled by the tester. For factory device test only. This input is connected to a pull-down resistor in the chip. It should be left unconnected.  |
| TCK                 | V17     | I   | LVTTL-5sp | <b>JTAG TAP Test Clock:</b> Clock input for JTAG boundary scan testing. This input is connected to a pull-up resistor on the chip. It should be left unconnected if no JTAG test is done.   |
| $\overline{TRST}$   | K17     | I   | LVTTL-5sp | <b>JTAG TAP Reset:</b> Resets the JTAG TAP controller. If the JTAG is not used, an external pull-down resistor can be connected to this pin.  |
| TMS                 | M17     | I   | LVTTL-5sp | <b>JTAG Test Mode Select:</b> Mode selection for JTAG TAP controller. This input is connected to a pull-up resistor on the chip. It should be left unconnected if no JTAG test is done.   |
| TDI                 | T17     | I   | LVTTL-5sp | <b>JTAG Test Data Input:</b> Input port for serial scan data. This input is connected to a pull-up resistor on the chip. It should be left unconnected if no JTAG test is done.   |

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**JTAG / LSSD / Analog Test Interface Pin Descriptions** (Sheet 2 of 2)

| Name                       | Pin No.      | I/O | Type      | Description  |
|----------------------------|--------------|-----|-----------|--|
| TDO                        | P17          | O   | LVTTTL-5s | <b>JTAG Test Data Output:</b> Output port for serial scan data. It should be left unconnected if no JTAG test is done.   |
| NCTY(0)                    | T19          | I   |           | <b>NCTY(0):</b> LSSD test clock input for SERDES section. This input is connected to an internal pull-up resistor on the chip. It should be left unconnected.          |
| NCTY(1)                    | P19          | I   |           | <b>NCTY(1):</b> LSSD test clock input for SERDES section. This input is connected to an internal pull-up resistor on the chip. It should be left unconnected.          |
| LSSD_TAP_C1<br>LSSD_TAP_C2 | AC05<br>AC07 | I   |           | <b>LSSD_TAP_C1/ C2 Clock:</b> LSSD test clocks for TAP controller. These inputs are each connected to a pull-up resistor on the chip. They should be left unconnected. |
| NCTZ(0)                    | C15          | I   |           | <b>NCTZ(0):</b> LSSD test clock input for SERDES section. This input is connected to an internal pull-up resistor on the chip. It should be left unconnected.          |
| NCTZ(1)                    | K19          | I   |           | <b>NCTZ(1):</b> LSSD test clock input for SERDES section. This input is connected to an internal pull-up resistor on the chip. It should be left unconnected.          |
| TCSEN                      | C11          | I   |           | <b>TCSEN:</b> LSSD control signal. This input is connected to a pull-up resistor in the chip; it should be left unconnected.   |
| PLLTEST                    | C09          | I   |           | <b>PLL Test Enable:</b> Used for module-level PLL tests. This input is connected to a pull-down resistor in the chip. It should be left unconnected.                   |
| MUXDIVCLK                  | D11          | O   |           | <b>MUXDIVCLK:</b> Diagnostic output of the SERDES section. This output is connected to an internal pull-down resistor on the chip.                                     |
| MUXLOCK                    | E09          | O   |           | <b>MUXLOCK:</b> PLL test output, used together with PLLTEST. This output is connected to an internal pull-down resistor on the chip.                                   |

**System Pin Descriptions**

| Pin Name                      | Pin No.           | I/O | Type       | Pin Description   |
|-------------------------------|-------------------|-----|------------|---|
| ACHCLK                        | N01               | I   | LVTTTL-5sp | <b>ATM Cell Handler Clock:</b><br>This is an asynchronous 25 MHz clock for the ATM cell handler part of the SONET/SDH framer. This clock can have a frequency lower than 25 MHz but cannot go below the 19.44 MHz clock used by the transmit SFH blocks.  |
| ADDR(2)<br>ADDR(1)<br>ADDR(0) | U15<br>V16<br>U17 | I   | LVTTTL-5sd | <b>SONET/SDH Framer Chip Address:</b><br>When there is more than one SONET/SDH framer on a board for OC-48/STM-16 applications, these pins are used to give each device a unique address. Bit 0 is the LSB. In OC-48/STM-16 operation the valid range of ADDR(2:0) would be set to 000-011.<br>These pins are connected to pull-down resistors in the chip. The default address is therefore 000. These pins should be left floating or pulled down for single-device operation (i.e., for non OC-48/ STM-16 applications). |

**SONET / SDH Pin Descriptions** (Sheet 1 of 3)

| Pin Name   | Pin No.  | I/O   | Type       | Pin Description   |
|--|--|-------|------------|---|
| TXSDAT1(0)<br>TXSDAT1(1)   | H18<br>G19   | O     | PPECL      | <b>Serial SONET/SDH Transmit Data 1:</b> (0=true, 1=inverted)<br>Bit-serial data to electro/optical transceivers.<br>Only TXSDAT1 is active in STS-12/12c, STM-4/4c modes.  |
| TXSDAT2(0)<br>TXSDAT2(1)   | L19<br>M18   | O     | PPECL      | <b>Serial SONET/SDH Transmit Data 2:</b> (0=true, 1=inverted)<br>Bit-serial data to electro/optical transceivers.<br>Not active in STS-12/12c, STM-4/4c modes.  |
| TXSDAT3(0)<br>TXSDAT3(1)   | R19<br>T18   | O     | PPECL      | <b>Serial SONET/SDH Transmit Data 3:</b> (0=true, 1=inverted)<br>Bit-serial data to electro/optical transceivers.<br>Not active in STS-12/12c, STM-4/4c modes.  |
| TXSDAT4(0)<br>TXSDAT4(1)   | W19<br>Y18   | O     | PPECL      | <b>Serial SONET/SDH Transmit Data 4:</b> (0=true, 1=inverted)<br>Bit-serial data to electro/optical transceivers.<br>Not active in STS-12/12c, STM-4/4c modes.  |
| TXPDAT1(7)<br>TXPDAT1(6)<br>TXPDAT1(5)<br>TXPDAT1(4)<br>TXPDAT1(3)<br>TXPDAT1(2)<br>TXPDAT1(1)<br>TXPDAT1(0) | A16<br>B16<br>C19<br>B19<br>A18<br>B18<br>B17<br>A17 | O (T) | LVTTTL-5fp | <b>Parallel SONET/SDH Transmit Data:</b><br>Byte-parallel data to external SONET/SDH serializer/mux such as AMCC3018. TXPDAT1(0) is the LSB.  |
| REFCLKT  | M19  | I     | LVTTTL-5sd | <b>Transmit Reference Clock TTL:</b><br>Reference clock inputs for the transmit clock generation system in the SONET/SDH framer.<br>The frequency of this clock can be selected via control bits to be either 19.44, 38.88, 51.84 or 77.76 MHz.   |
| REFCLKE(0)<br>REFCLKE(1)   | D18<br>C17   | I     | LPECL      | <b>Transmit Reference Clock ECL:</b> (0=true, 1=inverted)<br>Reference clock inputs for the transmit clock generation system in the SONET/SDH framer.<br>There is an internal 100Ω resistor connected across these pins.<br>The frequency of this clock can be selected via control bits to be either 19.44, 38.88, 51.84, 77.76 or 155.52 MHz. |
| TXDCLKT  | E17  | O (T) | LVTTTL-5s  | <b>Transmit Divided Clock:</b><br>Programmable external clock output with nominal 50% duty cycle.<br>The level and speed are selectable via control bits.<br>Frequencies of 19.44, 38.88, 51.84 and 77.76 MHz are available.  |
| TX_BYCLKINT  | A15  | I     | LVTTTL-5sp | <b>SONET/SDH Transmit Byte Clock TTL:</b><br>Byte clock for the parallel transmit interface supplied by the transmit clock system on the board, or by the external serializer/mux.<br>The clock rate is 77.76 MHz for STM-4/STM-4c/STS-12/STS-12c.  |
| TX_BYCLKINE(0)<br>TX_BYCLKINE(1)   | F14<br>E15   | I     | LPECL      | <b>SONET/SDH Transmit Byte Clock ECL:</b> (0=true, 1=inverted)<br>Byte clock for the parallel transmit interface supplied by the transmit clock system on the board, or by the external serializer/mux.<br>The clock rate is 77.76 MHz for STM-4/STM-4c/STS-12/STS-12c.<br>There is an internal 100 Ω resistor connected across these pins.     |
| TXLPOW1  | K16  | I     | LVTTTL-5s  | <b>Transmitter Low Power 1:</b><br>From external optical transmitter indicating low power output. In parallel mode, only TXLPOW1 is used.   |



IBM SONET/SDH Framer

SONET / SDH Pin Descriptions (Sheet 2 of 3)

| Pin Name   | Pin No.  | I/O | Type       | Pin Description   |
|--|--|-----|------------|---|
| TXLPOW2  | M16  | I   | LVTTTL-5s  | <b>Transmitter Low Power 2:</b><br>From external optical transmitter indicating low power output. In parallel mode, only TXLPOW1 is used.   |
| TXLPOW3  | P16  | I   | LVTTTL-5s  | <b>Transmitter Low Power 3:</b><br>From external optical transmitter indicating low power output. In parallel mode, only TXLPOW1 is used.   |
| TXLPOW4  | T16  | I   | LVTTTL-5s  | <b>Transmitter Low Power 4:</b><br>From external optical transmitter indicating low power output. In parallel mode, only TXLPOW1 is used.   |
| TXSDOWN1   | K15  | O   | LVTTTL-5sd | <b>Transmitter Shut Down 1:</b><br>To shut down the respective optical transmitter.<br>The level of this signal for shutdown depends on the transmitter used. The SONET/SDH framer is programmed accordingly via the management interface. In parallel mode, only TXSDOWN1 is used. |
| TXSDOWN2   | M15  | O   | LVTTTL-5sd | <b>Transmitter Shut Down 2:</b><br>To shut down the respective optical transmitter.<br>The level of this signal for shutdown depends on the transmitter used. The SONET/SDH framer is programmed accordingly via the management interface. In parallel mode, only TXSDOWN1 is used. |
| TXSDOWN3   | P15  | O   | LVTTTL-5sd | <b>Transmitter Shut Down 3:</b><br>To shut down the respective optical transmitter.<br>The level of this signal for shutdown depends on the transmitter used. The SONET/SDH framer is programmed accordingly via the management interface. In parallel mode, only TXSDOWN1 is used. |
| TXSDOWN4   | C07  | O   | LVTTTL-5sd | <b>Transmitter Shut Down 4:</b><br>To shut down the respective optical transmitter.<br>The level of this signal for shutdown depends on the transmitter used. The SONET/SDH framer is programmed accordingly via the management interface. In parallel mode, only TXSDOWN1 is used. |
| RXSDAT1(0)<br>RXSDAT1(1)   | E19<br>F18   | I   | PPECL      | <b>Serial SONET/SDH Receive Data 1:</b> (0=true, 1=inverted)<br>The supported data rates on RXSDAT1 are 155.52 and 622.08 Mb/s. An external 100 Ω resistor is required as close as possible to the SONET/SDH framer.  |
| RXSDAT2(0)<br>RXSDAT2(1)   | K18<br>J19   | I   | PPECL      | <b>Serial SONET/SDH Receive Data 2:</b> (0=true, 1=inverted)<br>The supported data rate on RXSDAT2-4 is 155.52 Mb/s. An external 100 Ω resistor is required as close as possible to the SONET/SDH framer.   |
| RXSDAT3(0)<br>RXSDAT3(1)   | P18<br>N19   | I   | PPECL      | <b>Serial SONET/SDH Receive Data 3:</b> (0=true, 1=inverted)<br>The supported data rate on RXSDAT2-4 is 155.52 Mb/s. An external 100 Ω resistor is required as close as possible to the SONET/SDH framer.   |
| RXSDAT4(0)<br>RXSDAT4(1)   | V18<br>U19   | I   | PPECL      | <b>Serial SONET/SDH Receive Data 4:</b> (0=true, 1=inverted)<br>The supported data rate on RXSDAT2-4 is 155.52 Mb/s. An external 100 Ω resistor is required as close as possible to the SONET/SDH framer.   |
| RXPDAT1(7)<br>RXPDAT1(6)<br>RXPDAT1(5)<br>RXPDAT1(4)<br>RXPDAT1(3)<br>RXPDAT1(2)<br>RXPDAT1(1)<br>RXPDAT1(0) | D16<br>F15<br>B15<br>D15<br>A14<br>D14<br>C14<br>B13 | I   | LVTTTL-5sd | <b>Parallel SONET/SDH Receive Data 1:</b><br>Byte-parallel input data from external SDH/SONET deserializer/demux, e.g., AMCC 3017. Bit 0 is the LSB. This data must be byte-aligned to the bytes in the incoming SONET/SDH frame.   |

**SONET / SDH Pin Descriptions** (Sheet 3 of 3)

| Pin Name | Pin No. | I/O   | Type       | Pin Description   |
|----------|---------|-------|------------|---|
| RXBYCLK1 | A09     | I     | LVTTTL-5sp | <b>SONET/SDH Receive Byte Clock:</b><br>Byte clock for the parallel input data on RXPDAT1. Possible clock rate is: 77.76 MHz for STM-4/STM-4c/STS-12/STS-12c.   |
| RXDCLKT1 | E16     | O (T) | LVTTTL-5s  | <b>Receive Divided Clock 1:</b><br>Programmable clock output derived from the serial data stream on channel 1. Clock rates are 19.44, 38.88, 51.84 and 77.76 MHz.   |
| RXDCLKT2 | C18     | O (T) | LVTTTL-5s  | <b>Receive Divided Clock 2:</b><br>Programmable clock output derived from the serial data stream on channel 2. Clock rates are 19.44, 38.88, 51.84 and 77.76 MHz.   |
| RXDCLKT3 | Y17     | O (T) | LVTTTL-5s  | <b>Receive Divided Clock 3:</b><br>Programmable clock output derived from the serial data stream on channel 3. Clock rates are 19.44, 38.88, 51.84 and 77.76 MHz.   |
| RXDCLKT4 | AA17    | O (T) | LVTTTL-5s  | <b>Receive Divided Clock 4:</b><br>Programmable clock output derived from the serial data stream on channel 4. Clock rates are 19.44, 38.88, 51.84 and 77.76 MHz.   |
| LOCKDET1 | D19     | I     | LVTTTL-5sd | <b>Lock Detect 1:</b><br>Signal from external SDH/SONET deserializer indicating that its PLL has locked to the incoming serial data stream. This pin is used when operating with the receive parallel line interface.   |
| LOSSSIG1 | F13     | I     | LVTTTL-5sp | <b>Loss of Signal 1:</b> Signal from optical receiver indicating loss of signal.  |
| LOSSSIG2 | G13     | I     | LVTTTL-5sp | <b>Loss of Signal 2:</b> Signal from optical receiver indicating loss of signal.  |
| LOSSSIG3 | H13     | I     | LVTTTL-5sp | <b>Loss of Signal 3:</b> Signal from optical receiver indicating loss of signal.  |
| LOSSSIG4 | H12     | I     | LVTTTL-5sp | <b>Loss of Signal 4:</b> Signal from optical receiver indicating loss of signal.  |
| OOF1     | D17     | O (T) | LVTTTL-5sd | <b>Out Of Frame 1:</b><br>Signal to the external SDH/SONET deserializer/demux indicating that frame synchronization has been lost and that the deserializer/demux should resume searching for the frame pattern. This pin is used when operating with the receive parallel line interface. If an out of frame condition exists then OOF1 is low. If n consecutive bad framing patterns are received (where n = 4 or 5 configurable), OOF1 goes high. Depending on the deserializer used, either the high level or this low to high transition will cause the external deserializer to resynchronize to the framing pattern. The external deserializer will pulse FP1 high for one clock cycle as it resynchronizes. If the next framing pattern after the pulse on FP1 is correct, the OOF1 will be driven low and remain low. If this framing pattern is incorrect OOF1 will be driven low for two clock cycles and then driven high again. Once again, either the edge or the high level will cause the external deserializer to resynchronize to the framing pattern and the process repeats. If three consecutive frame-periods elapse since the low to high transition of OOF1 and no pulse has been received on FP1, OOF1 will be driven low for two clock cycles then driven high again. |
| FP1      | A12     | I     | LVTTTL-5sd | <b>Frame Pulse 1:</b><br>Signal from an external SDH/SONET deserializer/demux e.g., AMCC 3017. Pulsed high for one clock cycle to indicate the boundary of an SDH/SONET frame. For OC-48 applications this signal will normally be aligned to the first SPE/VC-4 byte of the first row of the SONET/SDH frame. This pin is used when operating with the receive parallel line interface. The A2Frm control bits in the OFPRXGP2 register control the required alignment of the FP1 signal.  |
| RSTCREC1 | H19     | O     | LVTTTL-5sd | <b>Reset Deserializer 1:</b><br>Signal to force a reset of external deserializer. The level used to reset depends on the deserializer. This pin is used when operating with the receive parallel line interface.  |

## IBM SONET/SDH Framer

## PHY Layer Interface Pin Descriptions (Sheet 1 of 4)

| Pin Name   | Pin No.  | I/O | Type       | Pin Description  |
|--|--|-----|------------|--|
| TXUCLK1  | A05  | I   | LVTTTL-5sp | <p><b>Transmit UTOPIA Clock 1:</b> The data and control signals are transferred on the rising edge of this clock.</p> <p><b>UTOPIA Level 1:</b> This clock is used for transmit UTOPIA Level 1 interface 1. Maximum clock frequency is 25 MHz.</p> <p><b>UTOPIA Level 2:</b> This clock is used for the transmit UTOPIA Level 2 interface. Maximum clock frequency is 50 MHz.</p> <p><b>UTOPIA Level 2+:</b> This clock is used for the transmit UTOPIA Level 2+ interface. Maximum clock frequency is 50 MHz.</p>   |
| TXUCLK2  | C06  | I   | LVTTTL-5sp | <p><b>Transmit UTOPIA Clock 2:</b> The data and control signals are transferred on the rising edge of this clock.</p> <p><b>UTOPIA Level 1:</b> This clock is used for transmit UTOPIA Level 1 interface 2. Maximum clock frequency is 25 MHz.</p> <p><b>UTOPIA Level 2:</b> This clock is not used.</p> <p><b>UTOPIA Level 2+:</b> This clock is not used.</p>  |
| TXUDATA(15)<br>TXUDATA(14)<br>TXUDATA(13)<br>TXUDATA(12)<br>TXUDATA(11)<br>TXUDATA(10)<br>TXUDATA(9)<br>TXUDATA(8)<br>TXUDATA(7)<br>TXUDATA(6)<br>TXUDATA(5)<br>TXUDATA(4)<br>TXUDATA(3)<br>TXUDATA(2)<br>TXUDATA(1)<br>TXUDATA(0) | B07<br>A08<br>B08<br>D08<br>F08<br>H08<br>K08<br>D09<br>F09<br>G09<br>H09<br>J09<br>D10<br>F10<br>H10<br>F11 | I   | LVTTTL-5sp | <p><b>Transmit Data In:</b> 16-bit cell data input, valid when <math>\overline{\text{TXENB}}</math> asserted low. Bit 0 is the LSB.</p> <p><b>UTOPIA Level 1:</b> TXUDATA(15:8) is the data byte input for transmit UTOPIA Level 1 interface 1. Bit 15 is the MSB and is transmitted first. TXUDATA(7:0) is the data byte input for transmit UTOPIA Level 1 interface 2. Bit 7 is the MSB and is transmitted first.</p> <p><b>UTOPIA Level 2:</b> TXUDATA(15:0) is the word input for the transmit UTOPIA Level 2 interface. Bit 15 is the most significant bit and is transmitted first.</p> <p><b>UTOPIA Level 2+:</b> TXUDATA(15:0) is the word input for the transmit UTOPIA Level 2+ interface. Bit 15 is the most significant bit and is transmitted first.</p>            |
| TXUADDR(4)<br>TXUADDR(3)<br>TXUADDR(2)<br>TXUADDR(1)<br>TXUADDR(0)   | B09<br>A10<br>C10<br>B11<br>B12  | I   | LVTTTL-5sp | <p><b>Transmit Physical Device Address:</b></p> <p><b>UTOPIA Level 1:</b> TXUADDR(4) - TXUADDR(2) are the transmit Parity, Start of Cell, and Enable inputs, respectively, for transmit UTOPIA Level 1 interface 2.</p> <p><b>UTOPIA Level 2:</b> Five-bit wide address for the ports programmed in this device is provided on TXUADDR(4:0). Bit 0 is the LSB. If single-PHY operation is performed, such as when STM-4c or STS-12c frames are processed, then these pins should be set to '0'.</p> <p><b>UTOPIA Level 2+:</b> Five-bit wide address for the ports programmed in this device is provided on TXUADDR(4:0). Bit 0 is the LSB. If single-PHY operation is performed, such as when STM-4c or STS-12c frames are processed, then these pins should be set to '0'.</p> |
| TXPRTY   | D13  | I   | LVTTTL-5sd | <p><b>Transmit Parity Input:</b> Odd parity bit for UTOPIA Level 2+, Level 2, and Level 1 #1 interfaces. Parity can be calculated over data, or data and control signals, depending on a control bit setting.</p>  |
| TXSOC  | D12  | I   | LVTTTL-5sd | <p><b>Transmit Start-of-Cell/Chunk Input:</b> Indicates the start of cell/chunk for UTOPIA Level 2+, Level 2, and Level 1 #1 interfaces.</p>   |
| TXSOFI   | G11  | I   | LVTTTL-5sd | <p><b>Transmit Start-of-Frame Input:</b> Used only during UTOPIA Level 2+ operation, this pin indicates the start-of-frame data.</p>   |
| $\overline{\text{TXENB}}$  | K09  | I   | LVTTTL-5sp | <p><b>Transmit Read Enable Input:</b> Read enable signal for cell input for UTOPIA Level 2+, Level 2, and Level 1 #1 interfaces.</p>   |

**PHY Layer Interface Pin Descriptions** (Sheet 2 of 4)

| Pin Name  | Pin No.                  | I/O   | Type       | Pin Description   |
|---|--------------------------|-------|------------|---|
| TXCLAV(0)/PAVO<br>TXCLAV(1)<br>TXCLAV(2)<br>TXCLAV(3) | A06<br>D07<br>F07<br>G07 | O (T) | LVTTTL-5fd | <p><b>Transmit Payload Available Indicator:</b> TXCLAV/PAVO indicates that the SONET/SDH framer can accept a complete cell or chunk.</p> <p><b>UTOPIA Level 1:</b> TXCLAV(0) is the cell available indication for transmit UTOPIA Level 1 interface 1. TXCLAV(1) is the cell available indication for transmit UTOPIA Level 1 interface 2.</p> <p><b>UTOPIA Level 2:</b> TXCLAV(3:0) are the cell available indications for the transmit UTOPIA Level 2 interface. TXCLAV(3:0) can be configured for direct status (TXCLAV(0) only or TXCLAV(3:0)) or multiplexed status (TXCLAV(0) only or TXCLAV(3:0)) via the SIndT1(1:0) bits.</p> <p><b>UTOPIA Level 2+:</b> TXCLAV(3:0) are the chunk available indications for the transmit UTOPIA Level 2+ interface. TXCLAV(3:0) can be configured for direct status (TXCLAV(0) only or TXCLAV(3:0)) or multiplexed status (TXCLAV(0) only or TXCLAV(3:0)) via the SIndT1(1:0) bits. Chunks are analogous to cells. TXCLAV functions exactly the same way as in ATM mode, except that TXCLAV indicates the SONET/SDH framer's ability to accept chunks instead of cells.</p> |
| TXEOF1  | H11                      | I     | LVTTTL-5sd | <p><b>Transmit End-of-Frame Input:</b> Used only during UTOPIA Level 2+ operation, this pin indicates the end-of- frame data input.</p>   |
| TXMS1   | K10                      | I     | LVTTTL-5sd | <p><b>Transmit Most Significant Byte Input:</b> Used only during UTOPIA Level 2+ operation, this pin indicates the frame data ends on the MS byte of the current word transfer.</p>   |
| TXABTO  | F12                      | O (T) | LVTTTL-VD  | <p><b>Transmit Frame Abort Output:</b> Used only during UTOPIA Level 2+ operation, this pin indicates when a transmit FIFO has underflowed during the middle of the transfer of the "HDLC-like" frame. In MPHYS mode, if a transmit ACB FIFO underflow occurs in a macro, say macro n, while macro m is being accessed, the TXABTO indication for macro n will not be output until macro n is selected.</p> <p>An external 1-3 kΩ pull-down resistor is required for this pin to ensure that the TXABTO pin is pulled to its inactive state in a timely manner in order to avoid functional problems.</p>   |
| RXUCLK1   | AE05                     | I     | LVTTTL-5sp | <p><b>Receive UTOPIA Clock 1:</b> The data and control signals are transferred on the rising edge of this clock.</p> <p><b>UTOPIA Level 1:</b> This clock is used for receive UTOPIA Level 1 interface 1. Maximum clock frequency is 25 MHz.</p> <p><b>UTOPIA Level 2:</b> This clock is used for the receive UTOPIA Level 2 interface. Maximum clock frequency is 50 MHz.</p> <p><b>UTOPIA Level 2+:</b> This clock is used for the receive UTOPIA Level 2+ interface. Maximum clock frequency is 50 MHz.</p>  |
| RXUCLK2   | AD05                     | I     | LVTTTL-5sp | <p><b>Receive UTOPIA Clock 2:</b> The data and control signals are transferred on the rising edge of this clock.</p> <p><b>UTOPIA Level 1:</b> This clock is used for receive UTOPIA Level 1 interface 2. Maximum clock frequency is 25 MHz.</p> <p><b>UTOPIA Level 2:</b> This clock is not used.</p> <p><b>UTOPIA Level 2+:</b> This clock is not used.</p>   |



IBM SONET/SDH Framer

PHY Layer Interface Pin Descriptions (Sheet 3 of 4)

| Pin Name   | Pin No.   | I/O   | Type       | Pin Description   |
|--|---|-------|------------|---|
| RXUDATA(15)<br>RXUDATA(14)<br>RXUDATA(13)<br>RXUDATA(12)<br>RXUDATA(11)<br>RXUDATA(10)<br>RXUDATA(9)<br>RXUDATA(8)<br>RXUDATA(7)<br>RXUDATA(6)<br>RXUDATA(5)<br>RXUDATA(4)<br>RXUDATA(3)<br>RXUDATA(2)<br>RXUDATA(1)<br>RXUDATA(0) | AC06<br>AB06<br>AD07<br>AB07<br>Y07<br>AE08<br>AD08<br>AB08<br>Y08<br>V08<br>AD09<br>AB09<br>Y09<br>W09<br>V09<br>Y10 | O (T) | LVTTTL-5fp | <p><b>Receive Data Out:</b> Tri-stateable 16-bit cell data output bus, enabled only in cycles following those with <math>\overline{RXENB}</math> asserted low. Bit 0 is the LSB.</p> <p><b>UTOPIA Level 1:</b> RXUDATA(15:8) is the data byte output for receive UTOPIA Level 1 interface 1. Bit 15 is the MSB and is the first bit received. RXUDATA(7:0) is the data byte output for receive UTOPIA Level 1 interface 2. Bit 7 is the MSB and is the first bit received.</p> <p><b>UTOPIA Level 2:</b> RXUDATA(15:0) is the word output for the receive UTOPIA Level 2 interface. Bit 15 is the most significant bit and is the first bit received.</p> <p><b>UTOPIA Level 2+:</b> RXUDATA(15:0) is the word input for the receive UTOPIA Level 2+ interface. Bit 15 is the most significant bit and is the first bit received.</p> |
| RXUADDR(4)<br>RXUADDR(3)<br>RXUADDR(2)<br>RXUADDR(1)<br>RXUADDR(0)   | AE10<br>AC10<br>AB10<br>AB11<br>AD11  | I     | LVTTTL-5sp | <p><b>Receive Physical Device Address:</b></p> <p><b>UTOPIA Level 1:</b> RXUADDR(2) is the receive <math>\overline{Enable}</math> input, for receive UTOPIA Level 1 interface 2.</p> <p><b>UTOPIA Level 2:</b> Five-bit wide address for the ports programmed in this device is provided on RXUADDR(4:0). Bit 0 is the LSB. If single-PHY operation is performed, such as when STM-4c or STS-12c frames are processed, then these pins should be set to '0'.</p> <p><b>UTOPIA Level 2+:</b> Five-bit wide address for the ports programmed in this device is provided on RXUADDR(4:0). Bit 0 is the LSB. If single-PHY operation is performed, such as when STM-4c or STS-12c frames are processed, then these pins should be set to '0'.</p>   |
| RXPRTY   | V10   | O (T) | LVTTTL-5fd | <p><b>Receive Parity Output:</b> (Active high)</p> <p>Parity bit for UTOPIA Level 2+, Level 2, and Level 1 #1 interfaces. Parity can be generated over data, or over data and control signals, depending on a control bit setting. Parity can also be selected to be odd or even.</p>   |
| RXSOC  | AD12  | O (T) | LVTTTL-5fd | <p><b>Receive Start of Cell/Chunk Output:</b> (Active high)</p> <p>Tri-stateable output, enabled only in cycles following those with <math>\overline{RXENB}</math> asserted low. RXSOC indicates the start of each chunk or ATM cell for UTOPIA Level 2+, Level 2, and Level 1 #1 interfaces.</p>   |
| RXSOFO   | U09   | O (T) | LVTTTL-5fd | <p><b>Receive Start-of-Frame Output:</b> (Active high)</p> <p>Used only during UTOPIA Level 2+ operation, this pin indicates the start of a new block of frame data.</p>  |
| $\overline{RXENB}$   | AE06  | I     | LVTTTL-5sp | <p><b>Receive Read Enable Input:</b> (Active low)</p> <p>Read enable input signal for UTOPIA Level 2+, Level 2, and Level 1 #1 interfaces. Data and control outputs, except for the RXCLAV(3:0) signals, are output on the clock cycle following the assertion of this signal low.</p>  |

**PHY Layer Interface Pin Descriptions** (Sheet 4 of 4)

| Pin Name   | Pin No.                   | I/O   | Type       | Pin Description   |
|--|---------------------------|-------|------------|---|
| RXCLAV(0)<br>RXCLAV(1)<br>RXCLAV(2)<br>RXCLAV(3) | AB12<br>Y11<br>W11<br>V11 | O (T) | LVTTTL-5fd | <p><b>Receive Payload Available Indicator Output:</b> Tri-stateable output signal which indicates that a complete chunk or cell is available for transfer. RXCLAV is asserted high to indicate that it has a complete cell or chunk to transfer, otherwise RXCLAV is asserted low.</p> <p><b>UTOPIA Level 1:</b> RXCLAV(0) is the cell available indication for receive UTOPIA Level 1 interface 1. RXCLAV(1)-RXCLAV(3) are the receive CLAV, Start of Cell, and Parity outputs for receive UTOPIA Level 1 interface 2.</p> <p><b>UTOPIA Level 2:</b> RXCLAV(3:0) are the cell available indications for the receive UTOPIA Level 2 interface. RXCLAV(3:0) can be configured for direct status (RXCLAV(0) only or RXCLAV(3:0)) or multiplexed status (RXCLAV(0) only or RXCLAV(3:0)) via the SIndR1(1:0) bits.</p> <p><b>UTOPIA Level 2+:</b> RXCLAV(3:0) are the chunk available indications for the receive UTOPIA Level 2+ interface. RXCLAV(3:0) can be configured for direct status (RXCLAV(0) only or RXCLAV(3:0)) or multiplexed status (RXCLAV(0) only or RXCLAV(3:0)) via the SIndR1(1:0) bits. Chunks are analogous to cells. RXCLAV functions exactly the same way as in ATM mode, expect that RXCLAV indicates that the SONET/SDH framer has at least one chunk to transfer (as opposed to having cells to transfer).</p> |
| RXEFOFO  | T09                       | O (T) | LVTTTL-5fd | <p><b>Receive End-of-Frame Output:</b> (Active high)<br/>Used only during UTOPIA Level 2+ operation, this pin indicates the end of a block of frame data.</p>   |
| RXMSO  | T10                       | O (T) | LVTTTL-5fd | <p><b>Receive Most Significant Byte Output:</b> (Active high)<br/>Used only during UTOPIA Level 2+ operation, this pin indicates the frame data ends on the MSB of the current word transfer.</p>   |
| RXFCSEO  | U11                       | O (T) | LVTTTL-5fd | <p><b>Receive Frame FCS Error Output:</b> (Active high)<br/>Used only during UTOPIA Level 2+ operation, this pin indicates that an FCS error is detected on the current frame. When FCSABT control bit is set to a '1', this pin will also indicate when an ABORT sequence (i.e., an illegal sequence of 7D7E H) is received on the current frame.</p>  |
| RXABTO   | T11                       | O (T) | LVTTTL-5fd | <p><b>Receive Abort Output:</b><br/>This pin is used only during UTOPIA Level 2+ operation. When FCSABT is set to '0', this pin is an active high output signal that indicates that an ABORT condition (i.e., illegal sequence of 7D7E H detected or a receive ACB FIFO overflow) has been detected on the current frame. When FCSABT is set to '1', this pin is forced low. In MPHY mode, if a receive abort condition occurs in a macro, say macro n, while macro m is being accessed, the RXABTO indication for macro n will not be output until macro n is selected.</p>  |



IBM SONET/SDH Framer

Telecom Bus Interface Pin Descriptions (Sheet 1 of 6)

| Pin Name   | Pin No.  | I/O | Type       | Pin Description <sup>1</sup>   |
|--|--|-----|------------|--|
| TXCCLK   | D05  | O   | LVTTTL-5sp | <b>Transmit Reference Clock:</b><br>TXCCLK is provided as a transmit reference timebase for devices connected to the transmit Telecom Bus interface. TXCCLK is configured to be 19.44 MHz for STM-1/STS-3c/STM-4/STS-12/STM-4c/STS-12c operation.  |
| $\overline{\text{TXCCLK}}$   | E05  | O   | LVTTTL-5sp | <b>Transmit Reference Clock Not:</b><br>$\overline{\text{TXCCLK}}$ is the complement of TXCCLK and is provided to support devices that may have different timing requirements for clocking in the TXCFRM signal. $\overline{\text{TXCCLK}}$ is configured to be 19.44 MHz for STM-1/STS-3c/STM-4/STS-12/STM-4c/STS-12c operation.  |
| TXCFRM   | F06  | O   | LVTTTL-5sp | <b>Transmit Reference Frame Pulse:</b><br>TXCFRM must be used to synchronize the data that is input to the Telecom Bus ports. This signal is synchronous to TXCCLK.  |
| TXCC1J1  | D06  | O   |            | <b>No Connect:</b> Leave unconnected.  |
| TXCSPE   | B05  | O   |            | <b>No Connect:</b> Leave unconnected.  |
| TXTB1DATA(7)<br>TXTB1DATA(6)<br>TXTB1DATA(5)<br>TXTB1DATA(4)<br>TXTB1DATA(3)<br>TXTB1DATA(2)<br>TXTB1DATA(1)<br>TXTB1DATA(0) | A02<br>A03<br>B03<br>A04<br>B04<br>D04<br>E04<br>F05 | I   | LVTTTL-5sp | <b>Telecom Bus 1 Transmit Input Data:</b><br>19.44 Mbytes/s AU-4 (transmit retiming turned off) or VC-4 (transmit retiming turned on) data input on these pins are inserted into the outgoing STM-1 #1. This data is clocked into the SONET/SDH framer on the rising edge of TXTB1CLK. Bit 7 is the MSB and is transmitted first.  |
| TXTB1CLK   | B01  | I   | LVTTTL-5sp | <b>Telecom Bus 1 Transmit Input Clock:</b><br>All of the signals for Telecom Bus 1 are clocked into the SONET/SDH framer on the rising edge of this 19.44 MHz clock. TXTB1CLK <b>must</b> be frequency locked to either TXCCLK or $\overline{\text{TXCCLK}}$ if transmit retiming is not performed.  |
| TXTB1C1J1  | B02  | I   | LVTTTL-5sd | <b>Telecom Bus 1 Transmit Input Slot Indication:</b><br>When the TXTB1SPE signal is high, TXTB1C1J1 indicates the position of the J1 byte. When the TXTB1SPE signal is low, TXTB1C1J1 indicates the position of the C1 byte. The J1 and C1 pulses are required if transmit retiming is turned on. If transmit retiming is turned off, this signal becomes a slot identifier. |
| TXTB1SPE   | C03  | I   | LVTTTL-5sd | <b>Telecom Bus 1 Transmit Input Synchronous Payload Envelope Signal:</b><br>This signal is high for the SPE bytes and low for the TOH bytes on Telecom Bus 1. If transmit retiming is turned off, and no J1 pulse is present in TXTB1C1J1, then this pin can be tied low.  |
| TXTB1PAR   | D03  | I   | LVTTTL-5sp | <b>Telecom Bus 1 Transmit Input Parity:</b><br>Parity for the signals of Telecom Bus1. It should be calculated by the transmitting device according to the settings of the PFULL1, PEVEN1, and PENA1 control bits in the SONET/SDH framer. Parity errors are reported via the TB1PAR alarm bit, but no actions are taken.  |
| TXTB1FAIL  | E03  | I   | LVTTTL-5sp | <b>Telecom Bus 1 Transmit Input Failure Indication:</b><br>TXTB1FAIL indicates that a failure has occurred on the device transmitting on Telecom Bus 1. When TXTB1FAIL goes high, AIS-P is transmitted on STM-1 #1/STS-3c #1.  |

1. When STM-4c or STS-12c frames are processed, the four transmit and four receive Telecom Buses operate in parallel as two 32-bit wide Telecom Buses.

**Telecom Bus Interface Pin Descriptions** (Sheet 2 of 6)

| Pin Name   | Pin No.  | I/O | Type       | Pin Description <sup>1</sup>   |
|--|--|-----|------------|--|
| TXTB2DATA(7)<br>TXTB2DATA(6)<br>TXTB2DATA(5)<br>TXTB2DATA(4)<br>TXTB2DATA(3)<br>TXTB2DATA(2)<br>TXTB2DATA(1)<br>TXTB2DATA(0) | F02<br>F03<br>F04<br>E01<br>D01<br>D02<br>C01<br>C02 | I   | LVTTTL-5sp | <b>Telecom Bus 2 Transmit Input Data:</b><br>19.44 Mbytes/s AU-4 (transmit retiming turned off) or VC-4 (transmit retiming turned on) data input on these pins is inserted into the outgoing STM-1 #2. This data is clocked into the SONET/SDH framer on the rising edge of TXTB2CLK. Bit 7 is the MSB and is transmitted first.   |
| TXTB2CLK   | G01  | I   | LVTTTL-5sp | <b>Telecom Bus 2 Transmit Input Clock:</b><br>All of the signals for Telecom Bus 2 are clocked into the SONET/SDH framer on the rising edge of this 19.44 MHz clock. TXTB2CLK <b>must</b> be frequency locked to either TXCCLK or $\overline{\text{TXCCLK}}$ if transmit retiming is not performed.  |
| TXTB2C1J1  | G02  | I   | LVTTTL-5sd | <b>Telecom Bus 2 Transmit Input Slot Indication:</b><br>When the TXTB2SPE signal is high, TXTB2C1J1 indicates the position of the J1 byte. When the TXTB2SPE signal is low, TXTB2C1J1 indicates the position of the C1 byte. The J1 and C1 pulses are required if transmit retiming is turned on. If transmit retiming is turned off, this signal becomes a slot identifier. |
| TXTB2SPE   | G03  | I   | LVTTTL-5sd | <b>Telecom Bus 2 Transmit Input Synchronous Payload Envelope Signal:</b><br>This signal is high for the SPE bytes and low for the TOH bytes on Telecom Bus 2. If transmit retiming is turned off and no J1 pulse is present in TXTB2C1J1, this pin can be tied low.  |
| TXTB2PAR   | G05  | I   | LVTTTL-5sp | <b>Telecom Bus 2 Transmit Input Parity:</b><br>Parity for the signals of Telecom Bus 2. It should be calculated by the transmitting device according to the settings of the PFULL2, PEVEN2, and PENA2 control bits in the SONET/SDH framer. Parity errors are reported via the TB2PAR alarm bit, but no actions are taken.   |
| TXTB2FAIL  | F01  | I   | LVTTTL-5sp | <b>Telecom Bus 2 Transmit Input Failure Indication:</b><br>TXTB2FAIL indicates that a failure has occurred on the device transmitting on Telecom Bus 2. When TXTB2FAIL goes high, AIS-P is transmitted on STM-1 #2/STS-3c #2.  |
| TXTB3DATA(7)<br>TXTB3DATA(6)<br>TXTB3DATA(5)<br>TXTB3DATA(4)<br>TXTB3DATA(3)<br>TXTB3DATA(2)<br>TXTB3DATA(1)<br>TXTB3DATA(0) | J03<br>J05<br>J07<br>H02<br>H04<br>H05<br>H06<br>H07 | I   | LVTTTL-5sp | <b>Telecom Bus 3 Transmit Input Data:</b><br>19.44 Mbytes/s AU-4 (transmit retiming turned off) or VC-4 (transmit retiming turned on) data input on these pins is inserted into the outgoing STM-1 #3. This data is clocked into the SONET/SDH framer on the rising edge of TXTB3CLK. Bit 7 is the MSB and is transmitted first.   |
| TXTB3CLK   | K02  | I   | LVTTTL-5sp | <b>Telecom Bus 3 Transmit Input Clock:</b><br>All of the signals for Telecom Bus 3 are clocked into the SONET/SDH framer on the rising edge of this 19.44 MHz clock. TXTB1CLK <b>must</b> be frequency locked to either TXCCLK or $\overline{\text{TXCCLK}}$ if transmit retiming is not performed.  |
| TXTB3C1J1  | K04  | I   | LVTTTL-5sd | <b>Telecom Bus 3 Transmit Input Slot Indication:</b><br>When the TXTB3SPE signal is high, TXTB3C1J1 indicates the position of the J1 byte. When the TXTB3SPE signal is low, TXTB3C1J1 indicates the position of the C1 byte. The J1 and C1 pulses are required if transmit retiming is turned on. If transmit retiming is turned off, this signal becomes a slot identifier. |

1. When STM-4c or STS-12c frames are processed, the four transmit and four receive Telecom Buses operate in parallel as two 32-bit wide Telecom Buses.

## IBM SONET/SDH Framer

## Telecom Bus Interface Pin Descriptions (Sheet 3 of 6)

| Pin Name   | Pin No.  | I/O | Type       | Pin Description <sup>1</sup>   |
|--|--|-----|------------|--|
| TXTB3SPE   | K06  | I   | LVTTTL-5sd | <b>Telecom Bus 3 Transmit Input Synchronous Payload Envelope Signal:</b><br>This signal is high for the SPE bytes and low for the TOH bytes on Telecom Bus 3. If transmit retiming is turned off and no J1 pulse is present in TXTB3C1J1, this pin can be tied low.  |
| TXTB3PAR   | K07  | I   | LVTTTL-5sp | <b>Telecom Bus 3 Transmit Input Parity:</b><br>Parity for the signals of Telecom Bus 3. It should be calculated by the transmitting device according to the settings of the PFULL3, PEVEN3, and PENA3 control bits in the SONET/SDH framer. Parity errors are reported via the TB3PAR alarm bit, but no actions are taken.   |
| TXTB3FAIL  | J01  | I   | LVTTTL-5sp | <b>Telecom Bus 3 Transmit Input Failure Indication:</b><br>TXTB3FAIL indicates that a failure has occurred on the device transmitting on Telecom Bus 3. When TXTB3FAIL goes high, AIS-P is transmitted on STM-1 #3/STS-3c #3.  |
| TXTB4DATA(7)<br>TXTB4DATA(6)<br>TXTB4DATA(5)<br>TXTB4DATA(4)<br>TXTB4DATA(3)<br>TXTB4DATA(2)<br>TXTB4DATA(1)<br>TXTB4DATA(0)                           | M06<br>M07<br>M08<br>L01<br>L02<br>L03<br>L05<br>L07 | I   | LVTTTL-5sp | <b>Telecom Bus 4 Transmit Input Data:</b><br>19.44 Mbytes/s AU-4 (transmit retiming turned off) or VC-4 (transmit retiming turned on) data input on these pins is inserted into the outgoing STM-1 #4. This data is clocked into the SONET/SDH framer on the rising edge of TXTB4CLK. Bit 7 is the MSB and is transmitted first.   |
| TXTB4CLK   | N03  | I   | LVTTTL-5sp | <b>Telecom Bus 4 Transmit Input Clock:</b><br>All of the signals for Telecom Bus 4 are clocked into the SONET/SDH framer on the rising edge of this 19.44 MHz clock. TXTB4CLK <b>must</b> be frequency locked to either TXCCLK or $\overline{\text{TXCCLK}}$ if transmit retiming is not performed.  |
| TXTB4C1J1  | N05  | I   | LVTTTL-5sd | <b>Telecom Bus 4 Transmit Input Slot Indication:</b><br>When the TXTB4SPE signal is high, TXTB4C1J1 indicates the position of the J1 byte. When the TXTB4SPE signal is low, TXTB4C1J1 indicates the position of the C1 byte. The J1 and C1 pulses are required if transmit retiming is turned on. If transmit retiming is turned off, this signal becomes a slot identifier. |
| TXTB4SPE   | N07  | I   | LVTTTL-5sd | <b>Telecom Bus 4 Transmit Input Synchronous Payload Envelope Signal:</b><br>This signal is high for the SPE bytes and low for the TOH bytes on Telecom Bus 4. If transmit retiming is turned off and no J1 pulse is present in TXTB4C1J1, this pin can be tied low.  |
| TXTB4PAR   | M02  | I   | LVTTTL-5sp | <b>Telecom Bus 4 Transmit Input Parity:</b><br>Parity for the signals of Telecom Bus 4. It should be calculated by the transmitting device according to the settings of the PFULL4, PEVEN4, and PENA4 control bits in the SONET/SDH framer. Parity errors are reported via the TB4PAR alarm bit, but no actions are taken.   |
| TXTB4FAIL  | M04  | I   | LVTTTL-5sp | <b>Telecom Bus 4 Transmit Input Failure Indication:</b><br>TXTB4FAIL indicates that a failure has occurred on the device transmitting on Telecom Bus 4. When TXTB4FAIL goes high, AIS-P is transmitted on STM-1 #4/STS-3c #4.  |
| RXCCLK   | W07  | I   |            | <b>No Connect:</b> Leave unconnected.  |
| RXCFRM   | T08  | I   |            | <b>No Connect:</b> Leave unconnected.  |
| 1. When STM-4c or STS-12c frames are processed, the four transmit and four receive Telecom Buses operate in parallel as two 32-bit wide Telecom Buses. |  |     |            |  |

**Telecom Bus Interface Pin Descriptions** (Sheet 4 of 6)

| Pin Name   | Pin No.  | I/O   | Type     | Pin Description <sup>1</sup>   |
|--|--|-------|----------|--|
| RXTB1DATA(7)<br>RXTB1DATA(6)<br>RXTB1DATA(5)<br>RXTB1DATA(4)<br>RXTB1DATA(3)<br>RXTB1DATA(2)<br>RXTB1DATA(1)<br>RXTB1DATA(0) | P02<br>P04<br>P06<br>P07<br>P08<br>R01<br>R02<br>R03 | O (T) | LVTTL-5s | <b>Telecom Bus 1 Receive Data:</b><br>SPE and TOH data from STM-1 #1/STS-3c #1 are output on these pins. Bit 7 is the MSB and was received first. Bit 0 is the LSB and was received last. All TOH and SPE data are passed out of the SONET/SDH framer and are not modified. The data on these pins is clocked out of the SONET/SDH framer on either the rising or falling edge of RXTB1CLK depending on the setting of the CKINV1 control bit.           |
| RXTB1CLK   | R05  | O (T) | LVTTL-5s | <b>Telecom Bus 1 Receive Clock:</b><br>All Telecom Bus 1 receive signals are clocked out of the SONET/SDH framer on the falling edge of RXTB1CLK when the CKINV1 control bit is set to '0'. If CKINV1 is set to '1', the Telecom Bus 1 receive signals are clocked out on the rising edge of RXTB1CLK. This clock is 19.44 MHz.  |
| RXTB1C1J1  | R07  | O (T) | LVTTL-5s | <b>Telecom Bus 1 Receive C1J1 Signal:</b><br>When the control bit C1POS is set to '1', this signal identifies the first C1 byte in the RXTB1DATA(7:0) stream when RXTB1C1J1 is high and RXTB1SPE is low, while the J1 byte in the RXTB1DATA(7:0) stream is identified when RXTB1C1J1 and RXTB1SPE are high. When C1POS is set to '0', RXTB1C1J1 goes high only during the last A2 byte time of the RXTB1DATA(7:0) signal.                                |
| RXTB1SPE   | T02  | O (T) | LVTTL-5s | <b>Telecom Bus 1 Receive SPE Signal:</b><br>RXTB1SPE is high during the SPE bytes of RXTB1DATA(7:0). If a pointer decrement occurs, RXTB1SPE will go high coincident with the three H3 bytes in RXTB1DATA(7:0). If a pointer increment occurs, RXTB1SPE will go low coincident with the three SPE bytes immediately after the H3 bytes of the RXTB1DATA(7:0) stream.   |
| RXTB1PAR   | T04  | O (T) | LVTTL-5s | <b>Telecom Bus 1 Receive Parity Signal:</b><br>Parity for the receive signals of Telecom Bus 1. It is calculated by the SONET/SDH framer according to the settings of the PFULL1, PEVEN1, and PENA1 control bits.  |
| RXTB1FAIL  | T06  | O (T) | LVTTL-5s | <b>Telecom Bus 1 Receive Failure Indication:</b><br>RXTB1FAIL goes high when the SONET/SDH framer detects errors that would cause an AIS-P to be generated in the receive STM-1 #1/STS-3c #1 signal. These alarms are: Loss of Pointer, or Path AIS, or Line AIS detected in STM-1 #1/STS-3c #1, or Loss of Clock or Loss of Data detected at the SONET/SDH framer's receive inputs. RXTB1FAIL will stay active as long as the failure condition exists. |
| RXTB2DATA(7)<br>RXTB2DATA(6)<br>RXTB2DATA(5)<br>RXTB2DATA(4)<br>RXTB2DATA(3)<br>RXTB2DATA(2)<br>RXTB2DATA(1)<br>RXTB2DATA(0) | T07<br>U01<br>U03<br>U05<br>U07<br>V02<br>V04<br>V05 | O (T) | LVTTL-5s | <b>Telecom Bus 2 Receive Data:</b><br>SPE and TOH data from STM-1 #2/STS-3c #2 are output on these pins. Bit 7 is the MSB and was received first. Bit 0 is the LSB and was received last. All TOH and SPE data are passed out of the SONET/SDH framer and are not modified. The data on these pins is clocked out of the SONET/SDH framer on either the rising or falling edge of RXTB2CLK depending on the setting of the CKINV2 control bit.           |
| RXTB2CLK   | V06  | O (T) | LVTTL-5s | <b>Telecom Bus 2 Receive Clock:</b><br>All Telecom Bus 2 receive signals are clocked out of the SONET/SDH framer on the falling edge of RXTB2CLK when the CKINV2 control bit is set to '0'. If CKINV2 is set to '1', the Telecom Bus 2 receive signals are clocked out on the rising edge of RXTB2CLK. This clock is 19.44 MHz.  |

1. When STM-4c or STS-12c frames are processed, the four transmit and four receive Telecom Buses operate in parallel as two 32-bit wide Telecom Buses.

## IBM SONET/SDH Framer

## Telecom Bus Interface Pin Descriptions (Sheet 5 of 6)

| Pin Name   | Pin No.  | I/O   | Type      | Pin Description <sup>1</sup>   |
|--|--|-------|-----------|--|
| RXTB2C1J1  | V07  | O (T) | LVTTTL-5s | <b>Telecom Bus 2 Receive C1J1 Signal:</b><br>When the control bit C2POS is set to '1', this signal identifies the first C1 byte in the RXTB2DATA(7:0) stream when RXTB2C1J1 is high and RXTB2SPE is low, while the J1 byte in RXTB2DATA(7:0) is identified when RXTB2C1J1 and RXTB2SPE are high. When C2POS is set to '0', RXTB2C1J1 goes high only during the last A2 byte time of RXTB2DATA(7:0).  |
| RXTB2SPE   | W01  | O (T) | LVTTTL-5s | <b>Telecom Bus 2 Receive SPE Signal:</b><br>RXTB2SPE is high during the SPE bytes of RXTB2DATA(7:0). If a pointer decrement occurs, RXTB2SPE will go high coincident with the three H3 bytes in RXTB2DATA(7:0). If a pointer increment occurs, RXTB2SPE will go low coincident with the three SPE bytes immediately after the H3 bytes of the RXTB2DATA(7:0) stream.   |
| RXTB2PAR   | W02  | O (T) | LVTTTL-5s | <b>Telecom Bus 2 Receive Parity Signal:</b><br>Parity for the receive signals of Telecom Bus 2. It is calculated by the SONET/SDH framer according to the settings of the PFULL2, PEVEN2, and PENA2 control bits.  |
| RXTB2FAIL  | W03  | O (T) | LVTTTL-5s | <b>Telecom Bus 2 Receive Failure Indication:</b><br>RXTB2FAIL goes high when the SONET/SDH framer detects errors that would cause an AIS-P to be generated in the receive STM-1 #2/STS-3c #2 signal. These alarms are: Loss of Pointer, or Path AIS, or Line AIS detected in STM-1 #2/STS-3c #2, or Loss of Clock or Loss of Data detected at the SONET/SDH framer's receive inputs. RXTB2FAIL will stay active as long as the failure condition exists. |
| RXTB3DATA(7)<br>RXTB3DATA(6)<br>RXTB3DATA(5)<br>RXTB3DATA(4)<br>RXTB3DATA(3)<br>RXTB3DATA(2)<br>RXTB3DATA(1)<br>RXTB3DATA(0) | W05<br>Y01<br>Y02<br>Y03<br>Y04<br>Y05<br>AA01<br>AA03 | O (T) | LVTTTL-5s | <b>Telecom Bus 3 Receive Data:</b><br>SPE and TOH data from STM-1 #3/STS-3c #3 are output on these pins. Bit 7 is the MSB and was received first. Bit 0 is the LSB and was received last. All TOH and SPE data are passed out of the SONET/SDH framer and are not modified. The data on these pins is clocked out of the SONET/SDH framer on either the rising or falling edge of RXTB3CLK depending on the setting of the CKINV3 control bit.           |
| RXTB3CLK   | AB01   | O (T) | LVTTTL-5s | <b>Telecom Bus 3 Receive Clock:</b><br>All Telecom Bus 3 receive signals are clocked out of the SONET/SDH framer on the falling edge of RXTB3CLK when the CKINV3 control bit is set to '0'. If CKINV3 is set to '1', the Telecom Bus 3 receive signals are clocked out on the rising edge of RXTB3CLK. This clock is 19.44 MHz.  |
| RXTB3C1J1  | AB02   | O (T) | LVTTTL-5s | <b>Telecom Bus 3 Receive C1J1 Signal:</b><br>When the control bit C3POS is set to '1', this signal identifies the first C1 byte in the RXTB3DATA(7:0) stream when RXTB3C1J1 is high and RXTB3SPE is low, while the J1 byte in RXTB3DATA(7:0) is identified when RXTB3C1J1 and RXTB3SPE are high. When C3POS is set to '0', RXTB3C1J1 goes high only during the last A2 byte time of RXTB3DATA(7:0).  |
| RXTB3SPE   | AB03   | O (T) | LVTTTL-5s | <b>Telecom Bus 3 Receive SPE Signal:</b><br>RXTB3SPE is high during the SPE bytes of RXTB3DATA(7:0). If a pointer decrement occurs, RXTB3SPE will go high coincident with the three H3 bytes in RXTB3DATA(7:0). If a pointer increment occurs, RXTB3SPE will go low coincident with the three SPE bytes immediately after the H3 bytes of the RXTB3DATA(7:0) stream.   |

1. When STM-4c or STS-12c frames are processed, the four transmit and four receive Telecom Buses operate in parallel as two 32-bit wide Telecom Buses.

**Telecom Bus Interface Pin Descriptions** (Sheet 6 of 6)

| Pin Name   | Pin No.  | I/O   | Type     | Pin Description <sup>1</sup>   |
|--|--|-------|----------|--|
| RXTB3PAR   | AC01   | O (T) | LVTTL-5s | <b>Telecom Bus 3 Receive Parity Signal:</b><br>Parity for the receive signals of Telecom Bus 3. It is calculated by the SONET/SDH framer according to the settings of the PFULL3, PEVEN3, and PENA3 control bits.  |
| RXTB3FAIL  | AC02   | O (T) | LVTTL-5s | <b>Telecom Bus 3 Receive Failure Indication:</b><br>RXTB3FAIL goes high when the SONET/SDH framer detects errors that would cause an AIS-P to be generated in the receive STM-1 #3/STS-3c #3 signal. These alarms are: Loss of Pointer, or Path AIS, or Line AIS detected in STM-1 #3/STS-3c #3, or Loss of Clock or Loss of Data detected at the SONET/SDH framer's receive inputs. RXTB3FAIL will stay active as long as the failure condition exists. |
| RXTB4DATA(7)<br>RXTB4DATA(6)<br>RXTB4DATA(5)<br>RXTB4DATA(4)<br>RXTB4DATA(3)<br>RXTB4DATA(2)<br>RXTB4DATA(1)<br>RXTB4DATA(0) | AD01<br>AE02<br>AD02<br>AE03<br>AD03<br>AC03<br>AE04<br>AD04 | O (T) | LVTTL-5s | <b>Telecom Bus 4 Receive Data:</b><br>SPE and TOH data from STM-1 #4/STS-3c #4 are output on these pins. Bit 7 is the MSB and was received first. Bit 0 is the LSB and was received last. All TOH and SPE data are passed out of the SONET/SDH framer and are not modified. The data on these pins is clocked out of the SONET/SDH framer on either the rising or falling edge of RXTB4CLK depending on the setting of the CKINV4 control bit.           |
| RXTB4CLK   | AB04   | O (T) | LVTTL-5s | <b>Telecom Bus 4 Receive Clock:</b><br>All Telecom Bus 4 receive signals are clocked out of the SONET/SDH framer on the falling edge of RXTB4CLK when the CKINV4 control bit is set to '0'. If CKINV4 is set to '1', the Telecom Bus 4 receive signals are clocked out on the rising edge of RXTB4CLK. This clock is 19.44 MHz.  |
| RXTB4C1J1  | AA04   | O (T) | LVTTL-5s | <b>Telecom Bus 4 Receive C1J1 Signal:</b><br>When the control bit C4POS is set to '1', this signal identifies the first C1 byte in the RXTB4DATA(7:0) stream when RXTB4C1J1 is high and RXTB4SPE is low, while the J1 byte in RXTB4DATA(7:0) is identified when RXTB4C1J1 and RXTB4SPE are high. When C4POS is set to '0', RXTB4C1J1 goes high only during the last A2 byte time of RXTB4DATA(7:0).  |
| RXTB4SPE   | AB05   | O (T) | LVTTL-5s | <b>Telecom Bus 4 Receive SPE Signal:</b><br>RXTB4SPE is high during the SPE bytes of RXTB4DATA(7:0). If a pointer decrement occurs, RXTB4SPE will go high coincident with the three H3 bytes in RXTB4DATA(7:0). If a pointer increment occurs, RXTB4SPE will go low coincident with the three SPE bytes immediately after the H3 bytes of the RXTB4DATA(7:0) stream.   |
| RXTB4PAR   | AA05   | O (T) | LVTTL-5s | <b>Telecom Bus 4 Receive Parity Signal:</b><br>Parity for the receive signals of Telecom Bus 4. It is calculated by the SONET/SDH framer according to the settings of the PFULL4, PEVEN4, and PENA4 control bits.  |
| RXTB4FAIL  | Y06  | O (T) | LVTTL-5s | <b>Telecom Bus 4 Receive Failure Indication:</b><br>RXTB4FAIL goes high when the SONET/SDH framer detects errors that would cause an AIS-P to be generated in the receive STM-1 #4/STS-3c #4 signal. These alarms are: Loss of Pointer, or Path AIS, or Line AIS detected in STM-1 #4/STS-3c #4, or Loss of Clock or Loss of Data detected at the SONET/SDH framer's receive inputs. RXTB4FAIL will stay active as long as the failure condition exists. |

1. When STM-4c or STS-12c frames are processed, the four transmit and four receive Telecom Buses operate in parallel as two 32-bit wide Telecom Buses.



IBM SONET/SDH Framer

GPP Interface Pin Descriptions (Sheet 1 of 2)

| Pin Name   | Pin No.  | I/O     | Type       | Pin Description   |
|--|--|---------|------------|---|
| GPPCLK   | AE11   | I       | LVTTTL-5sp | <p><b>GPP Clock:</b><br/>                     Clock for the GPP interface in the SONET/SDH framer. This clock is always required, regardless of whether an asynchronous or synchronous interface is selected via the INTFMODE pin. When an asynchronous type interface is selected, this clock can have a maximum frequency of 50 MHz. When a synchronous interface is selected, this clock can have a maximum frequency of 33.3 MHz. All signals are transferred on the falling edge of this clock when the synchronous interface is selected. The lowest frequency that this clock can have is either 10 MHz or the frequency of the microprocessor clock, whichever is higher.</p> |
| GPDATA(7)<br>GPDATA(6)<br>GPDATA(5)<br>GPDATA(4)<br>GPDATA(3)<br>GPDATA(2)<br>GPDATA(1)<br>GPDATA(0)   | AE17<br>AD17<br>AC17<br>AB17<br>AE18<br>AD18<br>AC18<br>AB18   | I/O (T) | LVTTTL-5f  | <p><b>GPP Data: (True)</b><br/>                     Bidirectional bus for data to/from the SONET/SDH framer GPP interface. Bit 0 is the LSB.</p>  |
| GPADDR(13)<br>GPADDR(12)<br>GPADDR(11)<br>GPADDR(10)<br>GPADDR(9)<br>GPADDR(8)<br>GPADDR(7)<br>GPADDR(6)<br>GPADDR(5)<br>GPADDR(4)<br>GPADDR(3)<br>GPADDR(2)<br>GPADDR(1)<br>GPADDR(0) | Y13<br>AE14<br>AC14<br>AB14<br>Y14<br>AD15<br>AB15<br>AA15<br>Y15<br>AE16<br>AD16<br>AB16<br>AA16<br>Y16 | I       | LVTTTL-5s  | <p><b>GPP Address:</b><br/>                     The 14-bit address of the register or GRA location within the SONET/SDH framer that is to be read or written. Bit 0 is the LSB.</p>   |
| GPR $\overline{W}$ , GP $\overline{WR}$  | AE12   | I       | LVTTTL-5sp | <p><b>GPP Read/Write [R<math>\overline{W}</math>] (Motorola Mode) or Write [WR] (Intel Mode):</b><br/>                     Data transfer control signal.</p> <p><b>Motorola Mode:</b> This signal is high during a data read operation and low for a data write operation. A low enables data from the GPDATA(7:0) bus to be written into the addressed location. A high enables data to be read from the addressed location.</p> <p><b>Intel Mode:</b> This signal is high during a data read operation and low for a data write operation. A low enables data from the GPDATA(7:0) bus to be written into the addressed location.</p>   |
| GP $\overline{DS}$ , GP $\overline{RD}$  | AD13   | I       | LVTTTL-5sp | <p><b>GPP Data Strobe [DS] (Motorola Mode) or Read [RD] (Intel Mode):</b><br/>                     (Active low)</p> <p><b>Motorola Mode:</b> When asserted low during a read cycle, this signal indicates that the SONET/SDH framer is to put data out on the GPDATA(7:0) bus. When asserted low during a write cycle, this signal tells the SONET/SDH framer that there is valid data on the GPDATA(7:0) bus.</p> <p><b>Intel Mode:</b> This signal is high during a data write operation and low during a data read operation. A low enables data to be read from the addressed location.</p>   |

**GPP Interface Pin Descriptions** (Sheet 2 of 2)

| Pin Name  | Pin No. | I/O   | Type       | Pin Description   |
|---|---------|-------|------------|---|
| $\overline{\text{GPDTACK}}$ , $\overline{\text{GPRDY}}$ | Y12     | O (T) | LVTTTL-5sp | <p><b>Data Acknowledge [<math>\overline{\text{DTACK}}</math>] (Motorola Mode) or Ready [<math>\overline{\text{RDY}}</math>] (Intel Mode):</b> (Active low)<br/>Tri-state acknowledge signal.</p> <p>For either Intel or Motorola mode this signal is asserted low to tell the external microprocessor that it can end the bus cycle. An external 1-3 k<math>\Omega</math> pull-up resistor is required for this pin to ensure that the <math>\overline{\text{GPDTACK}}</math>, <math>\overline{\text{GPRDY}}</math> pin is pulled to its inactive state in a timely manner in order to avoid functional problems.</p> |
| $\overline{\text{GPSEL}}$                               | AB13    | I     | LVTTTL-5sp | <p><b>SONET/SDH framer Chip Select:</b><br/>Enable signal used to validate the address bus for read and write transfers to this particular SONET/SDH framer.</p>  |
| $\overline{\text{GPINT}}$                               | W15     | O (T) | LVTTTL-5sp | <p><b>Interrupt:</b><br/>Interrupt to microprocessor. For either Intel or Motorola mode, <math>\overline{\text{GPINT}}</math> is an active low output. In the inactive state this output is tri-stated. An external 1-3 k<math>\Omega</math> pull-up resistor is required for this pin to ensure that the <math>\overline{\text{GPINT}}</math> pin is pulled to its inactive state in a timely manner in order to avoid functional problems.</p>  |
| INTFMODE  | AD19    | I     | LVTTTL-5sd | <p><b>Interface Mode:</b><br/>Selects the mode of operation of the microprocessor interface.<br/>INTFMODE is set high for synchronous mode.<br/>INTFMODE is set low for asynchronous mode.</p>  |
| INTFSELECT  | W13     | I     | LVTTTL-5sd | <p><b>Interface Select:</b><br/>Selects the type of microprocessor interface.<br/>INTFSELECT is set high for the Intel microprocessor interface.<br/>INTFSELECT is set low for the Motorola microprocessor interface.</p>   |



IBM SONET/SDH Framer

Serial DCC Interface Pin Descriptions (Sheet 1 of 2)

| Pin Name | Pin No. | I/O | Type      | Pin Description  |
|----------|---------|-----|-----------|--|
| T1DATA1  | AC19    | I   | LVTTL-5sd | <b>DCC Transmit Data 1:</b><br>Bit-serial data from LAPD interface controller or similar device to SONET/SDH macro 1 in the SONET/SDH framer. This data can optionally be provided to either the D1-D3 or D4-D12 bytes in STM-1 #1/STS-3c #1 as selected by a control bit. The data on this pin is sampled with the T1DCLK1 clock.   |
| T1DATA2  | AB19    | I   | LVTTL-5sd | <b>DCC Transmit Data 2:</b><br>Bit-serial data from LAPD interface controller or similar device to SONET/SDH macro 2 in the SONET/SDH framer. This data can optionally be provided to either the D1-D3 or D4-D12 bytes in STM-1 #2/STS-3c #2 as selected by a control bit. The data on this pin is sampled with the T1DCLK2 clock.   |
| T1DATA3  | AA19    | I   | LVTTL-5sd | <b>DCC Transmit Data 3:</b><br>Bit-serial data from LAPD interface controller or similar device to SONET/SDH macro 3 in the SONET/SDH framer. This data can optionally be provided to either the D1-D3 or D4-D12 bytes in STM-1 #3/STS-3c #3 as selected by a control bit. The data on this pin is sampled with the T1DCLK3 clock.   |
| T1DATA4  | Y19     | I   | LVTTL-5sd | <b>DCC Transmit Data 4:</b><br>Bit-serial data from LAPD interface controller or similar device to SONET/SDH macro 4 in the SONET/SDH framer. This data can optionally be provided to either the D1-D3 or D4-D12 bytes in STM-1 #4/STS-3c #4 as selected by a control bit. The data on this pin is sampled with the T1DCLK4 clock.   |
| T1DCLK1  | AA07    | O   | LVTTL-5sd | <b>DCC Transmit Clock 1:</b><br>The signals on T1DATA1 are sampled with this clock. This is a bit clock for clocking either the D1-D3 or the D4-D12 DCC data bytes out of an external LAPD controller or similar device into macro 1 of the SONET/SDH framer. The clock edge used for data sampling is selectable via a control bit. |
| T1DCLK2  | AA09    | O   | LVTTL-5sd | <b>DCC Transmit Clock 2:</b><br>The signals on T1DATA2 are sampled with this clock. This is a bit clock for clocking either the D1-D3 or the D4-D12 DCC data bytes out of an external LAPD controller or similar device into macro 2 of the SONET/SDH framer. The clock edge used for data sampling is selectable via a control bit. |
| T1DCLK3  | AA11    | O   | LVTTL-5sd | <b>DCC Transmit Clock 3:</b><br>The signals on T1DATA3 are sampled with this clock. This is a bit clock for clocking either the D1-D3 or the D4-D12 DCC data bytes out of an external LAPD controller or similar device into macro 3 of the SONET/SDH framer. The clock edge used for data sampling is selectable via a control bit. |
| T1DCLK4  | AA13    | O   | LVTTL-5sd | <b>DCC Transmit Clock 4:</b><br>The signals on T1DATA4 are sampled with this clock. This is a bit clock for clocking either the D1-D3 or the D4-D12 DCC data bytes out of an external LAPD controller or similar device into macro 4 of the SONET/SDH framer. The clock edge used for data sampling is selectable via a control bit. |
| R1DATA1  | AC09    | O   | LVTTL-5sd | <b>DCC Receive Data 1:</b><br>Bit-serial D1-D3 or D4-D12 data from macro 1 of the SONET/SDH framer to an external LAPD controller device. The data on this pin is output with the R1DCLK1 clock.   |
| R1DATA2  | AC11    | O   | LVTTL-5sd | <b>DCC Receive Data 2:</b><br>Bit-serial D1-D3 or D4-D12 data from macro 2 of the SONET/SDH framer to an external LAPD controller device. The data on this pin is output with the R1DCLK2 clock.   |

**Serial DCC Interface Pin Descriptions** (Sheet 2 of 2)

| Pin Name | Pin No. | I/O | Type      | Pin Description   |
|----------|---------|-----|-----------|---|
| R1DATA3  | AC13    | O   | LVTTL-5sd | <b>DCC Receive Data 3:</b><br>Bit-serial D1-D3 or D4-D12 data from macro 3 of the SONET/SDH framer to an external LAPD controller device. The data on this pin is output with the R1DCLK3 clock.  |
| R1DATA4  | AC15    | O   | LVTTL-5sd | <b>DCC Receive Data 4:</b><br>Bit-serial D1-D3 or D4-D12 data from macro 4 of the SONET/SDH framer to an external LAPD controller device. The data on this pin is output with the R1DCLK4 clock.  |
| R1DCLK1  | AE07    | O   | LVTTL-5sd | <b>DCC Receive Clock 1:</b><br>A bit clock from the SONET/SDH framer for clocking the data on the R1DATA1 pin into an external LAPD controller or similar device. The clock edge used for output of the R1DATA1 signal is selectable via a control bit. |
| R1DCLK2  | AE09    | O   | LVTTL-5sd | <b>DCC Receive Clock 2:</b><br>A bit clock from the SONET/SDH framer for clocking the data on the R1DATA2 pin into an external LAPD controller or similar device. The clock edge used for output of the R1DATA2 signal is selectable via a control bit. |
| R1DCLK3  | AE13    | O   | LVTTL-5sd | <b>DCC Receive Clock 3:</b><br>A bit clock from the SONET/SDH framer for clocking the data on the R1DATA3 pin into an external LAPD controller or similar device. The clock edge used for output of the R1DATA3 signal is selectable via a control bit. |
| R1DCLK4  | AE15    | O   | LVTTL-5sd | <b>DCC Receive Clock 4:</b><br>A bit clock from the SONET/SDH framer for clocking the data on the R1DATA4 pin into an external LAPD controller or similar device. The clock edge used for output of the R1DATA4 signal is selectable via a control bit. |

## IBM SONET/SDH Framer

## APS Interface Pin Descriptions

| Pin Name  | Pin No.   | I/O   | Type       | Pin Description   |
|---|---|---|------------|---|
| TXAPSDAT(8)<br>TXAPSDAT(7)<br>TXAPSDAT(6)<br>TXAPSDAT(5)<br>TXAPSDAT(4)<br>TXAPSDAT(3)<br>TXAPSDAT(2)<br>TXAPSDAT(1)<br>TXAPSDAT(0) | R13<br>R15<br>P12<br>P13<br>P14<br>N11<br>N13<br>N15<br>M12 | I/O (T)<br>I/O (T)<br>I/O (T)<br>I/O (T)<br>I/O (T)<br>I/O (T)<br>I/O (T)<br>I/O (T)<br>I/O (T) | LVTTTL-5sd | <b>Transmit APS Data:</b> Bit 0 is the LSB. This is a bidirectional port. When the SONET/SDH framer is configured to output data on the transmit APS interface, these pins are outputs. When the SONET/SDH framer is configured to accept data from the transmit APS interface, these pins are inputs. This data bus is used to pass transmit C-4 (VC-4) data from one SONET/SDH framer to another.   |
| TXAPSPAR  | M13   | I/O (T)   | LVTTTL-5sd | <b>Transmit APS Parity:</b> This is a bidirectional pin. When the SONET/SDH framer is configured to output data on the transmit APS interface, this pin is an output and provides parity for the TXAPSDAT(8:0) bus. When the SONET/SDH framer is configured to accept data from the transmit APS interface, this pin is an input and accepts parity from the SONET/SDH framer that is driving the transmit APS interface.   |
| TXAPSDAVA   | M14   | I/O (T)   | LVTTTL-5sd | <b>Transmit APS Provided Data Valid:</b> This is a bidirectional pin. When the SONET/SDH framer is configured to output data on the transmit APS interface, this pin is an output and indicates when data on the TXAPSDAT(8:0) bus is valid. A high means that data is valid on the considered clock edge. A low means that data is not valid. When the SONET/SDH framer is configured to accept data from the transmit APS interface, this pin is an input and tells the SONET/SDH framer if the data being received on the TXAPSDAT(8:0) bus is valid or not. A high means that data is valid on the considered clock edge. A low means that data is not valid. |
| TXAPSDARQ   | L11   | I/O (T)   | LVTTTL-5sd | <b>Transmit APS Data Request:</b> This is a bidirectional pin. When the SONET/SDH framer is configured to output data on the transmit APS interface, this pin is an input and tells the SONET/SDH framer that one of the other connected SONET/SDH framers is requesting data. A high means that data is being requested. A low means that no data is requested. When the SONET/SDH framer is configured to accept data from the transmit APS interface, this pin is an output and indicates that this SONET/SDH framer is requesting data. A high means that data is being requested. A low means that no data is requested.                                     |
| RXAPSDAT(8)<br>RXAPSDAT(7)<br>RXAPSDAT(6)<br>RXAPSDAT(5)<br>RXAPSDAT(4)<br>RXAPSDAT(3)<br>RXAPSDAT(2)<br>RXAPSDAT(1)<br>RXAPSDAT(0) | L13<br>L15<br>K11<br>K12<br>K13<br>K14<br>J13<br>J15<br>H14 | I/O (T)<br>I/O (T)<br>I/O (T)<br>I/O (T)<br>I/O (T)<br>I/O (T)<br>I/O (T)<br>I/O (T)<br>I/O (T) | LVTTTL-5sd | <b>Receive APS Data:</b> Bit 0 is the LSB. This is a bidirectional port. When the SONET/SDH framer is configured to output data on the receive APS interface, these pins are outputs. When the SONET/SDH framer is configured to accept data from the receive APS interface, these pins are inputs. This data bus is used to pass receive C-4 (VC-4) data from one SONET/SDH framer to another.   |
| RXAPSPAR  | H15   | I/O (T)   | LVTTTL-5sd | <b>Receive APS Parity:</b> This is a bidirectional pin. When the SONET/SDH framer is configured to output data on the receive APS interface, this pin is an output and provides parity for the RXAPSDAT(8:0) bus. When the SONET/SDH framer is configured to accept data from the receive APS interface, this pin is an input and accepts parity from the SONET/SDH framer that is driving the receive APS interface.   |
| RXAPSDAVA   | G15   | I/O (T)   | LVTTTL-5sd | <b>Receive APS Provided Data Valid:</b> This is a bidirectional pin. When the SONET/SDH framer is configured to output data on the receive APS interface, this pin is an output and indicates when data on the RXAPSDAT(8:0) bus is valid. A high means that data is valid on the considered clock edge. A low means that data is not valid. When the SONET/SDH framer is configured to accept data from the receive APS interface, this pin is an input and tells the SONET/SDH framer if the data being received on the RXAPSDAT(8:0) bus is valid or not. A high means that data is valid on the considered clock edge. A low means that data is not valid.    |

## Expansion Interface Pin Descriptions

| Pin Name | Pin No. | I/O | Type      | Pin Description  |
|----------|---------|-----|-----------|--|
| TXEXPIN  | R09     | I   | LVTTL-5sd | <b>Expansion Interface Control:</b> Control pin for Expansion interface. This pin is used for STM-16/STS-48 operation. |
| TXEXPOUT | R11     | O   | LVTTL-5sd | <b>Expansion Interface Control:</b> Control pin for Expansion interface. This pin is used for STM-16/STS-48 operation. |
| RXEXPIN  | T12     | I   | LVTTL-5sd | <b>Expansion Interface Control:</b> Control pin for Expansion interface. This pin is used for STM-16/STS-48 operation. |
| RXEXPOUT | U13     | O   | LVTTL-5sd | <b>Expansion Interface Control:</b> Control pin for Expansion interface. This pin is used for STM-16/STS-48 operation. |
| TXFRMIN  | T13     | I   | LVTTL-5sd | <b>Expansion Interface Control:</b> Control pin for Expansion interface. This pin is used for STM-16/STS-48 operation. |
| TXFRMOUT | T14     | O   | LVTTL-5fd | <b>Expansion Interface Control:</b> Control pin for Expansion interface. This pin is used for STM-16/STS-48 operation. |

## Ring Port Interface Pin Descriptions

| Pin Name  | Pin No. | I/O | Type      | Pin Description   |
|-----------|---------|-----|-----------|---|
| TXRINGCLK | V13     | I   | LVTTL-5sd | <b>Transmit Ring Port Clock Input:</b> This signal is connected to the RXRINGCLK output of a mating SONET/SDH framer. TXRINGD is clocked into the SONET/SDH framer on the rising edge of this 19.44 MHz clock.  |
| TXRINGD   | V12     | I   | LVTTL-5sd | <b>Transmit Ring Port Data Input:</b> A serial input that is connected to a mating SONET/SDH framer's RXRINGD signal to allow communication of the debounced K1, K2 and K3 bytes, Path REI and 3-Bit Path RDI, Line RDI and Line REI, New K3 Indication, and New APS Indication for all four STM-1/STS-3cs or STM-4c/STS-12c to facilitate Ring mode operation. The data on this pin is clocked into the SONET/SDH framer on the rising edge of the TXRINGCLK signal. |
| RXRINGCLK | V15     | O   | LVTTL-5sd | <b>Receive Ring Port Clock Output:</b> RXRINGD is output on the falling edge of this 19.44 MHz clock, which is derived from the Transmit Line Reference Clock.  |
| RXRINGD   | V14     | O   | LVTTL-5sd | <b>Receive Ring Port Data Output:</b> A serial output that provides the debounced K1, K2, and K3 bytes, Path REI and 3-Bit Path RDI, Line RDI and Line REI, New K3 Indication, and New APS Indication for all four STM-1/STS-3cs or STM-4c/STS-12c to facilitate Ring mode operation. A start sequence and an address field is used to delineate the information contained on this signal output. RXRINGD is output on the falling edge of RXRINGCLK.                 |

## IBM SONET/SDH Framer

## Miscellaneous Pin Descriptions

| Pin Name  | Pin No.                         | I/O                   | Type      | Pin Description  |
|---|---------------------------------|-----------------------|-----------|--|
| ALARM1(0)<br>ALARM1(1)<br>ALARM1(2)<br>ALARM1(3)<br>ALARM1(4) | H01<br>H03<br>K01<br>K03<br>K05 | O<br>O<br>O<br>O<br>O | LVTTL-5sd | <p><b>Alarm Pins for Receive Macro 1:</b></p> <p>The ALARM1(0:4) outputs are controlled real time by the same internal control signals that also cause the corresponding microprocessor interrupt. The alarm conditions that are output on these pins are as follows:</p> <p>ALARM1(0) = Loss of Signal in Macro 1<br/> ALARM1(1) = Loss of Frame in Macro 1<br/> ALARM1(2) = Loss of Pointer in Macro 1<br/> ALARM1(3) = Path AIS in Macro 1<br/> ALARM1(4) = Line AIS in Macro 1</p> |
| ALARM2(0)<br>ALARM2(1)<br>ALARM2(2)<br>ALARM2(3)<br>ALARM2(4) | M01<br>M03<br>P01<br>P03<br>P05 | O<br>O<br>O<br>O<br>O | LVTTL-5sd | <p><b>Alarm Pins for Receive Macro 2:</b></p> <p>The ALARM2(0:4) outputs are controlled real time by the same internal control signals that also cause the corresponding microprocessor interrupt. The alarm conditions that are output on these pins are as follows:</p> <p>ALARM2(0) = Loss of Signal in Macro 2<br/> ALARM2(1) = Loss of Frame in Macro 2<br/> ALARM2(2) = Loss of Pointer in Macro 2<br/> ALARM2(3) = Path AIS in Macro 2<br/> ALARM2(4) = Line AIS in Macro 2</p> |
| ALARM3(0)<br>ALARM3(1)<br>ALARM3(2)<br>ALARM3(3)<br>ALARM3(4) | T01<br>T03<br>T05<br>C05<br>E07 | O<br>O<br>O<br>O<br>O | LVTTL-5sd | <p><b>Alarm Pins for Receive Macro 3:</b></p> <p>The ALARM3(0:4) outputs are controlled real time by the same internal control signals that also cause the corresponding microprocessor interrupt. The alarm conditions that are output on these pins are as follows:</p> <p>ALARM3(0) = Loss of Signal in Macro 3<br/> ALARM3(1) = Loss of Frame in Macro 3<br/> ALARM3(2) = Loss of Pointer in Macro 3<br/> ALARM3(3) = Path AIS in Macro 3<br/> ALARM3(4) = Line AIS in Macro 3</p> |
| ALARM4(0)<br>ALARM4(1)<br>ALARM4(2)<br>ALARM4(3)<br>ALARM4(4) | J11<br>L09<br>M10<br>N09<br>P10 | O<br>O<br>O<br>O<br>O | LVTTL-5sd | <p><b>Alarm Pins for Receive Macro 4:</b></p> <p>The ALARM4(0:4) outputs are controlled real time by the same internal control signals that also cause the corresponding microprocessor interrupt. The alarm conditions that are output on these pins are as follows:</p> <p>ALARM4(0) = Loss of Signal in Macro 4<br/> ALARM4(1) = Loss of Frame in Macro 4<br/> ALARM4(2) = Loss of Pointer in Macro 4<br/> ALARM4(3) = Path AIS in Macro 4<br/> ALARM4(4) = Line AIS in Macro 4</p> |

## Analog SIM Input/Output Pin Descriptions

| Pin Name           | Pin No.    | I/O    | Type | Pin Description   |
|--------------------|------------|--------|------|---|
| RXCAP1P<br>RXCAP1N | G17<br>G18 | I<br>I |      | <b>On-Board Capacitor for Receive PLL 1:</b><br>Reserved for test purposes. These pins must be left unconnected.    |
| RXCAP2P<br>RXCAP2N | L17<br>L18 | I<br>I |      | <b>On-Board Capacitor for Receive PLL 2:</b><br>Reserved for test purposes. These pins must be left unconnected.    |
| RXCAP3P<br>RXCAP3N | R17<br>R18 | I<br>I |      | <b>On-Board Capacitor for Receive PLL 3:</b><br>Reserved for test purposes. These pins must be left unconnected.    |
| RXCAP4P<br>RXCAP4N | W17<br>W18 | I<br>I |      | <b>On-Board Capacitor for Receive PLL 4:</b><br>Reserved for test purposes. These pins must be left unconnected.    |
| TXCAPP<br>TXCAPN   | H16<br>J17 | I<br>I |      | <b>On-Board Capacitor for the Transmit PLL:</b><br>Reserved for test purposes. These pins must be left unconnected. |
| SDATOUT            | F19        | O      |      | <b>Test Pin:</b> This pin must be left unconnected.   |
| RCLK00             | F17        | O      |      | <b>Test Pin:</b> This pin must be left unconnected.   |
| VCEXT              | N17        | O      |      | <b>Test Pin:</b> This pin must be left unconnected.   |
| IREFTTEST          | F16        | O      |      | <b>Test Pin:</b> This pin must be left unconnected.   |

## Power and Ground Pin Descriptions

| Pin Name | Pin Number  | Pin Description  |
|----------|---|--|
| GND      | A19, B06, B10, B14, E02, E08, E12, E18, G06, G10, G14, J04, J08, J12, J16, L06, L10, L14, N04, N08, N10, N12, N16, R06, R10, R14, U04, U08, U12, U16, W06, W10, W14, AA02, AA08, AA12, AA18, AD06, AD10, AD14, AE01, AE19 | <b>Ground:</b> 0 volt reference.   |
| VDD      | E06, E14, G08, G12, J02, J10, J18, L04, L16, M09, M11, N06, N14, P09, P11, R04, R16, U02, U10, U18, W08, W12, AA06, AA14  | <b>+3.3 V ± 5%</b> power supply (for logic section of SONET/SDH framer).   |
| VDD2     | C04, C08, C12, C16, E10, G04, G16, J06, J14, L08, L12, N02, N18, R08, R12, U06, U14, W04, W16, AA10, AC04, AC08, AC12, AC16   | <b>+3.3 V ± 5%</b> power supply (for analog circuits, PLLs). This supply should be filtered very carefully (max. ripple 5 mVpp) since the quality of this voltage determines the jitter performance of the PLLs. Use of a linear regulator is <b>mandatory</b> . |

## Electrical and Thermal Characteristics

### Absolute Maximum Ratings and Environmental Limitations

| Symbol            | Parameter  | Min  | Max      | Unit   | Notes |
|-------------------|--|------|----------|--------|-------|
| $V_{DD}, V_{DD2}$ | Supply Voltage   | 3.0  | 3.6      | V      | 1, 4  |
| $V_{IN1}$         | Input Voltage (LVTTTL)   | -0.6 | 5.5      | V      | 1, 3  |
| $V_{IN2}$         | Input Voltage (LPECL/PPECL)  | 0.0  | $V_{DD}$ | V      | 1     |
| $T_S$             | Storage Temperature  | -40  | 125      | °C     | 1     |
| $T_A$             | Ambient Operating Temperature Range (0 ft/min linear airflow)        | -40  | 85       | °C     |       |
| TI                | Component Temperature x Time   |      | 240 x 60 | °C x s | 1, 5  |
| ME                | Moisture Exposure Level (JEDEC A112 level 2)                         |      | 2        | Level  |       |
| RH                | Relative Humidity, during assembly up to 1 year (JEDEC A112 level 2) | 5    | 60       | %      | 2     |
| RH                | Relative Humidity, in-circuit non-condensing                         | 8    | 80       | %      |       |
|                   | Relative Humidity, shipment  | --   | --       | %      | 6     |
| ESD               | ESD Classification (JEDEC class 2)                                   |      | 3        | kV     |       |

1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Refer to the instructions on the "CAUTION" label on the dry-pack bag in which devices are supplied.
3. For this parameter, maximum value applies to overshoot; minimum value applies to undershoot.
4. Precautions have to be taken on the board to apply  $V_{DD}$  and  $V_{DD2}$  simultaneously.
5. This is the maximum temperature and duration that this maximum temperature can be applied to the SONET/SDH framer module during solder reflow on a printed circuit board before the SONET/SDH framer module is damaged. See also Temperature Limitations / Board Processing on page 51.
6. Drypack required for shipment.

## Temperature Limitations / Board Processing

The following limitations apply to CBGA-DLA packages:

1. Maximum number of thermal cycles above a particular temperature are cumulative (that is, 1 cycle above 250 °C is also 1 cycle above 220 °C). Five reflow cycles are designated to board processing.
2. The temperature profile limitations during board assembly and rework reflow operations are:
  - a. Maximum temperature: 260 °C (for one reflow only);
  - b. Maximum time above 250 °C: 30 seconds (for one reflow only);
  - c. Maximum temperature for reflows post one 260 °C reflow: 240 °C;
  - d. Maximum time above 220 °C: 60 seconds/cycle (5 cycles maximum);
  - e. Maximum time above 183 °C: 240 seconds/cycle (5 cycles maximum).
3. Double-sided two-pass assembly is permitted subject to the maximum thermal reflow count.
4. Double-sided two-pass assembly where the second pass is wave solder does not count as a reflow, provided thermal exposure is less than 183 °C.

## Thermal Characteristics

| Symbol        | Parameter   | Min | Typ | Max  | Unit |
|---------------|---|-----|-----|------|------|
| $\theta_{JA}$ | Thermal Resistance - junction to ambient<br>0 ft/min linear airflow |     | 9.1 | 11.6 | °C/W |

## Power Requirements

| Symbol   | Parameter                                       | Min  | Typ  | Max  | Unit | Notes |
|----------|---|------|------|------|------|-------|
| $V_{DD}$ | Supply Voltage                                  | 3.15 | 3.30 | 3.45 | V    | 1     |
| $I_{DD}$ | Supply Current - 4 x STS-3c/STM-1               |      |      | 1.34 | A    | 1     |
| $P_{DD}$ | Power Dissipation - 4 x STS-3c/STM-1            |      | 4.1  | 4.62 | W    | 1, 2  |
| $I_{DD}$ | Supply Current - STS-12/STS-12c/STM-4/STM-4c    |      |      | 1.06 | A    | 1     |
| $P_{DD}$ | Power Dissipation - STS-12/STS-12c/STM-4/STM-4c |      | 3.3  | 3.67 | W    | 1     |

1. Power measurements are for either Telecom Bus mode or ATM/PPP mode but not both. Furthermore, if the Telecom Bus is not used, the receive Telecom Bus outputs should be tri-stated.
2. A heat sink or airflow is required for 4 x STS-3c/STM-1 operation above 70 °C ambient air temperature.

**IBM SONET/SDH Framer**
**Input, Output and Input/Output Parameters**

On-chip pull-up and pull-down resistors are in the range of 10 to 15 k $\Omega$ . This implies that pulling the pin voltage up or down requires hundreds of nanoseconds when an output driver switches to tri-state. Transitions will be slower with large capacitive loads. For outputs going tri-state, where a slow transition might cause functional problems, an external 1 to 3 k $\Omega$  pull-up or pull-down resistor should be used.

When connecting any LVTTTL pin that does not have an internal pull resistor to another LVTTTL pin that has an internal pull-down resistor, an external pull-down resistor of 1-3 k $\Omega$  should be added to ensure that the signal is pulled to the appropriate logic level when the driving signal goes tri-state. This only applies to connections that have signals that go tri-state and we want to ensure that a valid logic level is present on the signals. An example of this would be when two SONET/SDH framers are connected back-to-back across their Telecom Bus interfaces. The signals that would need an external pull-down resistor are the TXTB#SPE to RXTB#SPE connections and the TXTB#C1J1 to RXTB#C1J1 connections.

**Input Parameters for LVTTTL-5sd** Low voltage TTL, 5 V tolerant with pull-down resistor, type sd

| Symbol   | Parameter  | Min  | Typ | Max  | Unit    | Notes |
|----------|--|------|-----|------|---------|-------|
| $V_{IH}$ | Input high voltage<br>$V_{DD} = 3.0$ V, Temp = 23 °C | 2.00 |     | 5.50 | V       | 1     |
| $V_{IL}$ | Input low voltage<br>$V_{DD} = 3.0$ V, Temp = 23 °C  | 0.00 |     | 0.80 | V       |       |
|          | Input leakage current<br>$V_{DD} = 3.6$ V            | 0.00 |     | 400  | $\mu$ A | 2     |
|          | Input capacitance                                    |      |     | 11   | pF      |       |

1. For this parameter, maximum level applies to overshoot only.
2. Input leakage current (min) measured at Input =  $V_{IH}(\text{min})$ . Input leakage current (max) measured at Input =  $V_{IH}(\text{max})$ .

**Input Parameters for LVTTTL-5sp** Low voltage TTL, 5 V tolerant with pull-up resistor, type sp

| Symbol   | Parameter  | Min  | Typ | Max  | Unit    | Notes |
|----------|--|------|-----|------|---------|-------|
| $V_{IH}$ | Input high voltage<br>$V_{DD} = 3.0$ V, Temp = 23 °C | 2.00 |     | 5.50 | V       | 1     |
| $V_{IL}$ | Input low voltage<br>$V_{DD} = 3.0$ V, Temp = 23 °C  | 0.00 |     | 0.80 | V       |       |
|          | Input leakage current<br>$V_{DD} = 3.6$ V            | -250 |     | 0    | $\mu$ A | 2     |
|          | Input capacitance                                    |      |     | 11   | pF      |       |

1. For this parameter, maximum level applies to overshoot only.
2. Input leakage current (min) measured at Input =  $V_{IH}(\text{min})$ . Input leakage current (max) measured at Input =  $V_{IH}(\text{max})$ .

**Input Parameters for LVTTTL- 5s** Low voltage TTL, 5 V tolerant, type s

| Symbol   | Parameter and Test Conditions                                | Min  | Typ | Max  | Unit          | Notes |
|----------|--|------|-----|------|---------------|-------|
| $V_{IH}$ | Input high voltage<br>$V_{DD} = 3.0\text{ V}$ , Temp = 23 °C | 2.00 |     | 5.50 | V             | 1     |
| $V_{IL}$ | Input low voltage<br>$V_{DD} = 3.0\text{ V}$ , Temp = 23 °C  | 0.00 |     | 0.80 | V             |       |
|          | Input leakage current<br>$V_{DD} = 3.6\text{ V}$             | 0    |     | 0    | $\mu\text{A}$ | 2     |
|          | Input capacitance  |      |     | 11   | pF            |       |

1. For this parameter, maximum level applies to overshoot only.  
2. Input leakage current (min) measured at Input =  $V_{IH}(\text{min})$ . Input leakage current (max) measured at Input =  $V_{IH}(\text{max})$ .

**Input Parameters for LVTTTL-5f** Low voltage TTL, 5 V tolerant, type f

| Symbol   | Parameter  | Min  | Typ | Max  | Unit          | Notes |
|----------|--|------|-----|------|---------------|-------|
| $V_{IH}$ | Input high voltage<br>$V_{DD} = 3.0\text{ V}$ , Temp = 23 °C | 2.00 |     | 5.50 | V             | 1     |
| $V_{IL}$ | Input low voltage<br>$V_{DD} = 3.0\text{ V}$ , Temp = 23 °C  | 0.00 |     | 0.80 | V             |       |
|          | Input leakage current<br>$V_{DD} = 3.6\text{ V}$             | 0    |     | 0    | $\mu\text{A}$ | 2     |
|          | Input capacitance  |      |     | 11   | pF            |       |

1. For this parameter, maximum level applies to overshoot only.  
2. Input leakage current (min) measured at Input =  $V_{IH}(\text{min})$ . Input leakage current (max) measured at Input =  $V_{IH}(\text{max})$ .

**Input Parameters for LPECL** Differential input, pseudo-ECL

| Symbol     | Parameter     | Min  | Typ | Max | Unit     | Notes |
|------------|---------------|------|-----|-----|----------|-------|
| $V_{DIFF}$ |               | 0.25 |     | 1.0 | V        | 1     |
| $V_{CM}$   | (common mode) | .95  | 2.0 | 2.6 | V        | 2     |
| $Z_{RIN}$  |               |      | 100 |     | $\Omega$ | 3     |
| $Z_{TLAC}$ |               |      | 100 |     | $\Omega$ | 4     |

1. Receiver input differential voltage swing. Allows for attenuation of 0.6 V between the driver and the receiver.  
2. Average differential voltage with respect to receiver ground, V-crosspoint at 200 Mhz.  
3. Receiver input impedance. Line to line receiver termination. There is an internal 100  $\Omega$  termination resistor connected across the differential inputs of all LPECL receivers. PPECL receivers do not have the internal termination resistor.  
4. Transmission line AC impedance. Equivalent to 50  $\Omega$  to ground on each line.

**IBM SONET/SDH Framer**
**Input Parameters for PPECL** Differential input, P-Pseudo-ECL

| Symbol     | Parameter                         | Min | Typ | Max       | Unit       | Notes |
|------------|-----------------------------------|-----|-----|-----------|------------|-------|
| $V_{DIFF}$ | Differential input signal voltage | 0.3 | 0.6 |           | V          |       |
| $V_{CM}$   | Common mode voltage               | 1.8 | 2.0 | 2.2       | V          |       |
| $C_{IN}$   | Input capacitance                 |     |     | 5         | pF         |       |
|            | Differential input slew rate      | 2.0 |     |           | V/ns       | 1     |
|            | Pulse width degradation           |     |     | $\pm 160$ | ps         |       |
| $Z_{RIN}$  | DC input impedance                | 100 |     |           | k $\Omega$ | 2     |
| $Z_{TLAC}$ | Transmission line AC impedance    |     | 100 |           | $\Omega$   | 3     |

- 311 MHz operation.
- PPECL receivers do not have an internal 100  $\Omega$  termination across their inputs.
- Equivalent to 50  $\Omega$  to ground on each line. If the common mode voltages of the attached OE module and the PPECL receiver are compatible, a termination resistor of 100  $\Omega$  should be connected in between the negative and positive input of the receiver. If  $V_{CM}$  is not compatible, 'adaptation' can be done by shifting the supply voltage of the OE module, or by using AC coupling capacitors.

**Output Parameters for LVTTTL-5sd** Low voltage TTL, 5 V tolerant with pull-down, 11 mA, type sd

| Symbol   | Parameter and/or Test Conditions  | Min  | Typ | Max      | Unit     |
|----------|---|------|-----|----------|----------|
| $V_{OH}$ | $V_{DD} = 3.0$ V, $I_{OUT} = 10$ mA, $T_j = 100$ °C                             | 2.40 |     | $V_{DD}$ | V        |
| $V_{OL}$ | $V_{DD} = 3.0$ V, $I_{OUT} = -7$ mA, $T_j = 100$ °C                             | 0.00 |     | 0.40     | V        |
| $I_{OL}$ | $V_{DD} = 3.0$ V, $V_{OUT} = 0.4$ V, $T_j = 100$ °C                             | -7   | -11 |          | mA       |
| $I_{OH}$ | $V_{DD} = 3.0$ V, $V_{OUT} = 2.4$ V, $T_j = 100$ °C                             | 10   | 11  |          | mA       |
|          | Tri-state leakage current<br>$V_{DD} = 3.0$ V, Temp = 23 °C, $V_{OUT} = V_{DD}$ | 0    |     | 400      | $\mu$ A  |
|          | Slew rate of output   |      | 30  |          | mA/ns    |
|          | Output impedance<br>Whole process, temperature, and $V_{DD}$ range              | 35   | 45  | 55       | $\Omega$ |
|          | Output capacitance  |      |     | 11       | pF       |

**Output Parameters for LVTTTL-5sp** Low voltage TTL, 5 V tolerant with pull-up, 11 mA, type sp

| Symbol   | Parameter and/or Test Conditions  | Min  | Typ | Max      | Unit          |
|----------|---|------|-----|----------|---------------|
| $V_{OH}$ | $V_{DD} = 3.0\text{ V}$ , $I_{OUT} = 10\text{ mA}$ , $T_j = 100\text{ }^\circ\text{C}$                              | 2.40 |     | $V_{DD}$ | V             |
| $V_{OL}$ | $V_{DD} = 3.0\text{ V}$ , $I_{OUT} = -7\text{ mA}$ , $T_j = 100\text{ }^\circ\text{C}$                              | 0.00 |     | 0.4      | V             |
| $I_{OL}$ | $V_{DD} = 3.0\text{ V}$ , $V_{OUT} = 0.4\text{ V}$ , $T_j = 100\text{ }^\circ\text{C}$                              | -7   | -11 |          | mA            |
| $I_{OH}$ | $V_{DD} = 3.0\text{ V}$ , $V_{OUT} = 2.4\text{ V}$ , $T_j = 100\text{ }^\circ\text{C}$                              | 10   | 11  |          | mA            |
|          | Tri-state leakage current<br>$V_{DD} = 3.0\text{ V}$ , Temp = $23\text{ }^\circ\text{C}$ , $V_{OUT} = 0.0\text{ V}$ | -250 |     | 0        | $\mu\text{A}$ |
|          | Slew rate of output   |      | 30  |          | mA/ns         |
|          | Output impedance<br>Whole process, temperature, and $V_{DD}$ range  | 35   | 45  | 55       | $\Omega$      |
|          | Output capacitance  |      |     | 11       | pF            |

**Output Parameters for LVTTTL-5s** Low voltage TTL, 5 V tolerant, 11 mA, type s

| Symbol   | Parameter and/or Test Conditions  | Min  | Typ | Max      | Unit          | Notes |
|----------|---|------|-----|----------|---------------|-------|
| $V_{OH}$ | $V_{DD} = 3.0\text{ V}$ , $I_{OUT} = 10\text{ mA}$ , $T_j = 100\text{ }^\circ\text{C}$                        | 2.40 |     | $V_{DD}$ | V             |       |
| $V_{OL}$ | $V_{DD} = 3.0\text{ V}$ , $I_{OUT} = -7\text{ mA}$ , $T_j = 100\text{ }^\circ\text{C}$                        | 0.00 |     | 0.4      | V             |       |
| $I_{OL}$ | $V_{DD} = 3.0\text{ V}$ , $V_{OUT} = 0.4\text{ V}$ , $T_j = 100\text{ }^\circ\text{C}$                        | -7   | -11 |          | mA            |       |
| $I_{OH}$ | $V_{DD} = 3.0\text{ V}$ , $V_{OUT} = 2.4\text{ V}$ , $T_j = 100\text{ }^\circ\text{C}$                        | 10   | 11  |          | mA            |       |
|          | Tri-state leakage current<br>$V_{DD} = 3.0\text{ V}$ , Temp = $23\text{ }^\circ\text{C}$ , $V_{OUT} = V_{DD}$ | 0    |     | 0        | $\mu\text{A}$ | 1, 2  |
|          | Slew rate of output   |      | 30  |          | mA/ns         |       |
|          | Approximate output impedance<br>Whole process, temperature, and $V_{DD}$ range                                | 35   | 45  | 55       | $\Omega$      |       |
|          | Output capacitance  |      |     | 11       | pF            |       |

1. The tri-state leakage current parameter applies only to outputs that tri-state.
2. The non-pull drivers will show a transient current during an external voltage transition; the peak current is  $\text{min} = -200\mu\text{A}$  @  $V_{DD} = 3.6\text{ V}$ ,  $T_j = 0\text{ }^\circ\text{C}$ .

**IBM SONET/SDH Framer**
**Output Parameters for LVTTTL-5f** Low voltage TTL, 5 V tolerant, 11 mA, type f

| Symbol   | Parameter and/or Test Conditions   | Min  | Typ | Max      | Unit     | Notes |
|----------|--|------|-----|----------|----------|-------|
| $V_{OH}$ | $V_{DD} = 3.0\text{ V}$ , $I_{OUT} = 10\text{ mA}$ , $T_j = 100\text{ }^\circ\text{C}$ | 2.40 |     | $V_{DD}$ | V        |       |
| $V_{OL}$ | $V_{DD} = 3.0\text{ V}$ , $I_{OUT} = -7\text{ mA}$ , $T_j = 100\text{ }^\circ\text{C}$ | 0.00 |     | 0.4      | V        |       |
| $I_{OL}$ | $V_{DD} = 3.0\text{ V}$ , $V_{OUT} = 0.4\text{ V}$ , $T_j = 100\text{ }^\circ\text{C}$ | -7   | -11 |          | mA       | 1     |
| $I_{OH}$ | $V_{DD} = 3.0\text{ V}$ , $V_{OUT} = 2.4\text{ V}$ , $T_j = 100\text{ }^\circ\text{C}$ | 10   | 11  |          | mA       | 1     |
|          | Slew rate of output  |      | 100 |          | mA/ns    |       |
|          | Approximate output impedance<br>Whole process, temperature, and $V_{DD}$ range         | 35   | 45  | 55       | $\Omega$ |       |
|          | Output capacitance   |      |     | 11       | pF       |       |

1. The non-pull drivers will show a transient current during an external voltage transition; the peak current is min =  $-200\mu\text{A}$  @  $V_{DD} = 3.6\text{ V}$ ,  $T_j = 0\text{ }^\circ\text{C}$ .

**Output Parameters for LVTTTL-5fp** Low voltage TTL, 5 V tolerant with pull-up, 11 mA, type fp

| Symbol   | Parameter and/or Test Conditions  | Min  | Typ | Max      | Unit          |
|----------|---|------|-----|----------|---------------|
| $V_{OH}$ | $V_{DD} = 3.0\text{ V}$ , $I_{OUT} = 10\text{ mA}$ , $T_j = 100\text{ }^\circ\text{C}$                              | 2.40 |     | $V_{DD}$ | V             |
| $V_{OL}$ | $V_{DD} = 3.0\text{ V}$ , $I_{OUT} = -7\text{ mA}$ , $T_j = 100\text{ }^\circ\text{C}$                              | 0.00 |     | 0.4      | V             |
| $I_{OL}$ | $V_{DD} = 3.0\text{ V}$ , $V_{OUT} = 0.4\text{ V}$ , $T_j = 100\text{ }^\circ\text{C}$                              | -7   | -11 |          | mA            |
| $I_{OH}$ | $V_{DD} = 3.0\text{ V}$ , $V_{OUT} = 2.4\text{ V}$ , $T_j = 100\text{ }^\circ\text{C}$                              | 10   | 11  |          | mA            |
|          | Tri-state leakage current<br>$V_{DD} = 3.0\text{ V}$ , Temp = $23\text{ }^\circ\text{C}$ , $V_{OUT} = 0.0\text{ V}$ | -250 |     | 0        | $\mu\text{A}$ |
|          | Slew rate of output   |      | 100 |          | mA/ns         |
|          | Output impedance<br>Whole process, temperature, and $V_{DD}$ range  | 35   | 45  | 55       | $\Omega$      |
|          | Output capacitance  |      |     | 11       | pF            |

**Output Parameters for LVTTTL-5fd** Low voltage TTL, 5 V tolerant, with pull-down, 11 mA, type fd

| Symbol   | Parameter and/or Test Conditions  | Min  | Typ | Max      | Unit          |
|----------|---|------|-----|----------|---------------|
| $V_{OH}$ | $V_{DD} = 3.0\text{ V}$ , $I_{OUT} = 10\text{ mA}$ , $T_j = 100\text{ }^\circ\text{C}$                        | 2.40 |     | $V_{DD}$ | V             |
| $V_{OL}$ | $V_{DD} = 3.0\text{ V}$ , $I_{OUT} = -7\text{ mA}$ , $T_j = 100\text{ }^\circ\text{C}$                        | 0.00 |     | 0.4      | V             |
| $I_{OL}$ | $V_{DD} = 3.0\text{ V}$ , $V_{OUT} = 0.4\text{ V}$ , $T_j = 100\text{ }^\circ\text{C}$                        | -7   | -11 |          | mA            |
| $I_{OH}$ | $V_{DD} = 3.0\text{ V}$ , $V_{OUT} = 2.4\text{ V}$ , $T_j = 100\text{ }^\circ\text{C}$                        | 10   | 11  |          | mA            |
|          | Tri-state leakage current<br>$V_{DD} = 3.0\text{ V}$ , Temp = $23\text{ }^\circ\text{C}$ , $V_{OUT} = V_{DD}$ | 0    |     | 400      | $\mu\text{A}$ |
|          | Slew rate of output   |      | 100 |          | mA/ns         |
|          | Output impedance<br>Whole process, temperature, and $V_{DD}$ range  | 35   | 45  | 55       | $\Omega$      |
|          | Output capacitance  |      |     | 11       | pF            |

**Output Parameters for PPECL 50 $\Omega$**  Push-pull differential output, P-Pseudo-ECL, 50 ohms

| Symbol      | Parameter and/or Test Conditions   | Min  | Typ  | Max  | Unit     |
|-------------|------------------------------------|------|------|------|----------|
| $V_{OH}$    | Output high voltage                | 2.00 | 2.42 | 2.78 | V        |
| $V_{OL}$    | Output low voltage                 | 1.40 | 1.58 | 1.75 | V        |
| $V_{OCM}$   | Output common mode voltage         | 1.70 | 2.00 | 2.22 | V        |
| $V_{ODIFF}$ | Differential output signal voltage | 0.60 | 0.83 | 1.20 | V        |
| $Z_{OUT}$   | Output impedance                   |      |      | 25   | $\Omega$ |

**Performance of PPECL 50 $\Omega$  Drivers vs Load**

| Parameter, Load <sup>1</sup> | Min | Typ | Max | Unit | Notes |
|------------------------------|-----|-----|-----|------|-------|
| Driver delay, 2 pF           | 280 | 440 | 715 | ps   | 2     |
| Driver delay, 8 pF           | 370 | 570 | 905 | ps   | 2     |
| Output slew rate, 2 pF       | 1.5 | 3.4 | 7.6 | V/ns |       |
| Output slew rate, 8 pF       | 1.1 | 2.4 | 4.8 | V/ns |       |
| Power consumption, 2 pF      | 27  | 49  | 80  | mW   | 3     |
| Power consumption, 8 pF      | 31  | 55  | 92  | mW   | 3     |

1. Performance is measured with 100  $\Omega$  termination of the differential line; capacitive load on each output.
2. Delays are measured from input crossing  $V_{DD} / 2$  to output V-crosspoint.
3. 311 MHz operation.

## Timing Characteristics

This section presents the detailed timing characteristics for the SONET/SDH framer. The load capacitances for the output times are indicated in each figure as applicable. Unless otherwise indicated, timing parameters are measured at specific signal voltage levels:

|               |   |                              |
|---------------|---|------------------------------|
| TTL Inputs    | - | .8 / 2.0 V                   |
| TTL Outputs   | - | .8 / 2.0 V                   |
| LPECL Inputs  | - | V-crosspoint to V-crosspoint |
| PPECL Inputs  | - | V-crosspoint to V-crosspoint |
| PPECL Outputs | - | V-crosspoint to V-crosspoint |

The specifications given in this section cover two sets of environmental conditions:

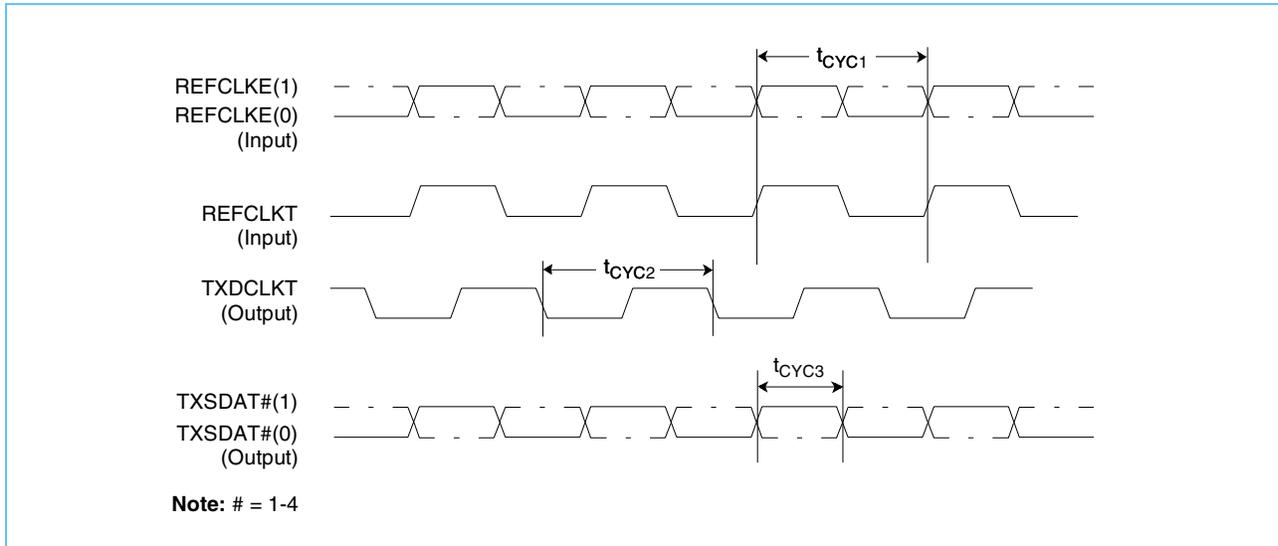
Set 1:  $T_j = 0\text{ }^{\circ}\text{C}$  to  $100\text{ }^{\circ}\text{C}$ ,  $V_{DD} = 3.3\text{ V} \pm 0.3\text{ V}$

Set 2:  $T_j = -40\text{ }^{\circ}\text{C}$  to  $125\text{ }^{\circ}\text{C}$ ,  $V_{DD} = 3.3\text{ V} \pm 5\%$

**Note:** Temperature and power supply conditions of the two sets above must not be mixed. Measurements assume input rise and fall times of 2 ns (except REFCLKT/REFCLKE/RXSDAT1(0:1)). Lower and upper limits for the pin capacitance  $C_L$  at the outputs are specified for each interface. All drivers are 50  $\Omega$  source-terminated. Impedance-matched interconnections are assumed.

In all timing diagrams the # symbol is used as an index and takes on the values 1-4. For instance, T1DCLK# is used to compactly represent T1DCLK1, T1DCLK2, T1DCLK3, and T1DCLK4.

## Serial Transmit Line Interface Timing



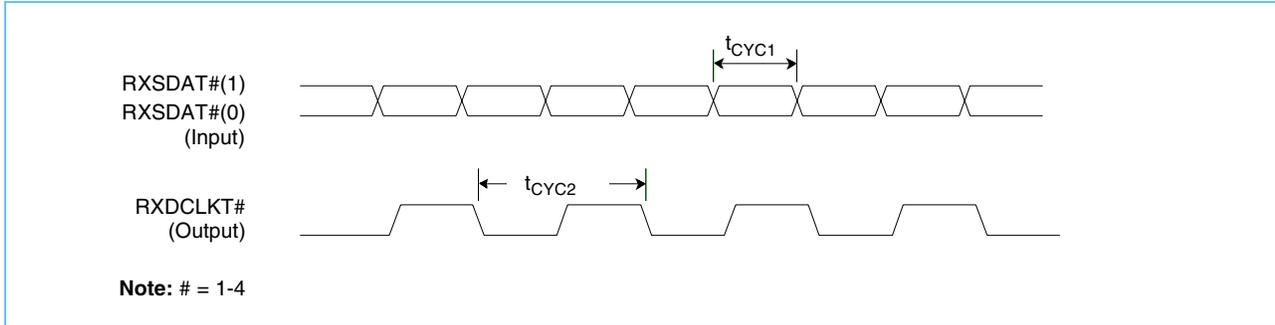
$C_L$  at outputs: 3 pF - 15 pF

| Symbol     | Parameter                            | Min   | Typ  | Max   | Unit |
|------------|--------------------------------------|-------|------|-------|------|
| $t_{CYC1}$ | REFCLKT clock period                 | 12.86 |      | 51.44 | ns   |
| $t_{CYC1}$ | REFCLKE clock period                 | 6.43  |      | 51.44 | ns   |
|            | REFCLKT/REFCLKE clock duty cycle     | 40    | 50   | 60    | %    |
|            | REFCLKT/REFCLKE input rise/fall time |       |      | 1.0   | ns   |
| $t_{CYC2}$ | TXDCLKT clock period                 | 12.86 |      | 51.44 | ns   |
| $t_{CYC3}$ | TXSDAT1 period                       |       | 1.61 |       | ns   |
| $t_{CYC3}$ | TXSDAT2-4 period                     |       | 6.43 |       | ns   |
| $t_r, t_f$ | TXSDAT1-4 output rise/fall times     | 0.15  |      | 0.5   | ns   |
| $t_r, t_f$ | TXDCLKT output rise/fall times       | 1.3   |      | 5.8   | ns   |

**Notes:**

1. Frequencies for REFCLKT and REFCLKE inputs are selected via the Tx\_RefFrq(2:0) configuration bits.
2. Frequency for TXDCLKT output is selected via the Tx\_DivFrq(2:0) configuration bits.
3. No phase relationship is indicated between REFCLKT/REFCLKE, TXDCLKT, or TXSDAT#.
4. TXLPOW# are asynchronous inputs and TXSDOWN# are asynchronous outputs. Asynchronous I/O need not be shown on the timing diagrams.

### Serial Receive Line Interface Timing



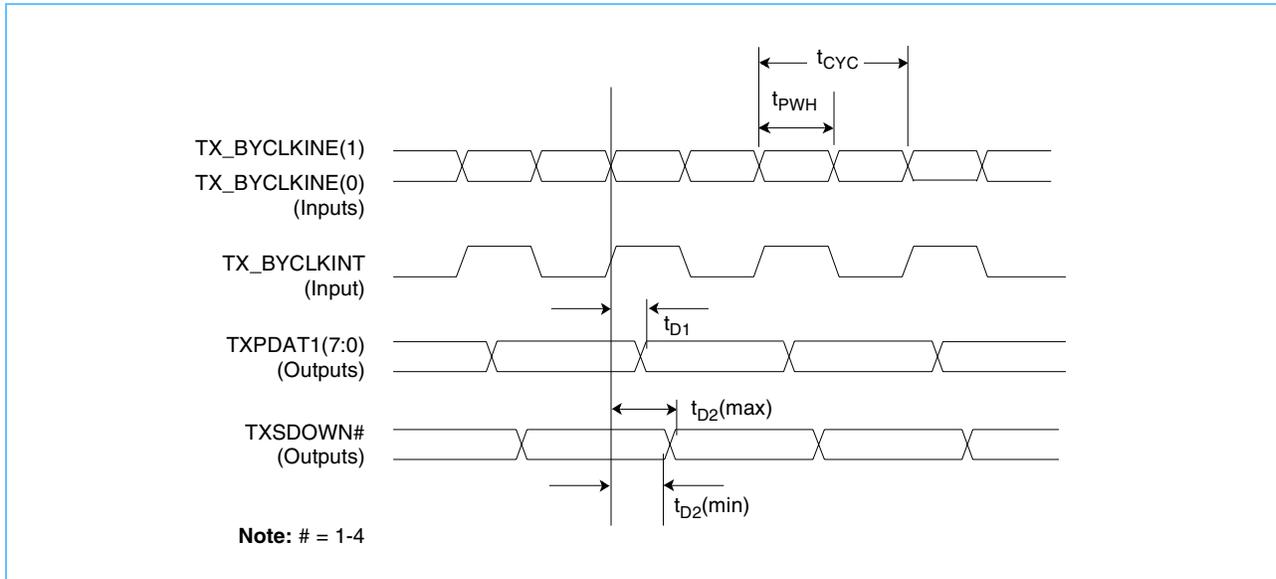
C<sub>L</sub> at outputs: 3 pF - 15 pF

| Symbol                            | Parameter                       | Min   | Typ  | Max   | Unit |
|-----------------------------------|---------------------------------|-------|------|-------|------|
| t <sub>CYC1</sub>                 | RXSDAT1 period                  |       | 1.61 |       | ns   |
| t <sub>CYC1</sub>                 | RXSDAT2-4 period                |       | 6.43 |       | ns   |
| t <sub>r</sub> , t <sub>f</sub>   | RXSDAT1 input rise/fall time    |       |      | 0.5   | ns   |
| t <sub>r</sub> , t <sub>f</sub>   | RXSDAT2-4 input rise/fall time  |       |      | 1.0   | ns   |
| t <sub>CYC2</sub>                 | RXDCLKT# clock period           | 12.86 |      | 51.44 | ns   |
| t <sub>rC</sub> , t <sub>fC</sub> | RXDCLKT# output rise/fall times | 1.3   |      | 5.0   | ns   |

**Notes:**

1. Frequencies for the RXDCLKT# outputs are selected via the Rx\_DivFrq#(2:0) configuration bits.
2. No phase relationship is indicated between RXDCLKT# and RXSDAT#.
3. LOSSSIG# are asynchronous inputs. Asynchronous I/O need not be shown on the timing diagrams.

## Byte-Parallel Transmit Line Interface Timing

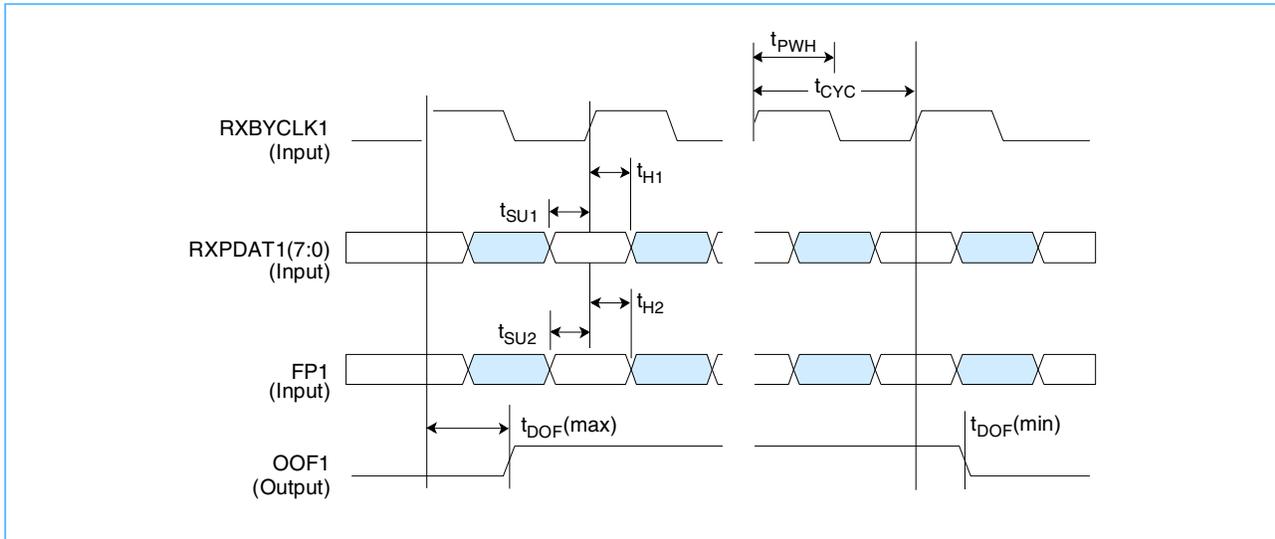


$C_L$  at outputs: 3 pF - 15 pF

| Symbol              | Parameter   | Min | Typ   | Max  | Unit |
|---------------------|---|-----|-------|------|------|
| $t_{CYC}$           | TX_BYCLKINT/TX_BYCLKINE clock period                                      |     | 12.86 |      | ns   |
| $t_{PWH} / t_{CYC}$ | TX_BYCLKINT/TX_BYCLKINE clock duty cycle                                  | 45  |       | 55   | %    |
| $t_{D1}$            | TXPDAT1(7:0) delay after TX_BYCLKINT $\uparrow$ or TX_BYCLKINE $\uparrow$ | 2.3 |       | 10.1 | ns   |
| $t_{D2}$            | TXSDOWN# delay after TX_BYCLKINT $\uparrow$ or TX_BYCLKINE $\uparrow$     | 4.5 |       | 20   | ns   |
| $t_r, t_f$          | TXPDAT1(7:0) output rise/fall times                                       | 0.8 |       | 4.8  | ns   |
| $t_{rC}, t_{fC}$    | TXSDOWN# output rise/fall times   | 1.3 |       | 5.8  | ns   |

1. TXLP0W# are asynchronous inputs. Asynchronous I/O need not be shown on the timing diagrams.
2. Duty cycles up to 40/60% are acceptable for TX\_BYCLKINT/TX\_BYCLKINE; but the duty cycle specs of the derived clock outputs TXCCLK,  $\overline{TXCCLK}$  and RXRINGCLK will also increase by  $\pm 5\%$ .

### Byte-Parallel Receive Line Interface Timing

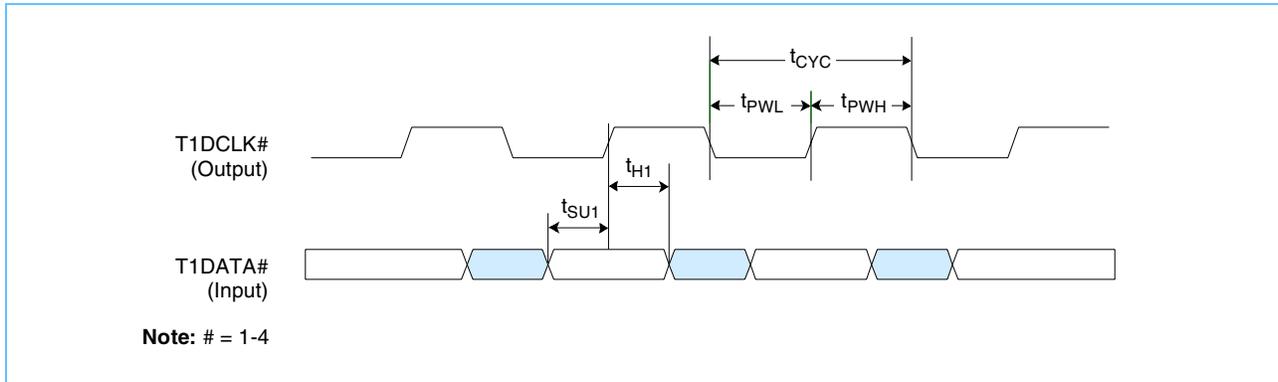


C<sub>L</sub> at outputs: 3 pF - 15 pF

| Symbol                              | Parameter                              | Min | Typ   | Max  | Unit |
|-------------------------------------|--|-----|-------|------|------|
| t <sub>CYC</sub>                    | RXBYCLK1 clock period                  |     | 12.86 |      | ns   |
| t <sub>PWH</sub> / t <sub>CYC</sub> | RXBYCLK1 clock duty cycle              | 45  |       | 55   | %    |
| t <sub>SU1</sub>                    | RXPDAT1(7:0) set-up time to RXBYCLK1↑  | 1.0 |       |      | ns   |
| t <sub>H1</sub>                     | RXPDAT1(7:0) hold time after RXBYCLK1↑ | 1.5 |       |      | ns   |
| t <sub>SU2</sub>                    | FP1 set-up time to RXBYCLK1↑           | 1.0 |       |      | ns   |
| t <sub>H2</sub>                     | FP1 hold time after RXBYCLK1↑          | 1.5 |       |      | ns   |
| t <sub>DOF</sub>                    | OOF1 output delay after RXBYCLK1↑      | 4.5 |       | 17.7 | ns   |
| t <sub>rC</sub> , t <sub>fC</sub>   | OOF1 output rise/fall times            | 1.3 |       | 5.8  | ns   |

1. RSTCREC1 is an asynchronous output with rise/fall times of 1.2-5 ns. LOCKDET1 and LOSSSIG1 are asynchronous inputs. Asynchronous I/O need not be shown on the timing diagrams.
2. Duty cycles up to 40/60% are acceptable for RXBYCLK1; but the duty cycle specs of the derived clock outputs RXTB#CLK will also increase by ± 5%.

## Transmit Serial DCC Interface Timing

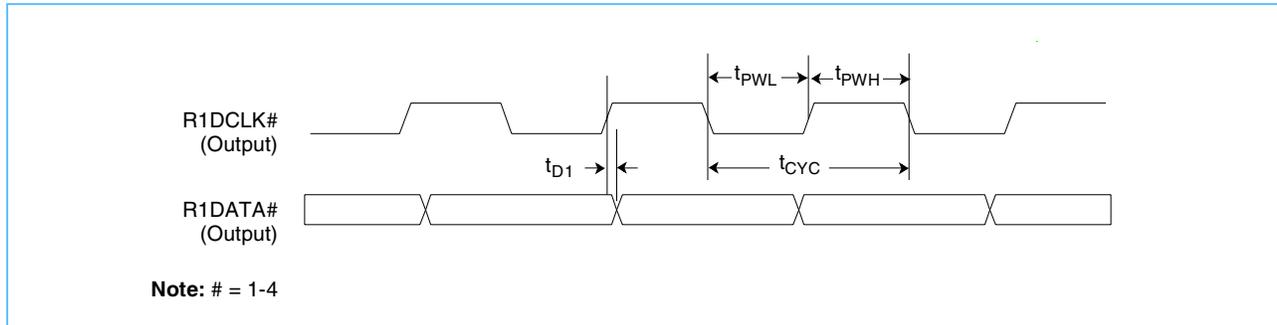


$C_L$  at outputs: 3 pF - 15 pF

| Symbol              | Parameter  | Min       | Typ  | Max  | Unit    |
|---------------------|--|-----------|------|------|---------|
| $t_{CYC}$           | T1DCLK# clock period for 192 kbit/s D1-D3 channel  | 5.19      | 5.21 | 5.25 | $\mu$ s |
| $t_{CYC}$           | T1DCLK# clock period for 576 kbit/s D4-D12 channel | 1.7       | 1.73 | 1.75 | $\mu$ s |
| $t_{PWH} / t_{CYC}$ | T1DCLK# duty cycle                                 | 45        |      | 55   | %       |
| $t_{SU1}$           | T1DATA# set-up time to T1DCLK# $\uparrow$          | 2 x 51.44 |      |      | ns      |
| $t_{H1}$            | T1DATA# hold time after T1DCLK# $\uparrow$         | 1 x 51.44 |      |      | ns      |

**Note:** The timing shown is for the EdgeMode bit of the OT#Conf7 register set to '1'. The timing parameters remain the same when the EdgeMode bit is set to '0', except that T1DATA# is sampled on the falling edge of the corresponding T1DCLK#. Each TX Serial DCC interface can be individually configured.

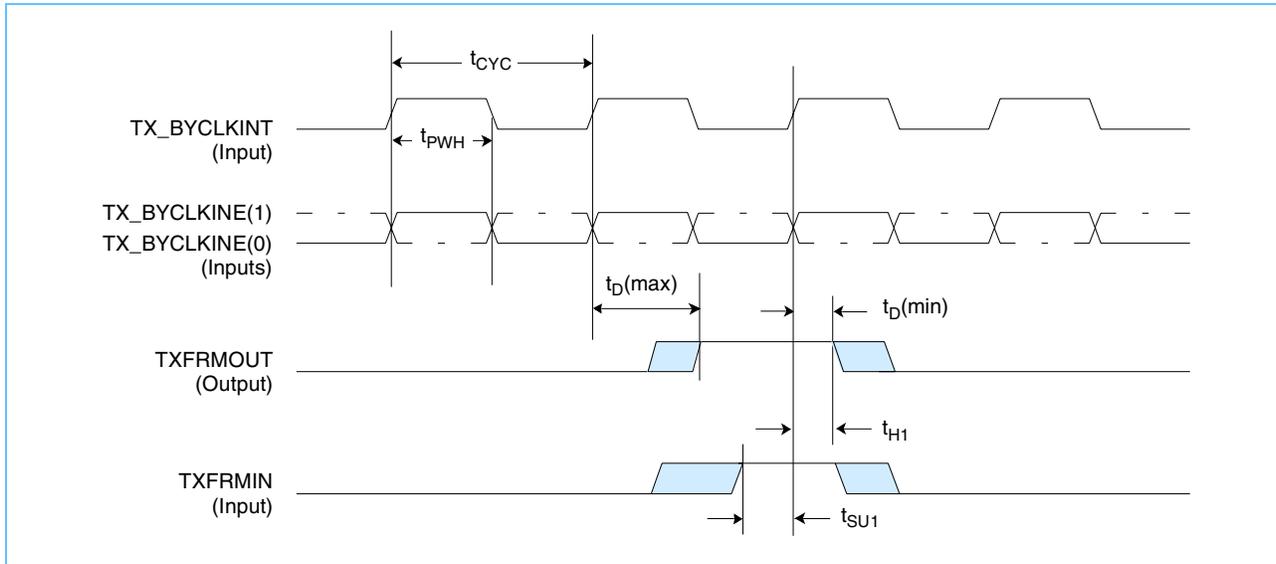
### Receive Serial DCC Interface Timing



C<sub>L</sub> at outputs: 3 pF - 15 pF

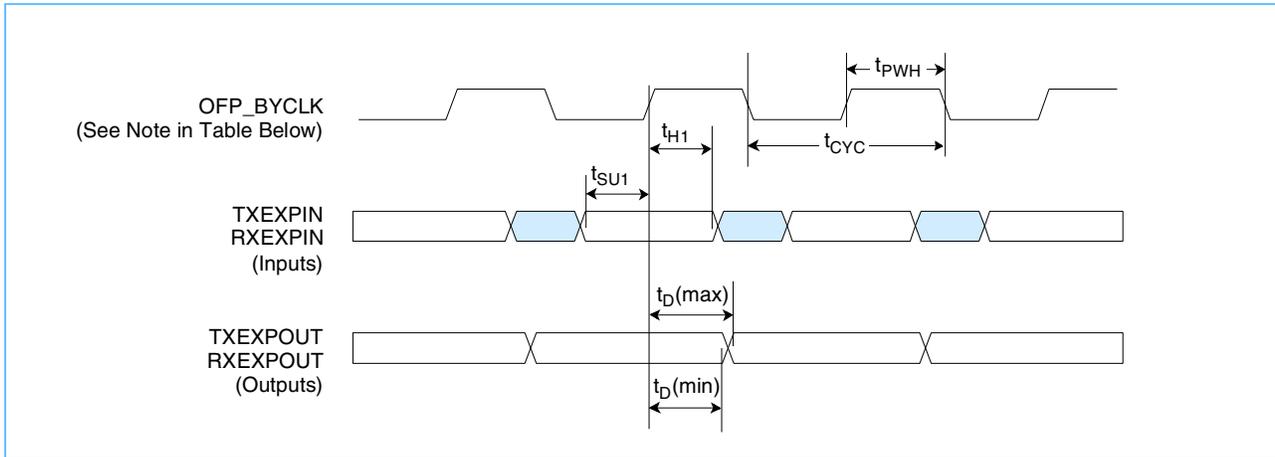
| Symbol                              | Parameter  | Min         | Typ  | Max         | Unit |
|-------------------------------------|--|-------------|------|-------------|------|
| t <sub>CYC</sub>                    | R1DCLK# clock period for 192 kbit/s D1-D3 channel  | 5.19        | 5.21 | 5.25        | μs   |
| t <sub>CYC</sub>                    | R1DCLK# clock period for 576 kbit/s D4-D12 channel | 1.7         | 1.73 | 1.75        | μs   |
| t <sub>PWH</sub> / t <sub>CYC</sub> | R1DCLK# clock duty cycle                           | 45          |      | 55          | %    |
| t <sub>D1</sub>                     | R1DATA# output delay from R1DCLK#↑                 | 51.44 - 3.0 |      | 51.44 + 3.0 | ns   |

**Note:** The timing shown is for the EdgeMode bit of the OT#Conf7 register set to '1'. The timing parameters remain the same when the EdgeMode bit is set to '0', except that R1DATA# is output on the falling edge of the corresponding R1DCLK#. Each receive Serial DCC interface can be individually configured.

**OC-48 Expansion Port Timing** (Sheet 1 of 2)

 $C_L$  at output: 15 pF - 30 pF

| Symbol              | Parameter  | Min | Typ   | Max  | Unit |
|---------------------|--|-----|-------|------|------|
| $t_{CYC}$           | TX_BYCLKINT/TX_BYCLKINE clock period                           |     | 12.86 |      | ns   |
| $t_{PWH} / t_{CYC}$ | TX_BYCLKINT/TX_BYCLKINE clock duty cycle                       | 45  |       | 55   | %    |
| $t_{SU1}$           | TXFRMIN set-up time to TX_BYCLKINT/TX_BYCLKINE $\uparrow$      | 0.7 |       |      | ns   |
| $t_{H1}$            | TXFRMIN hold time from TX_BYCLKINT/TX_BYCLKINE $\uparrow$      | 1.0 |       |      | ns   |
| $t_D$               | TXFRMOUT output delay after TX_BYCLKINT/TX_BYCLKINE $\uparrow$ | 2.7 |       | 11.1 | ns   |
| $t_r, t_f$          | TXFRMOUT rise/fall times                                       | 1.5 |       | 6.2  | ns   |
| $C_{IN}$            | TXFRMIN pin capacitance  | 5.0 |       | 7.5  | pF   |

OC-48 Expansion Port Timing (Sheet 2 of 2)



C<sub>L</sub> at outputs: 3 pF - 12 pF

| Symbol                              | Parameter                                       | Min | Typ   | Max | Unit |
|-------------------------------------|---|-----|-------|-----|------|
| t <sub>CYC</sub>                    | OFF_BYCLK clock period                          |     | 51.44 |     | ns   |
| t <sub>PWH</sub> / t <sub>CYC</sub> | OFF_BYCLK clock duty cycle                      | N/A |       | N/A | %    |
| t <sub>SU1</sub>                    | TXEXPIN/RXEXPIN set-up time to OFF_BYCLK↑       | 6.0 |       |     | ns   |
| t <sub>H1</sub>                     | TXEXPIN/RXEXPIN hold time from OFF_BYCLK↑       | 5.5 |       |     | ns   |
| t <sub>D</sub>                      | TXEXPOUT/RXEXPOUT output delay after OFF_BYCLK↑ | 4.5 |       | 19  | ns   |
| t <sub>r</sub> , t <sub>f</sub>     | TXEXPOUT/RXEXPOUT rise/fall times               | 1.3 |       | 5.0 | ns   |

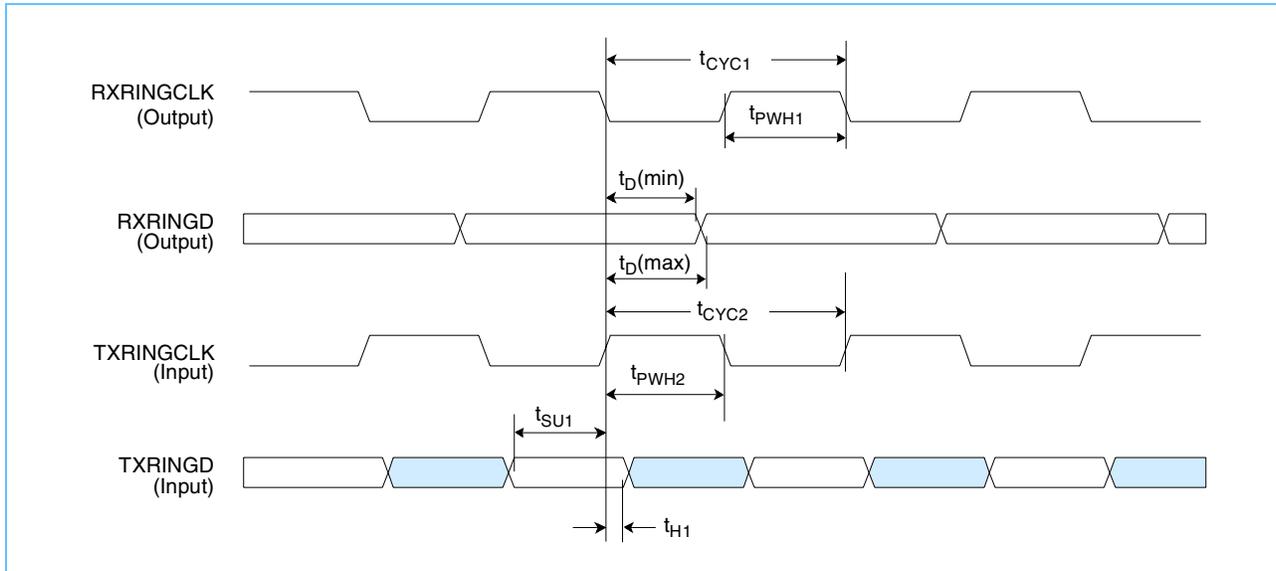
**Note:** The OFF\_BYCLK is a place holder for an internal clock running at 19.44 MHz. For TXEXPIN and TXEXPOUT, the rising edge of OFF\_BYCLK coincides with the rising edge of TX\_BYCLKINT/E. Likewise for RXEXPIN and RXEXPOUT, the rising edge of OFF\_BYCLK coincides with the rising edge of RXBYCLK1. Notice that both RXBYCLK1 and TX\_BYCLKINT/E operate at 77.76 MHz while OFF\_BYCLK operates at 19.44 MHz. In both cases, the phase between the internal OFF\_BYCLK and the external clock can vary in multiples of 12.86 ns. As long as the internal OFF clocks of the four SONET/SDH framers run synchronously, then all that needs to be considered are the allowable board delays of the four TXEXPOUT to TXEXPIN and RXEXPOUT to RXEXPIN connections. The maximum and minimum board delays are given by:

$$t_{BOARD(max)} = t_{CYC} - t_D(max) - t_{SU1(min)} - t_{CLOCKSKREW(max)}$$

$$t_{BOARD(min)} = -t_D(min) + t_{H1(min)} + t_{CLOCKSKREW(max)}$$

t<sub>CLOCKSKREW(max)</sub> is the maximum external device-to-device skew of TX\_BYCLKINT/E or RXBYCLK1 on the board.

## Ring Port Timing

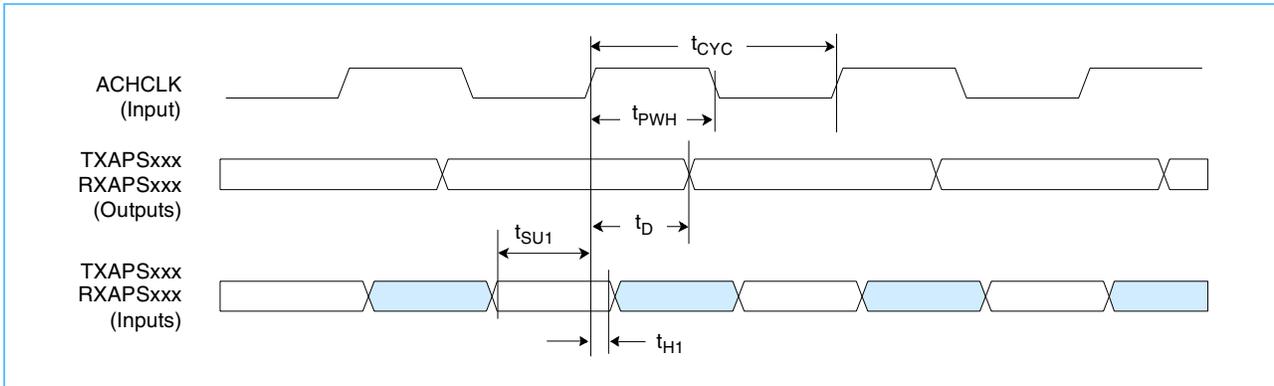


$C_L$  at outputs: 3 pF - 25 pF

| Symbol                | Parameter   | Min | Typ   | Max | Unit |
|-----------------------|---|-----|-------|-----|------|
| $t_{CYC1}$            | RXRINGCLK clock period                            |     | 51.44 |     | ns   |
| $t_{PWH1} / t_{CYC1}$ | RXRINGCLK clock duty cycle                        | 43  |       | 57  | %    |
| $t_D$                 | RXRINGD output delay after RXRINGCLK $\downarrow$ | 0   |       | 5.0 | ns   |
| $t_r, t_f$            | RXRINGCLK/RXRINGD output rise/fall times          | 1.3 |       | 7.0 | ns   |
| $t_{CYC2}$            | TXRINGCLK clock period                            |     | 51.44 |     | ns   |
| $t_{PWH2} / t_{CYC2}$ | TXRINGCLK clock duty cycle                        | 35  |       | 65  | %    |
| $t_{SU1}$             | TXRINGD set-up time to TXRINGCLK $\uparrow$       | 1.0 |       |     | ns   |
| $t_{H1}$              | TXRINGD hold time after TXRINGCLK $\uparrow$      | 2.0 |       |     | ns   |

IBM SONET/SDH Framer

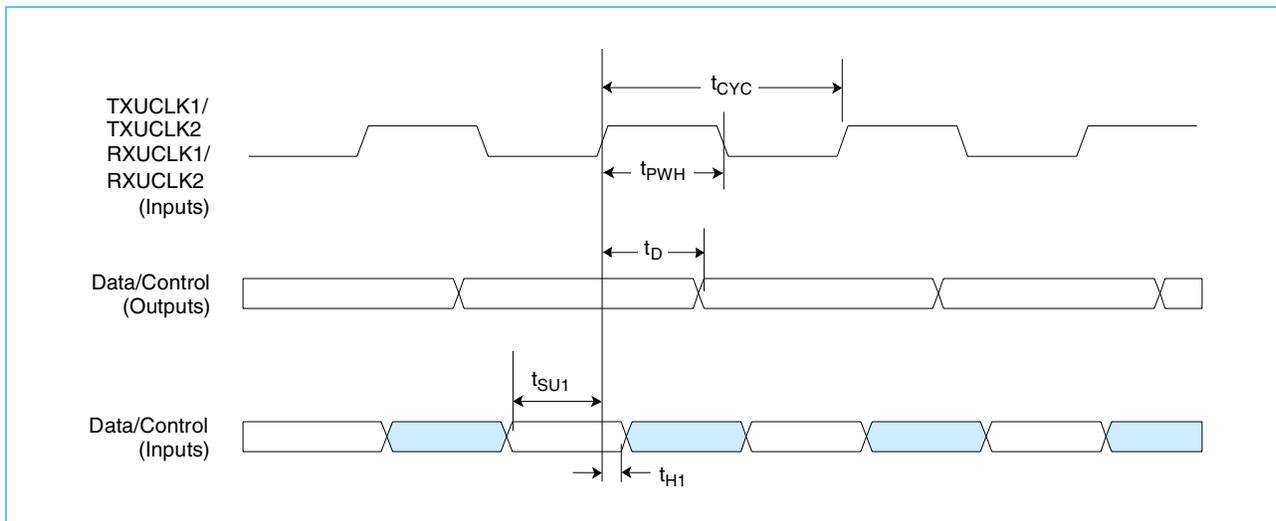
APS Port Timing



$C_L$  at outputs: 5 pF - 30 pF

| Symbol              | Parameter  | Min  | Typ | Max  | Unit |
|---------------------|--|------|-----|------|------|
| $t_{CYC}$           | ACHCLK clock period                                    | 38.4 | 40  | 44   | ns   |
| $t_{PWH} / t_{CYC}$ | ACHCLK clock duty cycle                                | 40   |     | 60   | %    |
| $t_D$               | TXAPSxxx/RXAPSxxx output delay after ACHCLK $\uparrow$ | 5.0  |     | 18.5 | ns   |
| $t_{SU1}$           | TXAPSxxx/RXAPSxxx set-up time to ACHCLK $\uparrow$     | 0.5  |     |      | ns   |
| $t_{H1}$            | TXAPSxxx/RXAPSxxx hold time after ACHCLK $\uparrow$    | 2.5  |     |      | ns   |
| $t_r, t_f$          | TXAPSxxx/RXAPSxxx output rise/fall times               | 1.5  |     | 8.0  | ns   |

## UTOPIA Level 1 Timing

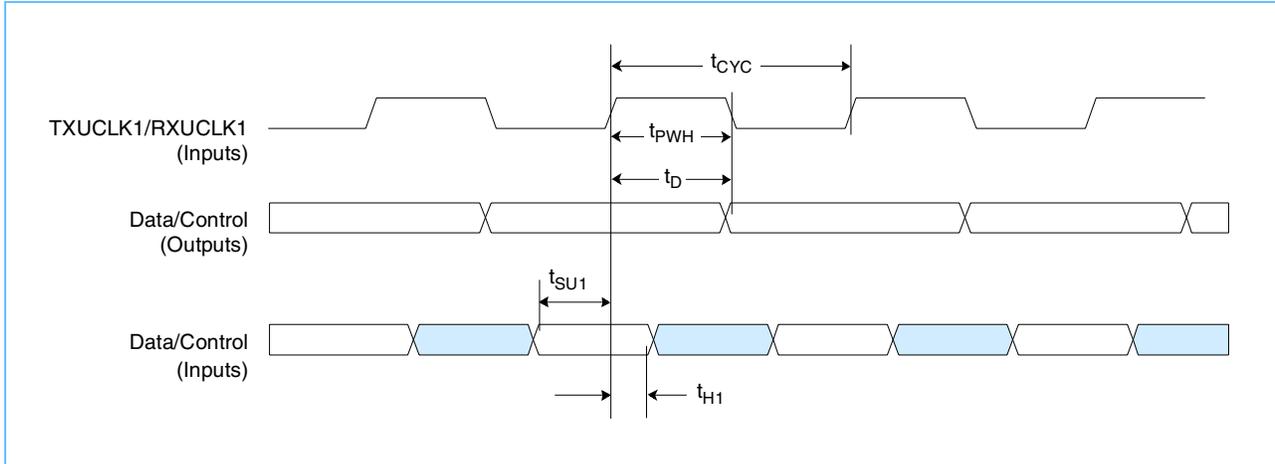


$C_L$  at outputs: 5 pF - 40 pF

| Symbol              | Parameter   | Min  | Typ | Max  | Unit |
|---------------------|---|------|-----|------|------|
| $t_{CYC}$           | TXUCLK1/2 / RXUCLK1/2 clock period  | 38.4 | 40  |      | ns   |
| $t_{PWH} / t_{CYC}$ | TXUCLK1/2 / RXUCLK1/2 clock duty cycle  | 40   |     | 60   | %    |
|                     | TXUCLK1/2 / RXUCLK1/2 peak-to-peak jitter                                     |      |     | 5.0  | %    |
| $t_D$               | TXCLAV delay after TXUCLK1/2 $\uparrow$                                       | 3.0  |     | 17   | ns   |
| $t_D$               | RXUDATA/RXPRTY/RXSOC/RXCLAV delay after RXUCLK1/2 $\uparrow$                  | 3.0  |     | 17.5 | ns   |
| $t_{SU1}$           | TXUDATA/TXPRTY/TXSOC / $\overline{TXENB}$ set-up time to TXUCLK1/2 $\uparrow$ | 6.0  |     |      | ns   |
| $t_{H1}$            | TXUDATA/TXPRTY/TXSOC $\overline{TXENB}$ hold time from TXUCLK1/2 $\uparrow$   | 0    |     |      | ns   |
| $t_{SU1}$           | $\overline{RXENB}$ set-up time to RXUCLK1/2 $\uparrow$                        | 6.0  |     |      | ns   |
| $t_{H1}$            | $\overline{RXENB}$ hold time from RXUCLK1/2 $\uparrow$                        | 1.0  |     |      | ns   |

**Note:** If the UTOPIA clock frequencies go below 2 MHz, the watchdog timer period (microprocessor interface) may need to be changed.

### UTOPIA Level 2 and Level 2+ Timing



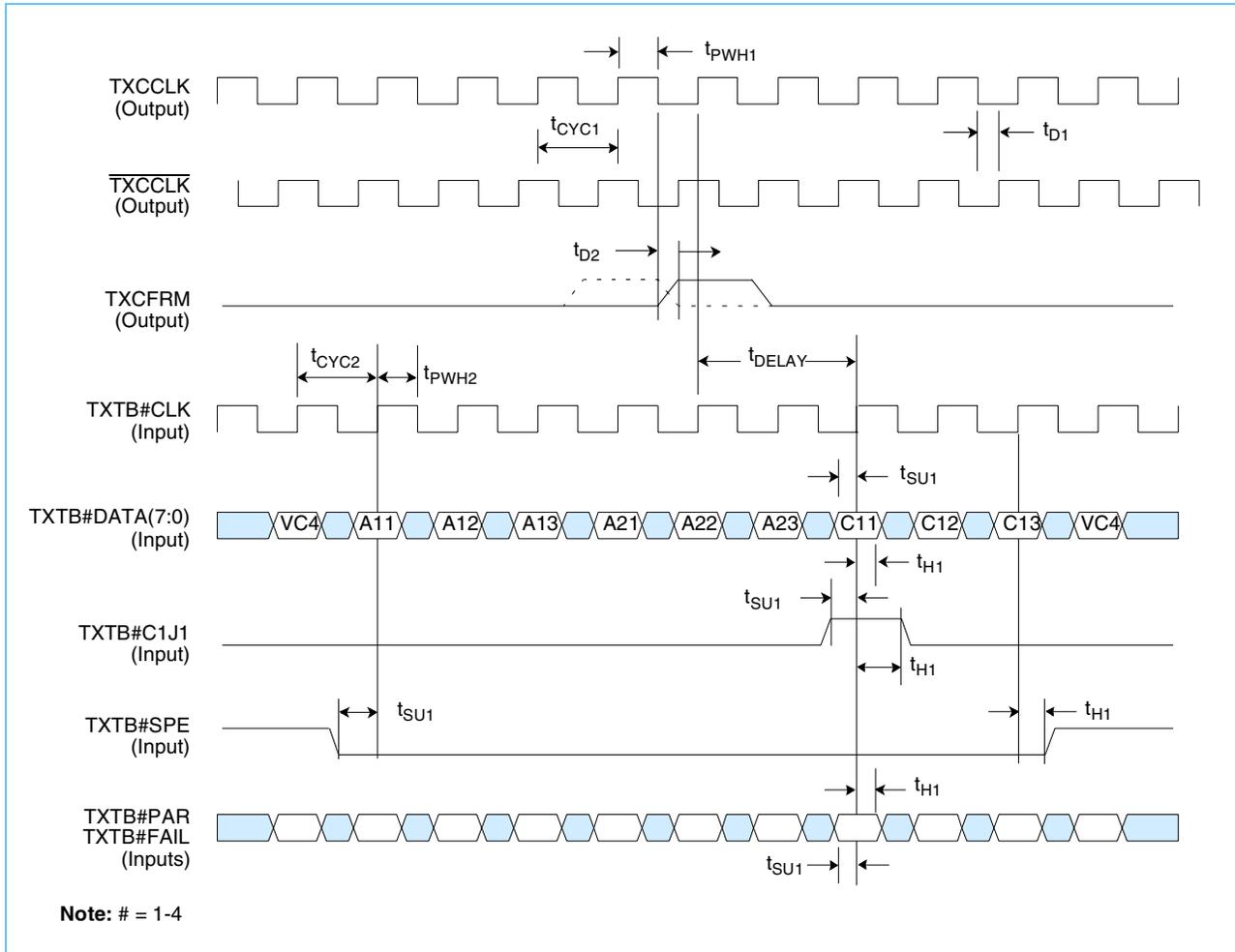
$C_L$  at outputs except for TXCLAV: 5 pF - 40 pF

$C_L$  at TXCLAV outputs: 5 pF - 30 pF

| Symbol              | Parameter  | Min  | Typ | Max  | Unit |
|---------------------|--|------|-----|------|------|
| $t_{CYC}$           | TXUCLK1/RXUCLK1 clock period   | 19.2 | 20  |      | ns   |
| $t_{PWH} / t_{CYC}$ | TXUCLK1/RXUCLK1 clock duty cycle   | 40   |     | 60   | %    |
|                     | TXUCLK1/RXUCLK1 peak-to-peak jitter  |      |     | 5    | %    |
| $t_D$               | TXCLAV delay after TXUCLK1↑  | 3.7  |     | 15.7 | ns   |
| $t_D$               | TXABTO delay after TXUCLK1↑  | 3.5  |     | 15   | ns   |
| $t_D$               | RXUDATA delay after RXUCLK1↑   | 3.3  |     | 15.5 | ns   |
| $t_D$               | RXCLAV/RXEFOF/RXMSO/RXFCSEO delay after RXUCLK1↑                                   | 3.5  |     | 15   | ns   |
| $t_D$               | RXPRTY/RXSOC/RXSOFO/RXABTO delay after RXUCLK1↑                                    | 3.3  |     | 14.5 | ns   |
| $t_{SU1}$           | TXUDATA/TXUADDR/TXPRTY/TXSOC/<br>TXSOFI/TXENB/TXEOF1/TXMSI set-up time to TXUCLK1↑ | 3.0  |     |      | ns   |
| $t_{H1}$            | TXUDATA/TXUADDR/TXPRTY/TXSOC/<br>TXSOFI/TXENB/TXEOF1/TXMSI hold time from TXUCLK1↑ | 0    |     |      | ns   |
| $t_{SU1}$           | RXUADDR/RXENB set-up time to RXUCLK1↑  | 4.0  |     |      | ns   |
| $t_{H1}$            | RXUADDR/RXENB hold time from RXUCLK1↑  | 1.0  |     |      | ns   |
| $t_r, t_f$          | UTOPIA interface output rise/fall times  | 0.8  |     | 8.0  | ns   |

**Note:** If the UTOPIA clock frequencies go below 2 MHz, the watchdog timer period (microprocessor interface) may need to be changed.

### Transmit Telecom Bus Timing



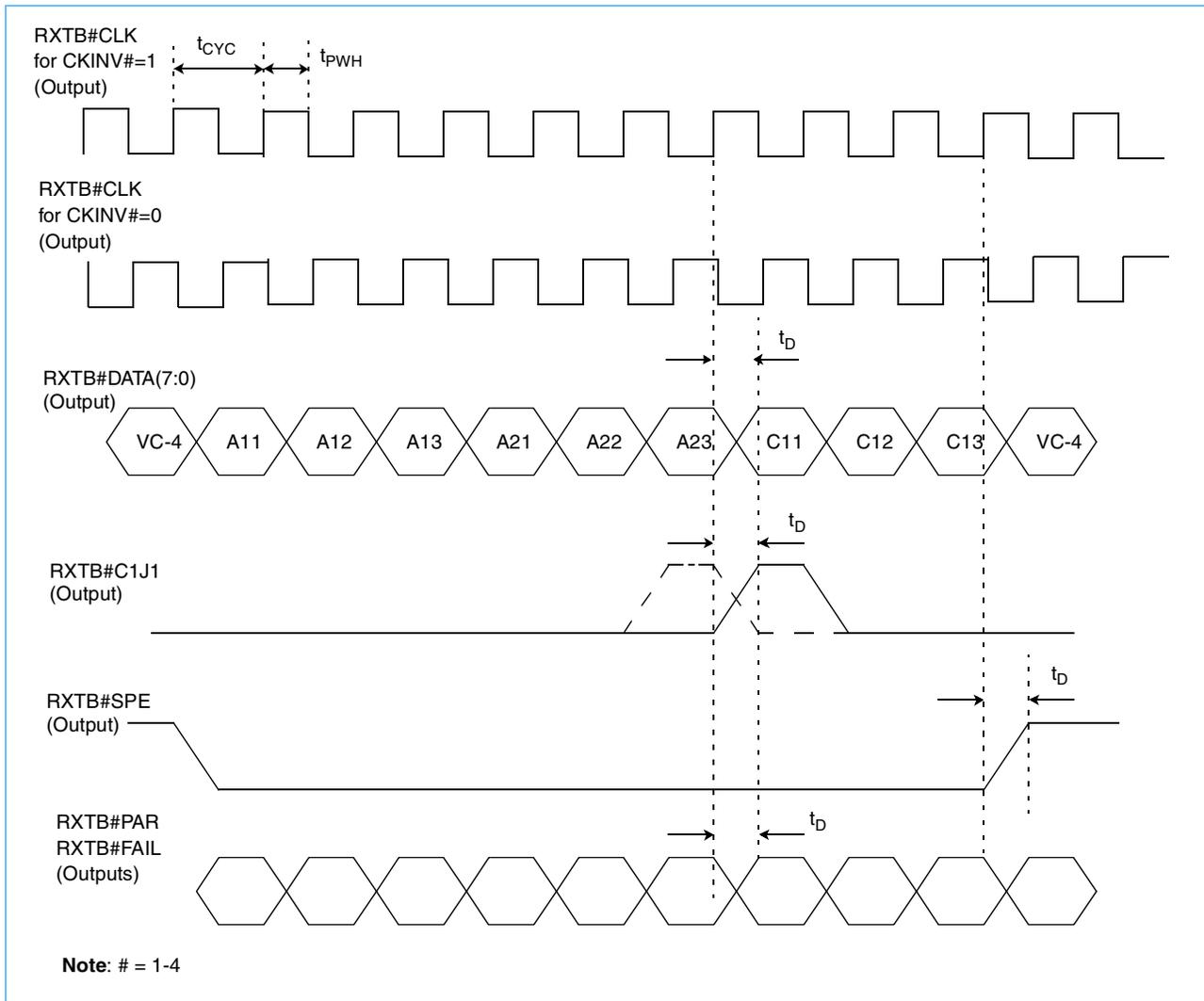
See parameter table on next page.

**IBM SONET/SDH Framer**
 $C_L$  at outputs: 3 pF - 25 pF

| Symbol                | Parameter  | Min  | Typ   | Max                      | Unit |
|-----------------------|--|------|-------|--------------------------|------|
| $t_{CYC1}$            | TXCCLK/ $\overline{\text{TXCCLK}}$ clock period  |      | 51.44 |                          | ns   |
| $t_{PWH1} / t_{CYC1}$ | TXCCLK/ $\overline{\text{TXCCLK}}$ duty cycle  | 42.5 |       | 57.5                     | %    |
| $t_{D1}$              | $\overline{\text{TXCCLK}}\uparrow$ delay from TXCCLK $\downarrow$                            | -1.0 |       | 1.0                      | ns   |
| $t_{D2}$              | TXCFRM output delay from TXCCLK $\downarrow$   | -2.5 |       | 1.0                      | ns   |
| $t_{CYC2}$            | TXTB#CLK clock period  |      | 51.44 |                          | ns   |
| $t_{PWH2} / t_{CYC2}$ | TXTB#CLK duty cycle  | 35   |       | 65                       | %    |
| $t_{SU1}$             | TXTB#DATA(7:0)/TXTB#C1J1/<br>TXTB#SPE/TXTB#PAR/TXTB#FAIL set-up time to TXTB#CLK $\uparrow$  | 1.0  |       |                          | ns   |
| $t_{H1}$              | TXTB#DATA(7:0)/TXTB#C1J1/<br>TXTB#SPE/TXTB#PAR/TXTB#FAIL hold time after TXTB#CLK $\uparrow$ | 1.0  |       |                          | ns   |
| $t_{DELAY}$           | Delay from TXCFRM high and TXCCLK $\uparrow$ to C11 byte clocked in by<br>TXTB#CLK           | 0    |       | $3 \times t_{CYC1} - 22$ | ns   |
| $t_r, t_f$            | Transmit Telecom Bus interface output rise and fall times                                    | 1.3  |       | 7.0                      | ns   |

1. The J1 pulse is not shown in the timing diagram but has the same timing parameters as the C1 pulse. See Functional Relationship of the Transmit Telecom Bus Signals on page 21.
2. The dashed line shows the TXCFRM pulse when the EFRM control bit is set to '1'. The solid pulse shows the TXCFRM pulse when the EFRM control bit is set to '0'. Be aware that the  $t_{DELAY}$  window always exists with respect to the position that TXCFRM/TXCCLK $\uparrow$  has when the EFRM control bit is '0'.
3. When transmit retiming is turned off, the C1 pulse in the TXTB#C1J1 signal does not need to be aligned to the C11 byte. In this case it can be aligned to any byte in the frame.

## Receive Telecom Bus Timing

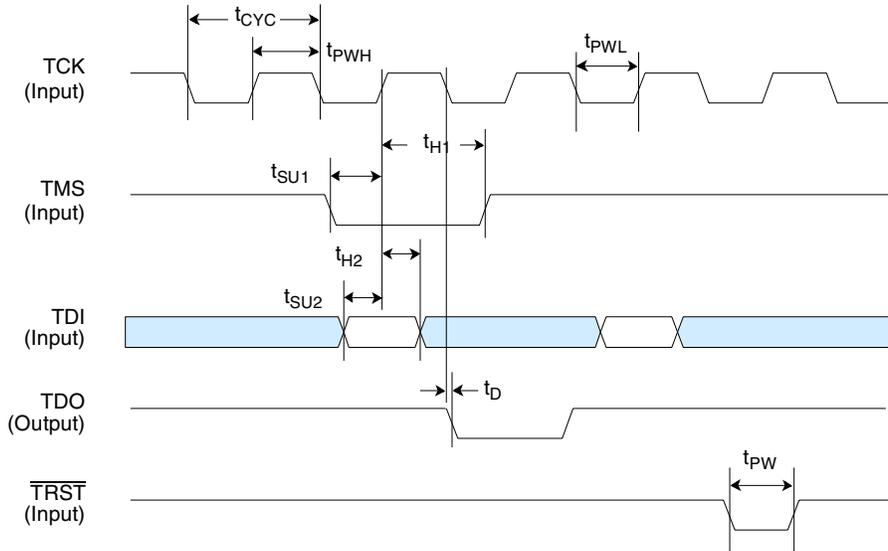


$C_L$  at outputs: 3 pF - 25 pF

| Symbol              | Parameter  | Min  | Typ   | Max  | Unit |
|---------------------|--|------|-------|------|------|
| $t_{CYC}$           | RXTB#CLK clock period  |      | 51.44 |      | ns   |
| $t_{PWH} / t_{CYC}$ | RXTB#CLK duty cycle  | 42.5 |       | 57.5 | %    |
| $t_D$               | RXTB#DATA(7:0)/RXTB#C1J1/<br>RXTB#SPE/RXTB#PAR/RXTB#FAIL delay after RXTB#CLK $\uparrow$<br>(CKINV#=1) or after RXTB#CLK $\downarrow$ (CKINV#=0) | -3.5 |       | 1.0  | ns   |
| $t_r, t_f$          | Receive Telecom Bus interface output rise and fall times   | 1.3  |       | 7.5  | ns   |

**Note:** The dashed line in the RXTB#C1J1 signal shows the position of the C1 pulse when the corresponding CPOS bit is set to '0'. When CPOS is set to '0', the J1 pulse is not present in the corresponding RXTB#C1J1 signal. The solid pulse in the RXTB#C1J1 signal shows the position of the C1 pulse when the corresponding CPOS bit is set to a '1'. When CPOS is set to '1', the J1 pulse is present in the corresponding RXTB#C1J1 signal. The J1 pulse is not shown in the timing diagram but has the same timing parameters as the C1 pulse.

## Boundary Scan Timing

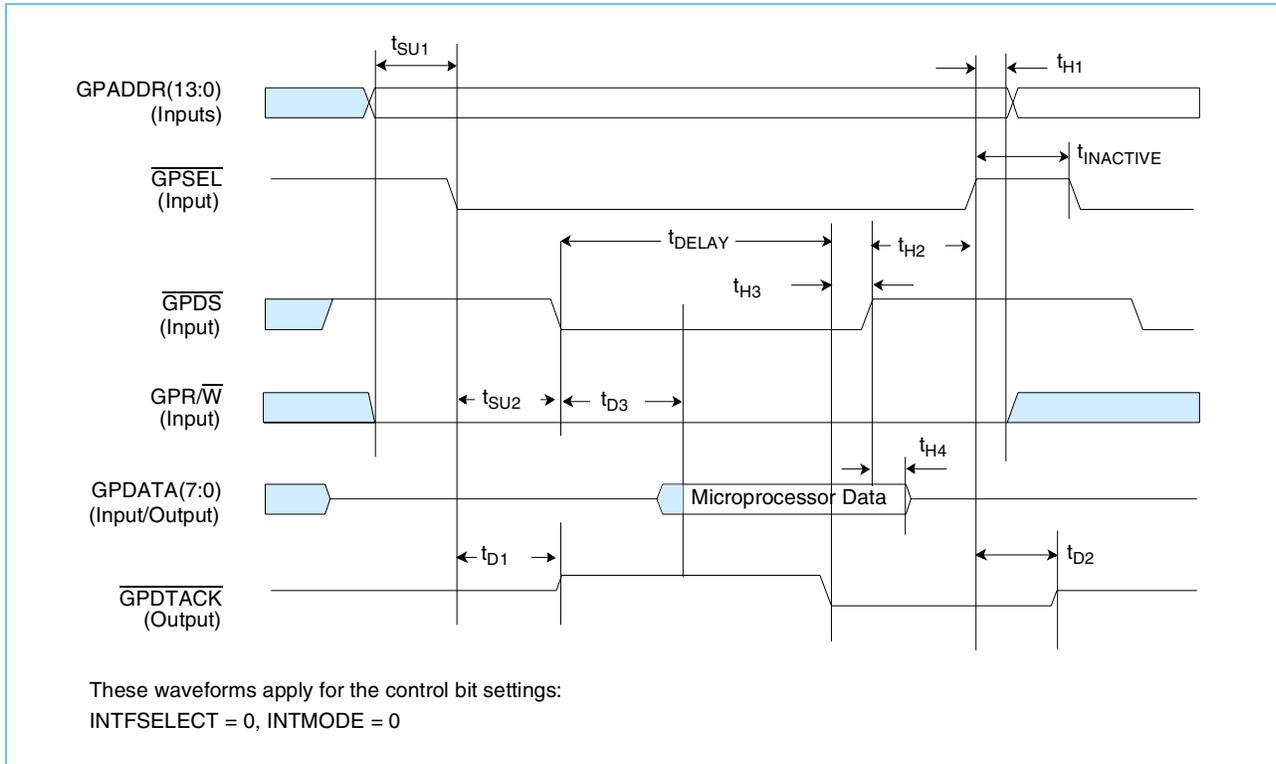


**Note:** The timing shown is for the EdgeMode bit of the OR#Conf7 register set to '1'. The timing parameters remain the same when the EdgeMode bit is set to '0', except that R1DATA# is outputted on the falling edge of the corresponding R1DCLK#. Each RX Serial DCC interface can be individually configured.

| Symbol              | Parameter <sup>1</sup>         | Min | Max | Unit |
|---------------------|--------------------------------|-----|-----|------|
| $t_{CYC}$           | TCK clock period               | 50  |     | ns   |
| $t_{PWH} / t_{PWL}$ | TCK clock pulse width high/low | 20  |     | ns   |
| $t_{SU1}$           | TMS set-up time to TCK↑        | 1.0 |     | ns   |
| $t_{H1}$            | TMS hold time after TCK↑       | 15  |     | ns   |
| $t_{SU2}$           | TDI set-up time to TCK↑        | 1.0 |     | ns   |
| $t_{H2}$            | TDI hold time after TCK↑       | 15  |     | ns   |
| $t_D$               | TDO delay from TCK↓            | 4.0 | 20  | ns   |
| $t_{PW}$            | $\overline{TRST}$ pulse width  | 50  |     | ns   |

1.  $\overline{TRST}$  should be stable during the rising transition of  $\overline{FRESET}$  at power on.

## Asynchronous Microprocessor Interface: Motorola-Type Write Cycle Timing



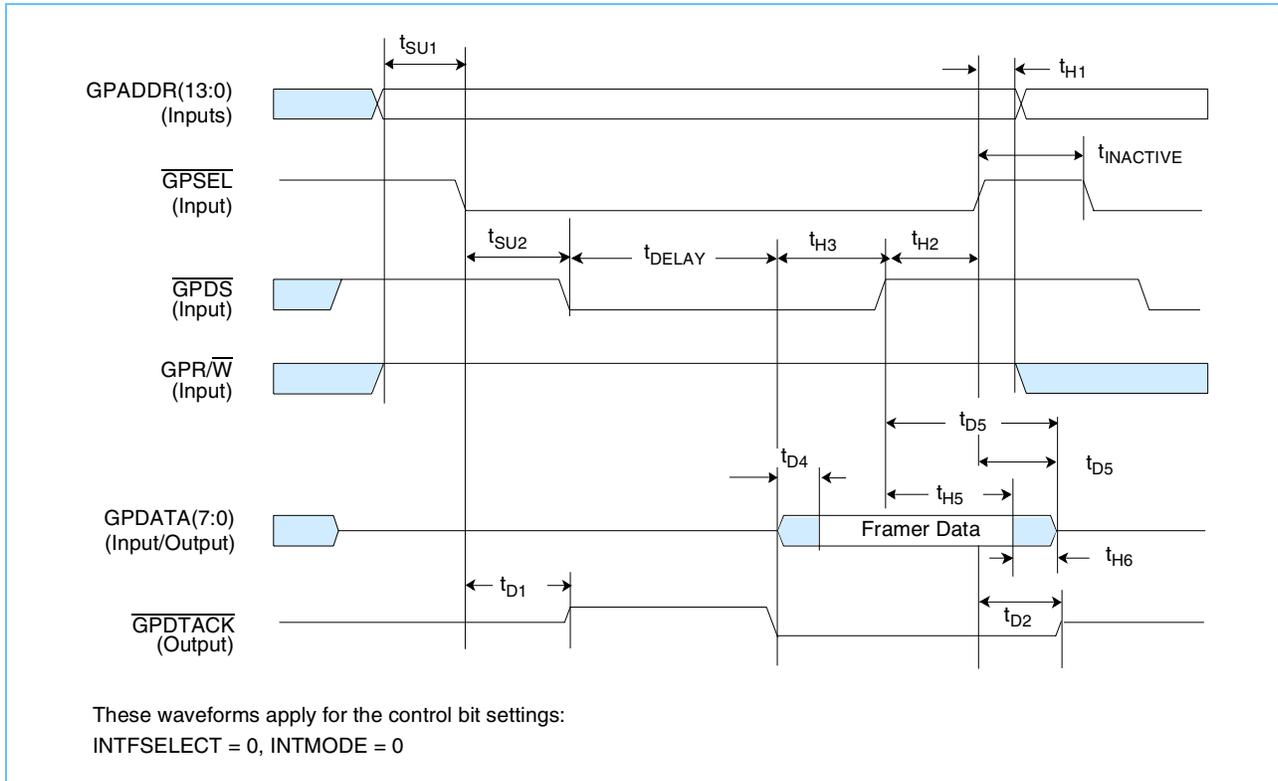
See parameter table on next page.

**IBM SONET/SDH Framer**
 $C_L$  at outputs: 5 pF - 40 pF

| Symbol              | Parameter  | Min       | Typ | Max              | Unit | Notes |
|---------------------|--|-----------|-----|------------------|------|-------|
| $t_{CYC}$           | GPPCLK clock period (not shown in diagram)                                     | 20        |     |                  | ns   | 1     |
| $t_{PWH} / t_{CYC}$ | GPPCLK duty cycle  | 40        |     | 60               | %    |       |
| $t_{SU1}$           | GPADDR(13:0)/GPR $\overline{W}$ set-up time to $\overline{GPSEL}$ assertion    | 0         |     |                  | ns   |       |
| $t_{H1}$            | GPADDR(13:0)/GPR $\overline{W}$ hold time from $\overline{GPSEL}$ de-assertion | 0         |     |                  | ns   |       |
| $t_{SU2}$           | $\overline{GPSEL}$ assertion set-up time to $\overline{GPDS}$ assertion        | -6.0      |     |                  | ns   |       |
| $t_{D1}$            | $\overline{GPSEL}$ assertion to $\overline{GPDTACK}$ valid delay               |           |     | 16               | ns   |       |
| $t_{D2}$            | $\overline{GPSEL}$ de-assertion to $\overline{GPDTACK}$ tri-state delay        | 4.0       |     | 16               | ns   | 2     |
| $t_{INACTIVE}$      | $\overline{GPSEL}$ de-assertion (high) time between accesses                   | $t_{CYC}$ |     |                  | ns   |       |
| $t_{H2}$            | $\overline{GPSEL}$ hold time from $\overline{GPDS}$ de-assertion               | 0         |     |                  | ns   |       |
| $t_{H3}$            | $\overline{GPDS}$ hold time from $\overline{GPDTACK}$ assertion                | 10        |     |                  | ns   |       |
| $t_{D3}$            | GPDATA(7:0) input valid delay from $\overline{GPDS}$ assertion                 |           |     | 20               | ns   |       |
| $t_{H4}$            | GPDATA(7:0) input valid hold from $\overline{GPDS}$ de-assertion               | 0         |     |                  | ns   |       |
| $t_{DELAY}$         | $\overline{GPDTACK}$ assertion from $\overline{GPDS}$ assertion                | $t_{CYC}$ |     | $t_{DELAY(max)}$ | ns   | 3     |

1. A clock still needs to be applied to the GPPCLK clock pin of the SONET/SDH framer even if an asynchronous microprocessor interface is used.
2. There might be a de-asserted (high) phase of  $\overline{GPDTACK}$  before turning tri-state if  $\overline{GPDS}$  is de-asserted early.
3.  $t_{DELAY(max)} = 7 \times t_{CYC} + 6 \times t_{min}$  where  $t_{min}$  is the cycle time of the lowest-frequency chiplet clock. The lowest frequency of the chiplet clocks is the lower of 6.48 MHz or the UTOPIA interface clock frequencies.

## Asynchronous Microprocessor Interface: Motorola-Type Read Cycle Timing



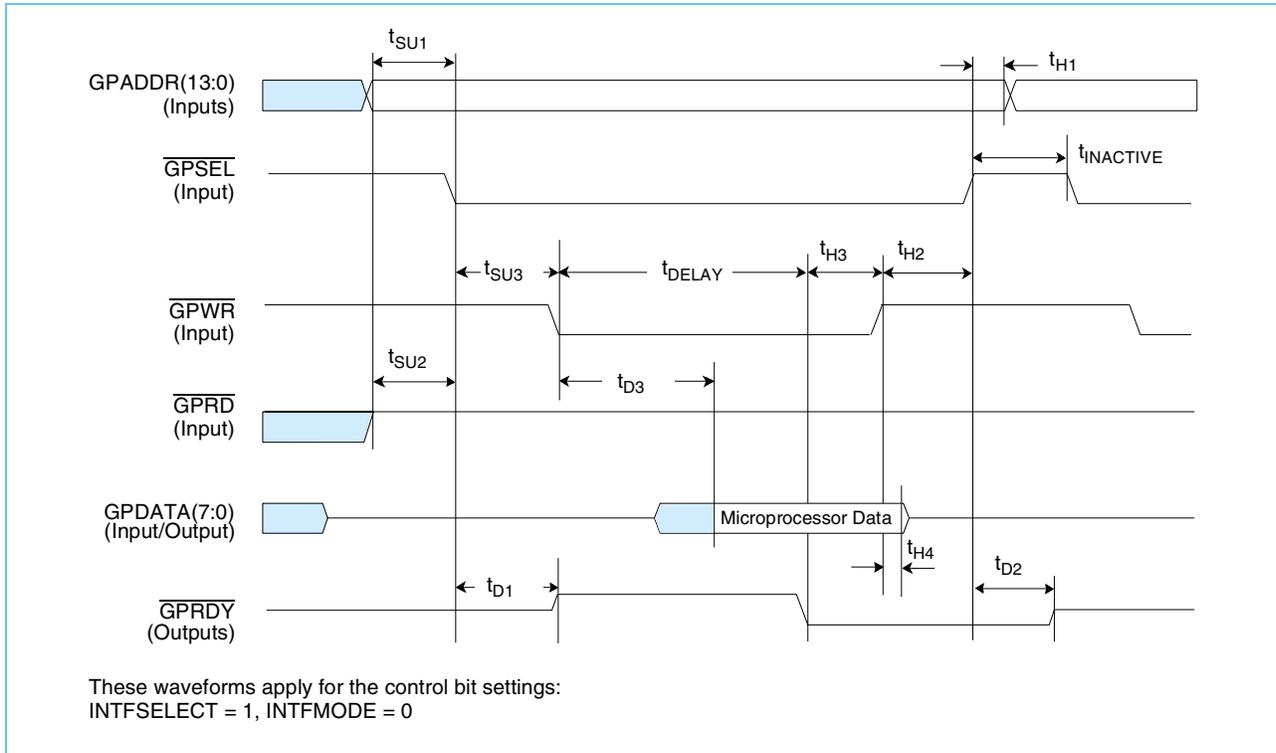
See parameter table on next page.

**IBM SONET/SDH Framer**
 $C_L$  at outputs: 5 pF - 40 pF

| Symbol              | Parameter   | Min       | Typ | Max              | Unit | Notes |
|---------------------|---|-----------|-----|------------------|------|-------|
| $t_{CYC}$           | GPPCLK clock period (not shown in diagram)  | 20        |     |                  | ns   | 1     |
| $t_{PWH} / t_{CYC}$ | GPPCLK duty cycle   | 40        |     | 60               | %    |       |
| $t_{SU1}$           | GPADDR/GPR/ $\overline{W}$ set-up time to $\overline{GPSEL}$ assertion                  | 0         |     |                  | ns   |       |
| $t_{H1}$            | GPADDR/GPR/ $\overline{W}$ hold time from $\overline{GPSEL}$ de-assertion               | 0         |     |                  | ns   |       |
| $t_{SU2}$           | $\overline{GPSEL}$ assertion set-up time to $\overline{GPDS}$ assertion                 | -6.0      |     |                  | ns   |       |
| $t_{D1}$            | $\overline{GPSEL}$ assertion to $\overline{GPDTACK}$ valid delay                        |           |     | 16               | ns   |       |
| $t_{D2}$            | $\overline{GPSEL}$ de-assertion to $\overline{GPDTACK}$ tri-state delay                 | 4.0       |     | 16               | ns   | 2     |
| $t_{INACTIVE}$      | $\overline{GPSEL}$ de-assertion (high) time between accesses                            | $t_{CYC}$ |     |                  | ns   |       |
| $t_{H2}$            | $\overline{GPSEL}$ hold time from $\overline{GPDS}$ de-assertion                        | 0         |     |                  | ns   |       |
| $t_{H3}$            | $\overline{GPDS}$ hold time from $\overline{GPDTACK}$ assertion                         | 10        |     |                  | ns   |       |
| $t_{DELAY}$         | $\overline{GPDTACK}$ assertion from $\overline{GPDS}$ assertion                         | $t_{CYC}$ |     | $t_{DELAY(max)}$ | ns   | 3     |
| $t_{D4}$            | GPDATA(7:0) output valid delay from $\overline{GPDTACK}$ assertion                      |           |     | 15               | ns   |       |
| $t_{H5}$            | GPDATA(7:0) output valid hold from $\overline{GPDS}$ de-assertion                       | 4.0       |     |                  | ns   |       |
| $t_{H6}$            | GPDATA output valid hold from $\overline{GPSEL}$ de-assertion                           | 3.0       |     |                  | ns   |       |
| $t_{D5}$            | GPDATA(7:0) output tri-state delay from $\overline{GPDS}/\overline{GPSEL}$ de-assertion |           |     | 17               | ns   |       |
| $t_r, t_f$          | GPDATA(7:0) output rise and fall times  | 0.8       |     | 8.5              | ns   |       |

1. A clock still needs to be applied to the GPPCLK clock pin of the SONET/SDH framer even if an asynchronous microprocessor interface is used.
2. There might be a de-asserted (high) phase of  $\overline{GPDTACK}$  before turning tri-state if  $\overline{GPDS}$  is de-asserted early.
3.  $t_{DELAY(max)} = 7 \times t_{CYC} + 6 \times t_{min}$  where  $t_{min}$  is the cycle time of the lowest-frequency chiplet clock.  
The lowest frequency of the chiplet clocks is the lower of 6.48 MHz or the UTOPIA interface clock frequencies.

## Asynchronous Microprocessor Interface: Intel-Type Write Cycle Timing



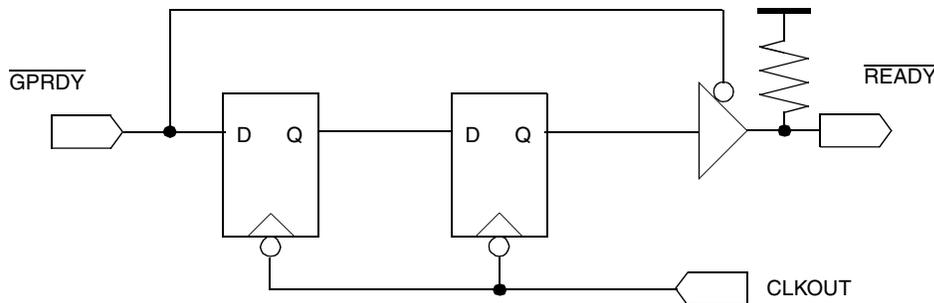
See parameter table on next page.

**IBM SONET/SDH Framer**

C<sub>L</sub> at outputs: 5 pF - 40 pF

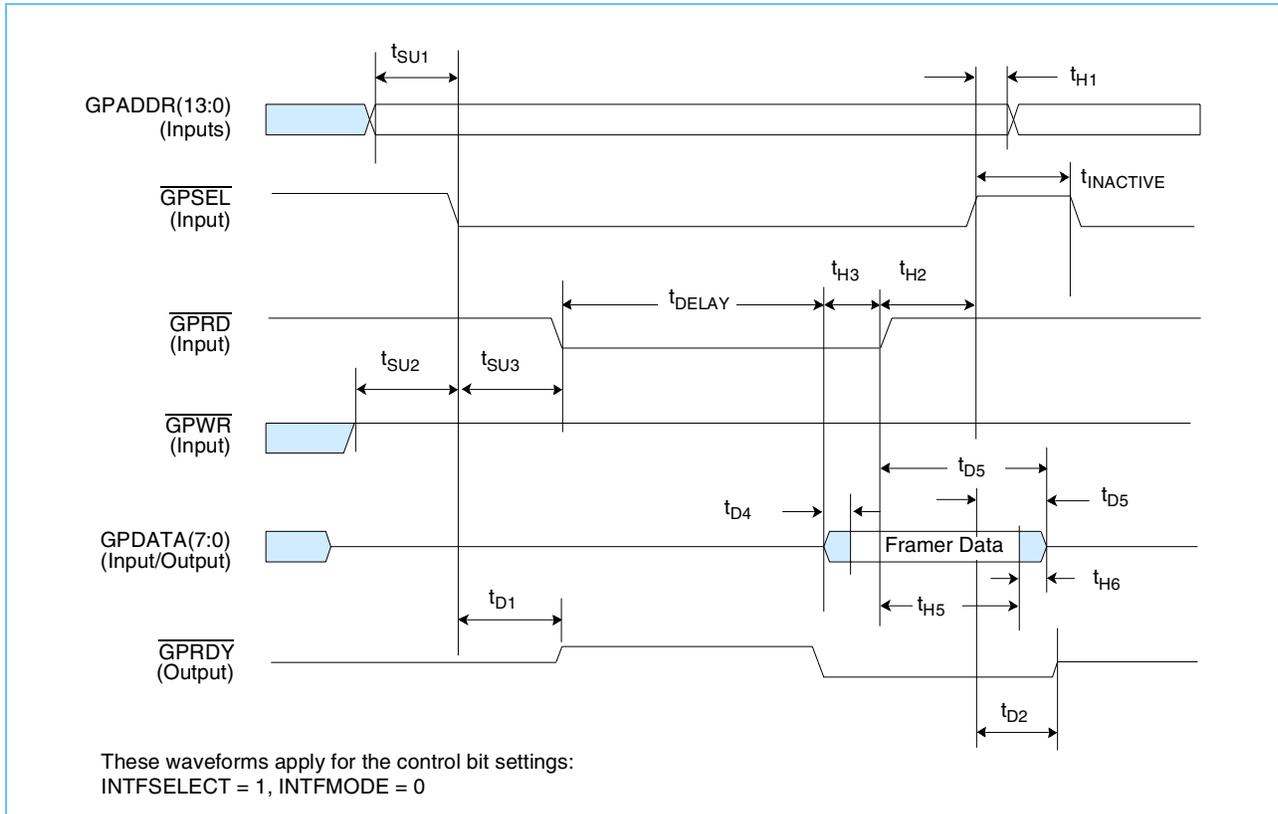
| Symbol                             | Parameter  | Min              | Typ | Max                     | Unit | Notes |
|------------------------------------|--|------------------|-----|-------------------------|------|-------|
| t <sub>CYC</sub>                   | GPPCLK clock period (not shown in diagram)   | 20               |     |                         | ns   | 1     |
| t <sub>PWH</sub> /t <sub>CYC</sub> | GPPCLK duty cycle  | 40               |     | 60                      | %    |       |
| t <sub>SU1</sub>                   | GPADDR(13:0) set-up time to $\overline{\text{GPSEL}}$ assertion                          | 0                |     |                         | ns   |       |
| t <sub>H1</sub>                    | GPADDR(13:0) hold time from $\overline{\text{GPSEL}}$ de-assertion                       | 0                |     |                         | ns   |       |
| t <sub>SU2</sub>                   | $\overline{\text{GPRD}}$ de-assertion set-up time to $\overline{\text{GPSEL}}$ assertion | 10               |     |                         | ns   |       |
| t <sub>SU3</sub>                   | $\overline{\text{GPSEL}}$ assertion set-up time to $\overline{\text{GPWR}}$ assertion    | 0                |     |                         | ns   |       |
| t <sub>D1</sub>                    | $\overline{\text{GPSEL}}$ assertion to $\overline{\text{GPRDY}}$ valid delay             |                  |     | 16                      | ns   |       |
| t <sub>D2</sub>                    | $\overline{\text{GPSEL}}$ de-assertion to $\overline{\text{GPRDY}}$ tri-state delay      | 4.0              |     | 16                      | ns   | 2     |
| t <sub>INACTIVE</sub>              | $\overline{\text{GPSEL}}$ de-assertion (high) time between accesses                      | t <sub>CYC</sub> |     |                         | ns   |       |
| t <sub>H2</sub>                    | $\overline{\text{GPSEL}}$ hold time from $\overline{\text{GPWR}}$ de-assertion           | 0                |     |                         | ns   |       |
| t <sub>H3</sub>                    | $\overline{\text{GPWR}}$ hold time from $\overline{\text{GPRDY}}$ assertion              | 10               |     |                         | ns   | 3     |
| t <sub>D3</sub>                    | GPDATA(7:0) input valid delay from $\overline{\text{GPWR}}$ assertion                    |                  |     | 20                      | ns   |       |
| t <sub>H4</sub>                    | GPDATA(7:0) input valid hold from $\overline{\text{GPWR}}$ de-assertion                  | 0                |     |                         | ns   |       |
| t <sub>DELAY</sub>                 | $\overline{\text{GPRDY}}$ assertion from $\overline{\text{GPWR}}$ assertion              | t <sub>CYC</sub> |     | t <sub>DELAY(max)</sub> | ns   | 4     |

1. A clock still needs to be applied to the GPPCLK clock pin of the SONET/SDH framer even if an asynchronous microprocessor interface is used.
2. There might be a de-asserted (high) phase of  $\overline{\text{GPRDY}}$  before turning tri-state if  $\overline{\text{GPWR}}$  is de-asserted early.
3. The Intel 286 and 386 microprocessors have synchronous  $\overline{\text{READY}}$  inputs, so external synchronization of the  $\overline{\text{GPRDY}}$  falling edge to the microprocessor clock is required to avoid metastability problems. Synchronization can be achieved by use of the circuit shown below:



4. t<sub>DELAY(max)</sub> = 7 x t<sub>CYC</sub> + 6 x t<sub>min</sub> where t<sub>min</sub> is the cycle time of the lowest-frequency chiplet clock. The lowest frequency of the chiplet clocks is the lower of 6.48 MHz or the UTOPIA interface clock frequencies.

## Asynchronous Microprocessor Interface: Intel-Type Read Cycle Timing



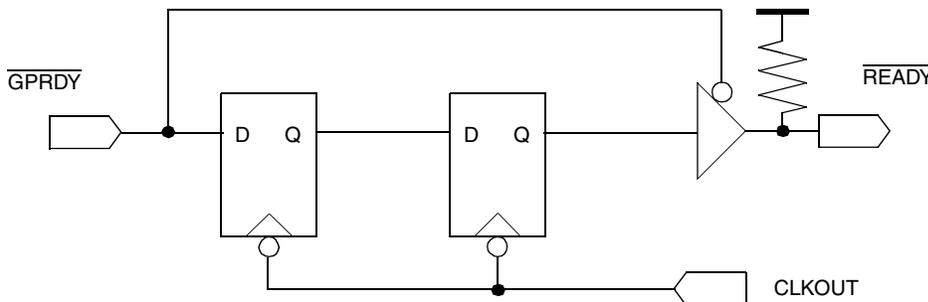
See parameter table on next page.

**IBM SONET/SDH Framer**

C<sub>L</sub> at outputs: 5 pF - 40 pF

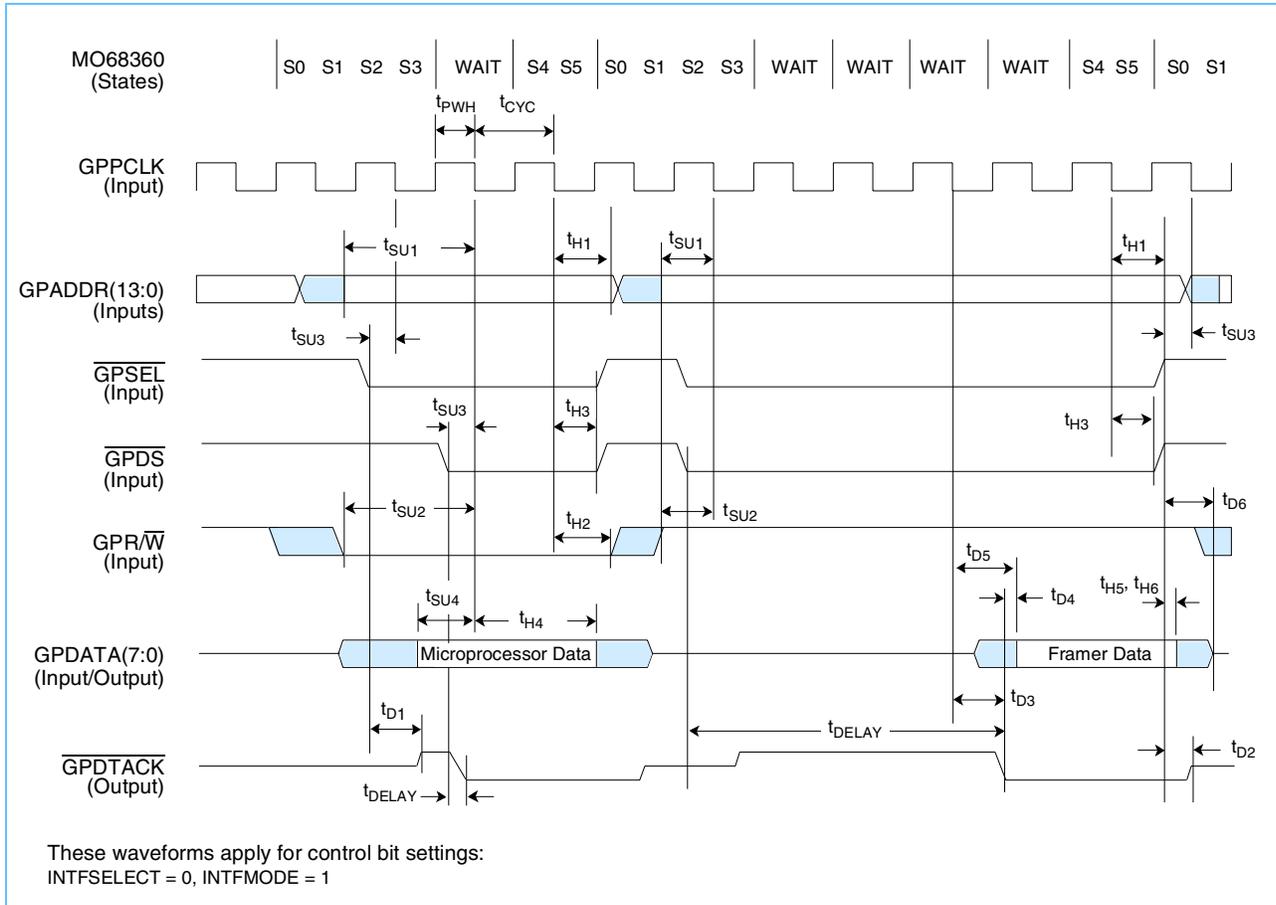
| Symbol                             | Parameter   | Min              | Typ | Max                     | Unit | Notes |
|------------------------------------|---|------------------|-----|-------------------------|------|-------|
| t <sub>CYC</sub>                   | GPPCLK clock period (not shown in diagram)  | 20               |     |                         | ns   | 1     |
| t <sub>PWH</sub> /t <sub>CYC</sub> | GPPCLK duty cycle   | 40               |     | 60                      | %    |       |
| t <sub>SU1</sub>                   | GPADDR(13:0) set-up time to $\overline{\text{GPSEL}}$ assertion                                       | 0                |     |                         | ns   |       |
| t <sub>H1</sub>                    | GPADDR(13:0) hold time from $\overline{\text{GPSEL}}$ de-assertion                                    | 0                |     |                         | ns   |       |
| t <sub>SU2</sub>                   | $\overline{\text{GPWR}}$ de-assertion set-up time to $\overline{\text{GPSEL}}$ assertion              | 10               |     |                         | ns   |       |
| t <sub>SU3</sub>                   | $\overline{\text{GPSEL}}$ assertion set-up time to $\overline{\text{GPRD}}$ assertion                 | 0                |     |                         | ns   |       |
| t <sub>D1</sub>                    | $\overline{\text{GPSEL}}$ assertion to $\overline{\text{GPRDY}}$ valid delay                          |                  |     | 16                      | ns   |       |
| t <sub>D2</sub>                    | $\overline{\text{GPSEL}}$ de-assertion to $\overline{\text{GPRDY}}$ tri-state delay                   | 4.0              |     | 16                      | ns   | 2     |
| t <sub>INACTIVE</sub>              | $\overline{\text{GPSEL}}$ de-assertion (high) time between accesses                                   | t <sub>CYC</sub> |     |                         | ns   |       |
| t <sub>H2</sub>                    | $\overline{\text{GPSEL}}$ hold time from $\overline{\text{GPRD}}$ de-assertion                        | 0                |     |                         | ns   |       |
| t <sub>H3</sub>                    | $\overline{\text{GPRD}}$ hold time from $\overline{\text{GPRDY}}$ assertion                           | 10               |     |                         | ns   | 3     |
| t <sub>DELAY</sub>                 | $\overline{\text{GPRDY}}$ assertion from $\overline{\text{GPRD}}$ assertion                           | t <sub>CYC</sub> |     | t <sub>DELAY(max)</sub> | ns   | 4     |
| t <sub>D4</sub>                    | GPDATA(7:0) output valid delay from $\overline{\text{GPRDY}}$ assertion                               |                  |     | 15                      | ns   |       |
| t <sub>H5</sub>                    | GPDATA(7:0) output valid hold from $\overline{\text{GPRD}}$ de-assertion                              | 4.0              |     |                         | ns   |       |
| t <sub>H6</sub>                    | GPDATA(7:0) output valid hold from $\overline{\text{GPSEL}}$ de-assertion                             | 3.0              |     |                         | ns   |       |
| t <sub>D5</sub>                    | GPDATA(7:0) output tri-state delay from $\overline{\text{GPRD}}/\overline{\text{GPSEL}}$ de-assertion |                  |     | 17                      | ns   |       |
| t <sub>r</sub> , t <sub>f</sub>    | GPDATA output rise and fall times   | 0.8              |     | 8.5                     | ns   |       |

1. A clock still needs to be applied to the GPPCLK clock pin of the SONET/SDH framer even if an asynchronous microprocessor interface is used.
2. There might be a de-asserted (high) phase of  $\overline{\text{GPRDY}}$  before turning tri-state if  $\overline{\text{GPRD}}$  is de-asserted early.
3. The Intel 286 and 386 microprocessors have synchronous  $\overline{\text{READY}}$  inputs, so external synchronization of the  $\overline{\text{GPRDY}}$  falling edge to the microprocessor clock is required to avoid metastability problems. Synchronization can be achieved by use of the circuit shown below:



4. t<sub>DELAY(max)</sub> = 7 × t<sub>CYC</sub> + 6 × t<sub>min</sub> where t<sub>min</sub> is the cycle time of the lowest-frequency chiplet clock. The lowest frequency of the chiplet clocks is the lower of 6.48 MHz or the UTOPIA interface clock frequencies.

## Synchronous Microprocessor Interface: Motorola-Type Write and Read Cycle Timing



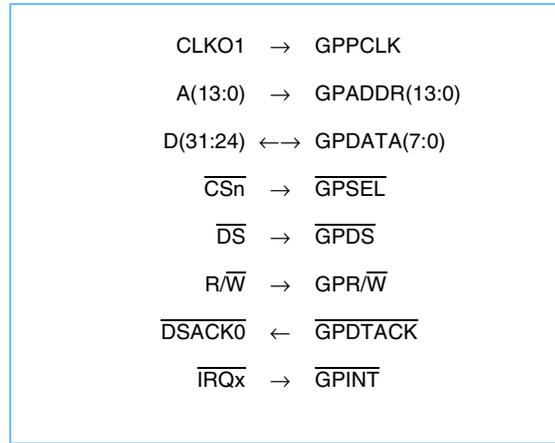
See parameter table on next page.

**IBM SONET/SDH Framer**
 $C_L$  at outputs: 5 pF - 40 pF

| Symbol            | Parameter   | Min | Typ | Max              | Unit | Notes |
|-------------------|---|-----|-----|------------------|------|-------|
| $t_{CYC}$         | GPPCLK clock period   | 30  |     |                  | ns   |       |
| $t_{PWH}/t_{CYC}$ | GPPCLK duty cycle   | 40  |     | 60               | %    |       |
| $t_{SU1}$         | GPADDR(13:0) set-up time to GPPCLK $\downarrow$   | 1.0 |     |                  | ns   | 1     |
| $t_{H1}$          | GPADDR(13:0) hold time from GPPCLK $\downarrow$   | 2.5 |     |                  | ns   | 1     |
| $t_{SU2}$         | GPR $\overline{W}$ set-up time to GPPCLK $\downarrow$                                   | 6.0 |     |                  | ns   | 1     |
| $t_{H2}$          | GPR $\overline{W}$ hold time from GPPCLK $\downarrow$                                   | 2.0 |     |                  | ns   | 1     |
| $t_{SU3}$         | $\overline{GPSEL}/\overline{GPDS}$ set-up time to GPPCLK $\downarrow$                   | 6.0 |     |                  | ns   |       |
| $t_{H3}$          | $\overline{GPSEL}/\overline{GPDS}$ hold time from GPPCLK $\downarrow$                   | 2.0 |     |                  | ns   |       |
| $t_{SU4}$         | GPDATA(7:0) set-up time to GPPCLK $\downarrow$  | 1.0 |     |                  | ns   | 2     |
| $t_{H4}$          | GPDATA(7:0) hold time from GPPCLK $\downarrow$  | 2.5 |     |                  | ns   | 2     |
| $t_{D1}$          | $\overline{GPSEL}$ assertion to $\overline{GPDTACK}$ valid delay                        |     |     | 16               | ns   | 3     |
| $t_{D2}$          | $\overline{GPSEL}$ de-assertion to $\overline{GPDTACK}$ tri-state delay                 | 4.0 |     | 16               | ns   | 4     |
| $t_{DELAY}$       | $\overline{GPDTACK}$ assertion from $\overline{GPDS}$ assertion                         | 4.5 |     | $t_{DELAY(max)}$ | ns   | 5     |
| $t_{D3}$          | $\overline{GPDTACK}$ assertion from GPPCLK $\downarrow$                                 | 5.0 |     | 20.5             | ns   | 6     |
| $t_{D4}$          | GPDATA(7:0) output valid delay from $\overline{GPDTACK}$ assertion                      |     |     | 15               | ns   |       |
| $t_{D5}$          | GPDATA(7:0) output delay from GPPCLK $\downarrow$                                       |     |     | 18.0             | ns   | 7     |
| $t_{H5}$          | GPDATA(7:0) output valid hold time from $\overline{GPDS}$ de-assertion                  | 4.0 |     |                  | ns   |       |
| $t_{H6}$          | GPDATA(7:0) output valid hold from $\overline{GPSEL}$ de-assertion                      | 3.0 |     |                  | ns   |       |
| $t_{D6}$          | GPDATA(7:0) output tri-state delay from $\overline{GPDS}/\overline{GPSEL}$ de-assertion |     |     | 17               | ns   |       |
| $t_r, t_f$        | GPDATA(7:0) output rise and fall times  | 0.8 |     | 8.5              | ns   |       |

1. This parameter applies to clock transitions during the  $\overline{GPDS}$  asserted phase only (when the device is selected); asynchronous signals are acceptable if GPADDR(13:0) and GPR $\overline{W}$  change early in the access cycle.
2. Input data is latched by the SONET/SDH framer at the falling clock edge of the last or second to last microprocessor WAIT state (the microprocessor is detecting  $\overline{GPDTACK}$  asserted at the same time or  $t_{CYC}$  later).
3. Depending on the relative speeds of the microprocessor and the SONET/SDH framer,  $\overline{GPDTACK}$  might switch from tri-state to asserted state directly (applies only to the first write cycle after the interface was idle).
4. There might be a de-asserted (high) phase of  $\overline{GPDTACK}$  before turning tri-state if  $\overline{GPDS}$  is de-asserted early.
5. The value shown for  $t_{DELAY(min)}$  applies to the first write cycle after the interface was idle. For all read cycles and for write cycles with more than one microprocessor WAIT cycle  $t_{DELAY(min)} = t_{CYC}$ .  $t_{DELAY(max)} = 5 \times t_{CYC} + 6 \times t_{min}$ , where  $t_{min}$  is the cycle time of the lowest-frequency chiplet clock. The lowest frequency of the chiplet clocks is the lower of 6.48 MHz or the UTOPIA interface clock frequencies.
6. The  $t_{D3}$  symbol applies to all read cycles and to write cycles with more than one microprocessor WAIT cycle.
7. The microprocessor latches SONET/SDH framer data at the end of state S4. This is  $t_{CYC}$  after detecting  $\overline{GPDTACK}$  asserted.

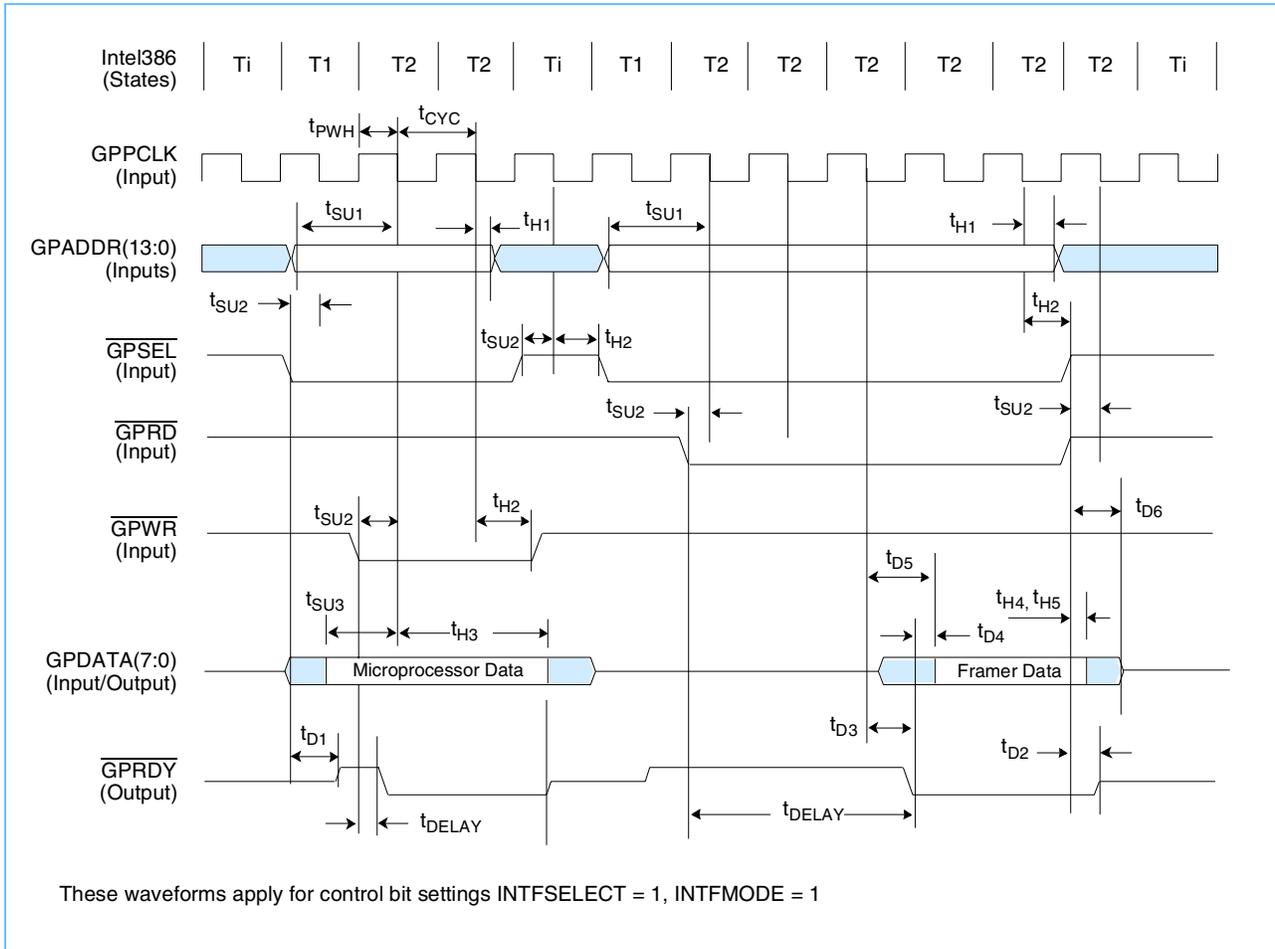
**Note:** The microprocessor interface of the SONET/SDH framer can be directly connected to a Motorola MC68360 microprocessor running synchronously at 25 MHz or 33.34 MHz. The connections are as follows:



The following conditions must be established for proper operation:

- Signal delay skew from MC68360 to SONET/SDH framer between +0 ns and +5 ns versus CLKO1 delay.
- Minimum total round-trip delay (CLKO1-> GPPCLK,  $\overline{GPDTACK}$ ->  $\overline{DSACK0}$ ) of 3 ns ( $t_{CYC} = 30$  ns) or 5 ns ( $t_{CYC} = 40$  ns); this avoids a possible fast path.
- The SONET/SDH framer must be deselected ( $\overline{GPSEL}$  high) between two accesses.

### Synchronous Microprocessor Interface: Intel-Type Write and Read Cycle Timing



See parameter table on next page.

$C_L$  at outputs: 5 pF - 40 pF

| Symbol              | Parameter   | Min | Typ | Max              | Unit | Notes |
|---------------------|---|-----|-----|------------------|------|-------|
| $t_{CYC}$           | GPPCLK clock period   | 30  |     |                  | ns   |       |
| $t_{PWH} / t_{CYC}$ | GPPCLK duty cycle   | 40  |     | 60               | %    |       |
| $t_{SU1}$           | GPADDR(13:0) set-up time to GPPCLK↓   | 1.0 |     |                  | ns   | 1     |
| $t_{H1}$            | GPADDR(13:0) hold time from GPPCLK↓   | 2.5 |     |                  | ns   | 1     |
| $t_{SU2}$           | $\overline{GPSEL}/\overline{GPWR}/\overline{GPRD}$ set-up time to GPPCLK↓               | 6.0 |     |                  | ns   |       |
| $t_{H2}$            | $\overline{GPSEL}/\overline{GPWR}/\overline{GPRD}$ hold time from GPPCLK↓               | 2.0 |     |                  | ns   |       |
| $t_{SU3}$           | GPDATA(7:0) input set-up time to GPPCLK↓  | 1.0 |     |                  | ns   |       |
| $t_{H3}$            | GPDATA(7:0) input hold time from GPPCLK↓  | 2.5 |     |                  | ns   |       |
| $t_{D1}$            | $\overline{GPSEL}$ assertion to $\overline{GPRDY}$ valid delay                          |     |     | 16               | ns   |       |
| $t_{D2}$            | $\overline{GPSEL}$ de-assertion to $\overline{GPRDY}$ tri-state delay                   | 4.0 |     | 16               | ns   | 2     |
| $t_{DELAY}$         | $\overline{GPRDY}$ assertion from $\overline{GPWR}/\overline{GPRD}$ assertion           | 4.5 |     | $t_{DELAY(max)}$ | ns   | 3     |
| $t_{D3}$            | $\overline{GPRDY}$ assertion from GPPCLK↓   | 5.0 |     | 20.5             | ns   | 4     |
| $t_{D4}$            | GPDATA(7:0) output valid delay from $\overline{GPRDY}$ assertion                        |     |     | 15               | ns   |       |
| $t_{D5}$            | GPDATA(7:0) output delay from GPPCLK↓   |     |     | 18.0             | ns   |       |
| $t_{H4}$            | GPDATA(7:0) output valid hold time from $\overline{GPRD}$ de-assertion                  | 4.0 |     |                  | ns   |       |
| $t_{H5}$            | GPDATA(7:0) output valid hold from $\overline{GPSEL}$ de-assertion                      | 3.0 |     |                  | ns   |       |
| $t_{D6}$            | GPDATA(7:0) output tri-state delay from $\overline{GPRD}/\overline{GPSEL}$ de-assertion |     |     | 17               | ns   |       |
| $t_r, t_f$          | GPDATA(7:0) output rise and fall times  | 0.8 |     | 8.5              | ns   |       |

1. This parameter applies to clock transitions during the  $\overline{GPRD}/\overline{GPWR}$  asserted phase only (when the device is selected); asynchronous signals are acceptable if GPADDR(13:0) change early in the access cycle.
2. There might be a de-asserted (high) phase of  $\overline{GPRDY}$  before turning tri-state if  $\overline{GPRD}/\overline{GPWR}$  is de-asserted early.
3. To avoid a fast path ( $\overline{GPRDY} \rightarrow \overline{READY}$ ,  $\overline{WR} \rightarrow \overline{GPWR}$ ) with the Intel 286 and Intel 386 microprocessors, two internal WAIT states should be programmed in the device select unit of the microprocessor. Alternatively, the use of a double D-Flip Flop is recommended to delay and re-synchronize the  $\overline{GPRDY}$  falling edge to the microprocessor clock.  $t_{DELAY(max)} = 5 \times t_{CYC} + 6 \times t_{min}$ , where  $t_{min}$  is the cycle time of the lowest-frequency chiplet clock. The lowest frequency of the chiplet clocks is the lower of 6.48 MHz or the UTOPIA interface clock frequencies.
4. The  $t_{D3}$  symbol applies to all read and write cycles with more than one microprocessor WAIT cycle.

**Note:** The microprocessor interface of the SONET/SDH framer cannot be directly connected to an Intel 286 or Intel 386 microprocessor at 25 MHz or 33.34 MHz clock frequency in synchronous mode because of the large spread in the timing specifications of these devices. Either device pre-selection for speed, or external re-synchronizing logic, or a reduction of the microprocessor clock frequency is required for proper operation. The SONET/SDH framer must be deselected ( $\overline{GPSEL}$  high) between two accesses. It is not recommended to use the synchronous Intel-type interface due to the requirement for special measures that is indicated Synchronous Microprocessor Interface: Intel-Type Write and Read Cycle Timing on page 86.

## Operation

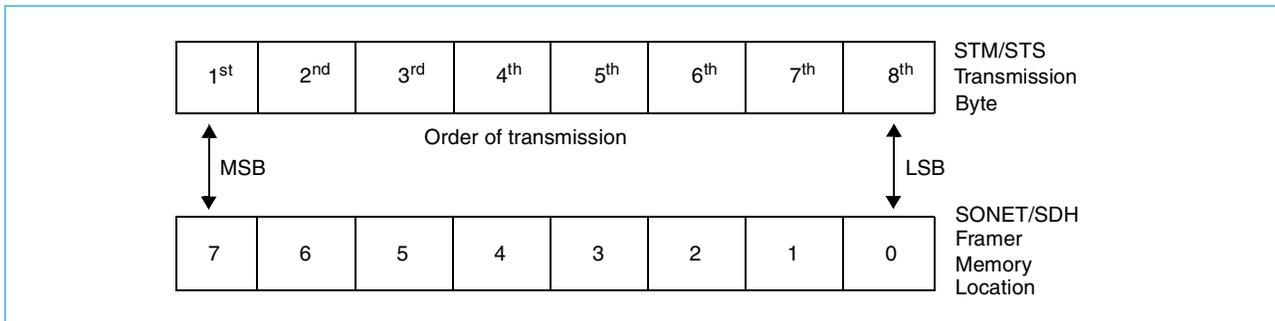
This Operation section provides additional detailed information on the operation of the functional units and processes of the SONET/SDH framer. It is by no means exhaustive and should be read in conjunction with the information contained in the other sections of this databook.

It should be noted that interrupt requests are not rationalized in the SONET/SDH framer hardware. That is, lower level alarms are not inhibited by higher level alarms. The rationalization of alarms needs to be handled in the software that monitors the SONET/SDH framer.

## Memory Map Bit Ordering

The memory map of the SONET/SDH framer is partitioned into named “chiptlet” segments, as shown in the table Chiptlet Address Map on page 110. Chiptlets are synonymous with “functional blocks”. Several chiptlets can make up a higher level functional block, like those shown in the High Level Block Diagram on page 7. For example, the UTOPIA Level1/2/2+ block in the block diagram is made up of the ACI\_xxx and PH\_xxx chiptlets, the APH block is composed of the ACH\_xxx and PPP chiptlets, the SFH blocks are composed of the OFP\_xxx chiptlets, the Telecom Bus block is not composed of chiptlets but is controlled by the GPPINT and OFP\_xxx chiptlets, the LIU blocks are also not composed of chiptlets but are controlled by the GPPINT chiptlet, and the T/RACC is a part of the ACH\_xxx chiptlets.

Memory map address locations are stated in Hexadecimal (H). The bit placement relationship between a receive and transmit serial SDH/SONET (STM/STS) byte (for example, C1) and its corresponding storage location in the SONET/SDH framer memory map is shown below:



## Chiplet-to-Clock Assignments

The GPPCLK input signal needs to be present to operate the GPPINT chiplet. The corresponding clocks for the other chiplets need to be present or access to those chiplets via the microprocessor interface will not succeed and will result in the watchdog timer timing out and a corresponding interrupt not being issued. The chiplets and the corresponding clocks that need to be present in order to access them are listed below. In the table and the text that follow, # refers to the macro number: 1, 2, 3, or 4.

| Chiplet / External Interface | Clock   |
|------------------------------|---|
| ACI_Tx1                      | TXUCLK1   |
| ACI_Tx2                      | TXUCLK2   |
| ACI_Rx1                      | RXUCLK1   |
| ACI_Rx2                      | RXUCLK2   |
| PH_Tx#                       | Depends on the setting of the PHT#(2:0) bits in the PHTXGP1 and PHTXGP2 global configuration registers. The clock can be either TXUCLK1, TXUCLK2, or ACHCLK (internal transit mode). If the PHT#(2:0) and PHR#(2:0) bits are contradictory, the PHT#(2:0) setting takes priority. |
| PH_Rx#                       | Depends on the setting of the PHR#(2:0) bits in the PHRXGP1 and PHRXGP2 global configuration registers. The clock can be either RXUCLK1, RXUCLK2, or ACHCLK (internal transit mode). If the PHT#(2:0) and PHR#(2:0) bits are contradictory, the PHT#(2:0) setting takes priority. |
| ACH_Tx#                      | ACHCLK  |
| ACH_Rx#                      | ACHCLK  |
| PPP                          | ACHCLK  |
| OFF_Tx#                      | Transmit line clock synthesized from REFCLKT/E or TX_BYCLKINT/E.  |
| OFF_Rx#                      | Corresponding recovered receive line clock or RXBYCLK1.   |
| GPPINT                       | GPPCLK  |
| Transmit Telecom Bus         | TXTB#CLK  |
| Receive Telecom Bus          | Corresponding recovered receive line clock or RXBYCLK1.   |
| AIP_TX <sup>1</sup>          | TXRINGCLK   |
| AIP_RX <sup>1</sup>          | Transmit line clock synthesized from REFCLKT/E or TX_BYCLKINT/E.  |

1. External interfaces, part of OFF\_xxx chiplets.

Other chiplets, or parts of chiplets, have their clocks selected according to global configuration parameter settings. For example, the ACB\_Tx# FIFOs write logic has the same clock as the corresponding PH\_Tx# port handler, whereas the read logic is always clocked by ACHCLK. The SDB\_Tx# FIFO's write port can be driven by TXTB#CLK (if GContTx# = '11') or ACHCLK (GContTx# /= '11'), whereas the read logic is always driven by the same clock as OFF\_Tx#.

## Line Interfaces

The SONET/SDH framer provides four serial line interfaces with differential I/O and integrated clock recovery and synthesis for STM-1/4/4c or STS-3c/STS-12/12c applications. Line Interface #1 can handle 622.08 Mb/s or 155.52 Mb/s data rates. Line interfaces #2 - #4 handle 155.52 Mb/s data rates. Either of two reference clock sources (TTL or differential pseudo-ECL) for transmit clock synthesis can be selected via the Tx\_RefSelS control bit in the SIMTConf2 register. The frequency of the reference clocks can be selected via the Tx\_RefFrq(2:0) control bits in the SIMTConf1 register to be either 19.44, 38.88, 51.84, 77.76, or

## IBM SONET/SDH Framer

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155.52 MHz (only for the pseudo-ECL input). Additionally, a divided-down version of the synthesized transmit SONET/SDH clock is provided on the TXDCLK pin. This pin can be enabled or disabled via the Tx\_DivEnt bit in the SIMTConf2 register. The frequency of the divided clock on the TXDCLK pin can be selected via the Tx\_DivFrq(2:0) control bits in the SIMTConf1 register to be either 19.44, 38.88, 51.84, or 77.76 MHz. In the receive direction, divided-down versions of the recovered clocks from the four macros are provided on four pins (RXDCLK#). The frequencies of the clocks on the RXDCLK# pins can be individually selected to be either 19.44, 38.88, 51.84, or 77.76 MHz via the Rx\_DivFrq#(2:0) bits in the SIMRConf1 and SIMRConf2 registers. The Rx\_DivEnt# bits in the SIMRConf4 register can be used to enable or disable the outputs of their respective RXDCLK# pins.

A byte-parallel interface is provided for STM-16/STS-48 multi-device applications as well as byte-parallel STM-4/4c/STS-12/12c single device applications. Off-chip byte clock recovery and synthesis are required when using the byte-parallel interface. The receive parallel data must be byte-aligned to the bytes in the incoming SONET/SDH frame.

Four low power inputs (TXLPOW#) and Loss of Signal inputs (LOSSSIG#) are provided for monitoring external interface circuitry for low power or loss of signal conditions. Also a lock detect status input is provided to monitor external clock recovery circuitry. When any of these pins are asserted high, a corresponding maskable interrupt request bit is set. Five control pins (TXSDOWN# and RSTCREC1) are provided for controlling external line interface circuitry via the register map of the SONET/SDH framer. The TXSDOWN# pins can be used to turn the lasers of a fiber optic module on or off. The RSTCREC1 pin can be used to reset an external clock recovery device.

When the byte-parallel line interface is used, a Frame Pulse input (FP1) is provided by an external deserializer/demux to identify the frame boundary. The A2Frm(1:0) bits in the OFPRXGP2 register can be programmed to indicate the location of the FP1 pulse in the RXPDAT1(7:0) stream. An OOF1 control signal is provided for controlling the byte and frame synchronization for an external deserializer/demux device. OOF1 is asserted to indicate to the external deserializer/demux device to resynch to the SONET/SDH frame pattern. If an out of frame condition does not exist, OOF1 is low. If then n (n=4 or 5, configurable) consecutive bad framing patterns are received, OOF1 goes high. This should cause the external deserializer/demux device to resynchronize to the framing pattern. The external deserializer/demux will pulse FP1 high for one clock cycle as it resynchronizes. If the next framing pattern after the pulse on FP1 is correct, the OOF1 will be driven low and remain low. If this framing pattern is incorrect, OOF1 will be driven low for two clock cycles and then driven high again to force the deserializer/demux device to resynchronize to the frame pattern. If three consecutive frame periods elapse since the low to high transition of OOF1 and no pulse has been received on FP1, OOF1 will be driven low for two clock cycles and then driven high again.

## Receive Transport Overhead Byte Processing

All 81 incoming overhead bytes for each individual STM-1/STS-3c or 324 overhead bytes for STM-4/STM-4c/STS-12/STS-12c are written into the OFP\_Rx# GRA locations. Each of the four SFH block processes the TOH associated with its corresponding receive STM-1/STS-3c. When STM-4/4c or STM-12/12c streams are being processed, SFH 1 processes the receive TOH from slot 1 of the frame. B2 errors are accumulated in SFH 3 since the transmit Z23/M1 byte resides in slot 3 of the transmitted frame. All of the receive SONET/SDH TOH bytes are passed through the SONET/SDH framer when operating in the Telecom Bus mode. When processing PPP or ATM data, the TOH is terminated in the SONET/SDH framer. Descrambling of the line signals can optionally be disabled. The descrambler consists of a frame synchronous descrambler with polynomial of  $1+X^6+X^7$ . The B1 byte is checked for errors and the errors are counted in a 16-bit counter. Four separate counters are provided for up to 4 x STM-1/STS-3c operation. Separate B1 block error counters are also provided.

The SONET/SDH framer also performs a B2 BIP-24 parity check. 16-bit counters with two programmable thresholds each (for signal fail and signal degradation detection) are provided for counting B2 BIP-24 bit errors. B2 BIP-24 Block errors are counted in 16-bit performance counters. Two programmable thresholds are provided for each B2 BIP-24 block error counter. The BIP-24 error counts are optionally provided for transmission as line FEBE in the Z23/M1 byte. The source is either local, or from the mate SONET/SDH framer in a ring configuration via the ring port.

The number of consecutive errored framing patterns and the number of bits monitored (all or 12) for OOF can be configured via the Algo#(1:0) control bits in the PIMRConf2 register. Programmable timer (0, 1, 2, or 3 ms) is provided for setting the entering or leaving of the LOF state.

Line AIS is automatically inserted downstream within two frames, when a LOF or LOS condition is detected.

A 16-byte long J0 message is stored in the receive GRA. A maskable interrupt request is generated when the received J0 message does not match a microprocessor-written message. J0 processing can be optionally disabled or enabled via a control bit.

The K1 and K2 bytes are debounced and placed in the OT#Stat3 and OT#Stat4 registers. If K1 and the first five MSBs of K2 are equal and new for three (SONET) or five (SDH) consecutive frames, the debounced values in OT#Stat3 and OT#Stat4 are updated. If the ring port is enabled, the new debounced values along with a New APS indication are sent to a mate SONET/SDH framer. In addition, bits 6, 7, and 8 of the K2 byte are monitored for a line RDI (110<sub>2</sub>) and a line AIS (111<sub>2</sub>) indication. If the ring port is enabled, alarm status can be provided, along with interrupt mask bits at the mate SONET/SDH framer. Line RDI status is also provided for a mate SONET/SDH framer in a ring configuration (Ring Port on page 24) when the ring port is enabled. MS-AIS is translated into MS-RDI in the transmit direction within two frames. If enabled by the SFen control bit, excessive error defects can also cause an MS-RDI to be sent in the transmit direction within two frames.

The H1 and H2 bytes for an STM-1 VC-4/STS-3c format and the three H1 and H2 pointer bytes for STS-3 are processed by pointer tracking state machines to determine the location of the J1 byte in the VC-4 format, or each of the three J1 bytes in the STS-3 STS-1 formats. The pointer tracking state machine is designed to meet the current ETSI and Bellcore standards (see Pointer Tracking Interpretation on page 103). In addition, when operating with the STS-3c/STS-3 formats, the AIS to LOP transition and the ss-bit checks can be disabled to conform to Bellcore/ANSI standards. Upon device reset, the pointer tracking state machines are forced to the AIS state. Pointer increments, pointer decrements, and New Data Flag (NDF) indications are counted in their corresponding 8-bit counters. The pointer is also monitored for path AIS and LOP, and interrupt request bits are provided. For STM-4c and STS-12c frames, macros 2-4 monitor the continuous reception of concatenation indicators and occupy LOP or AIS states (signaled as interrupts) according to the state machine shown in G.783 annex C.2.

## IBM SONET/SDH Framer

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The Z23/M1 byte can be monitored for a line FEBE/REI count in a 16-bit performance counter. A control bit is provided to enable the line FEBE/REI counter to count line FEBE/REI block errors. When operating in 4 x STM-1/STS-3c mode, any counts greater than 18H are counted as 00H. When STM-4/4c or STS-12/12c frames are being processed, counts greater than 60H are counted as 00H. For OC-48/STM-16 any count is accepted.

The received Regenerator Section DCC bytes (D1-D3) or the Multiplex Section Regenerator bytes (D4-D12) can be output to an external interface. Four of these interfaces are provided, one for each STM-1/STS-3c or one for each channel of an STM-4/4c or STS-12/12c frame. When a STM-4/4c or STS-12/12c frame is being processed, only DCC port 1 should be used as there is only one set of DCC bytes in the first channel of those frames.

The received S1 byte is checked against a microprocessor-written expected value. An interrupt is raised when a mismatch between the microprocessor-written expected value and the received value persists for a number of consecutive frames.

No processing is performed on the receive TOH bytes that are reserved for national use or international standardization.

## Transmit Transport Overhead Byte Processing

All 81 outgoing overhead bytes for each individual STM-1/STS-3c or 324 overhead bytes for STM-4/STM-4c/STS-12/STS-12c are stored in the OFP\_Tx# GRA locations by internal logic where they are retrieved for transmission or for access by a microprocessor. Scrambling of the line signals is provided and can optionally be disabled. The scrambler consists of a frame synchronous scrambler with polynomial of  $1+X^6+X^7$ . When operating in the Telecom Bus mode, the pointer bytes can be calculated internally (VC-4 mode) or can be sourced from the TELECOM Bus interface. Additional 16-byte blocks are provided in the transmit GRAs for transmitting a 16-byte long microprocessor-written J0 message. Optionally C1 byte transmission can be performed for STS slot identification purposes instead of the 16-byte J0 message.

B1 and B2 byte calculations are performed for either four individual STS-3c/STM-1 streams or for a single STS-12/12c or STM-4/4c stream. B1 and B2 bytes can be corrupted for a single frame by writing to the desired B1 or B2 location in the transmit GRA.

Four ports are provided for sourcing either the three Regenerator Section DCC bytes (D1-D3) or the Multiplex Section DCC bytes (D4-D12) associated with the four STM-1/STS-3c streams. The DCC bytes can also be sourced from the transmit GRA.

When MS-AIS is detected in the receive direction it is translated into MS-RDI in the transmit direction within two frames. If enabled by the SFen control bit, excessive receive error defects can also cause an MS-RDI to be sent in the transmit direction within two frames. MS-RDI can also be forced via software control.

MS-AIS can be forced under software control. MS-AIS is all ones in the Multiplex Section bytes and AU-4 bytes.

MS-REI (M1/Z23 byte) generation is based on receive B2 errors. For STM-1/STS-3c operation, receive B2 errors are turned around into MS-REI (in the transmit Z23/M1 byte) on a per SFH basis. For STM-4/4c or STS-12/12c operation, the receive B2 errors from all four SFHs are accumulated and are then turned around into MS-REI (in the transmit Z23/M1 byte) in transmit SFH 3. For OC-48/STM-16 applications (where four SONET/SDH framers are used), the B2 errors from the SFH blocks of each SONET/SDH framer are accumulated and then transferred to SONET/SDH framer 1 where they are summed in SFH 1, and then sent out as an MS-REI (in the transmit Z23/M1 byte). In OC-48/STM-16 mode, if the summed B2 error count is greater than FFH, it is truncated at FFH since the transmit M1 byte is only 8 bits long.

Outgoing Pointer Adjustment events and NDF events are counted in 8-bit counters. Pointer processing is performed per [G.783], [G.707], and [GR-253]. AU-4 Pointer adjustments, NDF events, and pointer defect events are counted in 8-bit counters. Optional transmit pointer retiming can be enabled for transmit Telecom Bus, ATM, or PPP applications. For ATM/PPP applications, the AU-4 pointer offset can be fixed to '0'.

**Note:** No processing is performed on the receive TOH bytes that are reserved for national use or international standardization.

## APS Functions

An integrated cross connect is provided for APS applications. For single device operation, 1:3 multiplex section trail protection can be achieved. If a multi-device configuration is implemented, a 1:N (N can range from 1 up to 14) multiplex section trail protection can be realized through the external bidirectional APS interface (see RACC and TACC - Receive/Transmit APS Cross Connect on page 9). Three maskable interrupt request bits are provided for indicating to the external microprocessor that a potential bridge, switch, or switch release is being requested and that the receive K1 and K2 bytes need to be read and interpreted. Based on the receive K1 and K2 bytes, the APSSELECT bits in the HT1Conf14 register and the ApsSource bits in the HR1Conf11 register can be written with the appropriate code to cause a bridge to the protection channel or switch to the protection channel as desired. A control bit (Pchan) is provided in each macro to enable a particular channel as the protection channel in order to cause the K1 bytes of the working channels to be ignored. An 8-bit counter is provided for counting parity errors that are detected on the APS bus.

## Transmit/Receive Higher-Order Path Connection Function Layer Options

The SONET/SDH framer has the ability to fold back a receive VC-4 from any of the four SFH Macros and assign them to any transmit VC-4 via software control. For instance, the receive VC-4 from STM-1 #1 can be folded back and applied to transmit VC-4 of STM-1 #3. In short, only the logical order of the VC-4 is changed. The higher-order path connection function can also be performed under software control at the TCS Function (TCSF) where only the C-4 s are folded back. This applies only to ATM-PPP mode.

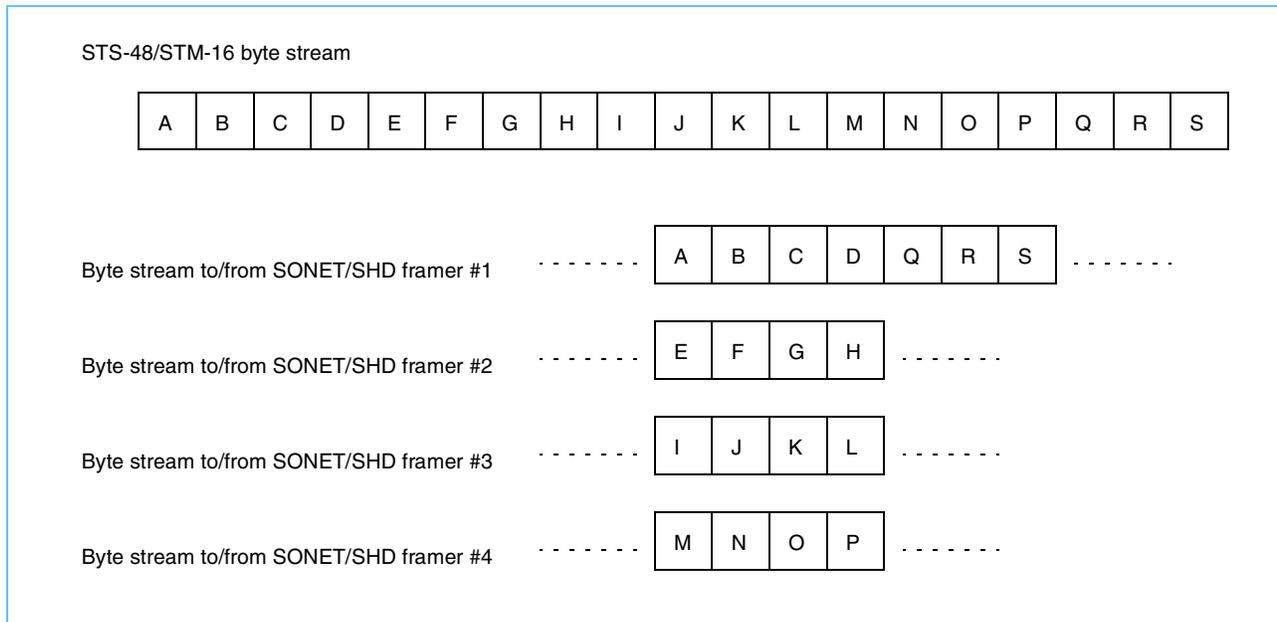
## OC-48/STM-16 Expansion Port

The SONET/SDH framer can be combined with three other SONET/SDH framers to form an STS-48 or STM-16 signal that consists of either 4 x STM-4, 4 x STM-4c, 4 x STS-12, or 4 x STS-12c. The parallel line interfaces are used in this application. A MUX/DEMUX device that performs clock recovery and synthesis is needed to interface the OC-48 or STM-16 serial stream to the SONET/SDH framers. The FP1 pulse in the receive direction should be aligned to the first SPE/VC-4 byte in the first row of the SONET/SDH frame.

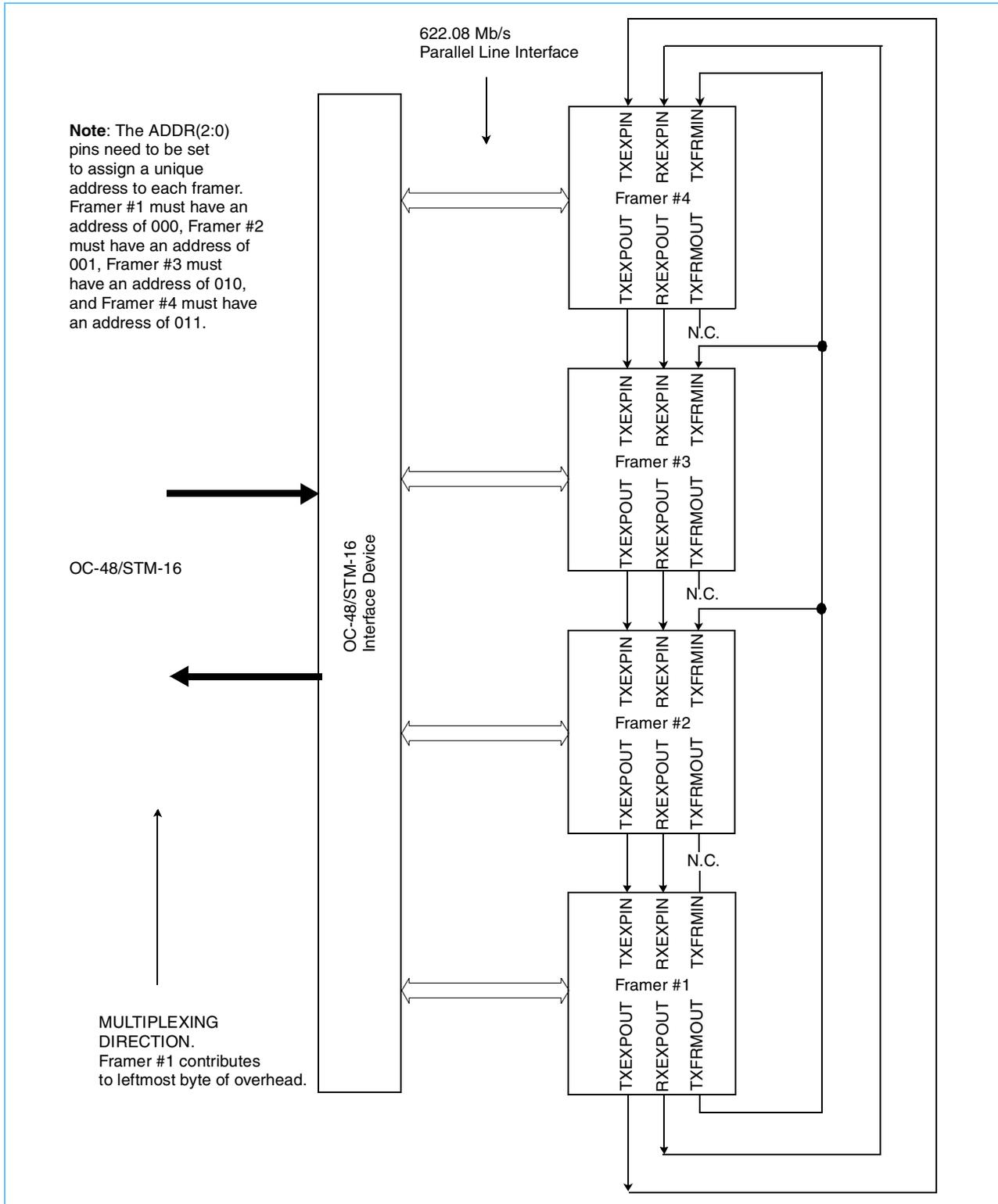
The OC-48/STM-16 expansion port is used to provide inter-SONET/SDH framer communication of B1 information, received B2 errors, and AIS indications. That is, a B1 calculation is performed across the data of all four SONET/SDH framers. B2 errors are summed up from all four SONET/SDH framers and put into the M1 byte. The detection of Line AIS as detected by the K2 byte in the first SONET/SDH framer is also indicated to the other three SONET/SDH framers. Additionally, the OC-48/STM-16 expansion port synchronizes the SONET/SDH framers together so that scrambling/descrambling can be performed by the SONET/SDH framers. The MUX/DEMUX needs to MUX/DEMUX the data between the OC-48 stream and the four SONET/SDH framers four bytes at a time, as shown in the following figure.

**IBM SONET/SDH Framers**

**OC-48/STM-16 Byte Interleaving for External MUX/DEMUX**



### OC-48/STM-16 Expansion Port Connection



## IBM SONET/SDH Framer

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OC-48/STM-16 Expansion Port Connection on page 95 shows four SONET/SDH framers connected for OC-48/STM-16 operation via their expansion ports. See OC-48 Expansion Port Timing on page 66 for notes on timing considerations. The ADDR(2:0) pins of each SONET/SDH framer need to be set to identify which SONET/SDH framer is number 1, which is 2, which is 3, and which is 4. The OC-48/STM-16 device provides multiplexing, parallel-to-serial conversion, and clock synthesis in the transmit direction, and performs clock recovery, byte alignment, and serial-to-parallel conversion in the receive direction. The byte-parallel interfaces of the SONET/SDH framer are used to interface to the OC-48/STM-16 Interface Device. The line side of each SONET/SDH framer can be individually configured to process STM-4, STM-4c, STS-12, or STS-12c frames. The terminal side of each SONET/SDH framer can be individually programmed to support Telecom Bus, UTOPIA Level 2+ (PPP over SONET/SDH), UTOPIA Level 2, or dual UTOPIA Level 1 interfaces).

## Ring Port

The ring port is used to communicate between K1, K2, K3, Path RDI, Line RDI, Path FEBE, Line FEBE, and the alarms associated with the K1, K2, and K3 bytes.

The ring port is a serial interface that is used to exchange various SONET/SDH-specific alarm, bit or block error information, and APS information, among SONET/SDH framers when operating in a counter-rotating unidirectional ring network. Thus, the ring port replaces the SONET/SDH framer internal remote alarm, bit/block error, and APS signaling which is used in bidirectional point-to-point SONET/SDH applications when the RING control bit is set to '1'. In other words, when RING is set to '1', path and line RDI and FEBE are not inserted into the local transmit SDH stream. Instead they are passed to a mating SONET/SDH framer via the ring port along with APS information. The mating SONET/SDH framer will then transmit the line or path FEBE or RDI. When RING is set to '0', the ring port is not used at all and the local SONET/SDH framer will generate line or path RDI as appropriate.

**Note:** When the SONET/SDH framer is operating in Telecom Bus mode, all of the transmit POH information output to the line will be derived from the transmit Telecom Bus inputs and not from the ring port regardless of the setting of the RING bit. This feature will allow a POH Processor to perform POH processing while the SONET/SDH framer processes TOH.

The functions of the ring port are indicated in the subsections below.

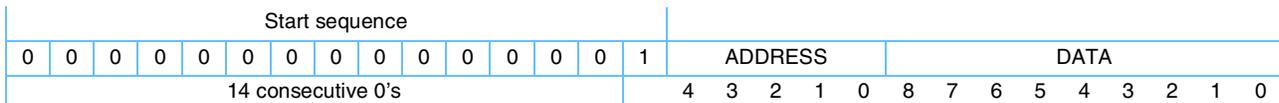
The RXRINGD and RXRINGCLK signals connect directly to their corresponding TXRINGD and TXRINGCLK pins on a mating SONET/SDH framer. The RXRINGCLK clock is 19.44 MHz  $\pm$ 20 ppm and is derived from the transmit Line Reference Clock of the SONET/SDH framer that is driving that signal.

The format of the ring port data that is output on the RXRINGD pin is shown in Ring Port Data Format on page 97. The leftmost bit is transmitted first. The information consists of twenty 29-bit fields, one for each of the K1, K2, and K3 bytes, and Line and Path FEBE values, plus their associated alarms, for all four STM-1/STS-3c signals. The sub-fields of the RXRINGD signal are:

- A 15-bit start sequence consisting of 14 consecutive '0's followed by a '1' (i.e., 0000 0000 0000 001). This field is used by the mating SONET/SDH framer to determine the location of the address and data fields.
- A 5-bit address field. This field identifies to the mating SONET/SDH framer what the contents of the 9-bit data field are and from which STM-1/STS-3c it came. When an STM-4c or STS-12c is processed, the section number field will be set to '0' since there is only one set of POH to process. Also note that when an STM-4 or STS-12 is processed, the section number field will indicate with which VC-4 (1-4) the ring port data is associated.
- A 9-bit data field. This field will contain one of the following:
  - Debounced K1 byte plus a reserved bit.
  - Debounced K2 byte plus New APS indication.

- Debounced K3 byte plus New K3 indication.
  - G1 path REI (Path FEBE) plus Path RDI.
  - M1 Line REI (Line FEBE) and Line RDI.
- The SONET/SDH framer will not lose data input on its transmit ring port interface if the frequency of its transmit ring port clock input signal is  $\pm 20$  ppm from nominal and its transmit line clock is  $\pm 20$  ppm from nominal. This also applies to the receive side. That is, if the receive line frequency is different from the RXRINGCLK frequency, then no data will be lost going from the receive side of the SONET/SDH framer over to its receive ring port interface.

### Ring Port Data Format

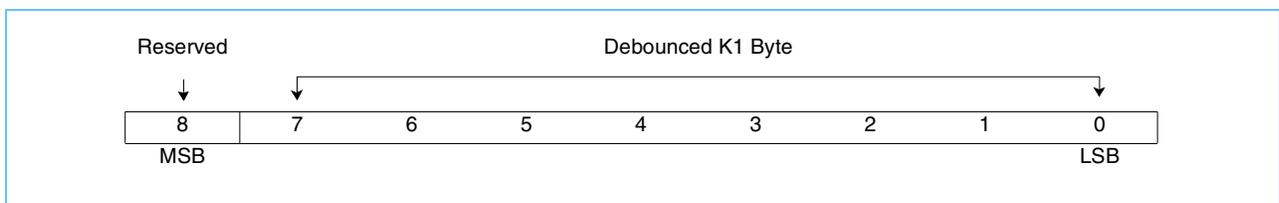


Address Field Bit Definitions indicates the meaning of the bits in the address field while the five figures that follow it indicate the formats of the nine-bit data field. The data fields contain information relating only to their corresponding STM-1/STM-4/STM-4c/STS-3c/STS-12/STS-12c.

### Address Field Bit Definitions

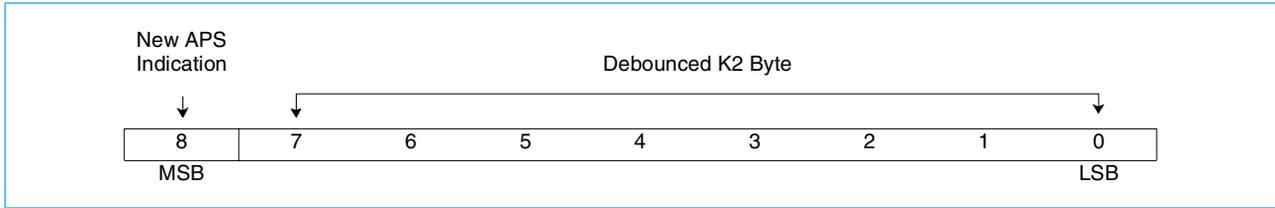
| Address Field |   |   |   |   |   |
|---------------|---|---|---|---|---|
| 4             | 3 | 2 | 1 | 0 |   |
| DATA_SEL      |   |   |   |   | section no.   |
| 0             | 0 | 0 |   |   | Data field contains New APS Indication and Debounced K2 Byte. |
| 0             | 0 | 1 |   |   | Data field contains New K3 Indication and Debounced K3 Byte.  |
| 0             | 1 | 0 |   |   | Data field contains Line RDI and Line FEBE.                   |
| 0             | 1 | 1 |   |   | Data field contains Path FEBE and Path RDI.                   |
| 1             | 0 | 0 |   |   | Data field contains a reserved bit and Debounced K1 Byte.     |
| 1             | 0 | 1 |   |   | Not Used.   |
| 1             | 1 | X |   |   | Not Used.   |
|               |   |   | 0 | 0 | Data Field is associated with STM-1/STS-3c #1.                |
|               |   |   | 0 | 1 | Data Field is associated with STM-1/STS-3c #2.                |
|               |   |   | 1 | 0 | Data Field is associated with STM-1/STS-3c #3.                |
|               |   |   | 1 | 1 | Data Field is associated with STM-1/STS-3c #4.                |

### Data Field is Carrying Debounced K1 Byte and a Reserved Bit



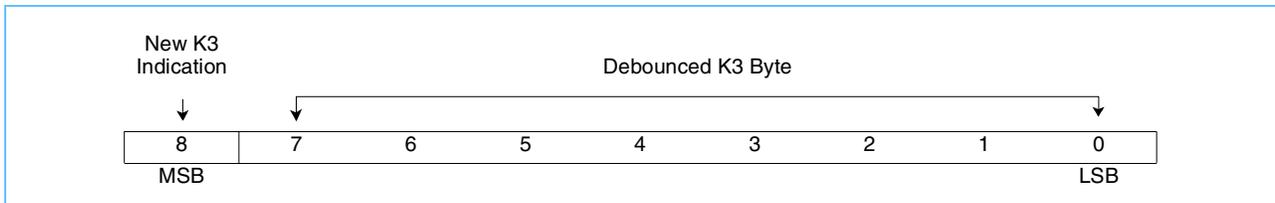
**IBM SONET/SDH Framer**

**Data Field is Carrying Debounced K2 Byte and New APS Indication Bit**



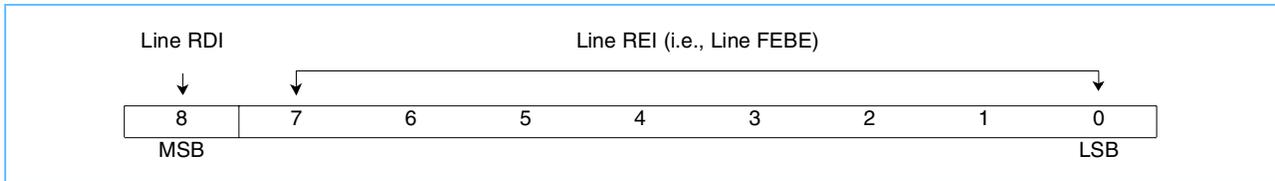
The New APS Indication bit becomes set when three (SONET) or five (SDH) consecutive and equal new values of K1 and the five MSBs of K2 are received by the SONET/SDH framer. The duration of the New APS Indication bit being set is for only one frame.

**Data Field is Carrying Debounced K3 Byte and New K3 Indication Bit**



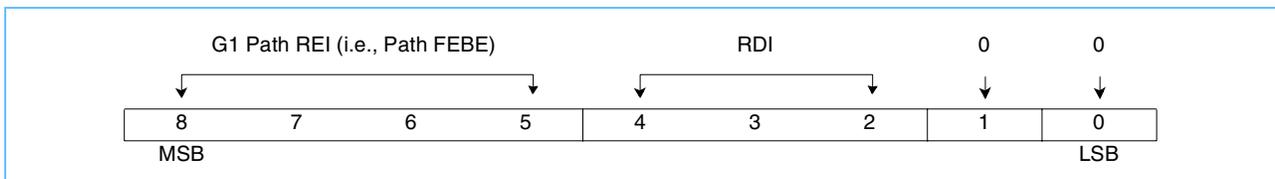
The New K3 Indication bit becomes set when three consecutive and equal new values of K3 are received by the SONET/SDH framer. The duration of the New K3 Indication bit being set is for only one frame.

**Data Field is Carrying M1 Line REI and RDI**



The Line REI field is set to the number of B2 errors received by the SONET/SDH framer plus those indicated on the expansion port. The Line RDI bit is generated immediately upon detection of a LOS, LOF, or AIS-L defect by the SONET/SDH framer. The Line RDI bit will persist for at least twenty frames. The line RDI is removed within 100 ms from when the SONET/SDH framer detects termination of the defect. The mating SONET/SDH framer will insert these Line RDI and Line REI into its transmit K2 and transmit M1 byte stream for the appropriate STM-1/STM-4/4c/STS-3c/STS-12/STS-12c. Again, while RING is set to '1', line FEBE and RDI are not locally transmitted but are instead communicated to a mating SONET/SDH framer, which will insert them into its transmit SDH stream.

**Data Field is Carrying Path REI and RDI**



The G1 path REI field will contain the count of B3 errors received in its corresponding VC-4 or VC-4c. The Path RDI is generated immediately after detection of the defect(s) that would cause the SONET/SDH framer to normally transmit the Path RDI. The path RDI is transmitted for a minimum of ten frames. The Path RDI

field is set to indicate no defect detected within 100 ms from when the SONET/SDH framer detects termination of the defect. The mating SONET/SDH framer will insert these path RDI and FEBE values into its transmit G1 byte stream for the appropriate VC-4 or VC-4c. Again, while RING is set to '1', path FEBE and RDI are not locally transmitted but are instead communicated to a mating SONET/SDH framer which will insert them into its transmit SONET/SDH stream.

All of the data fields depicted in the previous figures are output by the SONET/SDH framer even if there are no errors or actions to report.

Finally, when RING is set to '0', nothing is sent out on the transmit ring port but the transmit ring port clock remains active.

When the RING bit is set to '1', the SONET/SDH framer processes the K1-K3, G1 and Line RDI/REI and their associated indication bits via the ring port as indicated below. Keep in mind that no POH processing (particularly G1 and K3) is performed by the SONET/SDH framer when the Telecom Bus mode of operation is selected, regardless of the setting of the RING bit. Therefore, for the cases below where K3 and G1 processing are mentioned, Telecom Bus mode is assumed to be turned off.

- 4 x STM-1/STS-3c mode
  - K1 - K3, their associated indication bits, G1, and Line RDI/REI are processed for each individual STM-1/STS-3c.
- STM-4/STS-12 mode
  - K1, K2 plus the New APS indication bit, and Line RDI, are processed only for the first STM-1/STS-3c.
  - Line REI is processed only for the third STM-1/STS-3c. The receive B2 errors from the twelve B2 bytes received from the line are summed by macro 3 and transferred to a mating SONET/SDH framer which then outputs this value to its line via the transmit M1 byte. The M1 byte is located in row 9 column 15 (the third A2 byte is also in column 15) of the STM-4/STS-12 frame.
  - K3 is processed for all 4 VC-4.
  - G1 is processed for all 4 VC-4.
- STM-4c/STS-12c mode
  - K1, K2 plus the New APS indication bit, and Line RDI, are processed only for the first STM-1/STS-3c.
  - Line REI is processed only for the third STM-1/STS-3c. The receive B2 errors from the twelve B2 bytes received from the line are summed by macro 3 and transferred to a mating SONET/SDH framer which then outputs this value to its line output via the transmit M1 byte. The M1 byte is located in row 9 column 15 (the third A2 byte is also in column 15) of the STM-4c/STS-12c frame.
  - There is only one K3 byte that is processed since there is only one column of POH.
  - There is only one G1 byte that is processed since there is only one column of POH.
- STM-16/STM-4c or STS-48/STS-12c mode
  - K1, K2 plus the New APS indication bit, and Line RDI, are processed only for the first STM-1/STS-3c in the SONET/SDH framer that corresponds to STM-4c/STS-12c 1.
  - Line REI is processed only for the third STM-1/STS-3c in the SONET/SDH framer that corresponds to STM-4c/STS-12c 1. The receive B2 errors from the twelve B2 bytes received from the line and the expansion port are summed by macro 3 of the SONET/SDH framer that corresponds to STM-4c/STS-12c 1 and are transferred to a mating SONET/SDH framer which then outputs this value to its line output via the transmit M1 byte. The M1 byte is located in row 9 column 51 (the third A2 byte is also in column 51) of the STM-16/STS-48 frame.
  - Only one K3 byte is processed in each SONET/SDH framer as there is only one K3 byte in a VC-4c.
  - Only one G1 byte is processed in each SONET/SDH framer as there is only one G1 byte in a VC-4c.

## IBM SONET/SDH Framer

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- STM-16/STM-4 or STS-48/STS-12 mode
  - K1, K2 plus the New APS indication bit, and Line RDI, are processed only for the first STM-1/STS-3c in the SONET/SDH framer that corresponds to STM-4/STS-12 1.
  - Line REI is processed only for the third STM-1 in the SONET/SDH framer that corresponds to STM-4/STS-12 1. The receive B2 errors from the twelve B2 bytes received from the line and the expansion port are summed by macro 3 of the SONET/SDH framer that corresponds to STM-4/STS-12 1 and are transferred to a mating SONET/SDH framer which then outputs this value to its line output via the transmit M1 byte. The M1 byte is located in row 9 column 51 (the third A2 byte is also in column 51) of the STM-16/STS-48 frame.
  - K3 is processed for all 4 VC-4s of each SONET/SDH framer.
  - G1 is processed for all 4 VC-4 of each SONET/SDH framer.

Alarm bits are provided to indicate that an alarm was asserted in the corresponding alarm bit in bit location 8 of the data field; see Ring Port Data Format on page 97. If the RING control bit is set to '0', the SONET/SDH framer will ignore the ring port inputs and force its ring port outputs to a stable logic level. The loss of ring data (AIP\_DLoss bit in OT#IRQ2 #=1-4) and loss of ring clock (LTRC) event bits will also be disabled. This means that they will not be affected by TXRINGD and TXRINGCLK.

The K1, K2, and K3 bytes for all four STM-1/STS-3cs that are received at the ring port inputs are stored in registers in the SONET/SDH framer for access by the local microprocessor provided that the RING control bit is set to a '1'. The K1, K2, and K3 bytes are updated each time they are received at the transmit ring port inputs. The K1, K2, and K3 bytes are stored in the OT#Stat3-5 registers, where # = 1, 2, 3, 4. When the RING control bit is set to a '0', the SONET/SDH framer does not update the K1 - K3 register locations from the transmit ring port. Instead, these values are derived from the local receive SONET/SDH line. Each time the SONET/SDH framer receives a Line RDI Indication on its transmit ring port input the SONET/SDH framer will transmit a Line RDI at its transmit line output.

When the RING control bit is set to '1' and the SONET/SDH framer is set up to process four individual STM-1/STS-3cs, the Line REI received at the transmit ring port input is inserted into the M1 byte of the corresponding STM-1/STS-3c macro in the outgoing SONET/SDH stream of the SONET/SDH framer. When the SONET/SDH framer is set up to process an STM-4/4c or an STS-12/12c, the SONET/SDH framer will insert the Line REI count received at its ring port for macro 3 into the M1 byte for macro 3. When the SONET/SDH framer is set up for STM-16/STS-48 mode, macro 3 of the SONET/SDH framer that corresponds to STM-4/4c or STS-12/12c 1 will add the B2 errors indicated on its expansion port to the Line REI that it gets from the ring port and insert that count into the outgoing M1 byte of macro 3. The Line REIs due to B2 errors received from the receive line will not be inserted into the outgoing M1 byte(s) of their corresponding local STM-1/STS-3cs. No data is lost due to clock tolerance offsets between the TXRINGCLK signal and the SONET/SDH transmit clock of the same SONET/SDH framer.

When the RING control bit is set to '1', the Path FEBE and RDI inputs at the transmit ring port are inserted into the G1 byte of the corresponding VC-4 (or VC-4-4c) in the outgoing SONET/SDH stream of the SONET/SDH framer. Locally detected B3 errors and alarms will not have any effect on the transmit G1 bytes. *It is important to note that no POH processing is performed by the SONET/SDH framer when the Telecom Bus interface is used.* This includes the ring port. When the Telecom Bus interface is used, all Path FEBE and RDI values must be handled by the path layer device connected to the Telecom Bus.

When the RING control bit is set to '0', the G1 byte values in the TXRINGD stream are ignored by the SONET/SDH framer. Instead, the transmit G1 byte(s) is(are) determined by the locally-detected B3 errors and alarms, provided that Telecom Bus mode is not activated.

## Transmit Higher-Order Path Termination (HPT) Layer Options

The SONET/SDH framer provides the HPT functions when the UTOPIA or the UTOPIA Level 2+ interface is being used to interface PPP or ATM payloads. POH processing is not performed when the Telecom Bus is used.

All POH bytes are stored in on-chip RAM where they are retrieved for transmission or for access by a microprocessor. POH processing is provided for up to four SPE/VC-4s.

The J1 path trace can be written by the microprocessor into on-chip RAM (i.e., the transmit GRA) for transmission as a 16-byte or 64-byte long message. The B3 is calculated for each frame and written into the on-chip RAM for transmission. C2 bytes can be written to on-chip RAM by the microprocessor for transmission. When an unequipped signal is transmitted by setting the HUG bit in the OT#Conf2 register, the transmitted C2 and the C-4 payload section are forced to all '0's. In this case, the C2 value in the corresponding transmit GRA does not have an effect, but the other POH bytes in the transmit GRA do have an effect. Path FEBE is based on received B3 errors and is automatically inserted into the transmit G1 byte. Path RDI generation per [G.707] and [GR-253] are performed based on mode (SONET or SDH) as follows:

### RDI Generation for Transmit HPT

| Mode             | Interrupt Request or Status Indication          | Transmitted RDI Code <sup>1</sup> | Notes |
|------------------|---|-----------------------------------|-------|
| SDH              | HPAIS, LOP                                      | 101                               |       |
|                  | UNEQ, HPTIM                                     | 110                               |       |
|                  | SynchHunt (i.e., loss of cell delineation)      | 010                               |       |
|                  | No defects                                      | 001                               |       |
| SONET (Bellcore) | HPAIS, LOP                                      | 101                               |       |
|                  | UNEQ, HPTIM                                     | 110                               | 2     |
|                  | SynchHunt (i.e., loss of cell delineation), SLM | 010                               | 3     |
|                  | No defects                                      | 001                               |       |

1. Bit Number uses ITU-T and Bellcore bit numbering convention.

2. A control bit (TIM\_RDI) is used to disable or enable the HPTIM interrupt request bit from causing Path RDI to be transmitted. This bit should be set to disable HPTIM from causing a Path RDI to be transmitted.

3. A control bit (SLM\_RDI) is used to disable or enable the SLM interrupt request bit from causing Path RDI to be transmitted.

## IBM SONET/SDH Framer

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The transmitted G1 bytes can be generated from local alarm conditions or can be derived from the ring port when the RING control bit is set to '1'. The F2, F3, H4, K3, and N1 bytes can be written to the on-chip RAM by the microprocessor for transmission. These values are static and are not acted upon by the SONET/SDH framer's transmit logic. Path AIS can be forced in the transmit direction under software control or by an external pin (TXTB#FAIL).

### Receive Higher-Order Path Termination (HPT) Layer Options

The SONET/SDH framer provides the HPT functions when the UTOPIA or the UTOPIA Level 2+ interface is being used to interface PPP or ATM payloads. POH processing is not performed when the Telecom Bus is used.

All POH bytes are stored in on-chip RAM where they can be observed by the microprocessor. Either receive 64-byte free form or 16-byte ITU-T G.831-style messages can be received. The received 16-byte J1 message can be compared with a 16-byte microprocessor-written J1 compare message in the receive GRA. A Trace Identifier Mismatch alarm (HPTIM) is raised if no match occurs. 16-bit counters are provided for counting B3 errors, B3 block errors and Path REI. These counters have programmable threshold overstep registers that cause maskable interrupts to be generated when the counter value oversteps the programmed threshold. The Path REI counter regards values of 08 H or greater as a count of 0. The B3 block error counter increments by one each time an errored B3 byte is received, no matter how many bits are errored. The Unequipped defect (UNEQ) detection is performed on the received C2 bytes. If the received C2 bytes are set to '0' for five consecutive frames, the UNEQ interrupt request bit is set to a '1'. If the received C2 byte is not '0' for five consecutive frames, the UNEQ will be terminated. Path Signal Label mismatch detection is performed against a microprocessor-written expected C2 byte and an internal 01 H value. If a mismatch occurs between the received C2 byte and either the expected C2 byte or the internal 01 H value, the SLM interrupt request bit becomes set to a '1'. It should be noted that an unequipped condition does not cause the SLM interrupt request bit to go active.

### Transmit/Receive Lower-Order Path Adaptation Functions

In ATM/PPP mode, the transmit ATM/PPP streams are mapped into a C-4 or C-4-4c and the receive ATM/PPP streams are extracted from the C-4, or C-4-4c per [G.707] and [RFC-1619].

## Pointer Tracking Interpretation

The pointer tracking algorithm implemented in the SONET/SDH framer is illustrated in Pointer Tracking State Machine on page 104. Refer to [G.783] and [GR-253] for definitions of the transitions. The pointer tracking state machine is based on the pointer tracking state machine found in the ITU-T requirements, and is also valid for both Bellcore and ANSI. The AIS to LOP transition of the state machine does not occur in Bellcore mode (i.e., BELLCORE = 1).

Four pointer tracking state machines are employed, one for each AU-4/STS-3c. The pointer tracking uses the H11 and H21 bytes. The pointer is extracted from the concatenation of the H1n and H2n bytes, and is interpreted as follows:

| H1n Byte |   |   |   |         |   |   |   | H2n Byte |   |   |   |   |   |   |   |
|----------|---|---|---|---------|---|---|---|----------|---|---|---|---|---|---|---|
| 1        | 2 | 3 | 4 | 5       | 6 | 7 | 8 | 1        | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| N        | N | N | N | ss-bits |   | I | D | I        | D | I | D | I | D | I | D |

NNNN = New Data Flag Bits. This is interpreted as enabled = 1001 or 0001/1101/1011/1000, and normal or disabled = 0110 or 1110/0010/0100/0111 (i.e., a single-bit error is tolerated).

ss = Size bits used in pointer tracking state machine interpretation if enabled by BELLCORE control bit being set to '0'. When BELLCORE is set to '1' these bits are ignored but, when it is set to '0', these bits are expected to be 10.

I = Increment Bits defined as bit 7 of H1n and bits 1, 3, 5 and 7 of H2n.

D = Decrement Bits defined as bit 8 of H1n and bits 2, 4, 6 and 8 of H2n.

Negative Justification: Inverted 5 D-bits and accept majority rule. The 8 of 10 objective of O3-92 in [GR-253] can be enabled by setting the JusITU bit in OR#Conf3 to '0'.

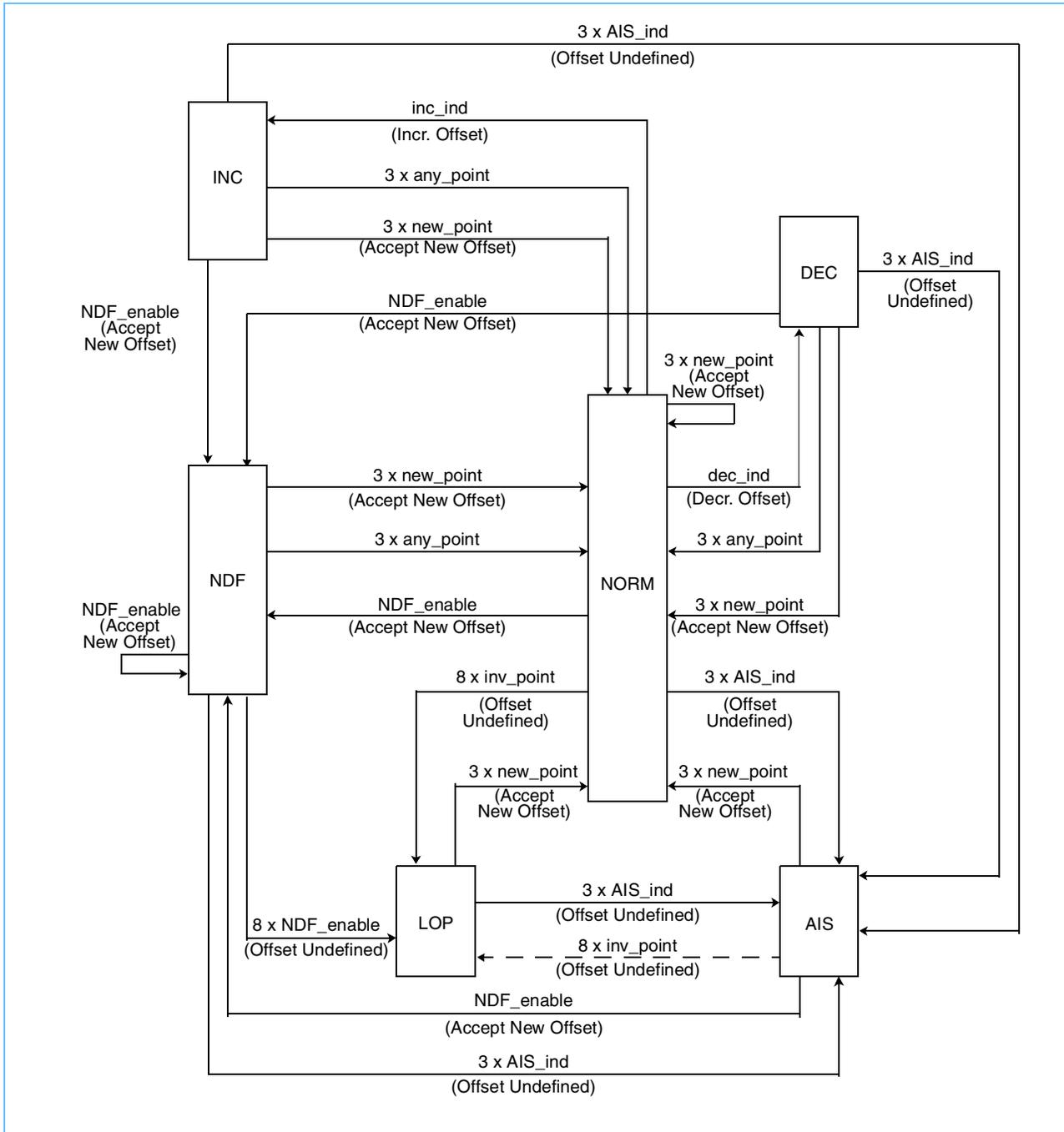
Positive Justification: Inverted 5 I-bits and accept majority rule. The 8 of 10 objective of O3-92 in [GR-253] can be enabled by setting the JusITU bit in OR#Conf3 to '0'.

For STM-1/STS-3c operation, the pointer is a binary number with the range of 0 to 782 (decimal). It is a 10-bit value derived from the two least significant bits of the H1 byte, with the H2 byte concatenated, to form an offset in 3-byte counts from the H3 byte location. For example, for an STM-1 signal, a pointer value of 0 indicates that the VC-4 starts in the byte location 3 bytes after the H3 byte, whereas an offset of 87 indicates that the VC-4 starts three bytes after the K2 byte.

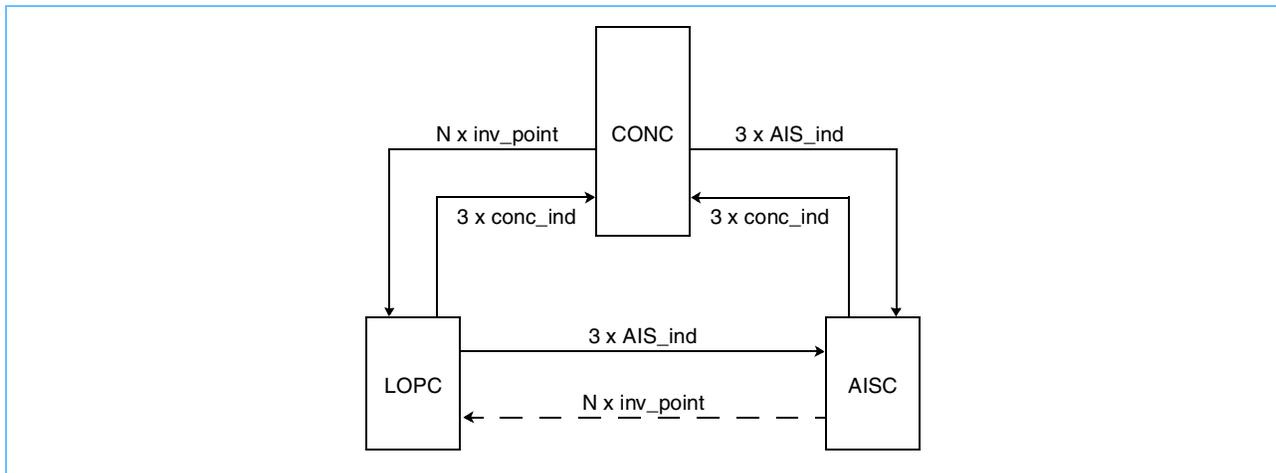
In STM-4/STS-12 modes, there are four byte-interleaved AU-4s, so there are four H1/H2 byte pairs for determining the beginning (i.e., the J1 byte location) of their respective VC-4s. The operation of the four pointer tracking state machines in this case is identical to that for 4 x STM-1/STS-3c operation.

When dealing with STS-12c/STM-4c, the pointer tracking state machine for macro 1 is used to locate the beginning of the VC-4-4c. The pointer tracking uses the H11 and H21 bytes. The pointer is extracted from the concatenation of the H11 and H21 bytes, and is interpreted as shown in the previous figure. However, the offset that is formed represents the number of 12-byte counts from the H3 byte location. For example, for an STM-12c signal, a pointer value of 0 indicates that the VC-4 starts in the byte location twelve bytes after the H3 byte, whereas an offset of 87 indicates that the VC-4 starts twelve bytes after the K2 byte. The concatenation indication bytes are also examined in the corresponding macros (macros 2-4) and are monitored for LOP and HPAIS per the state machine in Annex C of [G.783]. Concatenation Indication State Machine on page 105 illustrates the concatenation indicator state diagram. Refer to [G.783] for definitions of the transitions.

Pointer Tracking State Machine



## Concatenation Indication State Machine



Eight-bit counters are provided for counting positive and negative justification events, as well as NDF events. Status bits are provided for indicating the detection of negative justification, positive justification, NDF, invalid pointer, new pointer, and concatenation indication. When the LOP or LOPC states are entered as indicated in the two previous figures, the LOP interrupt request bit in the corresponding OR#IRQ2 register will be set. Likewise, if the AIS or AISC states are entered, the corresponding HPAIS interrupt request bit will become set.

## Transmit ATM/PPP Handler ATM Functions

The transmit ATM Transmission Convergence Sublayer Functions (TCSFs) are performed in the transmit APH blocks. Four individual AU-4 streams can be supported, such as in an STM-4/STS-12 or in four individual STM-1/STS-3c frames. 4 x STM-1/STS-3c looks just like 1 x STM-4/STS-12 to the SONET/SDH framer's transmit APH blocks. A single 622.08 Mb/s stream with a concatenated payload (i.e., a VC-4-4c) can be handled, such as would be found in an STM-4c/STS-12c frame. A four-cell-deep elastic store (i.e., the ACB) is provided between each transmit APH Block and the UTOPIA Level 1/2/2+ interface(s). When an STM-4c/STS-12c frame is being generated, the four transmit APH blocks work in parallel as a single transmit APH block. Idle cells per [I.432] or unassigned cells per [I.361] are provided towards the MSA Layer (i.e., the SFH blocks) when no ATM cells are available. Generation of Idle/Unassigned cells can be enabled or disabled via a control bit. The header bytes of Idle/Unassigned Cells can be programmed via on-chip registers. Payload of Idle/Unassigned cells can be programmed such that:

- Each payload byte of a cell is the same value in the range 0-255, and is configured through the microprocessor interface.
- An incrementing pattern is placed in all the payload bytes of each cell, e.g., all of the payload bytes in a cell are M, all of the payload bytes in the next cell are M+1, etc.
- An incrementing pattern can be placed in each payload byte of a cell where each successive payload byte contains a value that is one greater than the value of the previous byte.

The HEC calculation for Idle/Unassigned or ATM layer Cells can be enabled or disabled via software control. The HEC can be corrupted under microprocessor control via on-chip mask registers for test purposes. A self-synchronous scrambler of polynomial  $1+X^{43}$  is provided to scramble the payloads of the transmitted cells. 24-bit counters are provided to count generated idle/unassigned cells and ATM Layer cells read from the elastic store. An 8-bit counter is provided for counting corrupted ATM Layer cells read from the elastic store.

## Receive ATM/PPP Handler ATM Functions

The receive ATM Transmission Convergence Sublayer Functions (TCSFs) are performed in the receive APH blocks. Four individual AU-4 streams can be processed, such as in an STM-4/STS-12 or in four individual STM-1/STS-3c frames. 4 x STM-1/STS-3c looks just like 1 x STM-4/STS-12 to the SONET/SDH framer's receive APH blocks. A single 622.08 Mb/s stream with a concatenated payload (i.e., a VC-4-4c) can be handled, such as would be found in an STM-4c/STS-12c frame. A four-cell-deep elastic store (i.e., the ACB) is provided between each receive APH Block and the UTOPIA Level 1/2/2+ interface(s). When an STM-4c/STS-12c frame is being received, the four receive APH blocks work in parallel as a single receive APH block.

The ATM TCSF functions in the receive ATM/PPP Handler are implemented per [I.432.1]. ATM cell delineation is performed according to the algorithm in section 4.3.3.2 of [I.432.1]. Programmable ALPHA and DELTA registers are provided to allow users to program the thresholds for leaving and entering the SYNC state. Status bits are provided for indicating the transition from the SYNC to the HUNT state (i.e., Loss of Cell Delineation) and for indicating that the cell delineation state machine is in the HUNT, PRESYNC, or SYNC modes of operation. A control bit (LCD\_RDI) can be used to enable automatic Path RDI generation in the transmit G1 byte when loss of cell delineation is detected and sustained. Self-synchronizing cell descrambling is performed per section 4.3.4.1 of [I.432.1]. The ATM cell header is checked and error detection/correction is performed according to sections 4.3.2.1 and 4.3.2.2 in [I.432.1]. Single-bit errors can be corrected or not as enabled via a control bit (NCoRHECER). The coset (i.e., offset) byte of the HEC is user programmable and defaults to 01010101. Provision is made for additional control bits to:

- Enable the HEC checking state machine to stay in correction mode until the SYNC state is left, or to transition to the detection mode when a HEC error is detected.
- Allow/prevent IDLE cells to be written to the ACB FIFO.
- Enable/disable ATM cell payload descrambler.
- Enable/disable ATM cells with HEC errors from being written into the ACB FIFO.
- Enable/disable HEC error detection.

An Idle/Unassigned cell filter is provided whereby the five header and payload bytes can be defined so that cells meeting the criteria are identified as Idle/Unassigned cells and can be optionally discarded. Two 24-bit long counters are provided for counting received idle cells and ATM cells. Three 16-bit long counters with programmable thresholds (to signal an interrupt when the respective counters exceed the threshold) are provided for counting HEC errors, corrected HEC errors, and ATM cells that were discarded due to the receive ACB FIFO being full. When a receive loopback is enabled, no counting is performed.

## Transmit/Receive ATM/PPP Handler Features

Four independent PPP macros can be used to map/extract PPP into/from SONET/SDH Frames per [RFC1619] and [RFC1662] for STM-1, STS-3c, STM-4, STS-12, STM-4c, and STS-12c applications. A frame interface called UTOPIA Level 2+ based on the existing UTOPIA Level 2 interface is provided for transferring frame data on a single-PHY or multi-PHY interface between the SONET/SDH framer and a packet switch. Frames are transferred across the UTOPIA Level 2+ interface in programmable length chunks of either 16, 24, 32, or 64 bytes.

Transmitted frame data is processed per [RFC1662] and [RFC1619] as follows:

- Either a 16-bit or 32-bit FCS is calculated over the frame data per [RFC1662].
- FCS calculation can be disabled through control bits.
- Transparent mode can be enabled where chunks are mapped directly into the transmit SONET/SDH frame.

- Flag (7E H) and Control Escape (7D H) characters in the data plus FCS are stuffed per section 4.2 of [RFC1662].
- Frame delineation flags are inserted around the frame. At least one or at least two frame delineation flags can be inserted between transmitted frames as selected by a control bit (MFLAG).
- Transmit ACB FIFO underrun in the middle of a frame transfer causes an illegal sequence (7D7E H) to be transmitted.
- Inter-frame flag fill is added per section 4.4.1 of [RFC1662] to fill space between frames.
- Transmit C2 and H4 bytes can be programmed to appropriate values to satisfy [RFC1619].
- Optional scrambler ( $1+X^{43}$  polynomial) can be used to scramble HDLC stream before insertion into transmit SONET/SDH frame.
- PPP frames are mapped into SONET/SDH payload per [RFC1619].

Received frame data is processed per [RFC1662] and [RFC1619] as follows:

- The received frame data extracted from the SONET/SDH payload can optionally be descrambled with a descrambler ( $1+X^{43}$  polynomial).
- Frame delineation is performed by examining the payload stream for flag characters (7E H) per section 4.1 of [RFC1662]. All flags are discarded.
- All control escape sequences are processed (i.e., destuffed) per section 4.2 of [RFC1662].
- Either a 16-bit or 32-bit FCS is checked over the frame data per [RFC1662]. The FCS is not discarded.
- FCS errors are detected and registered in interrupt request bits, counted in an 8-bit combined Abort/FCS error counter, and signaled on an external FCS error pin.
- FCS check can be disabled through control bits. In this case, counters, interrupt request bits, and the FCS error pin are not active.
- Transparent mode can be enabled where chunks are passed directly into the receive UTOPIA Level 2+ interface without any frame delineation signals or processing.
- When not in transparent mode, frames (after destuffing and including FCS) that are greater than or equal to a user-defined maximum frame length (MAXFL(15:0)) are aborted.
- When not in transparent mode, frames (after destuffing and including FCS) that are less than a user-defined minimum frame length (MINFL(6:0)) can optionally be aborted based on a control bit setting (DMINF). This is used to comply with section 4.3 of [RFC1662].
- 8-bit counters are provided for counting frames that are discarded due to being too short or too long.
- Illegal sequences that are detected (7D7E H) are registered in an interrupt request bit and are counted in an 8-bit combined Abort/FCS Error counter, and signaled on an external Abort pin.
- A control bit is provided (FCSABT) to enable FCS errors and aborts to both be indicated on the FCS pin, or on their respective pins.
- Receive FIFO overflow causes an Abort to be signaled on the external pin.
- The remainder of all aborted frames are discarded and not counted as an FCS error.

## Utopia Levels 1 and 2 Block ATM Features

The SONET/SDH framer provides a PHY Layer interface with cell level handshaking for ATM applications. The interface can be configured to be two independent UTOPIA Level 1 interfaces or one UTOPIA Level 2 interface. The UTOPIA Level 1 interfaces have an 8-bit wide data path, are independent of each other, and can each support a single cell stream (contained in a C-4<sup>1</sup>). The UTOPIA Level 1 clock frequency can range from 2 to 25 MHz. The UTOPIA Level 2 interface can support either an 8-bit or 16-bit data bus. Up to four cell streams (contained in four C-4s) can be supported with multi-PHY operation. Single-PHY operation is provided so that cell streams in concatenated payloads (C-4-4c<sup>2</sup>) can be supported. In multi-PHY mode, polling/selection can be controlled by one or four CLAV signals. The UTOPIA Level 2 clock frequency can range from 2 to 50 MHz. A unique port address can be assigned to each of the APH macros through control registers. Depending on the payload being processed (C-4-4c or C-4), the PT#Conf2:NEWCONF, HT#Conf2:ACBTXTHPAE, HR#Conf10:PAFT and PR#Conf2:RXTHBUF registers need to be set as indicated in the memory map section of this databook to ensure the proper operation of the transmit and receive CLAV signals.

## Utopia Level 2+ Block PPP Features

The SONET/SDH framer provides a PHY Layer interface with chunk level handshaking for PPP applications. The data bus is 16-bits wide with a single multiplexed CLAV (chunk available) indication being employed for controlling transfers for both single and multi-PHY modes. A multi-PHY mode that follows UTOPIA Level 2 style handshaking is provided for terminating up to four C-4 data streams. The method of polling and PHY selection as outlined in [UL2v1] is followed. A single-PHY mode is provided for UTOPIA Level 2 style handshaking in cases where a concatenated payload, such as a C-4-4c, is being terminated. See UTOPIA Interface on page 14 for details on the handshaking.

The UTOPIA Level 2+ interface is basically a UTOPIA Level 2 interface plus some additional signals to facilitate frame delineation. These extra handshaking and status signals are added to indicate start and end-of-frame, FCS error, abort, last byte of frame is in the MSB position, and start of chunk. The frame data is passed across the interface in programmable size data blocks called chunks. Chunks are programmed to be 16, 32, 48, or 64 bytes. Data from several frame streams can be broken up into chunks and multiplexed to/from the appropriate PHY in much the same way that ATM cells are. The advantage to “chunking” the frame data is that short frames on PHY N do not have to wait for a long frame that is currently being transferred on PHY M to be completely transmitted/received. However, it is the responsibility of the ATM or controlling layer to ensure that PHYs are not starved or stuffed to overflowing. It is, therefore, strongly suggested that the UTOPIA Level 2+ interface clocks be run at, or very near 50 MHz, even though the frequency of the clocks can range down to 2 MHz. A unique port address can be assigned to each of the APH macros through control registers.

Depending on the payload being processed (C-4-4c or C-4) and the chunk size, the PT#Conf2:NEWCONF, HT#Conf2:ACBTXTHPAE, HR#Conf10:PAFT and PR#Conf2:RXTHBUF registers need to be set as indicated in the memory map section of this databook to ensure the proper operation of the transmit and receive CLAV signals.

## Transmit Telecom Bus Interface

The transmit Telecom Bus interface of the SONET/SDH framer provides an interface for accepting TDM data formatted as either an AU-4 or VC-4 signal. The GContTx#(1:0) bits in the GContTX register are used to

1. A C-4 is a VC-4/SPE without POH. That is, it is the STM-1/STS-3c payload or it can be one of the four STM-4/STS-12 payloads.
2. A C-4-4c is a VC-4-4c/SPE without POH. That is, it is the STM-4c/STS-12c payload.

select the mode of operation. When AU-4 mode is selected, an AU-4 is supplied to the SONET/SDH framer's transmit Telecom Bus. When AU-4 mode is selected, the AU-4 that is provided must be aligned to the TXC-FRM pulse output and must also be frequency synchronous with either of the TXCCLK or TXCCLK clocks. For more information on the timing modes, see Transmit Telecom Bus on page 20. In VC-4 mode, a VC-4 is supplied to the SONET/SDH framer; the SONET/SDH framer calculates a pointer and appends it to the input VC-4, thus creating an AU-4. When VC-4 mode is active, it is necessary to have both the C1 and J1 pulses present in the corresponding TXTB#C1J1 signal. In 4 x STM-1/STS-3c mode, the MS and RS Overhead are added to the AU-4 by the SONET/SDH framer and the completed frame is transmitted. In STM-4/STS-12 mode, the AU-4s are byte-interleaved, RS and MS Overhead are added to the multiplexed AU-4s, and the completed STM-4/STS-12 frame is transmitted. When operating in 4 x STM-1/STS-3c mode or STM-4/STS-12 mode, each transmit Telecom Bus interface can be individually configured for AU-4 or VC-4 mode.

In STM-4c/STS-12c mode, the four transmit Telecom Buses act as a single transmit Telecom Bus with a 32-bit wide data path. The byte associated with Telecom Bus 1 is the MSB and is the first byte that is transmitted. All of the C1J1, SPE, FAIL and clock inputs must be driven with the same signals and the GContTx#(1:0) bits should be set to configure each macro for the same mode, either VC-4 or AU-4.

**Note:** POH processing is not performed when the SONET/SDH framer is operating in Telecom Bus mode. All POH bytes in the transmit direction are derived from what is input at the transmit Telecom Bus inputs. All POH bytes at the receive Telecom Bus interface are derived directly from the line.

## Receive Telecom Bus Interface

Four output Telecom Buses are provided in the receive direction for interfacing TDM traffic from the line interfaces to path processing devices. Handshaking signals are provided for identifying the SPE and C1J1 bytes. Control bits exist to configure each receive Telecom Bus interface individually as to parity generation, clock edge selection, or C1J1 signal aligned to A23 byte only or to C1 and J1 bytes.

In STM-4/STS-12 and 4 x STM-1/STS-3c modes, the Telecom Buses act independently of each other. In STM-4c/STS-12c modes, the four Telecom Buses act in parallel as one Telecom Bus with a 32-bit wide data path. For details, see Receive Telecom Bus on page 23.

## Microprocessor Interface

The SONET/SDH framer can support either Motorola or Intel microprocessor bus types. The Motorola interface is designed to support a Motorola 68360 processor bus type interface (QUICC bus type). Either synchronous or asynchronous modes of operation can be selected. In synchronous mode, all of the bus transactions are synchronized to the microprocessor clock. In asynchronous mode, all of the bus transactions are asynchronous with respect to the microprocessor clock and are synchronized internally to the external GPPCLK signal. The Intel-compatible bus interface can also operate in a synchronous or asynchronous mode.

A watchdog timer is provided to allow transactions to a specific block to be completed when a programmable timer runs out, even if the clock for the block being accessed is not present. If a timeout occurs, an interrupt request bit corresponding to the offending block is set.

## Boundary Scan Interface

A boundary scan interface fully compliant with IEEE Standard 1149.1-1994 (JTAG) is provided for board level testing of the SONET/SDH framer. Details of the SONET/SDH framer boundary scan operation are provided in the section Boundary Scan on page 262.



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# Memory Map

## Chiplet Address Map

| Chiplet Name/Short Name | Base Address | Address Range | # of Bytes | See Page |
|-------------------------|--------------|---------------|------------|----------|
| Reserved                | 0000 H       | 0000 - 00FF H | 256        |          |
| ACI_Tx1/IT1             | 0100 H       | 0100 - 01FF H | 256        | 155      |
| ACI_Tx2/IT2             | 0200 H       | 0200 - 02FF H | 256        | 160      |
| ACI_Rx1/IR1             | 0300 H       | 0300 - 03FF H | 256        | 165      |
| ACI_Rx2/IR2             | 0400 H       | 0400 - 04FF H | 256        | 171      |
| PH_Tx1/PT1              | 0500 H       | 0500 - 05FF H | 256        | 174      |
| PH_Tx2/PT2              | 0600 H       | 0600 - 06FF H | 256        | 174      |
| PH_Tx3/PT3              | 0700 H       | 0700 - 07FF H | 256        | 174      |
| PH_Tx4/PT4              | 0800 H       | 0800 - 08FF H | 256        | 174      |
| PH_Rx1/PR1              | 0900 H       | 0900 - 09FF H | 256        | 177      |
| PH_Rx2/PR2              | 0A00 H       | 0A00 - 0AFF H | 256        | 177      |
| PH_Rx3/PR3              | 0B00 H       | 0B00 - 0BFF H | 256        | 177      |
| PH_Rx4/PR4              | 0C00 H       | 0C00 - 0CFF H | 256        | 177      |
| ACH_Tx1/HT1             | 0D00 H       | 0D00 - 0DFF H | 256        | 180      |
| ACH_Tx2/HT2             | 0E00 H       | 0E00 - 0EFF H | 256        | 190      |
| ACH_Tx3/HT3             | 0F00 H       | 0F00 - 0FFF H | 256        | 190      |
| ACH_Tx4/HT4             | 1000 H       | 1000 - 10FF H | 256        | 190      |
| ACH_Rx1/HR1             | 1100 H       | 1100 - 11FF H | 256        | 197      |
| ACH_Rx2/HR2             | 1200 H       | 1200 - 12FF H | 256        | 207      |
| ACH_Rx3/HR3             | 1300 H       | 1300 - 13FF H | 256        | 207      |
| ACH_Rx4/HR4             | 1400 H       | 1400 - 14FF H | 256        | 207      |
| PPP/PPP                 | 1500 H       | 1500 - 15FF H | 256        | 215      |
| Reserved                | 1600 H       | 1600 - 17FF H | 512        |          |
| OFP_Tx1/OT1             | 1800 H       | 1800 - 1BFF H | 1024       | 225      |
| OFP_Tx2/OT2             | 1C00 H       | 1C00 - 1FFF H | 1024       | 225      |
| OFP_Tx3/OT3             | 2000 H       | 2000 - 23FF H | 1024       | 225      |
| OFP_Tx4/OT4             | 2400 H       | 2400 - 27FF H | 1024       | 225      |
| OFP_Rx1/OR1             | 2800 H       | 2800 - 2BFF H | 1024       | 240      |
| OFP_Rx2/OR2             | 2C00 H       | 2C00 - 2FFF H | 1024       | 240      |
| OFP_Rx3/OR3             | 3000 H       | 3000 - 33FF H | 1024       | 240      |
| OFP_Rx4/OR4             | 3400 H       | 3400 - 37FF H | 1024       | 240      |
| GPPINT/GP               | 3800 H       | 3800 - 38FF H | 256        | 113      |
| Reserved                | 3900 H       | 3900 - 3FAF H | 1712       |          |
| Reserved                | 3FB0 H       | 3FB0 - 3FBE H | 15         |          |
| GP Access Protection    | 3FBF H       | 3FBF H        | 1          | 152      |
| Reserved                | 3FC0 H       | 3FC0 - 3FFF H | 64         |          |

## Register Descriptions

This section contains the address maps and register bit descriptions for the internal memory locations of the SONET/SDH framer. The Access columns of the tables specify bit access as Read-only (R), Write-only (W) or Read/Write (R/W). When writing to registers that contain bits designated in the following tables as Reserved or Not Used, care should be taken to write those bits with their default values (if specified), or with '0' if no default value is specified.

### GPPINT Architecture

The General Purpose Processor interface provides direct access to registers located in the GPPINT module and direct, but delayed, access to registers and counters located in the GppHandler modules of the various chiplets of the SONET/SDH framer. GPPINT controls the handshaking with the external microprocessor as well as the handshaking with the GppHandlers at the asynchronous chiplet interfaces.

Address decoding is done to the chiplet level in GPPINT. In addition, addresses are decoded to the register level for the local GPPINT registers.

### Reset Registers

Each chiplet is controlled by one reset bit. At power-on, all reset bits are active and the chiplets are disabled. They can be released by the GPP only after all global configuration parameters have been set and the clocks to the chiplets have been established. In addition, there are reset bits for parts of the device that do not have their own GppHandler.

It should be noted that the bits in the GPPINT chiplet are only reset by the assertion and de-assertion of the hardware reset pin (FRESET).

### Interrupt Registers

The MAIN interrupt register is used as a pointer to the other interrupt registers with pending requests, the MAIN clock status error register, and the MAIN handshaking error register. The interrupt bits indicate pending interrupt requests from individual chiplets. An active bit of the interrupt registers is reset by removing the cause for the request in the corresponding chiplet or by masking the active IRQ bit(s) in the chiplet; therefore, the interrupt registers (including the pointer) are read-only. All interrupt and pointer registers have a corresponding MASK register (R/W). Every unmasked, active interrupt bit causes an active pointer bit. Every unmasked, active pointer bit causes activation of the interrupt signal to the microprocessor.

### Handshaking Error Registers

The MAIN handshaking error register is used as a pointer to the other handshaking error registers with pending requests. Each bit of the handshaking error registers indicates a locked interface to one of the GppHandlers. Two additional bits indicate various time-out events. To reset an individual bit of the handshaking error registers, the cause for the request must be removed AND a '1' must be written into the bit location of the register (R/W). Reading one of the registers will reset the whole (8-bit) register if the corresponding "clear-register" option is set in the configuration register. All handshaking error indication and pointer registers have a corresponding MASK register (R/W).

Every unmasked, active handshaking error bit causes an active pointer bit. Every unmasked, active pointer bit causes activation of the pointer bit in the MAIN interrupt register.

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### Clock Monitor Status Registers

The MAIN clock monitor status register is used as a pointer to the other clock monitor status registers with active error indication bit(s). The clock monitor status register bits indicate the loss of a specific chiplet's clock. They are set whenever a difference between the clock test signal and the individual chiplets clock acknowledge signal occurs after one clock monitor test period. To reset an individual bit of the clock monitor status registers, the clock of the corresponding chiplet must be restored **and** a '1' must be written into the bit location of the register (R/W). Reading one of the registers will reset the whole (8-bit) register if the corresponding "clear-register" option is set in the configuration register. All clock monitor status and pointer registers have a corresponding MASK register (R/W). Every unmasked, active clock monitor status bit causes an active pointer bit. Every unmasked, active pointer bit causes activation of the pointer bit in the MAIN interrupt register.

### Local GPPINT Configuration Registers

There are registers (R/W) for the Clock Monitor Test Period, the Watchdog Timer Period, and the "clear-register" option.

### Global Static Configuration Registers

These registers contain configuration parameters that are shared by many chiplets or that are needed by chiplets that have no GppHandler. The initial values can be modified by the microprocessor after power-on, but should not be changed later. All global static configuration registers are R/W. In order to ensure proper device operation the following reset procedure must be followed:

Reset Sequence:

1. During power-up, the  $\overline{\text{FRESET}}$  signal pin needs to be set low.
2. The  $\overline{\text{FRESET}}$  signal pin can be brought high only after the GPPCLK clock has been applied.
3. After the  $\overline{\text{FRESET}}$  signal is de-asserted, the microprocessor configures all of the static configuration bits in the global GPPINT registers and sets the SIM reset bits in RESGP6-7 to '1'.
4. The microprocessor can selectively enable individual chiplets by deactivating the corresponding chiplet reset bits in the RESGP1-7 registers, provided that particular chiplet's clock is present.
5. The microprocessor then sets the configuration bits in the enabled chiplets.
6. Each chiplet also has an additional reset bit (not in the GPPINT chiplet) that must be set to '0' in order to cause the chiplet to operate.
7. If it is desired to change the static configuration bits, steps 2-5 above must be performed. Changing the register settings in an individual chiplet can be done on the fly. It should be noted that when a chiplet's reset bit is set to a '1', the registers of that chiplet go to their default values.

### Status Registers

These registers provide status information from chiplets that have no GppHandler and are read-only. Presently, there is only one status register for the SIM chiplet (PLL lock status). The bit values follow the driving signal immediately.

**GPPINT Address Map** Base Address 3800H (Sheet 1 of 3)

| Register Name | Address Offset (Hex) | Access | Initial Value (Binary) | Description<br>(All Registers Are 8-bits Wide) | See Page |
|---------------|----------------------|--------|------------------------|--|----------|
| RESGP1        | 00                   | R/W    | 11111111               | Reset register #1                              | 116      |
| RESGP2        | 01                   | R/W    | 11111111               | Reset register #2                              | 116      |
| RESGP3        | 02                   | R/W    | 11111111               | Reset register #3                              | 117      |
| RESGP4        | 03                   | R/W    | 11111111               | Reset register #4                              | 117      |
| RESGP5        | 04                   | R/W    | 11111111               | Reset register #5                              | 117      |
| RESGP6        | 05                   | R/W    | 11000000               | Reset register #6                              | 118      |
| RESGP7        | 06                   | R/W    | 00000000               | Reset register #7                              | 118      |
|               | 07 - 0F              |        |                        | Reserved                                       |          |
| IRQGP1        | 10                   | R      | 00000000               | Chiplet interrupt request register #1          | 119      |
| IRQGP2        | 11                   | R      | 00000000               | Chiplet interrupt request register #2          | 119      |
| IRQGP3        | 12                   | R      | 00000000               | Chiplet interrupt request register #3          | 120      |
| IRQGP4        | 13                   | R      | 00000000               | Chiplet interrupt request register #4          | 120      |
| IRQGP5        | 14                   | R      | 00000000               | Chiplet interrupt request register #5          | 120      |
|               | 15 - 17              |        |                        | Reserved                                       |          |
| IRMGP1        | 18                   | R/W    | 00000000               | Chiplet interrupt mask register #1             | 119      |
| IRMGP2        | 19                   | R/W    | 00000000               | Chiplet interrupt mask register #2             | 119      |
| IRMGP3        | 1A                   | R/W    | 00000000               | Chiplet interrupt mask register #3             | 120      |
| IRMGP4        | 1B                   | R/W    | 00000000               | Chiplet interrupt mask register #4             | 120      |
| IRMGP5        | 1C                   | R/W    | 00000000               | Chiplet interrupt mask register #5             | 120      |
|               | 1D - 1F              |        |                        | Reserved                                       |          |
| HShake1       | 20                   | R/W    | 00000000               | Handshaking error register #1                  | 121      |
| HShake2       | 21                   | R/W    | 00000000               | Handshaking error register #2                  | 122      |
| HShake3       | 22                   | R/W    | 00000000               | Handshaking error register #3                  | 122      |
| HShake4       | 23                   | R/W    | 00000000               | Handshaking error register #4                  | 122      |
| HShake5       | 24                   | R/W    | 00000000               | Handshaking error register #5                  | 123      |
|               | 25 - 27              |        |                        | Reserved                                       |          |
| HSMask1       | 28                   | R/W    | 00000000               | Handshaking error mask register #1             | 121      |
| HSMask2       | 29                   | R/W    | 00000000               | Handshaking error mask register #2             | 122      |
| HSMask3       | 2A                   | R/W    | 00000000               | Handshaking error mask register #3             | 122      |
| HSMask4       | 2B                   | R/W    | 00000000               | Handshaking error mask register #4             | 122      |
| HSMask5       | 2C                   | R/W    | 00000000               | Handshaking error mask register #5             | 123      |
|               | 2D - 2F              |        |                        | Reserved                                       |          |
| ClkStat1      | 30                   | R/W    | 00000000               | Clock status register #1                       | 124      |
| ClkStat2      | 31                   | R/W    | 00000000               | Clock status register #2                       | 124      |
| ClkStat3      | 32                   | R/W    | 00000000               | Clock status register #3                       | 125      |



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**GPPINT Address Map** Base Address 3800H (Sheet 2 of 3)

| Register Name | Address Offset (Hex) | Access | Initial Value (Binary) | Description (All Registers Are 8-bits Wide)              | See Page |
|---------------|----------------------|--------|------------------------|--|----------|
| ClkStat4      | 33                   | R/W    | 00000000               | Clock status register #4                                 | 125      |
|               | 34 - 37              |        |                        | Reserved   |          |
| ClkMask1      | 38                   | R/W    | 00000000               | Clock status mask register #1                            | 124      |
| ClkMask2      | 39                   | R/W    | 00000000               | Clock status mask register #2                            | 124      |
| ClkMask3      | 3A                   | R/W    | 00000000               | Clock status mask register #3                            | 125      |
| ClkMask4      | 3B                   | R/W    | 00000000               | Clock status mask register #4                            | 125      |
|               | 3C - 47              |        |                        | Reserved   |          |
| CMonGP1       | 48                   | R/W    | 00000000               | Clock monitor test period                                | 126      |
| WDTGP1        | 49                   | R/W    | 11111111               | Watchdog timer period                                    | 127      |
| ConfGP1       | 4A                   | R/W    | 11111111               | "Clear-register" option register                         | 128      |
|               | 4B - 4F              |        |                        | Reserved   |          |
| VPD           | 50                   | R      | 100000vv               | IBM internal use register                                | 128      |
|               | 51 - 57              |        |                        | Reserved   |          |
| GContTx       | 58                   | R/W    | 00000000               | ATM/Loop/TB static configuration register for transmit   | 129      |
| GContRx       | 59                   | R/W    | 00000000               | ATM/Loop/TB static configuration register for receive    | 129      |
| GCasc         | 5A                   | R/W    | 10001000               | Common Cascading static configuration register           | 130, 130 |
| GLoopTx1      | 5B                   | R/W    | 00000000               | Transmit Loopback 1 static configuration register        | 132      |
| GLoopTx2      | 5C                   | R/W    | 00000000               | Transmit Loopback 2 static configuration register        | 133      |
| GLoopRx       | 5D                   | R/W    | 00000000               | Receive Loopback static configuration register           | 134      |
| GExtRes       | 5E                   | R/W    | 00000000               | External clock recovery circuit reset register           | 134      |
|               | 5F                   |        |                        | Reserved   |          |
| ACITXGP       | 60                   | R/W    | 00010110               | ACI_Tx UTOPIA static configuration register              | 136      |
| PHTXGP1       | 61                   | R/W    | 00010001               | ACI_Tx Source selection static configuration register #1 | 137      |
| PHTXGP2       | 62                   | R/W    | 00010001               | ACI_Tx Source selection static configuration register #2 | 137      |
| ACIRXGP       | 63                   | R/W    | 00010110               | ACI_Rx UTOPIA static configuration register              | 138      |
| PHRXGP1       | 64                   | R/W    | 00010001               | ACI_Rx Sink selection static configuration register #1   | 138      |
| PHRXGP2       | 65                   | R/W    | 00010001               | ACI_Rx Sink selection static configuration register #2   | 139      |
| PPPGP1        | 66                   | R/W    | 00000000               | PPP static configuration register #1                     | 139      |
| PPPGP2        | 67                   | R/W    | 00000110               | PPP static configuration register #2                     | 140      |
| OFPTXGP       | 68                   | R/W    | 00000000               | OFP_Tx static configuration register                     | 140      |
| OFPRXGP1      | 69                   | R/W    | 00000000               | OFP_Rx static configuration register #1                  | 141      |
| OFPRXGP2      | 6A                   | R/W    | 00000000               | OFP_Rx static configuration register #2                  | 141      |
| AIPConf       | 6B                   | R/W    | 00000000               | AIP (Ring Port) configuration register                   | 141      |
| CBCConf1      | 6C                   | R/W    | 00000000               | Telecom Bus static configuration register #1             | 135      |
| CBCConf2      | 6D                   | R/W    | 00000000               | Telecom Bus static configuration register #2             | 135      |
|               | 6E - 6F              |        |                        | Reserved   |          |

**GPPINT Address Map** Base Address 3800H (Sheet 3 of 3)

| Register Name | Address Offset (Hex) | Access | Initial Value (Binary) | Description<br>(All Registers Are 8-bits Wide)   | See Page |
|---------------|----------------------|--------|------------------------|--|----------|
| PIMTConf1     | 70                   | R/W    | 00000101               | PIM_Tx static configuration register #1          | 142      |
|               | 71                   |        |                        | Reserved   |          |
| PIMRConf1     | 72                   | R/W    | 00000001               | PIM_Rx static configuration register #1          | 142      |
| PIMRConf2     | 73                   | R/W    | 00000000               | PIM_Rx static configuration register #2          | 143      |
| PIMSelec      | 74                   | R/W    | 00000000               | PIM operation mode static configuration register | 143      |
|               | 75 - 77              |        |                        | Reserved   |          |
| SIMTConf1     | 78                   | R/W    | 11011010               | SIM_Tx static configuration register #1          | 144      |
| SIMTConf2     | 79                   | R/W    | 00100000               | SIM_Tx static configuration register #2          | 144      |
| SIMRConf1     | 7A                   | R/W    | 11011010               | SIM_Rx static configuration register #1          | 145      |
| SIMRConf2     | 7B                   | R/W    | 11011000               | SIM_Rx static configuration register #2          | 145      |
| SIMRConf3     | 7C                   | R/W    | 00000001               | SIM_Rx static configuration register #3          | 146      |
| SIMRConf4     | 7D                   | R/W    | 00000000               | SIM_Rx static configuration register #4          | 146      |
| SIMWrap       | 7E                   | R/W    | 00000000               | SIM wrap mode static configuration register      | 147      |
| SIMStat       | 7F                   | R      | N.A.                   | SIM status register                              | 148      |
| SIMATConf1    | 80                   | R/W    | 10111010               | SIM analog transmit stored parameters #1         | 148      |
| SIMATConf2    | 81                   | R/W    | 00000110               | SIM analog transmit stored parameters #2         | 149      |
| SIMATConf3    | 82                   | R/W    | 01001101               | SIM analog transmit stored parameters #3         | 148      |
| SIMATConf4    | 83                   | R/W    | 00000001               | SIM analog transmit stored parameters #4         | 149      |
| SIMARConf1    | 84                   | R/W    | 10111010               | SIM analog receive stored parameters #1          | 150      |
| SIMARConf2    | 85                   | R/W    | 00000110               | SIM analog receive stored parameters #2          | 150      |
| SIMARConf3    | 86                   | R/W    | 00011101               | SIM analog receive stored parameters #3          | 151      |
| SIMARConf4    | 87                   | R/W    | 00100110               | SIM analog receive stored parameters #4          | 151      |
| SIMParConf    | 88                   | W      | 00000000               | SIM analog parameter selection                   | 151      |
|               | 89 - FF              |        |                        | Reserved   |          |

## Chiplet Reset Registers

The bits of the chiplet reset registers control the enabling and disabling of complete chiplets.

For each bit position: 0: Reset inactive for this chiplet

1: Reset active (chiplet is disabled; DEFAULT)

### 1.1: RESGP1 [3800 H]

| Signal Name | Bits | Access | Default | Description              |
|-------------|------|--------|---------|--------------------------|
| ResPT4      | 0    | R/W    | 1       | Reset to chiplet PH_Tx4  |
| ResPT3      | 1    | R/W    | 1       | Reset to chiplet PH_Tx3  |
| ResPT2      | 2    | R/W    | 1       | Reset to chiplet PH_Tx2  |
| ResPT1      | 3    | R/W    | 1       | Reset to chiplet PH_Tx1  |
| ResIR2      | 4    | R/W    | 1       | Reset to chiplet ACI_Rx2 |
| ResIR1      | 5    | R/W    | 1       | Reset to chiplet ACI_Rx1 |
| ResIT2      | 6    | R/W    | 1       | Reset to chiplet ACI_Tx2 |
| ResIT1      | 7    | R/W    | 1       | Reset to chiplet ACI_Tx1 |

### 1.2: RESGP2 [3801 H]

| Signal Name | Bits | Access | Default | Description              |
|-------------|------|--------|---------|--------------------------|
| ResHT4      | 0    | R/W    | 1       | Reset to chiplet ACH_Tx4 |
| ResHT3      | 1    | R/W    | 1       | Reset to chiplet ACH_Tx3 |
| ResHT2      | 2    | R/W    | 1       | Reset to chiplet ACH_Tx2 |
| ResHT1      | 3    | R/W    | 1       | Reset to chiplet ACH_Tx1 |
| ResPR4      | 4    | R/W    | 1       | Reset to chiplet PH_Rx4  |
| ResPR3      | 5    | R/W    | 1       | Reset to chiplet PH_Rx3  |
| ResPR2      | 6    | R/W    | 1       | Reset to chiplet PH_Rx2  |
| ResPR1      | 7    | R/W    | 1       | Reset to chiplet PH_Rx1  |

### 1.3: RESGP3 [3802 H]

| Signal Name | Bits | Access | Default | Description              |
|-------------|------|--------|---------|--------------------------|
| ResOT4      | 0    | R/W    | 1       | Reset to chiplet OFP_Tx4 |
| ResOT3      | 1    | R/W    | 1       | Reset to chiplet OFP_Tx3 |
| ResOT2      | 2    | R/W    | 1       | Reset to chiplet OFP_Tx2 |
| ResOT1      | 3    | R/W    | 1       | Reset to chiplet OFP_Tx1 |
| ResHR4      | 4    | R/W    | 1       | Reset to chiplet ACH_Rx4 |
| ResHR3      | 5    | R/W    | 1       | Reset to chiplet ACH_Rx3 |
| ResHR2      | 6    | R/W    | 1       | Reset to chiplet ACH_Rx2 |
| ResHR1      | 7    | R/W    | 1       | Reset to chiplet ACH_Rx1 |

### 1.4: RESGP4 [3803 H]

| Signal Name | Bits | Access | Default | Description              |
|-------------|------|--------|---------|--------------------------|
| APSRxRes    | 0    | R/W    | 1       | Reset to APS_Rx          |
| APSTxRes    | 1    | R/W    | 1       | Reset to APS_Tx          |
| ResPPP      | 2    | R/W    | 1       | Reset to chiplet PPP     |
| Reserved    | 3    | R/W    | 1       | Reserved                 |
| ResOR4      | 4    | R/W    | 1       | Reset to chiplet OFP_Rx4 |
| ResOR3      | 5    | R/W    | 1       | Reset to chiplet OFP_Rx3 |
| ResOR2      | 6    | R/W    | 1       | Reset to chiplet OFP_Rx2 |
| ResOR1      | 7    | R/W    | 1       | Reset to chiplet OFP_Rx1 |

### 1.5: RESGP5 [3804 H]

| Signal Name | Bits | Access | Default | Description              |
|-------------|------|--------|---------|--------------------------|
| RxRPIS4     | 0    | R/W    | 1       | Reset to chiplet PIS_Rx4 |
| RxRPIS3     | 1    | R/W    | 1       | Reset to chiplet PIS_Rx3 |
| RxRPIS2     | 2    | R/W    | 1       | Reset to chiplet PIS_Rx2 |
| RxRPIS1     | 3    | R/W    | 1       | Reset to chiplet PIS_Rx1 |
| TxRPIS4     | 4    | R/W    | 1       | Reset to chiplet PIS_Tx4 |
| TxRPIS3     | 5    | R/W    | 1       | Reset to chiplet PIS_Tx3 |
| TxRPIS2     | 6    | R/W    | 1       | Reset to chiplet PIS_Tx2 |
| TxRPIS1     | 7    | R/W    | 1       | Reset to chiplet PIS_Tx1 |

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**1.6: RESGP6 [3805 H]**

| Signal Name | Bits | Access | Default | Description              |
|-------------|------|--------|---------|--------------------------|
| Reserved    | 3:0  | R/W    | 0000    | Reserved                 |
| RxRESET     | 4    | R/W    | 0       | Reset to chiptlet SIM_Rx |
| TxRESET     | 5    | R/W    | 0       | Reset to chiptlet SIM_Tx |
| RxRPIM      | 6    | R/W    | 1       | Reset to chiptlet PIM_Rx |
| TxRPIM      | 7    | R/W    | 1       | Reset to chiptlet PIM_Tx |

**1.7: RESGP7 [3806 H]**

| Signal Name | Bits | Access | Default | Description               |
|-------------|------|--------|---------|---------------------------|
| RxReset4    | 0    | R/W    | 0       | Reset to chiptlet SIM_Rx4 |
| RxReset3    | 1    | R/W    | 0       | Reset to chiptlet SIM_Rx3 |
| RxReset2    | 2    | R/W    | 0       | Reset to chiptlet SIM_Rx2 |
| RxReset1    | 3    | R/W    | 0       | Reset to chiptlet SIM_Rx1 |
| TxReset4    | 4    | R/W    | 0       | Reset to chiptlet SIM_Tx4 |
| TxReset3    | 5    | R/W    | 0       | Reset to chiptlet SIM_Tx3 |
| TxReset2    | 6    | R/W    | 0       | Reset to chiptlet SIM_Tx2 |
| TxReset1    | 7    | R/W    | 0       | Reset to chiptlet SIM_Tx1 |

## Chiptlet Interrupt Request and Mask Registers

The chiptlet interrupt request registers indicate pending interrupt requests from individual chiptlets. An active bit of these registers is reset by removing the cause for the request in the corresponding chiptlet or by masking the active IRQ bit(s) in the chiptlet; therefore, these registers are read-only.

For each bit position: 0: No chiptlet interrupt request pending  
1: Chiptlet has pending interrupt request(s)

The chiptlet interrupt request mask register bits control the propagation of a chiptlet interrupt request to the SONET/SDH framer interrupt output pin. The mask registers allow read and write access.

For each bit position: 0: The corresponding interrupt request bit is masked (DEFAULT)  
1: The corresponding interrupt request bit is active (for IRMG1, the corresponding interrupt request bit activates the SONET/SDH framer Interrupt)

### 2.1: IRQGP1, IRMG1 [3810 H Request, 3818 H Mask]

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| FElocHS     | 0    | R      | 0       | Pending handshaking error active. This bit is set when a bit in the HShake1 register and its corresponding interrupt mask bit in the HSMask1 register are both set to '1'.    |
| FElocCS     | 1    | R      | 0       | Pending clock status error active. This bit is set when a bit in the ClkStat1 register and its corresponding interrupt mask bit in the ClkMask1 register are both set to '1'. |
| Reserved    | 2    | R      | 0       | Reserved  |
| Reserved    | 3    | R      | 0       | Reserved  |
| IRQGP5      | 4    | R      | 0       | Pending IRQ active in IRQGP5 register   |
| IRQGP4      | 5    | R      | 0       | Pending IRQ active in IRQGP4 register   |
| IRQGP3      | 6    | R      | 0       | Pending IRQ active in IRQGP3 register   |
| IRQGP2      | 7    | R      | 0       | Pending IRQ active in IRQGP2 register   |

### 2.2: IRQGP2, IRMG2 [3811 H Request, 3819 H Mask]

| Signal Name | Bits | Access | Default | Description      |
|-------------|------|--------|---------|------------------|
| IRQPT4      | 0    | R      | 0       | IRQ from PH_Tx4  |
| IRQPT3      | 1    | R      | 0       | IRQ from PH_Tx3  |
| IRQPT2      | 2    | R      | 0       | IRQ from PH_Tx2  |
| IRQPT1      | 3    | R      | 0       | IRQ from PH_Tx1  |
| IRQIR2      | 4    | R      | 0       | IRQ from ACI_Rx2 |
| IRQIR1      | 5    | R      | 0       | IRQ from ACI_Rx1 |
| IRQIT2      | 6    | R      | 0       | IRQ from ACI_Tx2 |
| IRQIT1      | 7    | R      | 0       | IRQ from ACI_Tx1 |

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**2.3: IRQGP3, IRMG3 [3812 H Request, 381A H Mask]**

| Signal Name | Bits | Access | Default | Description      |
|-------------|------|--------|---------|------------------|
| IRQHT4      | 0    | R      | 0       | IRQ from ACH_Tx4 |
| IRQHT3      | 1    | R      | 0       | IRQ from ACH_Tx3 |
| IRQHT2      | 2    | R      | 0       | IRQ from ACH_Tx2 |
| IRQHT1      | 3    | R      | 0       | IRQ from ACH_Tx1 |
| IRQPR4      | 4    | R      | 0       | IRQ from PH_Rx4  |
| IRQPR3      | 5    | R      | 0       | IRQ from PH_Rx3  |
| IRQPR2      | 6    | R      | 0       | IRQ from PH_Rx2  |
| IRQPR1      | 7    | R      | 0       | IRQ from PH_Rx1  |

**2.4: IRQGP4, IRMG4 [3813 H Request, 381B H Mask]**

| Signal Name | Bits | Access | Default | Description      |
|-------------|------|--------|---------|------------------|
| IRQOT4      | 0    | R      | 0       | IRQ from OFP_Tx4 |
| IRQOT3      | 1    | R      | 0       | IRQ from OFP_Tx3 |
| IRQOT2      | 2    | R      | 0       | IRQ from OFP_Tx2 |
| IRQOT1      | 3    | R      | 0       | IRQ from OFP_Tx1 |
| IRQHR4      | 4    | R      | 0       | IRQ from ACH_Rx4 |
| IRQHR3      | 5    | R      | 0       | IRQ from ACH_Rx3 |
| IRQHR2      | 6    | R      | 0       | IRQ from ACH_Rx2 |
| IRQHR1      | 7    | R      | 0       | IRQ from ACH_Rx1 |

**2.5: IRQGP5, IRMG5 [3814 H Request, 381C H Mask]**

| Signal Name | Bits | Access | Default | Description      |
|-------------|------|--------|---------|------------------|
| Reserved    | 2:0  | R      | 000     | Reserved         |
| IRQPPP      | 3    | R      | 0       | IRQ from PPP     |
| IRQOR4      | 4    | R      | 0       | IRQ from OFP_Rx4 |
| IRQOR3      | 5    | R      | 0       | IRQ from OFP_Rx3 |
| IRQOR2      | 6    | R      | 0       | IRQ from OFP_Rx2 |
| IRQOR1      | 7    | R      | 0       | IRQ from OFP_Rx1 |

## Handshaking Error Indication and Mask Registers

The local handshaking error indication registers indicate pending handshaking error requests from the GPPINT chiplet. HShake1 consists of pointer bits that indicate active requests in registers HShake2/3/4/5.

For each bit position: 0: Normal operation of the corresponding chiplet

1: The corresponding chiplet did not de-assert its DTACK signal

Exception: The signals TOError and IntError (HShake5(1:0)) have the following meaning:

### 3.1: TOError and IntError Meanings

| TOError | IntError | Description  |
|---------|----------|--|
| 0       | 0        | Normal operation   |
| 0       | 1        | GPP de-asserts strobes without waiting for $\overline{\text{GPDTACK}}$ assertion. This means that the external microprocessor, instead of inserting more wait states, has de-asserted either GPSEL or GPDS (GPRD/GPWR in Intel mode) before the $\overline{\text{GPDTACK}}$ signal was asserted. |
| 1       | 0        | Watchdog Timeout in REST state. A timeout in this state indicates that the chiplet addressed in the current read cycle has a problem.  |
| 1       | 1        | Watchdog Timeout in REQ state. A timeout in this state indicates that the SONET/SDH framer was busy working on the prior read or write transaction when the timeout occurred and the current transaction has also failed.  |

An active bit of the handshaking error indication registers is reset by removing the cause for the malfunctioning of the chiplet and by writing a '1' into the corresponding bit position. Reading one of these registers will reset all bits of this register if the "clear-register" option is set in ConfGP1(2).

The handshaking error indication mask register bits control the propagation of the GPPINT handshaking error requests to bits 7 to 4 of register HShake1. HSMask1 controls propagation to the signal FElocHS (bit 0 of IRQGP1 register). The mask registers allow read and write access.

For each bit position: 0: The corresponding handshaking error indication bit is masked (DEFAULT)

1: The corresponding request bit is active (for HSMask1, the corresponding request bit activates signal FElocHS (bit 0 of IRQGP1 register))

### 3.2: HShake1, HSMask1 [3820 H Error, 3828 H Mask]

| Signal Name | Bits | Access | Default | Description                        |
|-------------|------|--------|---------|------------------------------------|
| Reserved    | 0:3  | R/W    | 0000    | Reserved (pointers)                |
| HShake5     | 4    | R/W    | 0       | Pending HS error active in HShake5 |
| HShake4     | 5    | R/W    | 0       | Pending HS error active in HShake4 |
| HShake3     | 6    | R/W    | 0       | Pending HS error active in HShake3 |
| HShake2     | 7    | R/W    | 0       | Pending HS error active in HShake2 |

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**3.3: HShake2, HSMask2 [3821 H Error, 3829 H Mask]**

| Signal Name | Bits | Access | Default | Description                     |
|-------------|------|--------|---------|---------------------------------|
| PH_Tx4      | 0    | R/W    | 0       | DTACK from PH_Tx4 stuck at ONE  |
| PH_Tx3      | 1    | R/W    | 0       | DTACK from PH_Tx3 stuck at ONE  |
| PH_Tx2      | 2    | R/W    | 0       | DTACK from PH_Tx2 stuck at ONE  |
| PH_Tx1      | 3    | R/W    | 0       | DTACK from PH_Tx1 stuck at ONE  |
| ACI-Rx2     | 4    | R/W    | 0       | DTACK from ACI_Rx2 stuck at ONE |
| ACI-Rx1     | 5    | R/W    | 0       | DTACK from ACI_Rx1 stuck at ONE |
| ACI-Tx2     | 6    | R/W    | 0       | DTACK from ACI_Tx2 stuck at ONE |
| ACI-Tx1     | 7    | R/W    | 0       | DTACK from ACI_Tx1 stuck at ONE |

**3.4: HShake3, HSMask3 [3822 H Error, 382A H Mask]**

| Signal Name | Bits | Access | Default | Description                     |
|-------------|------|--------|---------|---------------------------------|
| ACH_Tx4     | 0    | R/W    | 0       | DTACK from ACH_Tx4 stuck at ONE |
| ACH_Tx3     | 1    | R/W    | 0       | DTACK from ACH_Tx3 stuck at ONE |
| ACH_Tx2     | 2    | R/W    | 0       | DTACK from ACH_Tx2 stuck at ONE |
| ACH_Tx1     | 3    | R/W    | 0       | DTACK from ACH_Tx1 stuck at ONE |
| PH_Rx4      | 4    | R/W    | 0       | DTACK from PH_Rx4 stuck at ONE  |
| PH_Rx3      | 5    | R/W    | 0       | DTACK from PH_Rx3 stuck at ONE  |
| PH_Rx2      | 6    | R/W    | 0       | DTACK from PH_Rx2 stuck at ONE  |
| PH_Rx1      | 7    | R/W    | 0       | DTACK from PH_Rx1 stuck at ONE  |

**3.5: HShake4, HSMask4 [3823 H Error, 382B H Mask]**

| Signal Name | Bits | Access | Default | Description                     |
|-------------|------|--------|---------|---------------------------------|
| OFF_Tx4     | 0    | R/W    | 0       | DTACK from OFF_Tx4 stuck at ONE |
| OFF_Tx3     | 1    | R/W    | 0       | DTACK from OFF_Tx3 stuck at ONE |
| OFF_Tx2     | 2    | R/W    | 0       | DTACK from OFF_Tx2 stuck at ONE |
| OFF_Tx1     | 3    | R/W    | 0       | DTACK from OFF_Tx1 stuck at ONE |
| ACH_Rx4     | 4    | R/W    | 0       | DTACK from ACH_Rx4 stuck at ONE |
| ACH_Rx3     | 5    | R/W    | 0       | DTACK from ACH_Rx3 stuck at ONE |
| ACH_Rx2     | 6    | R/W    | 0       | DTACK from ACH_Rx2 stuck at ONE |
| ACH_Rx1     | 7    | R/W    | 0       | DTACK from ACH_Rx1 stuck at ONE |

**3.6: HShake5, HSMask5 [3824 H Error, 382C H Mask]**

| Signal Name | Bits | Access | Default | Description  |
|-------------|------|--------|---------|--|
| IntError    | 0    | R/W    | 0       | GPP Interface Error (see TOError and IntError Meanings on page 121)                |
| TOError     | 1    | R/W    | 0       | Timeout Error of the GPP interface (see TOError and IntError Meanings on page 121) |
| AccViol     | 2    | R/W    | 0       | Write access to protected register was attempted                                   |
| PPP         | 3    | R/W    | 0       | DTACK from PPP stuck at ONE  |
| OFP_Rx4     | 4    | R/W    | 0       | DTACK from OFP_Rx4 stuck at ONE  |
| OFP_Rx3     | 5    | R/W    | 0       | DTACK from OFP_Rx3 stuck at ONE  |
| OFP_Rx2     | 6    | R/W    | 0       | DTACK from OFP_Rx2 stuck at ONE  |
| OFP_Rx1     | 7    | R/W    | 0       | DTACK from OFP_Rx1 stuck at ONE  |

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### Clock Monitor Status and Mask Registers

The clock monitor status register bits indicate the loss of a specific island's clock. They are set whenever a difference between the clock test signal and the individual island's clock acknowledge signal occurs after the clock monitor test period. ClkStat1 consists of pointer bits that indicate active clock status errors in ClkStat2/3/4.

For each bit position: 0: Normal operation of the corresponding clock island  
1: The corresponding island clock is lost

An active bit of these registers is reset by restoring the clock of the corresponding clock island and by writing a '1' into the corresponding bit position. Reading one register will reset all bits of this register if the "clear-register" option is set in bit ConfGP1(3).

The clock monitor mask registers ClkMask2/3/4 control the propagation of active clock monitor status signals to bits 7/6/5 of ClkStat1. ClkMask1 controls propagation to the signal FElocCS (bit 1 of IRQGP1 register). The mask registers allow read and write access.

For each bit position: 0: The corresponding clock status bit is masked (DEFAULT)  
1: The corresponding clock status bit is active (for ClkMask1, the corresponding bit activates the signal FElocCS (bit 1 of IRQGP1 register))

#### 4.1: ClkStat1, ClkMask1 [3830 H Status, 3838 H Mask]

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| Reserved    | 4:0  | R/W    | 00000   | Reserved (pointers)   |
| ClkStat4    | 5    | R/W    | 0       | Pending active clock status error indication in ClkStat4 register |
| ClkStat3    | 6    | R/W    | 0       | Pending active clock status error indication in ClkStat3 register |
| ClkStat2    | 7    | R/W    | 0       | Pending active clock status error indication in ClkStat2 register |

#### 4.2: ClkStat2, ClkMask2 [3831 H Status, 3839 H Mask]

| Signal Name | Bits | Access | Default | Description                     |
|-------------|------|--------|---------|---------------------------------|
| PH_Tx4      | 0    | R/W    | 0       | Clock island PH_Tx4 lost clock  |
| PH_Tx3      | 1    | R/W    | 0       | Clock island PH_Tx3 lost clock  |
| PH_Tx2      | 2    | R/W    | 0       | Clock island PH_Tx2 lost clock  |
| PH_Tx1      | 3    | R/W    | 0       | Clock island PH_Tx1 lost clock  |
| ACI_Rx2     | 4    | R/W    | 0       | Clock island ACI_Rx2 lost clock |
| ACI_Rx1     | 5    | R/W    | 0       | Clock island ACI_Rx1 lost clock |
| ACI_Tx2     | 6    | R/W    | 0       | Clock island ACI_Tx2 lost clock |
| ACI_Tx1     | 7    | R/W    | 0       | Clock island ACI_Tx1 lost clock |

**4.3: ClkStat3, ClkMask3 [3832 H Status, 383A H Mask]**

| Signal Name | Bits | Access | Default | Description                     |
|-------------|------|--------|---------|---------------------------------|
| OFF_Rx2     | 0    | R/W    | 0       | Clock island OFF_Rx2 lost clock |
| OFF_Rx1     | 1    | R/W    | 0       | Clock island OFF_Rx1 lost clock |
| OFF_Tx2     | 2    | R/W    | 0       | Clock island OFF_Tx2 lost clock |
| OFF_Tx1     | 3    | R/W    | 0       | Clock island ACH_Tx1 lost clock |
| PH_Rx4      | 4    | R/W    | 0       | Clock island PH_Rx4 lost clock  |
| PH_Rx3      | 5    | R/W    | 0       | Clock island PH_Rx3 lost clock  |
| PH_Rx2      | 6    | R/W    | 0       | Clock island PH_Rx2 lost clock  |
| PH_Rx1      | 7    | R/W    | 0       | Clock island PH_Rx1 lost clock  |

**4.4: ClkStat4, ClkMask4 [3833 H Status, 383B H Mask]**

| Signal Name | Bits | Access | Default | Description                           |
|-------------|------|--------|---------|---------------------------------------|
| Reserved    | 0    | R/W    | 0       | Reserved                              |
| COMBUS4     | 1    | R/W    | 0       | Clock island Telecom Bus 4 lost clock |
| COMBUS3     | 2    | R/W    | 0       | Clock island Telecom Bus 3 lost clock |
| COMBUS2     | 3    | R/W    | 0       | Clock island Telecom Bus 2 lost clock |
| COMBUS1     | 4    | R/W    | 0       | Clock island Telecom Bus 1 lost clock |
| LTRC        | 5    | R/W    | 0       | Clock island AIP lost clock           |
| OFF_Rx4     | 6    | R/W    | 0       | Clock island OFF_Rx4 lost clock       |
| OFF_Rx3     | 7    | R/W    | 0       | Clock island OFF_Rx3 lost clock       |

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**Clock Monitor Test Period Register**

CMonGP1: Divider ratio to derive the clock monitor test period from the GPPCLK clock. Clock monitoring is disabled if equal to 00 H (DEFAULT). A 50 MHz GPPCLK frequency results in a maximum of 5.1  $\mu$ s for the clock test period. This allows clock islands down to a frequency of 197 kHz to be monitored.

**Note:** If the UTOPIA interface clocks go below 197 kHz when a 50 MHz GPPCLK clock is used and the Clock Monitor Test Period Register is set to FF H, then an interrupt will be generated because the UTOPIA clock period will be smaller than the clock monitor test period. In this case, the interrupt could be masked or the Clock Monitor Test Period Register can be set to 00 H.

**5.1: CMonGP1 [3848 H]**

| Signal Name  | Bits | Access | Default  | Description                         |
|--------------|------|--------|----------|-------------------------------------|
| CMonGP1(7:0) | 7:0  | R/W    | 00000000 | Number of GPPCLK cycles/test period |

## Watchdog Timer Period Register

WDTGP1: Divider ratio to derive the interface time-out period from the GPPCLK clock. This register is reset to FF H whenever a timeout occurs; it has to be reconfigured by a GPP write access. The purpose of the watchdog timer is to set a limit as to how long an access is allowed to last before that access is terminated by the  $\overline{\text{GPDTACK}}/\overline{\text{GPRDY}}$  signal being forced active. A maskable interrupt can be generated to the external microprocessor when the watchdog timer times out.

The watchdog timer counts the number of GPPCLK clocks since the time that a register has been accessed. The access will terminate when either of the following two events occurs:

1. The watchdog timer times out (the  $\overline{\text{GPDTACK}}/\overline{\text{GPRDY}}$  signal is forced active so that the cycle terminates). In this case the write does not occur or the read does not return valid data.
2. The cycle terminates naturally.

### 6.1: WDTGP1 [3849 H]

| Signal Name | Bits | Access | Default  | Description                                       |
|-------------|------|--------|----------|---|
| WDTGP1(7:0) | 7:0  | R/W    | 11111111 | Number of GPPCLK clock cycles per time-out period |

**IBM SONET/SDH Framer**
**Local (GPPINT) Configuration Register**

ConfGP1: The bits of this local configuration register control the resetting of complete registers upon read access (“clear-register” option).

For each bit position: 0: No action upon read access

1: The corresponding register is reset upon read access (DEFAULT)

**7.1: ConfGP1 [384A H]**

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| Reserved    | 0    | R/W    | 1       | Reserved  |
| SIMStat     | 1    | R/W    | 1       | Clear-bit for register SIMStat. When this bit is set to a '1' the bits in the SIMStat register clear on read. When set to a '0', the bits in the SIMStat register do not clear on read. For either setting of this bit, the bits in the SIMStat register can be individually cleared by writing a '1' to them, provided that the alarm condition is removed.                  |
| HShake      | 2    | R/W    | 1       | Clear-bit for registers HShake1-5. When this bit is set to a '1' the bits in the HShake1-5 registers clear on read. When set to a '0', the bits in the HShake1-5 registers do not clear on read. For either setting of this bit, the bits in the HShake1-5 registers can be individually cleared by writing a '1' to them, provided that the alarm condition is removed.      |
| ClkStat     | 3    | R/W    | 1       | Clear-bit for registers ClkStat1-4. When this bit is set to a '1', the bits in the ClkStat1-4 registers clear on read. When set to a '0', the bits in the ClkStat1-4 registers do not clear on read. For either setting of this bit, the bits in the ClkStat1-4 registers can be individually cleared by writing a '1' to them, provided that the alarm condition is removed. |
| Reserved    | 7:4  | R/W    | 1111    | Reserved  |

**IBM Internal Use Register**

This read-only register is for IBM internal use only.

**8.1: VPD [3850 H]**

| Signal Name | Bits | Access | Default | Description                                 |
|-------------|------|--------|---------|---|
| TESTSITE    | 4:0  | R      | 000vv   | This register is for IBM internal use only. |
| SMART       | 7:5  | R      | 100     | This register is for IBM internal use only. |

## Static Configuration Registers

Common static configuration data, providing control signals that are distributed to multiple chiplets. This is set once by the GPP before the individual chiplets get enabled and is not changed during normal operation.

### 9.1: GContTx [3858 H]

GContTx: Container handling in transmit macros.

| Signal Name   | Bits | Access | Default | Description  |
|---------------|------|--------|---------|--|
| GContTx1(1:0) | 1:0  | R/W    | 00      | Set ATM, Loop or TB mode for each SONET/SDH macro in transmit direction:<br>00: SONET/SDH macro in ATM/PPP mode (C4).<br>01: SONET/SDH macro in Loop mode (VC-4).<br>10: SONET/SDH macro in TB mode (AU-4). In this mode, transmit retiming is not performed. Therefore, an AU-4 (i.e., VC-4 with pointers) must be provided to the SONET/SDH framer's transmit Telecom Bus. The TXCFRM and either the TXCCLK or TXCCLK signals must be used to source data into the transmit Telecom Bus. See Telecom Bus Interface on page 19.<br>11: SONET/SDH macro in TB mode (VC-4). In this mode, transmit retiming is performed. |
| GContTx2(1:0) | 3:2  | R/W    | 00      |  |
| GContTx3(1:0) | 5:4  | R/W    | 00      |  |
| GContTx4(1:0) | 7:6  | R/W    | 00      |  |

### 9.2: GConRx [3859 H]

GConRx: Container handling in receive macros.

| Signal Name  | Bits | Access | Default | Description  |
|--------------|------|--------|---------|--|
| GConRx1(1:0) | 1:0  | R/W    | 00      | Set ATM, Loop or TB mode for each SONET/SDH macro in receive direction:<br>00: SONET/SDH macro in ATM/PPP mode (C4).<br>01: SONET/SDH macro in Loop mode (VC-4).<br>10: SONET/SDH macro in TB mode.<br>11: Do not use. |
| GConRx2(1:0) | 3:2  | R/W    | 00      |  |
| GConRx3(1:0) | 5:4  | R/W    | 00      |  |
| GConRx4(1:0) | 7:6  | R/W    | 00      |  |

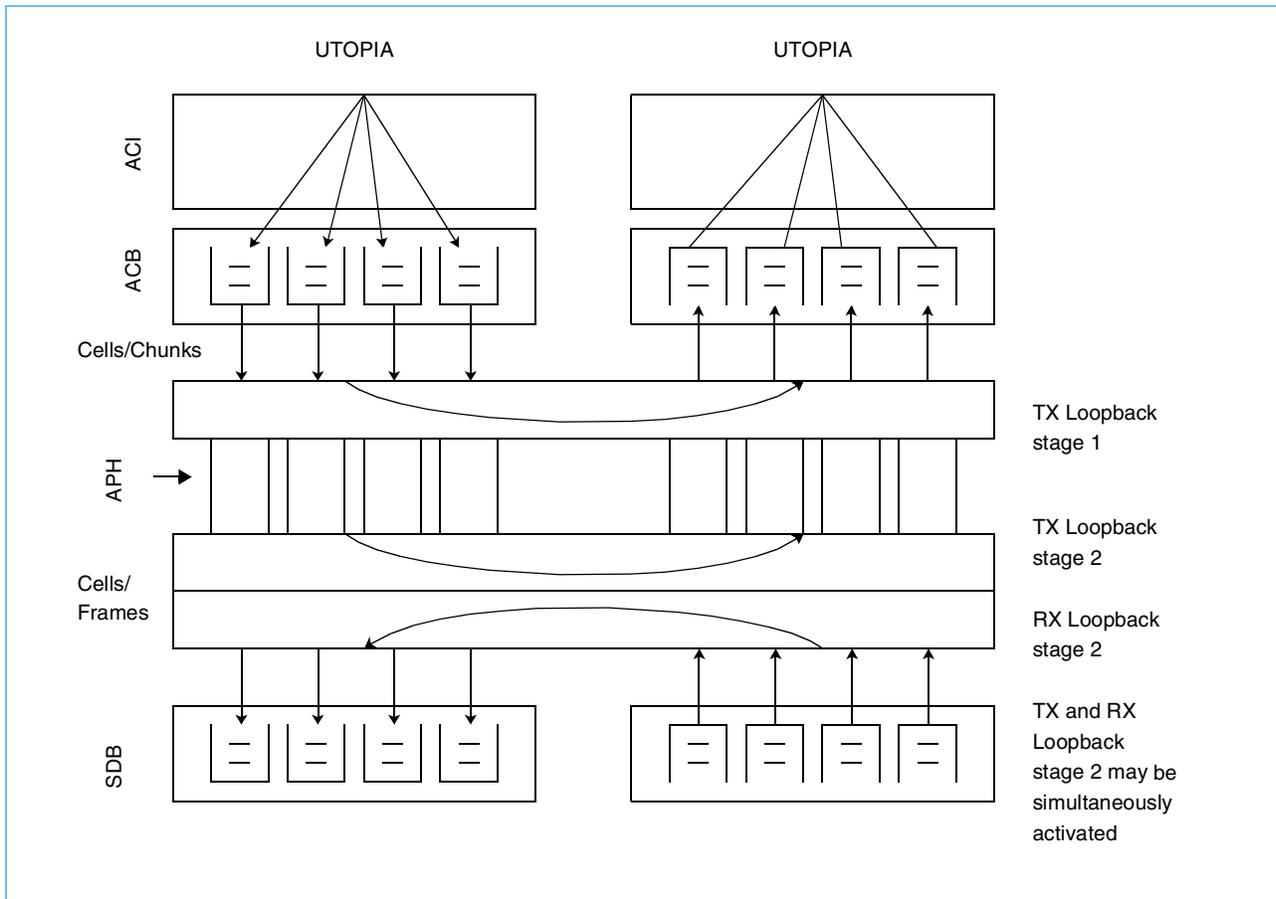
**IBM SONET/SDH Framer**
**9.3: GCasc (Lower Nibble) [385A H]**

| Signal Name  | Bits | Access | Default | Description   |
|--------------|------|--------|---------|---|
| GCascTx(3:0) | 3:0  | R/W    | 1000    | <p>Defines cascading of SONET/SDH macros and SONET/SDH framer chips in transmit direction:</p> <p>One SONET/SDH framer used, each SONET/SDH macro operates individually (8 bits):<br/>           0001,0111: up to 4 x STS-3c (4 x 155 Mb/s ATM )<br/>           1000: up to 4 x STM-1 (4 x 155 Mb/s ATM )</p> <p>One SONET/SDH framer used, four SONET/SDH macros operate in parallel:<br/>           0011: 1 x STS-12 (4 x 155 Mb/s ATM)<br/>           1001: 1 x STM-4 (4 x 155 Mb/s ATM or 4 x VC4)<br/>           1010,1101,1110,1111: 1 x STM-4c (1 x 622 Mb/s ATM or 1 x VC4-4c)</p> <p>Four SONET/SDH framers used, all SONET/SDH macros operate in parallel:<br/>           1011: 1 x STM-16 (16 x 155 Mb/s ATM or 16 x VC4)<br/>           1100: 1 x STM-16 (4 x 622 Mb/s ATM or 4 x VC4-4c)<br/>           0000, 0010, 0100, 0101, 0110: Do Not Use</p> |

**9.4: GCasc (Upper Nibble) [385A H]**

| Signal Name  | Bits | Access | Default | Description  |
|--------------|------|--------|---------|--|
| GCascRx(3:0) | 7:4  | R/W    | 1000    | <p>Defines cascading of SONET/SDH macros and SONET/SDH framer chips in receive direction:</p> <p>One SONET/SDH framer used, each SONET/SDH macro operates individually (8 bits):<br/>           0001,0111: up to 4 x STS-3c (4 x 155 Mb/s ATM )<br/>           1000: up to 4 x STM-1(4 x 155 Mbit/s ATM )</p> <p>One SONET/SDH framer used, four SONET/SDH macros operate in parallel:<br/>           0011: 1 x STS-12 (4 x 155 Mb/s ATM)<br/>           1001: 1 x STM-4(4 x 155 Mb/s ATM or 4 x VC4)<br/>           1010,1101,1110,1111: 1 x STM-4c (1 x 622 Mb/s ATM or 1 x VC4-4c)</p> <p>Four SONET/SDH framers used, all SONET/SDH macros operate in parallel:<br/>           1011: 1 x STM-16 (16 x 155 Mb/s ATM or 16 x VC4)<br/>           1100: 1 x STM-16 (4 x 622 Mb/s ATM or 4 x VC4-4c)<br/>           0000, 0010, 0100, 0101, 0110: Do Not Use</p> |

### Loopback Capabilities





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**9.5: GLoopTx1 [385B H]**

Transmit loopback stage 1 control. When this loopback is enabled, cells/chunks that are put into the transmit ACB are looped back to their corresponding receive ACB without TCSF processing. Bit positions 7-4 set the mode of the respective loopback to on-the-fly monitoring or loopback- only. On-the-fly monitoring allows cells/chunks to be forwarded to the SONET/SDH line after TCSF processing has been performed, while cells/chunks are internally looped back before TCSF processing is performed. Loopback-only mode disables cells/chunks from being transmitted out to the SONET/SDH line; only the loopback function is performed. Refer to Loopback Capabilities on page 131.

For bit positions 3 to 0: 0: ACH Loopback #1 disabled (DEFAULT)  
 1: ACH Loopback #1 enabled

For bit positions 7 to 4: 0: On-the-fly monitoring (LpB #1)  
 1: Loopback #1 only

| Signal Name | Bit | Access | Default | Description                            |
|-------------|-----|--------|---------|--|
| TxLpB11     | 0   | R/W    | 0       | Loopback #1 control, transmit macro #1 |
| TxLpB12     | 1   | R/W    | 0       | Loopback #1 control, transmit macro #2 |
| TxLpB13     | 2   | R/W    | 0       | Loopback #1 control, transmit macro #3 |
| TxLpB14     | 3   | R/W    | 0       | Loopback #1 control, transmit macro #4 |
| TxLpB11only | 4   | R/W    | 0       | Loopback #1 only, transmit macro #1    |
| TxLpB12only | 5   | R/W    | 0       | Loopback #1 only, transmit macro #2    |
| TxLpB13only | 6   | R/W    | 0       | Loopback #1 only, transmit macro #3    |
| TxLpB14only | 7   | R/W    | 0       | Loopback #1 only, transmit macro #4    |

## 9.6: GLoopTx2 [385C H]

Transmit loopback stage 2 control. When this loopback is enabled, cells/chunks that are put into the transmit ACB are looped back towards their corresponding receive ACB after the TCSF or PPP processing functions are performed. Bit positions 7-4 set the mode of the respective loopback to on-the-fly monitoring or loopback-only. On-the-fly monitoring allows cells/frames to be transmitted towards the SONET/SDH line in addition to being looped back towards the receive APH blocks. Loopback-only mode disables cells/frames from being transmitted out to the SONET/SDH line; only the loopback function is performed. Refer to Loopback Capabilities on page 131.

For bit positions 3 to 0: 0: ACH Loopback #2 disabled (DEFAULT)

1: ACH Loopback #2 enabled

For bit positions 7 to 4: 0: On-the-fly monitoring (LpB #2)

1: Loopback #2 only

| Signal Name | Bits | Access | Default | Description                            |
|-------------|------|--------|---------|--|
| TxLpB21     | 0    | R/W    | 0       | Loopback #2 control, transmit macro #1 |
| TxLpB22     | 1    | R/W    | 0       | Loopback #2 control, transmit macro #2 |
| TxLpB23     | 2    | R/W    | 0       | Loopback #2 control, transmit macro #3 |
| TxLpB24     | 3    | R/W    | 0       | Loopback #2 control, transmit macro #4 |
| TxLpB21only | 4    | R/W    | 0       | Loopback #2 only, transmit macro #1    |
| TxLpB22only | 5    | R/W    | 0       | Loopback #2 only, transmit macro #2    |
| TxLpB23only | 6    | R/W    | 0       | Loopback #2 only, transmit macro #3    |
| TxLpB24only | 7    | R/W    | 0       | Loopback #2 only, transmit macro #4    |

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### 9.7: GLoopRx [385D H]

Receive loopback control. Cells/frames that are received by the SFH blocks are looped back towards the transmit line. Refer to Loopback Capabilities on page 131.

For bit positions 3 to 0: 0: ACH Loopback #2 disabled (DEFAULT)  
1: ACH Loopback #2 enabled

For bit positions 7 to 4: 0: On-the-fly monitoring (LpB #2)  
1: Loopback #2 only

| Signal Name | Bits | Access | Default | Description                           |
|-------------|------|--------|---------|---------------------------------------|
| RxLpB21     | 0    | R/W    | 0       | Loopback #2 control, receive macro #1 |
| RxLpB22     | 1    | R/W    | 0       | Loopback #2 control, receive macro #2 |
| RxLpB23     | 2    | R/W    | 0       | Loopback #2 control, receive macro #3 |
| RxLpB24     | 3    | R/W    | 0       | Loopback #2 control, receive macro #4 |
| RxLpB21only | 4    | R/W    | 0       | Loopback #2 only, receive macro #1    |
| RxLpB22only | 5    | R/W    | 0       | Loopback #2 only, receive macro #2    |
| RxLpB23only | 6    | R/W    | 0       | Loopback #2 only, receive macro #3    |
| RxLpB24only | 7    | R/W    | 0       | Loopback #2 only, receive macro #4    |

### 9.8: GExtRes [385E H]

External clock recovery circuit reset signal. Delivered to external circuit (deserializer) via device pin. The active level depends on the external circuit used. Default value at power-on reset is low.

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| RSTCRec1    | 0    | R/W    | 0       | External clock recovery circuit reset. The state of this bit is driven out onto the RSTCREC1 pin. |
| Reserved    | 7:1  | R/W    | 0000000 | Reserved  |

### 9.9: CBConf1 [386C H]

Static configuration data, providing control signals for chiplets Telecom Bus and CMUX. This is set once by the GPP before the individual chiplets are enabled and is not changed during normal operation.

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| CKINV4      | 0    | R/W    | 0       | Telecom Bus 4 output clocking:<br>0 on the falling edge of RXTB4CLK<br>1 on the rising edge of RXTB4CLK |
| CKINV3      | 1    | R/W    | 0       | Telecom Bus 3 output clocking:<br>0 on the falling edge of RXTB3CLK<br>1 on the rising edge of RXTB3CLK |
| CKINV2      | 2    | R/W    | 0       | Telecom Bus 2 output clocking:<br>0 on the falling edge of RXTB2CLK<br>1 on the rising edge of RXTB2CLK |
| CKINV1      | 3    | R/W    | 0       | Telecom Bus 1 output clocking:<br>0 on the falling edge of RXTB1CLK<br>1 on the rising edge of RXTB1CLK |
| RATE77      | 4    | R/W    | 0       | This bit is reserved and should always be set to '0'.   |
| EFRM        | 5    | R/W    | 0       | 0 normal position of TXCFRM<br>1 TXCFRM one TXCCLK cycle earlier  |
| Reserved    | 7:6  | R/W    | 00      | Reserved  |

### 9.10: CBConf2 [386D H]

Static configuration data, providing control signals for Telecom Bus \_Rx drivers (tri-state control).

| Signal Name | Bits | Access | Default | Description                    |
|-------------|------|--------|---------|--------------------------------|
| CB_RX1_En   | 0    | R/W    | 0       | Telecom Bus _Rx1 driver enable |
| CB_RX2_En   | 1    | R/W    | 0       | Telecom Bus _Rx2 driver enable |
| CB_RX3_En   | 2    | R/W    | 0       | Telecom Bus _Rx3 driver enable |
| CB_RX4_En   | 3    | R/W    | 0       | Telecom Bus _Rx4 driver enable |
| Reserved    | 7:4  | R/W    | 0000    | Reserved                       |



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**9.11: ACITXGP [3860 H]**

Static configuration data, providing control signals for chiplets ACI\_Tx1 and ACI\_Tx2. This register is set once by the GPP before the individual chiplets are enabled and is not changed during normal operation.

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| L1L2Tx(2:0) | 2:0  | R/W    | 110     | Configuration of the ATM Cell interface, transmit direction:<br>000: all ATM cell interfaces disabled. This mode is not valid for PPP operation.<br>001: UTOPIA interface 1 active only (1 x UTOPIA Level 1, 1 x 8-bit mode), non-STM-4c. This mode is not valid for PPP operation.<br>010: UTOPIA interface 2 active only (1 x UTOPIA Level 1, 1 x 8-bit mode), non-STM-4c. This mode is not valid for PPP operation.<br>011: UTOPIA interface 1 and 2 active (2 x UTOPIA Level 1, 2 x 8-bit mode), non-STM-4c. This mode is not valid for PPP operation.<br>100: all ATM cell interfaces disabled.<br>101: UTOPIA interface 1 active only (1 x UTOPIA Level 2, 1 x 8-bit mode), non-STM-4c. This mode is not valid for PPP operation.<br>110: UTOPIA interface 1 active only (1 x UTOPIA Level 2, 1 x 16-bit mode), non-STM-4c. This mode is valid for PPP operation.<br>111: UTOPIA interface 1 active only (1 x UTOPIA Level 2, 1 x 16-bit mode), STM-4c. This mode is valid for PPP operation. |
| SIndT1(1:0) | 4:3  | R/W    | 10      | Type of status indication for UTOPIA interface 1 (Level 2 only). 10 is the only valid setting when processing PPP data.<br>00: Direct status indication, one status line only (TxClav[0]). (TxClav[1:3] always high impedance).<br>01: Direct status indication, four status lines (TxClav[0:3]).<br>10: Multiplexed status indication, one status line only (TxClav[0]). (TxClav[1:3] always high impedance).<br>11: Multiplexed status indication, four status lines (TxClav[0:3]).   |
| Reserved    | 7:5  | R/W    | 000     | Reserved  |

### 9.12: PHTXGP1 [3861 H]

Static configuration data, providing control signals for chiplets ACI\_Tx1 and ACI\_Tx2. This register is set once by the GPP before the individual chiplets are enabled and must not be changed during normal operation.

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| PHT1(2:0)   | 2:0  | R/W    | 001     | Source of data/control for Transmit Port Handler SONET/SDH macro #1:<br>001: UTOPIA interface 1 (L2 8-bit, L2 16-bit, L1 8-bit)<br>010: UTOPIA interface 2 (L1 8-bit)<br>100: SONET/SDH receive macro #1 (transit mode)<br>101: SONET/SDH receive macro #2 (transit mode)<br>110: SONET/SDH receive macro #3 (transit mode)<br>111: SONET/SDH receive macro #4 (transit mode)<br>others: No source selected (port handler disabled) |
| Reserved    | 3    | R/W    | 0       | Reserved  |
| PHT2(2:0)   | 6:4  | R/W    | 001     | Source of data/control for Transmit Port Handler SONET/SDH macro #2:<br>Same effect as for PHT1 above.  |
| Reserved    | 7    | R/W    | 0       | Reserved  |

### 9.13: PHTXGP2 [3862 H]

Static configuration data, providing control signals for chiplets ACI\_Tx1 and ACI\_Tx2. This register is set once by the GPP before the individual chiplets are enabled and must not be changed during normal operation.

| Signal Name | Bit Pos. | Access | Default | Description  |
|-------------|----------|--------|---------|--|
| PHT3(2:0)   | 2:0      | R/W    | 001     | Source of data/control for Transmit Port Handler SONET/SDH macro #3:<br>Same effect as for PHT1 in previous table. |
| Reserved    | 3        | R/W    | 0       | Reserved   |
| PHT4(2:0)   | 6:4      | R/W    | 001     | Source of data/control for Transmit Port Handler SONET/SDH macro #4:<br>Same effect as for PHT1 in previous table. |
| Reserved    | 7        | R/W    | 0       | Reserved   |



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**9.14: ACIRXGP [3863 H]**

Static configuration data, providing control signals for chiplets ACI\_Rx1 and ACI\_Rx2. This register is set once by the GPP before the individual chiplets are enabled and is not changed during normal operation.

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| L1L2Rx(2:0) | 2:0  | R/W    | 110     | Selection of the configuration of the ATM Cell interface, receive direction:<br>000: All ATM cell interfaces disabled. This mode is not valid for PPP operation.<br>001: UTOPIA interface 1 active only (1 x UTOPIA Level 1, 1 x 8-bit mode), non-STM-4c. This mode is not valid for PPP operation.<br>010: UTOPIA interface 2 active only (1 x UTOPIA Level 1, 1 x 8-bit mode), non-STM-4c. This mode is not valid for PPP operation.<br>011: UTOPIA interface 1 and 2 active (2 x UTOPIA Level 1, 2 x 8-bit mode), non-STM-4c. This mode is not valid for PPP operation.<br>100: All ATM cell interfaces disabled. This mode is not valid for PPP operation.<br>101: UTOPIA interface 1 active only (1 x UTOPIA Level 2, 1 x 8-bit mode), non-STM-4c. This mode is not valid for PPP operation.<br>110: UTOPIA interface 1 active only (1 x UTOPIA Level 2, 1 x 16-bit mode), non-STM-4c. This mode is valid for PPP operation.<br>111: UTOPIA interface 1 active only (1 x UTOPIA Level 2, 1 x 16-bit mode), STM-4c. This mode is not valid for PPP operation. |
| SIndR1(1:0) | 4:3  | R/W    | 10      | Type of status indication for UTOPIA interface 1 (Level 2 only). 10 is the only valid setting when processing PPP data.<br>00: Direct status indication, one status line only (RxClav[0]). (RxClav[1:3] always high impedance).<br>01: Direct status indication, four status lines (RxClav[0:3]).<br>10: Multiplexed status indication, one status line only (RxClav[0]). (RxClav[1:3] always high impedance).<br>11: Multiplexed status indication, four status lines (RxClav[0:3]).   |
| Reserved    | 7:5  | R/W    | 000     | Reserved  |

**9.15: PHRXGP1 [3864 H]**

Static configuration data, providing control signals for chiplets ACI\_Rx1 and ACI\_Rx2. This register is set once by the GPP before the individual chiplets are enabled and must not be changed during normal operation.

| Signal Name | Bits | Access | Default | Description  |
|-------------|------|--------|---------|--|
| PHR1(2:0)   | 2:0  | R/W    | 001     | Sink of data selected for Receive Port Handler macro #1:<br>001: UTOPIA interface 1<br>010: UTOPIA interface 2<br>100: Transmit macros (internal transit mode)<br>others: No sink selected (port handler disabled) |
| Reserved    | 3    | R/W    | 0       | Reserved   |
| PHR2(2:0)   | 6:4  | R/W    | 001     | Sink of data selected for Receive Port Handler macro #2: Same effect as for PHR1 above.  |
| Reserved    | 7    | R/W    | 0       | Reserved   |

### 9.16: PHRXGP2 [3865 H]

Static configuration data, providing control signals for chiplets ACI\_Rx1 and ACI\_Rx2. This register is set once by the GPP before the individual chiplets are enabled and must not be changed during normal operation.

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| PHR3(2:0)   | 2:0  | R/W    | 001     | Sink of data selected for Receive Port Handler macro #3: Same effect as for PHR1 in previous table. |
| Reserved    | 3    | R/W    | 0       | Reserved  |
| PHR4(2:0)   | 6:4  | R/W    | 001     | Sink of data selected for Receive Port Handler macro #4: Same effect as for PHR1 in previous table. |
| Reserved    | 7    | R/W    | 0       | Reserved  |

### 9.17: PPPGP1 [3866 H]

Static configuration data, providing control signals for chiplets PPP, ACI\_Rx1, ACI\_Rx2, ACI\_Tx1, ACI\_Tx2 and the Port Handlers. This register is set once by the GPP before the individual chiplets are enabled and is not changed during normal operation.

These signals determine whether a port handler is in ATM or in PPP mode.

| Signal Name | Bits | Access | Default | Description  |
|-------------|------|--------|---------|--|
| TxPPP(3:0)  | 3:0  | R/W    | 0000    | B=0: ATM mode B=1: PPP mode<br>Bxxx: Mode of transmit Port Handler #1<br>xBxx: Mode of transmit Port Handler #2<br>xxBx: Mode of transmit Port Handler #3<br>xxxB: Mode of transmit Port Handler #4<br>(for STM-4c, only 0000 or 1111 allowed) |
| RxPPP(3:0)  | 7:4  | R/W    | 0000    | B=0: ATM mode B=1: PPP mode<br>Bxxx: Mode of receive Port Handler #1<br>xBxx: Mode of receive Port Handler #2<br>xxBx: Mode of receive Port Handler #3<br>xxxB: Mode of receive Port Handler #4<br>(for STM-4c, only 0000 or 1111 allowed)     |

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**9.18: PPPGP2 [3867 H]**

Static configuration data, providing control signals for chiplets PPP, ACI\_Rx1, ACI\_Rx2, ACI\_Tx1, ACI\_Tx2 and the Port Handlers. This register is set once by the GPP before the individual chiplets are enabled and is not changed during normal operation.

| Signal Name | Bits | Access | Default | Description  |
|-------------|------|--------|---------|--|
| CHNKSZ(2:0) | 2:0  | R/W    | 110     | Chunk Size: 8-64 bytes in increments of 8. Only 16, 32, 48, and 64-byte chunk sizes are currently supported.<br>000 = 64-byte chunk size<br>010 = 16-byte chunk size<br>100 = 32-byte chunk size<br>110 = 48-byte chunk size |
| Reserved    | 7:3  | R/W    | 00000   | Reserved   |

**9.19: OFPTXGP [3868 H]**

Static configuration data, providing control signals for chiplets OFP\_Tx1/2/3/4. This is set once by the GPP before the individual chiplets are enabled and not changed during normal operation.

| Signal Name  | Bits | Access | Default | Description  |
|--------------|------|--------|---------|--|
| SDHC1Tx(3:0) | 3:0  | R/W    | 0000    | B = 0: C1 byte replaced by section trace J0 byte (ITU-T standard).<br>B = 1: Old numbering scheme is used. That is, the on-chip values in offsets 106 H - 108 H of the OFP_Tx1/2/3/4 GRAs are transmitted.<br>Bxxx: OFP_Tx1 numbering scheme info<br>xBxx: OFP_Tx2 numbering scheme info<br>xxBx: OFP_Tx3 numbering scheme info<br>xxxB: OFP_Tx4 numbering scheme info |
| PtrProc(3:0) | 7:4  | R/W    | 0000    | B = 0: AU pointer processing disabled in ATM/PPP mode. In this case, a pointer with a constant offset of '0' is transmitted.<br>B = 1: AU pointer processing enabled in ATM/PPP mode.<br>Bxxx: OFP_Tx1 pointer processing<br>xBxx: OFP_Tx2 pointer processing<br>xxBx: OFP_Tx3 pointer processing<br>xxxB: OFP_Tx4 pointer processing                                  |

### 9.20: OFPRXGP1 [3869 H]

Static configuration data, providing control signals for chiplets OFP\_Rx1/2/3/4. This register is set once by the GPP before the individual chiplets are enabled and is not changed during normal operation.

| Signal Name  | Bits | Access | Default | Description   |
|--------------|------|--------|---------|---|
| SDHC1Rx(3:0) | 3:0  | R/W    | 0000    | B = 0: The new (ITU-T standard) numbering scheme is used.<br>B = 1: Old numbering scheme is used.<br>Bxxx: OFP_Rx1 numbering scheme info<br>xBxx: OFP_Rx2 numbering scheme info<br>xxBx: OFP_Rx3 numbering scheme info<br>xxxB: OFP_Rx4 numbering scheme info |
| Reserved     | 7:4  | R/W    | 0000    | Reserved  |

### 9.21: OFPRXGP2 [386A H]

Static configuration data, providing control signals for chiplets OFP\_Rx1/2/3/4. This register is set once by the GPP before the individual chiplets are enabled and is not changed during normal operation.

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| A2Frm(1:0)  | 1:0  | R/W    | 00      | OFP_Rx1 FP1 assertion control:<br>00: FP1 asserted during 3rd A2 byte<br>01: FP1 asserted during 1st A2 byte<br>10: FP1 asserted during 2nd A2 byte<br>11: FP1 asserted during 1st Payload Byte |
| A2Frm(3:2)  | 3:2  | R/W    | 00      | Do not use.   |
| A2Frm(5:4)  | 5:4  | R/W    | 00      | Do not use.   |
| A2Frm(7:6)  | 7:6  | R/W    | 00      | Do not use.   |

### 9.22: AIPConf [386B H]

Ring Port static configuration data. This register is set once by the GPP and is not changed during normal operation.

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| RING        | 0    | R/W    | 0       | 0: Disabled - Ring Port input is ignored<br>1: Enabled - Ring Port accepts all inputs |
| Reserved    | 7:1  | R/W    | 0000000 | Reserved  |



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**9.23: PIMTConf1 [3870 H]**

Static configuration data, providing control signals for chiplet PIM\_Tx. This register is set once by the GPP before the individual chiplets are enabled and is not changed during normal operation.

| Signal Name   | Bits | Access | Default | Description  |
|---------------|------|--------|---------|--|
| TxLModeP(1:0) | 1:0  | R/W    | 01      | Mode of operation of PIM (PIS transmit direction):<br>00: Mode 1 - Do not use.<br>01: Mode 2 - 4 x 155.52 Mb/s.<br>10: Mode 3 - Do not use.<br>11: Mode 4 - 1 x 622.08 Mb/s.                       |
| TCSen         | 2    | R/W    | 1       | Transmit Clock Synthesis (TCS):<br>0: TCS disabled, internal Ref_Clk bypasses synthesis.<br>1: TCS enabled, internal Ref_Clk used to synthesize internal TX_Byte_Clock and Ser_Byte_Clock signals. |
| TxRefSelP     | 3    | R/W    | 0       | Reference clock input selection:<br>0: TX_BYCLKINT is selected.<br>1: TX_BYCLKINE is selected.   |
| Reserved      | 7:4  | R/W    | 0000    | Reserved   |

**9.24: PIMRConf1 [3872 H]**

Static configuration data, providing control signals for chiplet PIM\_Tx. This register is set once by the GPP before the individual chiplets are enabled and is not changed during normal operation.

| Signal Name   | Bits | Access | Default | Description  |
|---------------|------|--------|---------|--|
| RxLModeP(1:0) | 1:0  | R/W    | 01      | Mode of operation of PIM (PIR receive direction):<br>00: Mode1 - Do not use.<br>01: Mode 2 - 4 x 155.52 Mb/s.<br>10: Mode 3 - Do not use.<br>11: Mode 4 - 1 x 622.08 Mb/s. |
| Reserved      | 7:2  | R/W    | 000000  | Reserved   |

### 9.25: PIMRConf2 [3873 H]

Static configuration data, providing control signals for chiplets PIM\_Tx/PIM\_Rx. This register is set once by the GPP before the individual chiplets are enabled and is not changed during normal operation.

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| Algo1(1:0)  | 1:0  | R/W    | 00      | Selects frame pattern recognition algorithm for macro #1:<br>00: All A1 and A2 bits checked, maximum four consecutive bad frames received will cause the corresponding OOF interrupt request bit to become set.<br>01: A13 and the first four bits of A21 checked (12 bits total), maximum four bad frames received will cause the corresponding OOF interrupt request bit to become set.<br>10: All A1 and A2 bits checked, maximum five consecutive bad frames received will cause the corresponding OOF interrupt request bit to become set.<br>11: A13 and the first four bits of A21 checked (12 bits total), maximum five bad frames received will cause the corresponding OOF interrupt request bit to become set. |
| Algo2(1:0)  | 3:2  | R/W    | 00      | Selects frame pattern recognition algorithm for macro #2:<br>00: All bits checked, max. 4 bad frames<br>01: 12 bits checked only, max. 4 bad frames<br>10: All bits checked, max. 5 bad frames<br>11: 12 bits checked only, max. 5 bad frames   |
| Algo3(1:0)  | 5:4  | R/W    | 00      | Selects frame pattern recognition algorithm for macro #3:<br>00: All bits checked, max. 4 bad frames<br>01: 12 bits checked only, max. 4 bad frames<br>10: All bits checked, max. 5 bad frames<br>11: 12 bits checked only, max. 5 bad frames   |
| Algo4(1:0)  | 7:6  | R/W    | 00      | Selects frame pattern recognition algorithm for macro #4:<br>00: All bits checked, max. 4 bad frames<br>01: 12 bits checked only, max. 4 bad frames<br>10: All bits checked, max. 5 bad frames<br>11: 12 bits checked only, max. 5 bad frames   |

### 9.26: PIMSelec [3874 H]

Static configuration data, providing control signals for chiplets PIM\_Tx/PIM\_Rx. This register is set once by the GPP before the individual chiplets are enabled and is not changed during normal operation.

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| TxSePar1    | 0    | R/W    | 0       | Transmit direction:<br>0: SIS1 serial operation<br>1: SIS1 parallel operation |
| Reserved    | 3:1  |        | 000     | Reserved  |
| RxSePar1    | 4    | R/W    | 0       | Receive direction:<br>0: SIS1 serial operation<br>1: SIS1 parallel operation  |
| Reserved    | 7:5  |        | 000     | Reserved  |

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**9.27: SIMTConf1 [3878 H]**

Static configuration data, providing control signals for chiplet SIM\_Tx. This register is set once by the GPP before the individual chiplets are enabled and is not changed during normal operation.

| Signal Name    | Bits | Access | Default | Description  |
|----------------|------|--------|---------|--|
| Tx_LModeS(1:0) | 1:0  | R/W    | 10      | Select input frequency for Tx_RefCLK:<br>00: Mode 1 - Do Not Use<br>10: Mode 2 - 4 x 155.52 Mb/s<br>01: Mode 3 - Do Not Use<br>11: Mode 4 - 1 x 622.08 Mb/s.                         |
| Tx_RefFrq(2:0) | 4:2  | R/W    | 110     | Select input frequency for REFCLKT/REFCLKE:<br>000: 19.44 MHz<br>100: 51.84 MHz<br>010: 38.88 MHz<br>110: 77.76 MHz<br>001: 155.52 MHz (valid only for REFCLKE)<br>others: 77.76 MHz |
| Tx_DivFrq(2:0) | 7:5  | R/W    | 110     | Select frequency for TXDCLK:<br>000: 19.44 MHz<br>100: 51.84 MHz<br>010: 38.88 MHz<br>110: 77.76 MHz<br>001: Do Not Use<br>others: 77.76 MHz   |

**9.28: SIMTConf2 [3879 H]**

Static configuration data, providing control signals for chiplet SIM\_Tx. This register is set once by the GPP before the individual chiplets are enabled and is not changed during normal operation.

| Signal Name    | Bits | Access | Default | Description  |
|----------------|------|--------|---------|--|
| Tx_RefSelS     | 0    | R/W    | 0       | Select input signal standard for Tx_RefCLK:<br>0: TTL input.<br>1: LPECL input.  |
| Tx_DivEnT      | 1    | R/W    | 0       | 0: Disable TTL output of TXDCLKT.<br>1: Enable TTL output of TXDCLKT.  |
| Reserved       | 2    | R/W    | 0       | Reserved   |
| Tx_force_lt    | 3    | R/W    | 0       | 0: Do nothing.<br>1: Force leakage test on PLL transmit. The transmit PLL is disabled.   |
| Start_AutoTrim | 4    | W      | 0       | Command bit: writing a '1' into this bit location forces a high start pulse of >50 ns length (3 GPPCLK cycles) to SIM auto-trim circuit. |
| En_AutoTrim    | 5    | R/W    | 1       | 0: Disables PLL transmit auto-trim function.<br>1: Enables PLL transmit auto-trim function.  |
| Reserved       | 7:6  | R/W    | 00      | Reserved   |

### 9.29: SIMRConf1 [387A H]

Static configuration data, providing control signals for chiplet SIM\_Rx. This register is set once by the GPP before the individual chiplets are enabled and is not changed during normal operation.

| Signal Name     | Bits | Access | Default | Description  |
|-----------------|------|--------|---------|--|
| Rx_LModeS(1:0)  | 1:0  | R/W    | 10      | Select input frequency for internal Rx_RefCLK:<br>00: Mode 1 - Do Not Use<br>10: Mode 2 - 4 x 155.52 Mb/s<br>01: Mode 3 - Do Not Use<br>11: Mode 4 - 1 x 622.08 Mb/s |
| Rx_DivFrq1(2:0) | 4:2  | R/W    | 110     | Select frequency for RXDCLKT1:<br>000: 19.44 MHz<br>100: 51.84 MHz<br>010: 38.88 MHz<br>110: 77.76 MHz<br>001: Do Not Use<br>others: 77.76 MHz                       |
| Rx_DivFrq2(2:0) | 7:5  | R/W    | 110     | Select frequency for RXDCLKT2:<br>000: 19.44 MHz<br>100: 51.84 MHz<br>010: 38.88 MHz<br>110: 77.76 MHz<br>001: Do Not Use<br>others: 77.76 MHz                       |

### 9.30: SIMRConf2 [387B H]

Static configuration data, providing control signals for chiplet SIM\_Rx. This register is set once by the GPP before the individual chiplets are enabled and is not changed during normal operation.

| Signal Name     | Bits | Access | Default | Description  |
|-----------------|------|--------|---------|--|
| Reserved        | 1:0  | R/W    | 00      | Reserved   |
| Rx_DivFrq3(2:0) | 4:2  | R/W    | 110     | Select frequency for RXDCLKT3:<br>000: 19.44 MHz<br>100: 51.84 MHz<br>010: 38.88 MHz<br>110: 77.76 MHz<br>001: Do Not Use<br>others: 77.76 MHz |
| Rx_DivFrq4(2:0) | 7:5  | R/W    | 110     | Select frequency for RXDCLKT4:<br>000: 19.44 MHz<br>100: 51.84 MHz<br>010: 38.88 MHz<br>110: 77.76 MHz<br>001: Do Not Use<br>others: 77.76 MHz |

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**9.31: SIMRConf3 [387C H]**

Static configuration data, providing control signals for chiplet SIM\_Rx. This register is set once by the GPP before the individual chiplets are enabled and is not changed during normal operation.

| Signal Name  | Bits | Access | Default | Description  |
|--------------|------|--------|---------|--|
| AutoLTR      | 0    | R/W    | 1       | 0: Enable manual control of cross-over.<br>1: Enable automatic control of crossover.   |
| LockToRef    | 1    | R/W    | 0       | 0: Receive PLL in data recovery mode.<br>1: Receive PLL in frequency acquisition.  |
| Invert_LOS   | 2    | R/W    | 0       | 0: LOSSSIG# inputs are active high.<br>1: LOSSSIG# inputs are active low.  |
| EnableArLTR  | 3    | R/W    | 0       | In case of an active LOSSSIG# input, the lock-to-reference circuit:<br>0: Needs reset by microprocessor.<br>1: Automatically reset.                                      |
| Rx1_force_lt | 4    | R/W    | 0       | 0: Do nothing.<br>1: Force leakage test on PLL receive #1. PLL receive #1 is disabled.   |
| Rx2_force_lt | 5    | R/W    | 0       | 0: Do nothing.<br>1: Force leakage test on PLL receive #2. PLL receive #2 is disabled.<br>PLL Rx #2 <b>must</b> be disabled for STM-4, STM-4c, STS-12, or STS-12c modes. |
| Rx3_force_lt | 6    | R/W    | 0       | 0: Do nothing.<br>1: Force leakage test on PLL receive #3. PLL receive #3 is disabled.<br>PLL Rx #3 <b>must</b> be disabled for STM-4, STM-4c, STS-12, or STS-12c modes. |
| Rx4_force_lt | 7    | R/W    | 0       | 0: Do nothing.<br>1: Force leakage test on PLL receive #4. PLL receive #4 is disabled.<br>PLL Rx #4 <b>must</b> be disabled for STM-4, STM-4c, STS-12, or STS-12c modes. |

**9.32: SIMRConf4 [387D H]**

Static configuration data, providing control signals for chiplet SIM\_Rx. This register is set once by the GPP before the individual chiplets are enabled and is not changed during normal operation.

| Signal Name  | Bits | Access | Default | Description   |
|--------------|------|--------|---------|---|
| Rx_DivEnT1   | 0    | R/W    | 0       | 0: Disable TTL output of RXDCLKT1<br>1: Enable TTL output of RXDCLKT1 |
| Rx_DivEnT2   | 1    | R/W    | 0       | 0: Disable TTL output of RXDCLKT2<br>1: Enable TTL output of RXDCLKT2 |
| Rx_DivEnT3   | 2    | R/W    | 0       | 0: Disable TTL output of RXDCLKT3<br>1: Enable TTL output of RXDCLKT3 |
| Rx_DivEnT4   | 3    | R/W    | 0       | 0: Disable TTL output of RXDCLKT4<br>1: Enable TTL output of RXDCLKT4 |
| Rx1_resetLTR | 4    | R/W    | 0       | Reset lock control output #1  |
| Rx2_resetLTR | 5    | R/W    | 0       | Reset lock control output #2  |
| Rx3_resetLTR | 6    | R/W    | 0       | Reset lock control output #3  |
| Rx4_resetLTR | 7    | R/W    | 0       | Reset lock control output #4  |

**9.33: SIMWrap [387E H]**

Static configuration data, providing control signals for chiplets SIM\_Tx and SIM\_Rx. This register is set once by the GPP before the individual chiplets are enabled and is not changed during normal operation.

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| En_Wrap1    | 0    | R/W    | 0       | 0: Disable local wrap mode of SIM1<br>1: Enable local wrap mode of SIM1 |
| En_Wrap2    | 1    | R/W    | 0       | 0: Disable local wrap mode of SIM2<br>1: Enable local wrap mode of SIM2 |
| En_Wrap3    | 2    | R/W    | 0       | 0: Disable local wrap mode of SIM3<br>1: Enable local wrap mode of SIM3 |
| En_Wrap4    | 3    | R/W    | 0       | 0: Disable local wrap mode of SIM4<br>1: Enable local wrap mode of SIM4 |
| En_DWrap1   | 4    | R/W    | 0       | 0: Disable a digital wrap on SIM1<br>1: Enable a digital wrap on SIM1   |
| En_DWrap2   | 5    | R/W    | 0       | 0: Disable a digital wrap on SIM2<br>1: Enable a digital wrap on SIM2   |
| En_DWrap3   | 6    | R/W    | 0       | 0: Disable a digital wrap on SIM3<br>1: Enable a digital wrap on SIM3   |
| En_DWrap4   | 7    | R/W    | 0       | 0: Disable a digital wrap on SIM4<br>1: Enable a digital wrap on SIM4   |



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**9.34: SIMStat [387F H]**

Status register, providing the GPP with information from the SIM chiplet via PIM. Either SIM-internal or external PLL lock status. The “clear-register” option is set in ConfGP1(1).

| Signal Name   | Bits | Access | Default | Description  |
|---------------|------|--------|---------|--|
| Rx_Lock1      |      | R      | N.A.    | 0: Receive PLL #1 is still in phase acquisition process<br>1: Receive PLL #1 is enabled and has locked to the incoming data stream |
| Rx_Lock2      | 1    | R      | N.A.    | 0: Receive PLL #2 is still in phase acquisition process<br>1: Receive PLL #2 is enabled and has locked to the incoming data stream |
| Rx_Lock3      | 2    | R      | N.A.    | 0: Receive PLL #3 is still in phase acquisition process<br>1: Receive PLL #3 is enabled and has locked to the incoming data stream |
| Rx_Lock4      | 3    | R      | N.A.    | 0: Receive PLL #4 is still in phase acquisition process<br>1: Receive PLL #4 is enabled and has locked to the incoming data stream |
| Done_AutoTrim | 4    | R      | N.A.    | 0: Auto-trim function still running<br>1: Auto-trim function has finished  |
| Reserved      | 6:5  | R/W    | 00      | Reserved   |
| TCM_Lock      | 7    | R      | N.A.    | 0: TCS is still in phase acquisition process<br>1: TCS is enabled and has locked to the reference clock                            |

**9.35: SIMATConf1 [3880 H]**

Static configuration data, providing stored parameters for the analog parts of chiplet SIM\_Tx. This is set once by the GPP before the individual chiplets are enabled and is not changed during normal operation. The defaults are for a device configuration of 4 x STM-1 and a reference clock frequency of 77.76 MHz. The stored values can be overwritten byte-wise with the default parameter values calculated from system configuration bits by writing a '1' into the corresponding bit location of the write-only SIMParConf command register.

| Signal Name    | Bits | Access | Default | Description   |
|----------------|------|--------|---------|---|
| TX_ATEN        | 0    | R/W    | 0       | Analog Test Enable  |
| TX_CMFBSSEL    | 1    | R/W    | 1       | Common Mode Feedback Select   |
| TX_CPFDIS      | 2    | R/W    | 0       | Disable Charge Pump Filter  |
| TX_CPFRESET    | 3    | R/W    | 1       | Charge Pump Filter Reset on startup                                     |
| TX_IntRefSel   | 4    | R/W    | 1       | Bandgap current reference control:<br>0: Switched off<br>1: Switched on |
| TX_lcpSel(2:0) | 7:5  | R/W    | 101     | Select Charge Pump Capacitance  |

### 9.36: SIMATConf2 [3881 H]

Static configuration data, providing stored parameters for the analog parts of chiplet SIM\_Tx. This is set once by the GPP before the individual chiplets are enabled and is not changed during normal operation. The defaults are for a device configuration of 4 x STM-1 and a reference clock frequency of 77.76 MHz. The stored values can be overwritten byte-wise with the default parameter values calculated from system configuration bits by writing a '1' into the corresponding bit location of the write-only SIMParConf command register.

| Signal Name   | Bits | Access | Default | Description                          |
|---------------|------|--------|---------|--------------------------------------|
| TX_Icpgm(4:0) | 4:0  | R/W    | 00110   | Program proportional gain            |
| TX_ExtSel     | 5    | R/W    | 0       | Select external programming currents |
| TX_PCFFD1     | 6    | R/W    | 0       | Feed-forward capacitor 1 selected    |
| TX_PCFFD9     | 7    | R/W    | 0       | Feed-forward capacitor 9 selected    |

### 9.37: SIMATConf3 [3882 H]

Static configuration data, providing stored parameters for the analog parts of chiplet SIM\_Tx. This is set once by the GPP before the individual chiplets are enabled and is not changed during normal operation. The defaults are for a device configuration of 4 x STM-1 and a reference clock frequency of 77.76 MHz. The stored values can be overwritten byte-wise with the default parameter values calculated from system configuration bits by writing a '1' into the corresponding bit location of the write-only SIMParConf command register.

| Signal Name     | Bits | Access | Default | Description             |
|-----------------|------|--------|---------|-------------------------|
| TX_IcpiPgm(3:0) | 3:0  | R/W    | 1101    | Program integral gain   |
| DivClkSel(2:0)  | 6:4  | R/W    | 100     | Divided clock selection |
| Reserved        | 7    | R/W    | 0       | Reserved                |

### 9.38: SIMATConf4 [3883 H]

Static configuration data, providing stored parameters for the analog parts of chiplet SIM\_Tx. This is set once by the GPP before the individual chiplets are enabled and is not changed during normal operation. The defaults are for a device configuration of 4 x STM-1 and a reference clock frequency of 77.76 MHz. The stored values can be overwritten byte-wise with the default parameter values calculated from system configuration bits by writing a '1' into the corresponding bit location of the write-only SIMParConf command register.

| Signal Name     | Bits | Access | Default | Description  |
|-----------------|------|--------|---------|--|
| Tx_VCOtrim(1:0) | 1:0  | R/W    | 01      | Fine tune for TCS VCO center frequency (default for 4 x STM-1) |
| Reserved        | 7:2  | R/W    | 000000  | Reserved   |

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**9.39: SIMARConf1 [3884 H]**

Static configuration data, providing stored parameters for the analog parts of chiplet SIM\_Rx. This is set once by the GPP before the individual chiplets are enabled and is not changed during normal operation. The defaults are for a device configuration of 4 x STM-1 and a reference clock frequency of 77.76 MHz. The stored values can be overwritten byte-wise with the default parameter values calculated from system configuration bits by writing a '1' into the corresponding bit location of the write-only SIMParConf command register.

| Signal Name    | Bits | Access | Default | Description   |
|----------------|------|--------|---------|---|
| RX_ATEN        | 0    | R/W    | 0       | Analog Test Enable  |
| RX_CMFBSSEL    | 1    | R/W    | 1       | Common Mode Feedback Select   |
| RX_CPFDIS      | 2    | R/W    | 0       | Disable Charge Pump Filter  |
| RX_CPFRESET    | 3    | R/W    | 1       | Charge Pump Filter Reset on start-up                                    |
| RX_IntRefSel   | 4    | R/W    | 1       | Bandgap current reference control:<br>0: Switched off<br>1: Switched on |
| RX_lcpSel(2:0) | 7:5  | R/W    | 101     | Select Charge Pump Capacitance  |

**9.40: SIMARConf2 [3885 H]**

Static configuration data, providing stored parameters for the analog parts of chiplet SIM\_Rx. This is set once by the GPP before the individual chiplets are enabled and is not changed during normal operation. The defaults are for a device configuration of 4 x STM-1 and a reference clock frequency of 77.76 MHz. The stored values can be overwritten byte-wise with the default parameter values calculated from system configuration bits by writing a '1' into the corresponding bit location of the write-only SIMParConf command register.

| Signal Name      | Bits | Access | Default | Description                         |
|------------------|------|--------|---------|-------------------------------------|
| RX_lcppPgmA(4:0) | 4:0  | R/W    | 00110   | Program proportional gain           |
| RX_lextSel       | 5    | R/W    | 0       | Select external programming current |
| RX_PCFFD1        | 6    | R/W    | 0       | Feed-forward capacitor 1 selected   |
| RX_PCFFD9        | 7    | R/W    | 0       | Feed-forward capacitor 9 selected   |

### 9.41: SIMARConf3 [3886 H]

Static configuration data, providing stored parameters for the analog parts of chiplet SIM\_Rx. This is set once by the GPP before the individual chiplets are enabled and is not changed during normal operation. The defaults are for a device configuration of 4 x STM-1 and a reference clock frequency of 77.76 MHz. The stored values can be overwritten byte-wise with the default parameter values calculated from system configuration bits by writing a '1' into the corresponding bit location of the write-only SIMParConf command register.

| Signal Name      | Bits | Access | Default | Description           |
|------------------|------|--------|---------|-----------------------|
| RX_IcpiPgmA(3:0) | 3:0  | R/W    | 1101    | Program integral gain |
| RX_IcpiPgmR(3:0) | 7:4  | R/W    | 0001    | Program integral gain |

### 9.42: SIMARConf4 [3887 H]

Static configuration data, providing stored parameters for the analog parts of chiplet SIM\_Rx. This is set once by the GPP before the individual chiplets are enabled and is not changed during normal operation. The defaults are for a device configuration of 4 x STM-1 and a reference clock frequency of 77.76 MHz. The stored values can be overwritten byte-wise with the default parameter values calculated from system configuration bits by writing a '1' into the corresponding bit location of the write-only SIMParConf command register.

| Signal Name      | Bits | Access | Default | Description                                    |
|------------------|------|--------|---------|--|
| RX_IcppPgmR(4:0) | 4:0  | R/W    | 00110   | Program proportional gain                      |
| Rx_VCOtrim(1:0)  | 6:5  | R/W    | 01      | Fine tune for receive PLL VCO center frequency |
| Reserved         | 7    | R/W    | 0       | Reserved                                       |

### 9.43: SIMParConf [3888 H]

Command register. Writing a '1' into a bit location will overwrite the associated SIM parameter configuration register with the default values. The defaults are generated internally according to the settings of the Rx\_LModeS (SIMRConf1(1:0)) and Tx\_RefFrq (SIMTConf1(4:2)).

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| ParSel7     | 0    | W      | N.A.    | Load default SIM parameters into SIMATConf1 register. |
| ParSel6     | 1    | W      | N.A.    | Load default SIM parameters into SIMATConf2 register. |
| ParSel5     | 2    | W      | N.A.    | Load default SIM parameters into SIMATConf3 register. |
| ParSel4     | 3    | W      | N.A.    | Load default SIM parameters into SIMATConf4 register. |
| ParSel3     | 4    | W      | N.A.    | Load default SIM parameters into SIMARConf1 register. |
| ParSel2     | 5    | W      | N.A.    | Load default SIM parameters into SIMARConf2 register. |
| ParSel1     | 6    | W      | N.A.    | Load default SIM parameters into SIMARConf3 register. |
| ParSel0     | 7    | W      | N.A.    | Load default SIM parameters into SIMARConf4 register. |

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**GP Access Protection Address Map** Base Address: 3FBF

| Register Name | Address Offset (Hex) | Access | Initial Value (Binary) | Description (All Registers Are Of 8-bit Width) |
|---------------|----------------------|--------|------------------------|--|
| ProtReg       | 0                    | R/W    | 11001100               | Write protection control                       |

ProtReg: The bits of this configuration register control the Write Access Protection as follows:

ProtReg is 11001100: free read and write access to all SONET/SDH framer registers (DEFAULT).

ProtReg is not 11001100: free read access to all SONET/SDH framer registers; write access to register ProtReg only. If a write to a protected register is attempted, an access violation error is generated (AccViol = HShake5(2)).

## GPP Handler Architecture

### General Register Structure for GPP Handlers

| Address Range (Hex) | Register Function  |
|---------------------|--|
| 0 - 1               | Read-on-the-fly registers  |
| 2 - 3               | Counter enable registers   |
| 4 - 2F              | Counters and counter threshold registers   |
| 30                  | Reset register   |
| 31 - 32             | Command registers  |
| 33 - 37             | Status and event latch registers   |
| 38 - 47             | Interrupt registers (even address = interrupt register, following odd address = interrupt mask register) |
| 48 - 57             | Configuration registers  |

### Counters

Every counter has an enable bit in the counter enable register (address 2 or 3), and optionally up to two programmable thresholds. Each counter has an interrupt bit for overflow and up to two interrupt bits for threshold crossing in the counter interrupt registers. For all counters in one handler there is one common read-on-the-fly register, that is used to store the higher-order bytes to obtain a correct readback value for counters larger than 8-bits. Counters are read-only registers; the count enable registers are read/write.

**Note:** Independent of the counter length, given that a counter has address  $n$  as base, reading address  $n$  or address  $n+1$  both yield the LSB of the counter. Reading address  $n$  has no influence on the counter, but reading address  $n+1$  will reset the counter after the read. Reading address  $n$  or  $n+1$  will always latch the higher-order bytes into the read-on-the-fly register (before the optional automatic reset). Counters can only be read and not written to. For a 16-bit counter, the MSB should be read from ROFmid (address 0). For a 24-bit counter, the MSB is read from ROFhi (address 1), the next byte from ROFmid (address 0). To completely read a 24-bit counter, first read the LSB from counter address  $n$  or  $n+1$ , followed by reading ROFmid and ROFhi (address 0 and address 1, respectively).

### Reset Register

Each handler has a one-bit reset register. Bit 0 is the chiplet reset control. This bit is active high after power-on-reset, causing the chiplet to be disabled. This is a read/write register.

### Command Registers

The optional command register(s) will generate events to the chiplet. When a bit is written high by the microprocessor, it will remain high for one chiplet clock cycle. Therefore, reading back a command register will always read back zeros. This is a read/write register.

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### Status and Event Latch Registers

The value of the optional status registers always follows the driving signal immediately. In contrast, the optional event latch register(s) remember(s) one or more occurrences of events that happen in a chiplet. This may be considered as a 1-bit saturating counter. Each bit in the register corresponds to an event in the chiplet. Such bits remain high after the event has happened until the microprocessor implicitly or explicitly resets the bit. This is configurable. Implicit reset is done by writing a '1' to the bit that is to be reset. Explicit reset will reset all bits of one register when the register is read. Status bits are read-only latches, whereas event latch bits are read/write. Both kind of bits can be present in the same 8-bit register.

### Interrupt Registers

When there are counters, user interrupts or fatal bits in a chiplet, a MAIN INTERRUPT register will be present. Bit 0 always is the fatal interrupt bit, which is set as soon as a FSM enters an undefined state. The other bits refer to counters or user interrupt registers, to allow easy determination of the interrupt cause. Each Interrupt register has an interrupt MASK register to enable or disable interrupt. After power-on-reset, interrupts are disabled. The interrupt registers are the same as the event latch registers, with the addition that when an interrupt register bit is set, and the corresponding mask register bit is set, the interrupt signal to the GPPINT chiplet is activated. The same mechanism to reset the interrupt register bits is used as for the event latch registers. The interrupt MASK registers are only changed by the microprocessor. The interrupt and interrupt mask registers are read/write.

### Configuration Registers

These registers are programmed by the microprocessor with set-up information, and are read/write. The first configuration register reserves bits 1 and 0 to configure explicit or implicit reset of the event latch registers and interrupt registers, respectively (when such registers are present).

### Register Types

|          |                             |
|----------|-----------------------------|
| <b>F</b> | Read-On-The-Fly Register    |
| <b>N</b> | Counter Register            |
| <b>R</b> | Reset Register              |
| <b>I</b> | Interrupt Register          |
| <b>C</b> | Configuration Register      |
| <b>X</b> | Control or Mask Register    |
| <b>S</b> | Status/event Latch Register |
| <b>O</b> | Command Register            |

**ACI\_Tx1 Chiplet Address Map** Base Address: 0100 H

| Register Name   | Address Offset (Hex) | Type/Width | Initial Value (Binary) | Description                                      | See Page |
|-----------------|----------------------|------------|------------------------|--|----------|
| IT1ROFmid       | 0                    | F 8        | 00000000               | Read-on-the-fly register (MidSB)                 | 155      |
| IT1ROFhi        | 1                    | F 8        | 00000000               | Read-on-the-fly register (MSB)                   | 155      |
| IT1CntEn1       | 2                    | X 4        | 0000                   | COUNT ENABLE register                            | 157      |
| IT1Cnt1:PACNT   | 4/5                  | N 8        | 00000000               | Parity error counter, with threshold             | 156      |
| IT1Th1:PACNTTh  | 6                    | X 8        | 01111111               | Threshold register for counter PACNT             | 156      |
| IT1Cnt2:PECNT   | 8/9                  | N 8        | 00000000               | Protocol error counter, with threshold           | 156      |
| IT1Th2:PECNTTh  | A                    | X 8        | 01111111               | Threshold register for counter PECNT             | 156      |
| IT1Cnt3:ATMCELL | C/D                  | N 24       | 000000 H               | LS byte of 24-bit ATM cell counter, no threshold | 156      |
| IT1Cnt4:CORCELL | E/F                  | N 8        | 00000000               | Corrupted cell counter, no threshold             | 157      |
| IT1RESET        | 30                   | R 1        | 1                      | Default RESET register                           | 157      |
| IT1MainIRQ      | 38                   | I 2        |                        | MAIN INTerrupt register                          | 158      |
| IT1M_MainIRQ    | 39                   | X 2        | 00                     | INT MASK register (for IT1MainIRQ)               | 158      |
| IT1CntIRQ1      | 3A                   | I 6        |                        | COUNTER INTerrupt register                       | 158      |
| IT1M_CntIRQ1    | 3B                   | X 6        | 000000                 | INT MASK register (for IT1CntIRQ1)               | 158      |
| IT1Conf1        | 48                   | C 3        | 001                    | 0=R and R INT 1:2=TMOPAIT1                       | 159      |
| IT1Conf2:ADDR1  | 49                   | C 5        | 00000                  | PHY port address SONET/SDH macro 1               | 159      |
| IT1Conf3:ADDR2  | 4A                   | C 5        | 00001                  | PHY port address SONET/SDH macro 2               |          |
| IT1Conf4:ADDR3  | 4B                   | C 5        | 00010                  | PHY port address SONET/SDH macro 3               |          |
| IT1Conf5:ADDR4  | 4C                   | C 5        | 00011                  | PHY port address SONET/SDH macro 4               |          |

**ACI\_Tx1 (IT1) Counters**
**10.1: IT1ROFmid [0100 H]**

Read-on-the-fly register.

| Signal Name    | Bits | Access | Default  | Description                      |
|----------------|------|--------|----------|----------------------------------|
| IT1ROFmid(7:0) | 7:0  | R      | 00000000 | Read-on-the-fly register (MidSB) |

**10.2: IT1ROFhi [0101 H]**

Read-on-the-fly register.

| Signal Name   | Bits | Access | Default  | Description                    |
|---------------|------|--------|----------|--------------------------------|
| IT1ROFhi(7:0) | 7:0  | R      | 00000000 | Read-on-the-fly register (MSB) |

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**10.3: IT1Cnt1:PACNT [0104 H / 0105 H]**

Number of parity errors detected on this UTOPIA interface. Counter overflow leads to an interrupt request.

| Signal Name | Bits | Access | Default  | Description          |
|-------------|------|--------|----------|----------------------|
| PACNT(7:0)  | 7:0  | R      | 00000000 | Parity error counter |

**10.4: IT1Th1:PACNTTh [0106 H]**

Threshold register for number of parity errors detected on this UTOPIA interface; threshold overstep leads to an interrupt request.

| Signal Name  | Bits | Access | Default  | Description        |
|--------------|------|--------|----------|--------------------|
| PACNTTh(7:0) | 7:0  | R/W    | 01111111 | Threshold register |

**10.5: IT1Cnt2:PECNT [0108 H / 0109 H]**

Number of UTOPIA protocol errors detected on this UTOPIA interface. The counter value is half the number of clock cycles that cells have been transmitted on a PHY where it was not allowed to, due to TXCLAV=0 (polling of the ATM device that led to PHY selection). Counter overflow leads to an interrupt request.

| Signal Name | Bit | Access | Default  | Description            |
|-------------|-----|--------|----------|------------------------|
| PECNT(7:0)  | 7:0 | R      | 00000000 | Protocol error counter |

**10.6: IT1Th2:PECNTTh [010A H]**

Threshold register for number of protocol errors detected on this UTOPIA interface; threshold overstep leads to an interrupt request.

| Signal Name  | Bit | Access | Default  | Description        |
|--------------|-----|--------|----------|--------------------|
| PECNTTh(7:0) | 7:0 | R/W    | 01111111 | Threshold register |

**10.7: IT1Cnt3:ATMCELL [010C H / 010D H]**

Number of cells received by this UTOPIA interface from the ATM layer. No threshold register. Counter overflow leads to an interrupt request.

| Signal Name  | Bits | Access | Default  | Description            |
|--------------|------|--------|----------|------------------------|
| ATMCELL(7:0) | 7:0  | R      | 00000000 | ATM cell counter (LSB) |

### 10.8: IT1Cnt4:CORCELL [010E H / 010F H]

Number of corrupted cell errors. The Corrupted Cell counter is counting missing SOC (StartOfCell, StartOfChunk) events, which is slightly different from a pure corrupted cell counter. If there was an initial SOC, the ACI\_Tx is able to continue to read in data even if there are no SOCs with the following cells. A corrupted cell will only result if finally a SOC arrives that is not aligned with the H1 byte. So, even if there is no real cell corruption, this counter is counting missing SOCs to indicate to the user that something is wrong at the UTOPIA interface. Counter overflow leads to an interrupt request.

| Signal Name  | Bits | Access | Default  | Description                    |
|--------------|------|--------|----------|--------------------------------|
| CORCELL(7:0) | 7:0  | R      | 00000000 | ACI_Tx1 Corrupted cell counter |

### 10.9: IT1CntEn1 [0102 H]

Counter On/Off control register.

For each bit position: 0: Counter is disabled

1: Counter is enabled

| Signal Name | Bits | Access | Default | Description                          |
|-------------|------|--------|---------|--------------------------------------|
| EN-PACNT    | 0    | R/W    | 0       | UTOPIA parity error counter enable   |
| EN-PECNT    | 1    | R/W    | 0       | UTOPIA protocol error counter enable |
| EN-ATMCELL  | 2    | R/W    | 0       | ATM cell counter enable              |
| EN-CORCELL  | 3    | R/W    | 0       | Corrupted cell counter enable        |
| Reserved    | 7:4  |        |         | Not used                             |

## ACI\_Tx1 (IT1) Reset Register

### 11.1: IT1RESET [1030 H]

Reset chiplet control register. This register is automatically preset to the default value by the reset signal ResIT1 from the GPPINT.

For each bit position: 0: Reset not active

1: Reset active

| Signal Name | Bits | Access | Default | Description                     |
|-------------|------|--------|---------|---------------------------------|
| Reset       | 0    | R/W    | 1       | Reset (disable) ACI_Tx1 chiplet |
| Reserved    | 7:1  |        |         | Not used                        |

## ACI\_Tx1 Interrupt Request and Mask Registers

### 12.1: IT1MainIRQ [1038 H]

Register to indicate fatal interrupt events and to point to user IRQ registers with active requests.

For each bit position: 0: No interrupt request pending  
1: Interrupt request pending

### 12.2: IT1M\_MainIRQ [1039 H]

Register to mask pending interrupt requests. A masked request will not generate an outgoing IRQ to the GPPINT.

For each bit position: 0: The corresponding pending request bit is masked (DEFAULT)  
1: The corresponding pending request bit activates signal IRQIT1 to GPPINT

| Signal Name | Bits | Access | Default | Description                           |
|-------------|------|--------|---------|---------------------------------------|
| Fatal       | 0    | R/W    | 0       | Fatal event occurred                  |
| CntIRQ1     | 1    | R/W    | 0       | Active request in IT1CntIRQ1 register |
| Reserved    | 7:2  |        |         | Not used                              |

### 12.3: IT1CntIRQ1 [103A H]

Register to indicate active counter interrupt requests of this chiplet.

For each bit position: 0: No interrupt request pending  
1: Interrupt request pending

### 12.4: IT1M\_CntIRQ1 [103B H]

Register to mask pending counter interrupt requests.

For each bit position: 0: The corresponding pending request bit is masked (DEFAULT)  
1: The corresponding pending request bit activates the pointer bit in IT1MainIRQ register

| Signal Name | Bits | Access | Default | Description                               |
|-------------|------|--------|---------|---|
| OV-PACNT    | 0    | R/W    | 0       | Overflow parity error counter             |
| TH-PACNT    | 1    | R/W    | 0       | Threshold overstep parity error counter.  |
| OV-PECNT    | 2    | R/W    | 0       | Overflow protocol error counter           |
| TH-PECNT    | 3    | R/W    | 0       | Threshold overstep protocol error counter |
| OV-ATMCELL  | 4    | R/W    | 0       | Overflow ATM cell counter                 |
| OV-CORCELL  | 5    | R/W    | 0       | Overflow corrupted cell counter           |
| Reserved    | 7:6  |        |         | Not used                                  |

## ACI\_Tx1 Configuration Registers

### 13.1: IT1Conf1 [1048 H]

Register to control various modes of operation of this chiplet.

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| AutRst_Int  | 0    | R/W    | 1       | 0: No action on read access<br>1: Auto-reset interrupt request registers upon read access<br>Regardless of the setting of this bit, individual interrupt request bits can be cleared by writing a '1' to that bit provided that the corresponding alarm condition is removed. |
| TMOPAIT1(1) | 1    | R/W    | 0       | Mode for UTOPIA (ATM/PPP) parity error detection:<br>0: Parity check off<br>1: Parity check on  |
| TMOPAIT1(0) | 2    | R/W    | 0       | Mode of parity calculation:<br>0: Parity calculated over data only<br>1: Parity calculated over data and control  |
| Reserved    | 7:3  |        |         | Not used  |

### 13.2: IT1Conf2-5 [1049 H, 104A H, 104B H, 104C H]

ADDR1-ADDR4: Registers that control the PHY port addresses according to UTOPIA Level 2.

Used in 1 x UTOPIA Level 2 multi-PHY/multi-port configuration (non-STM-4c), multi-PHY/single-port configuration (STM-4c), MULTIPLEXED status indication; for bit positions (4:0) of each register:

00000 to 11110: valid address for PHY port selection

11111: PHY port is never selected

Used in 1 x UTOPIA Level 2 multi-PHY/multi-port configuration (non-STM-4c), multi-PHY/single-port configuration (STM-4c), DIRECT status indication; for bit positions (4:0) of each register:

00000 to 11111: valid address for PHY port selection

For UTOPIA Level 1: don't care

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| ADDR1(4:0)  | 4:0  | R/W    | 00000   | PHY port address of SONET/SDH macro #1 (also port address for STM-4c) |
| Reserved    | 7:5  |        |         | Not used  |
| ADDR2(4:0)  | 4:0  | R/W    | 00001   | PHY port address of SONET/SDH macro #2 (for STM-4c: don't care)       |
| Reserved    | 7:5  |        |         | Not used  |
| ADDR3(4:0)  | 4:0  | R/W    | 00010   | PHY port address of SONET/SDH macro #3 (for STM-4c: don't care)       |
| Reserved    | 7:5  |        |         | Not used  |
| ADDR4(4:0)  | 4:0  | R/W    | 00011   | PHY port address of SONET/SDH macro #4 (for STM-4c: don't care)       |
| Reserved    | 7:5  |        |         | Not used  |

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**ACI\_Tx2 Chiplet Address Map** Base Address 0200 H

| Register Name   | Address Offset (Hex) | Type/Width | Initial Value (Binary) | Description                                      | See Page |
|-----------------|----------------------|------------|------------------------|--|----------|
| IT2ROFmid       | 0                    | F 8        | 00000000               | Read-on-the-fly register (MidSB)                 | 160      |
| IT2ROFhi        | 1                    | F 8        | 00000000               | Read-on-the-fly register (MSB)                   | 160      |
| IT2CntEn1       | 2                    | X 4        | 0000                   | COUNT ENABLE register                            | 162      |
| IT2Cnt1:PACNT   | 4/5                  | N 8        | 00000000               | Parity error counter, with threshold             | 160      |
| IT2Th1:PACNTTh  | 6                    | X 8        | 01111111               | Threshold register for counter PACNT             | 161      |
| IT2Cnt2:PECNT   | 8/9                  | N 8        | 00000000               | Protocol error counter, with threshold           | 161      |
| IT2Th2:PECNTTh  | A                    | X 8        | 01111111               | Threshold register for counter PECNT             | 161      |
| IT2Cnt3:ATMCELL | C/D                  | N 24       | 000000 H               | LS byte of 24-bit ATM cell counter, no threshold | 161      |
| IT2Cnt4:CORCELL | E/F                  | N 8        | 00000000               | Corrupted cell counter, no threshold             | 161      |
| IT2RESET        | 30                   | R 1        | 1                      | Default RESET register                           | 162      |
| IT2MainIRQ      | 38                   | I 2        |                        | MAIN INTerrupt register                          | 163      |
| IT2M_MainIRQ    | 39                   | X 2        | 00                     | INT MASK register (for IT2MainIRQ)               | 163      |
| IT2CntIRQ1      | 3A                   | I 6        |                        | COUNTER INTerrupt register                       | 163      |
| IT2M_CntIRQ1    | 3B                   | X 6        | 00000                  | INT MASK register (for IT2CntIRQ1)               | 163      |
| IT2Conf1        | 48                   | C 3        | 001                    | 0=R and R INT 1:2=TMOPAIT2                       | 164      |

**ACI\_Tx2 (IT2) Counters**
**14.1: IT2ROFmid [0200 H]**

Read-on-the-fly register.

| Signal Name    | Bits | Access | Default  | Description                      |
|----------------|------|--------|----------|----------------------------------|
| IT2ROFmid(7:0) | 7:0  | R      | 00000000 | Read-on-the-fly register (MidSB) |

**14.2: IT2ROFhi [0201 H]**

Read-on-the-fly register.

| Signal Name   | Bits | Access | Default  | Description                    |
|---------------|------|--------|----------|--------------------------------|
| IT2ROFhi(7:0) | 7:0  | R      | 00000000 | Read-on-the-fly register (MSB) |

**14.3: IT2Cnt1:PACNT [0204 H / 0205 H]**

Number of parity errors detected on this UTOPIA interface. Counter overflow leads to an interrupt request.

| Signal Name | Bits | Access | Default  | Description          |
|-------------|------|--------|----------|----------------------|
| PACNT(7:0)  | 7:0  | R      | 00000000 | Parity error counter |

#### 14.4: IT2Th1:PACNTTh [0206 H]

Threshold register for number of parity errors detected on this UTOPIA interface; threshold overstep leads to an interrupt request.

| Signal Name  | Bits | Access | Default  | Description        |
|--------------|------|--------|----------|--------------------|
| PACNTTh(7:0) | 7:0  | R/W    | 01111111 | Threshold register |

#### 14.5: IT2Cnt2:PECNT [0208 H / 0209 H]

The counter value is half the number of clock cycles that cells have been transmitted where it was not allowed to, due to TXCLAV=0 . Counter overflow leads to an interrupt request.

| Signal Name | Bits | Access | Default  | Description            |
|-------------|------|--------|----------|------------------------|
| PECNT(7:0)  | 7:0  | R      | 00000000 | Protocol error counter |

#### 14.6: IT2Th2:PECNTTh [020A H]

Threshold register for number of protocol errors detected on this UTOPIA interface; threshold overstep leads to an interrupt request.

| Signal Name  | Bits | Access | Default  | Description        |
|--------------|------|--------|----------|--------------------|
| PECNTTh(7:0) | 7:0  | R/W    | 01111111 | Threshold register |

#### 14.7: IT2Cnt3:ATMCELL [020C H / 020D H]

Number of cells received by this UTOPIA interface from the ATM layer. No threshold register. Counter overflow leads to an interrupt request.

| Signal Name  | Bits | Access | Default  | Description            |
|--------------|------|--------|----------|------------------------|
| ATMCELL(7:0) | 7:0  | R      | 00000000 | ATM cell counter (LSB) |

#### 14.8: IT2Cnt4:CORCELL [020E H / 020F H]

Number of corrupted cell errors. The Corrupted Cell counter is counting missing SOC (StartOfCell, StartOfChunk) events, which is slightly different from a 'pure corrupted cell counter'. If there was an initial SOC, the ACI\_Tx is able to continue to read in data even if there are no SOCs with the following cells. A corrupted cell will only result if finally a SOC arrives that is not aligned with the H1 byte. So, even if there is no real cell corruption, this counter is counting missing SOCs to indicate to the user that something is wrong at the UTOPIA interface. Counter overflow leads to an interrupt request.

| Signal Name  | Bits | Access | Default  | Description                    |
|--------------|------|--------|----------|--------------------------------|
| CORCELL(7:0) | 7:0  | R      | 00000000 | ACI_Tx2 corrupted cell counter |

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**14.9: IT2CntEn1 [0202 H]**

Counter On/Off control register.

For each bit position: 0: Counter is disabled  
1: Counter is enabled

| Signal Name | Bits | Access | Default | Description                          |
|-------------|------|--------|---------|--------------------------------------|
| EN-PACNT    | 0    | R/W    | 0       | UTOPIA parity error counter enable   |
| EN-PECNT    | 1    | R/W    | 0       | UTOPIA protocol error counter enable |
| EN-ATMCELL  | 2    | R/W    | 0       | ATM cell counter enable              |
| EN-CORCELL  | 3    | R/W    | 0       | Corrupted cell counter enable        |
| Reserved    | 7:4  |        |         | Not used                             |

**ACI\_Tx2 (IT2) Reset Register**
**15.1: IT2RESET [2030 H]**

Reset chiplet control register. This register is automatically preset to the default value by the reset signal ResIT2 from the GPPINT.

For each bit position: 0: Reset not active  
1: Reset active

| Signal Name | Bits | Access | Default | Description                     |
|-------------|------|--------|---------|---------------------------------|
| Reset       | 0    | R/W    | 1       | Reset (disable) ACI_Tx2 chiplet |
| Reserved    | 7:1  |        |         | Not used                        |

## ACI\_Tx2 Interrupt Request and Mask Registers

### 16.1: IT2MainIRQ [0238 H]

Register to indicate fatal interrupt events and to point to user IRQ registers with active requests.

For each bit position: 0: No interrupt request pending  
1: Interrupt request pending

### 16.2: IT2M\_MainIRQ [0239 H]

Register to mask pending interrupt requests. A masked request will not generate an outgoing IRQ to the GPPINT.

For each bit position: 0: The corresponding pending request bit is masked (DEFAULT)  
1: The corresponding pending request bit activates signal IRQIT2 to GPPINT

| Signal Name | Bits | Access | Default | Description                           |
|-------------|------|--------|---------|---------------------------------------|
| Fatal       | 0    | R/W    | 0       | Fatal event occurred                  |
| CntIRQ1     | 1    | R/W    | 0       | Active request in IT2CntIRQ1 register |
| Reserved    | 7:2  |        |         | Not used                              |

### 16.3: IT2CntIRQ1 [023A H]

Register to indicate active counter interrupt requests of this chiplet.

For each bit position: 0: No interrupt request pending  
1: Interrupt request pending

### 16.4: IT2M\_CntIRQ1 [023B H]

Register to mask pending counter interrupt requests.

For each bit position: 0: The corresponding pending request bit is masked (DEFAULT)  
1: The corresponding pending request bit activates the pointer bit in IT2MainIRQ register

| Signal Name | Bits | Access | Default | Description                               |
|-------------|------|--------|---------|---|
| OV-PACNT    | 0    | R/W    | 0       | Overflow parity error counter             |
| TH-PACNT    | 1    | R/W    | 0       | Threshold overstep parity error counter   |
| OV-PECNT    | 2    | R/W    | 0       | Overflow protocol error counter           |
| TH-PECNT    | 3    | R/W    | 0       | Threshold overstep protocol error counter |
| OV-ATMCELL  | 4    | R/W    | 0       | Overflow ATM cell counter                 |
| OV-CORCELL  | 5    | R/W    | 0       | Overflow corrupted cell counter           |
| Reserved    | 7:6  |        |         | Not used                                  |

## ACI\_Tx2 Configuration Register

### 16.5: IT2Conf1 [0248 H]

Register to control various modes of operation of this chiplet.

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| AutRst_Int  | 0    | R/W    | 1       | 0: No action upon read access<br>1: Auto-reset interrupt request registers upon read access<br>Regardless of the setting of this bit, individual interrupt request bits can be cleared by writing a '1' to that bit provided that the corresponding alarm condition is removed. |
| TMOPAIT2(0) | 1    | R/W    | 0       | Mode for UTOPIA (ATM/PPP) parity error detection:<br>0: Parity check off<br>1: Parity check on  |
| TMOPAIT2(1) | 2    | R/W    | 0       | Mode of parity calculation:<br>0: Parity calculated over data only<br>1: Parity calculated over data and control  |
| Reserved    | 7:3  |        |         | Not used  |

## ACI\_Rx1 Chiplet Address Map Base Address 0300 H

| Register Name   | Address Offset (Hex) | Type/Width | Initial Value (Binary) | Description   | See Page |
|-----------------|----------------------|------------|------------------------|---|----------|
| IR1ROFmid       | 0                    | F 8        | 00000000               | Read-on-the-fly register (MidSB)                              | 165      |
| IR1ROFhi        | 1                    | F 8        | 00000000               | Read-on-the-fly register (MSB)                                | 165      |
| IR1CntEn1       | 2                    | X 2        | 00                     | COUNT ENABLE register   | 166      |
| IR1Cnt1:ATMCELL | 4/5                  | N 24       | 000000 H               | LS byte of 24-bit ATM cell counter, no threshold              | 166      |
| IR1Cnt2:PRERR   | 6/7                  | N 8        | 00000000               | Protocol error counter, with threshold                        | 166      |
| IR1Th2:PRERRTh  | 8                    | X 8        | 01111111               | Threshold register for counter PRERR                          | 166      |
| IR1RESET        | 30                   | R 1        |                        | Default RESET register  | 167      |
| IR1Stat1        | 33                   | S 4        |                        | 0=PsellR1 1=PsellR2 2=PsellR3 3=PsellR4                       | 167      |
| IR1Stat2        | 34                   | S 5        |                        | 4:0 = selected UTOPIA Level 2 port address                    | 167      |
| IR1MainIRQ      | 38                   | I 2        |                        | MAIN INTerrupt register                                       | 168      |
| IR1M_MainIRQ    | 39                   | X 2        | 00                     | INT MASK register (for IR1MainIRQ)                            | 168      |
| IR1CntIRQ1      | 3A                   | I 3        |                        | COUNTER INTerrupt register                                    | 168      |
| IR1M_CntIRQ1    | 3B                   | X 3        | 000                    | INT MASK register (for IR1CntIRQ1)                            | 168      |
| IR1Conf1        | 48                   | C 5        | 00011                  | 0=R and R INT 1=Not used. 2=RX1PAMO<br>3=RX1PAODD 4=RX1PA_ALL | 169      |
| IR1Conf2:P1ADDR | 49                   | C 5        | 00000                  | PHY port address of SONET/SDH macro 1                         | 170      |
| IR1Conf3:P2ADDR | 4A                   | C 5        | 00001                  | PHY port address of SONET/SDH macro 2                         |          |
| IR1Conf4:P3ADDR | 4B                   | C 5        | 00010                  | PHY port address of SONET/SDH macro 3                         |          |
| IR1Conf5:P4ADDR | 4C                   | C 5        | 00011                  | PHY port address of SONET/SDH macro 4                         |          |

## ACI\_Rx1 (IR1) Counters

### 17.1: IR1ROFmid [0300 H]

Read-on-the-fly register.

| Signal Name    | Bits | Access | Default  | Description                      |
|----------------|------|--------|----------|----------------------------------|
| IR1ROFmid(7:0) | 7:0  | R      | 00000000 | Read-on-the-fly register (MidSB) |

### 17.2: IR1ROFhi [0301 H]

Read-on-the-fly register.

| Signal Name   | Bits | Access | Default  | Description                    |
|---------------|------|--------|----------|--------------------------------|
| IR1ROFhi(7:0) | 7:0  | R      | 00000000 | Read-on-the-fly register (MSB) |

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**17.3: IR1Cnt1:ATMCELL [0304 H / 0305 H]**

Number of cells transmitted by this UTOPIA interface towards the ATM layer. Counter overflow leads to an interrupt request.

| Signal Name  | Bits | Access | Default  | Description            |
|--------------|------|--------|----------|------------------------|
| ATMCELL(7:0) | 7:0  | R      | 00000000 | ATM cell counter (LSB) |

**17.4: IR1Cnt2:PRERR [0306 H / 0307 H]**

Number of UTOPIA protocol errors detected on this UTOPIA interface. This covers unexpected port change during cell transfer. Counter overflow leads to an interrupt request.

| Signal Name | Bits | Access | Default  | Description            |
|-------------|------|--------|----------|------------------------|
| PRERR(7:0)  | 7:0  | R      | 00000000 | Protocol error counter |

**17.5: IR1Th2:PRERRTh [0308 H]**

Threshold for number of UTOPIA protocol errors detected on this UTOPIA interface. Threshold overstep leads to an interrupt request.

| Signal Name  | Bits | Access | Default  | Description        |
|--------------|------|--------|----------|--------------------|
| PRERRTh(7:0) | 7:0  | R/W    | 01111111 | Threshold register |

**17.6: IR1CntEn1 [0302 H]**

Counter On/Off control register.

For each bit position: 0: Counter is disabled

1: Counter is enabled

| Signal Name | Bits | Access | Default | Description                          |
|-------------|------|--------|---------|--------------------------------------|
| EN-ATM      | 0    | R/W    | 0       | ATM cell counter enable              |
| EN-PRERR    | 1    | R/W    | 0       | UTOPIA protocol error counter enable |
| Reserved    | 7:2  |        |         | Not used                             |

## ACI\_Rx1 (IR1) Reset Register

### 18.1: IR1RESET [0330 H]

Reset chiplet control register. This register is automatically preset to the default value by the reset signal ResIR1 from the GPPINT.

For each bit position: 0: Reset not active

1: Reset active

| Signal Name | Bits | Access | Default | Description                     |
|-------------|------|--------|---------|---------------------------------|
| Reset       | 0    | R/W    | 1       | Reset (disable) ACI_Rx1 chiplet |
| Reserved    | 7:1  |        |         | Not used                        |

## ACI\_Rx1 (IR1) Status Register

### 19.1: IR1Stat1 [0333 H]

Status register #1 of this chiplet. These are status bits that follow the driving signal immediately.

| Signal Name | Bits | Access | Default | Description  |
|-------------|------|--------|---------|--|
| PselIR1     | 0    | R      |         | 0: Macro #1 is not selected<br>1: Macro #1 selected by PHY port selected |
| PselIR2     | 1    | R      |         | 0: Macro #2 is not selected<br>1: Macro #2 selected by PHY port selected |
| PselIR3     | 2    | R      |         | 0: Macro #3 is not selected<br>1: Macro #3 selected by PHY port selected |
| PselIR4     | 3    | R      |         | 0: Macro #4 is not selected<br>1: Macro #4 selected by PHY port selected |
| Reserved    | 7:4  |        |         | Not used   |

### 19.2: IR1Stat2 [0334 H]

Status register #2 of this chiplet. These are status bits that follow the driving signal immediately.

| Signal Name | Bits | Access | Default | Description                          |
|-------------|------|--------|---------|--------------------------------------|
| UPaddr      | 4:0  | R      |         | Selected UTOPIA Level 2 port address |
| Reserved    | 7:5  |        |         | Not used                             |



## ACI\_Rx1 (IR1) Interrupt Request and Mask Registers

### 20.1: IR1MainIRQ [0338 H]

Register to indicate fatal interrupt events and to point to user IRQ registers with active requests.

For each bit position: 0: No interrupt request pending  
 1: Interrupt request pending

### 20.2: IR1M\_MainIRQ [0339 H]

Register to mask pending interrupt requests. A masked request will not generate an outgoing IRQ to the GPPINT.

For each bit position: 0: The corresponding pending request bit is masked (DEFAULT)  
 1: The corresponding pending request bit activates signal IRQIR1 to GPPINT

| Signal Name | Bits | Access | Default | Description                           |
|-------------|------|--------|---------|---------------------------------------|
| Fatal       | 0    | R/W    | 0       | Fatal event occurred                  |
| CntIRQ1     | 1    | R/W    | 0       | Active request in IR1CntIRQ1 register |
| Reserved    | 7:2  |        |         | Not used                              |

### 20.3: IR1CntIRQ1 [033A H]

Register to indicate active counter interrupt requests of this chiplet.

For each bit position: 0: No interrupt request pending  
 1: Interrupt request pending

### 20.4: IR1M\_CntIRQ1 [033B H]

Register to mask pending counter interrupt requests.

For each bit position: 0: The corresponding pending request bit is masked (DEFAULT)  
 1: The corresponding pending request bit activates the pointer bit in IR1MainIRQ register

| Signal Name | Bits | Access | Default | Description                               |
|-------------|------|--------|---------|---|
| OV-ATM      | 0    | R/W    | 0       | Overflow ATM cell counter                 |
| OV-PRERR    | 1    | R/W    | 0       | Overflow protocol error counter           |
| TH-PRERR    | 2    | R/W    | 0       | Threshold overstep protocol error counter |
| Reserved    | 7:3  |        |         | Not used                                  |

## ACI\_Rx1 Configuration Registers

### 21.1: IR1Conf1 [0348 H]

Register to control various modes of operation of this chiplet.

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| AutRst_Int  | 0    | R/W    | 1       | 0: No action on read access<br>1: Auto-reset interrupt request registers upon read access<br>Regardless of the setting of this bit, individual interrupt request bits can be cleared by writing a '1' to that bit provided that the corresponding alarm condition is removed. |
| AutRst_Sta  | 1    | R/W    | 1       | Not used  |
| RX1PAMO     | 2    | R/W    | 0       | Control of UTOPIA (ATM/PPP) parity generation:<br>0: Parity generation off<br>1: Parity generation on   |
| RX1PAODD    | 3    | R/W    | 0       | Mode for UTOPIA (ATM/PPP) parity generation:<br>0: Even parity<br>1: Odd parity   |
| RX1PA_ALL   | 4    | R/W    | 0       | Mode of parity calculation:<br>0: Parity calculated over data only<br>1: Parity calculated over data and control  |
| Reserved    | 7:5  |        |         | Not used  |

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**21.2: IR1Conf2-5:P1ADDR-P4ADDR [0349 H, 034A H, 034B H, 034C H]**

Registers that control the PHY port addresses according to UTOPIA Level 2.

Used in 1 x UTOPIA Level 2 multi-PHY/multi-port configuration (non-STM-4c), multi-PHY/single-port configuration (STM-4c), MULTIPLEXED status indication; for bit positions (4:0) of each register:

00000 to 11110: valid address for PHY port selection

11111: PHY port is never selected

Used in 1 x UTOPIA Level 2 multi-PHY/multi-port configuration (non-STM-4c), multi-PHY/single-port configuration (STM-4c), DIRECT status indication; for bit positions (4:0) of each register:

00000 to 11111: valid address for PHY port selection

For UTOPIA Level 1: don't care

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| P1ADDR(4:0) | 4:0  | R/W    | 00000   | PHY port address of SONET/SDH macro #1 (also port address for STM-4c) |
| Reserved    | 7:5  |        |         | Not used  |
| P2ADDR(4:0) | 4:0  | R/W    | 00001   | PHY port address of SONET/SDH macro #2 (for STM-4c: don't care)       |
| Reserved    | 7:5  |        |         | Not used  |
| P3ADDR(4:0) | 4:0  | R/W    | 00010   | PHY port address of SONET/SDH macro #3 (for STM-4c: don't care)       |
| Reserved    | 7:5  |        |         | Not used  |
| P4ADDR(4:0) | 4:0  | R/W    | 00011   | PHY port address of SONET/SDH macro #4 (for STM-4c: don't care)       |
| Reserved    | 7:5  |        |         | Not used  |

## ACI\_Rx2 Chiplet Address Map Base Address 0400 H

| Register Name   | Address Offset (Hex) | Type/Width | Initial Value (Binary) | Description  | See Page |
|-----------------|----------------------|------------|------------------------|--|----------|
| IR2ROFmid       | 0                    | F 8        | 00000000               | Read-on-the-fly register (MidSB)   | 171      |
| IR2ROFhi        | 1                    | F 8        | 00000000               | Read-on-the-fly register (MSB)   | 171      |
| IR2CntEn1       | 2                    | X 1        | 0                      | COUNT ENABLE register  | 172      |
| IR2Cnt1:ATMCELL | 4/5                  | N 24       | 000000 H               | LS Byte of 24-bit ATM cell counter, no threshold                           | 171      |
| IR2RESET        | 30                   | R 1        | 1                      | Default RESET register   | 172      |
| IR2MainIRQ      | 38                   | I 2        |                        | MAIN INTerrupt register  | 172      |
| IR2M_MainIRQ    | 39                   | X 2        | 00                     | INT MASK register (for IR2MainIRQ)   | 172      |
| IR2CntIRQ1      | 3A                   | I 1        |                        | COUNTER INTerrupt register   | 173      |
| IR2M_CntIRQ1    | 3B                   | X 1        | 0                      | INT MASK register (for IR2CntIRQ1)   | 173      |
| IR2Conf1        | 48                   | C 5        | 00001                  | 0: R and R INT<br>1: Reserved<br>2: RX2PAMO<br>3: RX2PAODD<br>4: RX2PA_ALL | 173      |

## ACI\_Rx2 (IR2) Counters

### 22.1: IR2ROFmid [0400 H]

Read-on-the-fly registers.

| Signal Name    | Bits | Access | Default  | Description                      |
|----------------|------|--------|----------|----------------------------------|
| IR2ROFmid(7:0) | 7:0  | R      | 00000000 | Read-on-the-fly register (MidSB) |

### 22.2: IR2ROFhi [0401 H]

Read-on-the-fly registers.

| Signal Name   | Bits | Access | Default  | Description                    |
|---------------|------|--------|----------|--------------------------------|
| IR2ROFhi(7:0) | 7:0  | R      | 00000000 | Read-on-the-fly register (MSB) |

### 22.3: IR2Cnt1:ATMCELL [0404 H, 0405 H]

Number of cells transmitted by this UTOPIA interface towards the ATM layer. Counter overflow leads to an interrupt request.

| Signal Name  | Bits | Access | Default  | Description            |
|--------------|------|--------|----------|------------------------|
| ATMCELL(7:0) | 7:0  | R      | 00000000 | ATM cell counter (LSB) |

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### 22.4: IR2CntEn1 [0402 H]

Counter On/Off control register.

For each bit position: 0: Counter is disabled  
1: Counter is enabled

| Signal Name | Bits | Access | Default | Description             |
|-------------|------|--------|---------|-------------------------|
| EN-ATM      | 0    | R/W    | 0       | ATM cell counter enable |
| Reserved    | 7:1  |        |         | Not used                |

## ACI\_Rx2 (IR2) Reset Register

### 23.1: IR2RESET [0430 H]

Reset chiplet control register. This register is automatically preset to the default value by the reset signal ResIR2 from the GPPINT.

For each bit position: 0: Reset not active  
1: Reset active

| Signal Name | Bits | Access | Default | Description                     |
|-------------|------|--------|---------|---------------------------------|
| Reset       | 0    | R/W    | 1       | Reset (disable) ACI_Rx2 chiplet |
| Reserved    | 7:1  |        |         | Not used                        |

## ACI\_Rx2 Interrupt Request and Mask Registers

### 24.1: IR2MainIRQ [0438 H]

Register to indicate fatal interrupt events and to point to user IRQ registers with active requests.

For each bit position: 0: No interrupt request pending  
1: Interrupt request pending

### 24.2: IR2M\_MainIRQ [0439 H]

Register to mask pending interrupt requests. A masked request will not generate an outgoing IRQ to the GPPINT.

For each bit position: 0: The corresponding pending request bit is masked (DEFAULT)  
1: The corresponding pending request bit activates signal IRQIR2 to GPPINT

| Signal Name | Bits | Access | Default | Description                           |
|-------------|------|--------|---------|---------------------------------------|
| Fatal       | 0    | R/W    | 0       | Fatal event occurred                  |
| CntIRQ1     | 1    | R/W    | 0       | Active request in IR2CntIRQ1 register |
| Reserved    | 7:2  |        |         | Not used                              |

### 24.3: IR2CntIRQ1 [043A H]

Register to indicate active counter interrupt requests of this chiplet.

For each bit position: 0: No interrupt request pending  
1: Interrupt request pending

### 24.4: IR2M\_CntIRQ1 [043B H]

Register to mask pending counter interrupt requests.

For each bit position: 0: The corresponding pending request bit is masked (DEFAULT)  
1: The corresponding pending request bit activates the pointer bit in IR2MainIRQ register

| Signal Name | Bits | Access | Default | Description               |
|-------------|------|--------|---------|---------------------------|
| OV-ATM      | 0    | R/W    | 0       | Overflow ATM cell counter |
| Reserved    | 7:1  |        |         | Not used                  |

## ACI\_Rx2 Configuration Register

### 25.1: IR2Conf1 [0448 H]

Register to control various modes of operation of this chiplet.

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| AutRst_Int  | 0    | R/W    | 1       | 0: No action on read access<br>1: Auto-reset interrupt request registers upon read access<br>Regardless of the setting of this bit, individual interrupt request bits can be cleared by writing a '1' to that bit provided that the corresponding alarm condition is removed. |
| Reserved    | 1    |        | 0       | Not used  |
| RX2PAMO     | 2    | R/W    | 0       | Control of UTOPIA (ATM/PPP) parity generation:<br>0: Parity generation off<br>1: Parity generation on   |
| RX2PAODD    | 3    | R/W    | 0       | Mode for UTOPIA (ATM/PPP) parity generation:<br>0: Even parity<br>1: Odd parity   |
| RX2PA_ALL   | 4    | R/W    | 0       | Mode of parity calculation:<br>0: Parity calculated over data only<br>1: Parity calculated over data and control  |
| Reserved    | 7:5  |        |         | Not used  |



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**PH\_Tx1/2/3/4 Chiplet Address Map** Base Address: PH\_Tx1 0500 H, PH\_Tx2 0600 H, PH\_Tx3 0700 H, PH\_Tx4 0800 H

| Register Name <sup>1</sup> | Address Offset (Hex) | Type/Width | Initial Value (Binary) | Description                        | See Page |
|----------------------------|----------------------|------------|------------------------|------------------------------------|----------|
| PT#Reset                   | 30                   | R 1        | 1                      | Default RESET register             | 174      |
| PT#Stat1                   | 33                   | S 2        |                        | 0 = FF 1 = PAF                     | 174      |
| PT#MainIRQ                 | 38                   | I 1        |                        | MAIN INTerrupt register            | 175      |
| PT#M_MainIRQ               | 39                   | X 1        | 0                      | INT MASK register (for PT#MainIRQ) | 175      |
| PT#Conf1:REFSPT1           | 48                   | C 2        | 11                     | 0 = R and R INT 1 = R and R STAT   | 176      |
| PT#Conf2:NEWCONF           | 49                   | C 7        | 1011111                | 6:0 = PAF threshold                | 176      |

1. # = Port Handler SONET/SDH macro: 1, 2, 3, or 4.

**PH\_Tx1/2/3/4 (PT1/2/3/4) Reset and Status Registers**

**26.1: PT#RESET [0530 H, 0630 H, 0730 H, 0830 H]**

Reset chiplet control register. These registers are automatically preset to the default value by the reset signals ResPT1, ResPT2, ResPT3 and ResPT4, respectively, from the GPPINT.

For each bit position: 0: Reset not active  
1: Reset active

| Signal Name | Bits | Access | Default | Description                          |
|-------------|------|--------|---------|--------------------------------------|
| Reset       | 0    | R/W    | 1       | Reset (disable) PH_Tx1/2/3/4 chiplet |
| Reserved    | 7:1  |        |         | Not used                             |

**26.2: PT#Stat1 [0533 H, 0633 H, 0733 H, 0833 H]**

Status register of this chiplet. Bit 0 is an event latch register. Bit 1 immediately follows the driving signal (static).

| Signal Name | Bits | Access | Default | Description                   |
|-------------|------|--------|---------|-------------------------------|
| acbtxFF     | 0    | R/W    |         | ACB_Tx Fifo Full flag was set |
| acbtxPAF    | 1    | R      |         | ACB_Tx Fifo Almost Full flag  |
| Reserved    | 7:2  |        |         | Not used                      |

## PH\_Tx1/2/3/4 Interrupt Request and Mask Registers

### 27.1: PT#MainIRQ [0538 H, 0638 H, 0738 H, 0838 H]

Register to indicate fatal interrupt events.

For each bit position: 0: No interrupt request pending  
1: Interrupt request pending

### 27.2: PT#M\_MainIRQ [0539 H, 0639 H, 0739 H, 0839 H]

Register to mask pending interrupt requests. A masked request will not generate an outgoing IRQ to the GPPINT.

For each bit position: 0: The corresponding pending request bit is masked (DEFAULT)  
1: The corresponding pending request bit activates signal IRQPT1/2/3/4 to GPPINT

| Signal Name | Bits | Access | Default | Description          |
|-------------|------|--------|---------|----------------------|
| Fatal       | 0    | R/W    | 0       | Fatal event occurred |
| Reserved    | 7:1  |        |         | Not used             |



**PH\_Rx1/2/3/4 Chiplet Address Map** Base Address: PH\_Rx1 0900 H, PH\_Rx2 0A00 H, PH\_Rx3 0B00 H, PH\_Rx4 0C00 H

| Register Name <sup>1</sup> | Address Offset (Hex) | Type/Width | Initial Value (Binary) | Description                                | See Page |
|----------------------------|----------------------|------------|------------------------|--|----------|
| PR#Reset                   | 30                   | R 1        | 1                      | Default RESET register                     | 177      |
| PR#Stat1                   | 33                   | S 3        |                        | 0 = PAE flag<br>1 = EF flag<br>2 = CC flag | 177      |
| PR#MainIRQ                 | 38                   | I 1        |                        | MAIN INTerrupt register                    | 178      |
| PR#M_MainIRQ               | 39                   | X 1        | 0                      | INT MASK register (for PR#MainIRQ)         | 178      |
| PR#Conf1                   | 48                   | C 2        | 11                     | 0 = R and R INT<br>1 = R and R STAT        | 178      |
| PR#Conf2:RXTHBUF           | 49                   | C 7        | 0011011                | 6:0 = PAE threshold                        | 179      |

1. # = Port Handler SONET/SDH macro: 1, 2, 3, or 4.

**PH\_Rx1/2/3/4 (PR1/2/3/4) Reset and Status Registers**
**28.1: PR#RESET [0930 H, 0A30 H, 0B30 H, 0C30 H]**

Reset chiplet control register. These registers are automatically preset to the default value by the reset signals ResPR1, ResPR2, ResPR3 and ResPR4, respectively, from the GPPINT.

For each bit position: 0: Reset not active  
1: Reset active

| Signal Name | Bits | Access | Default | Description                          |
|-------------|------|--------|---------|--------------------------------------|
| Reset       | 0    | R/W    | 1       | Reset (disable) PH_Rx1/2/3/4 chiplet |
| Reserved    | 7:1  |        |         | Not used                             |

**28.2: PR#Stat1 [0933 H, 0A33 H, 0B33 H, 0C33 H]**

Status register of this chiplet. Bit 0 immediately follows the driving signal (static). Bits 2 and 1 are event latch registers.

| Signal Name | Bits | Access | Default | Description                                |
|-------------|------|--------|---------|--|
| acbrxPAE    | 0    | R      |         | ACB_Rx FIFO Programmable Almost Empty flag |
| acbrxEF     | 1    | R/W    |         | ACB_Rx FIFO Empty flag                     |
| acbrxCC     | 2    | R/W    |         | A corrupted cell was sent to UTOPIA        |
| Reserved    | 7:5  |        |         | Not used                                   |

## PH\_Rx1/2/3/4 Interrupt Request and Mask Registers

### 29.1: PR#MainIRQ [0938 H, 0A38 H, 0B38 H, 0C38 H]

Register to indicate fatal interrupt events.

For each bit position: 0: No interrupt request pending  
1: Interrupt request pending

### 29.2: PR#M\_MainIRQ [0939 H, 0A39 H, 0B39 H, 0C39 H]

Register to mask pending interrupt requests. A masked request will not generate an outgoing IRQ to the GPPINT.

For each bit position: 0: The corresponding pending request bit is masked (DEFAULT)  
1: The corresponding pending request bit activates signal IRQPR1/2/3/4 to GPPINT

| Signal Name | Bits | Access | Default | Description          |
|-------------|------|--------|---------|----------------------|
| Fatal       | 0    | R/W    | 0       | Fatal event occurred |
| Reserved    | 7:1  |        |         | Not used             |

## PH\_Rx Configuration Registers

### 30.1: PR#Conf1 [0948 H, 0A48 H, 0B48 H, 0C48 H]

Register to control various modes of operation of this chiplet.

| Signal Name | Bits | Access | Default | Description  |
|-------------|------|--------|---------|--|
| AutRst_Int  | 0    | R/W    | 1       | 0: No action on read access<br>1: Auto-reset interrupt request register upon read access<br>Regardless of the setting of this bit, individual interrupt request bits can be cleared by writing a '1' to that bit provided that the corresponding alarm condition is removed. |
| AutRst_Sta  | 1    | R/W    | 1       | 0: No action on read access<br>1: Auto-reset bits 2 and 1 of the PR#Stat1 status register upon read access   |
| Reserved    | 7:2  |        |         | Not used   |



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## ACH\_Tx1 Chiplet Address Map Base Address: 0D00 H

| Register Name        | Address Offset (Hex) | Type/Width | Initial Value (Binary) | Description  | See Page |
|----------------------|----------------------|------------|------------------------|--|----------|
| HT1ROFmid            | 0                    | F 8        | 00000000               | Read-on-the-fly register (MidSB)                             | 181      |
| HT1ROFhi             | 1                    | F 8        | 00000000               | Read-on-the-fly register (MSB)                               | 181      |
| HT1CntEn1            | 2                    | X 3        | 000                    | COUNT ENABLE register  | 182      |
| HT1Cnt1:ACBC         | 4/5                  | N 24       | 000000 H               | LS byte of 24-bit ACB cell counter, no threshold             | 181      |
| HT1Cnt2:IUC          | 6/7                  | N 24       | 000000 H               | LS byte of 24-bit idle/unassigned cell counter, no threshold | 181      |
| HT1Cnt3:APSPE        | 8/9                  | N 8        | 00000000               | APS parity error counter                                     | 181      |
| HT1Th3:APSPETH       | A                    | X 8        | 01111111               | Threshold register for counter APSPE                         | 181      |
| HT1RESET             | 30                   | R 1        | 1                      | Default RESET register                                       | 182      |
| HT1Stat1             | 33                   | S 8        |                        | Status register #1   | 183      |
| HT1Stat2             | 34                   | S 4        |                        | Status register #2   | 183      |
| HT1MainIRQ           | 38                   | I 2        |                        | MAIN INTerrupt register                                      | 184      |
| HT1M_MainIRQ         | 39                   | X 2        | 00                     | INT MASK register (for HT1MainIRQ)                           | 184      |
| HT1CntIRQ1           | 3A                   | I 4        |                        | COUNTER INTerrupt register                                   | 184      |
| HT1M_CntIRQ1         | 3B                   | X 4        | 0000                   | INT MASK register (for HT1CntIRQ1)                           | 184      |
| HT1Conf1:CELLTENABLE | 48                   | C 4        | 1111                   | Chiplet configuration register                               | 185      |
| HT1Conf2:ACBTXTHPAE  | 49                   | C 7        | 0011011                | Programmable Almost Empty threshold                          | 185      |
| HT1Conf3:HEADERBYTE1 | 4A                   | C 8        | 00000000               | IU-cell header byte 1, defaults according to [I.432]         | 186      |
| HT1Conf4:HEADERBYTE2 | 4B                   | C 8        | 00000000               | IU-cell header byte 2, defaults according to [I.432]         |          |
| HT1Conf5:HEADERBYTE3 | 4C                   | C 8        | 00000000               | IU-cell header byte 3, defaults according to [I.432]         |          |
| HT1Conf6:HEADERBYTE4 | 4D                   | C 8        | 00000001               | IU-cell header byte 4, defaults according to [I.432]         |          |
| HT1Conf7:HEADERBYTE5 | 4E                   | C 8        | 01010010               | IU-cell header byte 5  |          |
| HT1Conf8:PAYLOADBYTE | 4F                   | C 8        | 01101010               | IU-cell payload byte   | 186      |
| HT1Conf9:HECENCTRL   | 50                   | C 7        | 0001100                | HEC processing control                                       | 186      |
| HT1Conf10:HECOFFSET  | 51                   | C 8        | 01010101               | HEC offset pattern register                                  | 187      |
| HT1Conf11:HECMASKAND | 52                   | C 8        | 11111111               | HEC error corruption mask (AND)                              | 187      |
| HT1Conf12:HECMASKOR  | 53                   | C 8        | 00000000               | HEC error corruption mask (OR)                               | 187      |
| HT1Conf13:SDBTXTHPAF | 54                   | C 6        | 010011                 | Programmable Almost Full threshold                           | 185      |
| HT1Conf14:APSELECT   | 55                   | C 6        | 111111                 | APS select matrix (transmit direction)                       | 188      |
| HT1Conf15:APSCONF    | 56                   | C 4        | 1010                   | APS parity handling (transmit direction)                     | 189      |

## ACH\_Tx1 (HT1) Counters

### 31.1: HT1ROFmid [0D00 H]

Read-on-the-fly register.

| Signal Name    | Bits | Access | Default  | Description                      |
|----------------|------|--------|----------|----------------------------------|
| HT1ROFmid(7:0) | 7:0  | R      | 00000000 | Read-on-the-fly register (MidSB) |

### 31.2: HT1ROFhi [0D01 H]

Read-on-the-fly register.

| Signal Name   | Bits | Access | Default  | Description                    |
|---------------|------|--------|----------|--------------------------------|
| HT1ROFhi(7:0) | 7:0  | R      | 00000000 | Read-on-the-fly register (MSB) |

### 31.3: HT1Cnt1:ACBC [0D04 H / 0D05 H]

Number of cells transmitted from this ATM Cell Buffer (ACB\_Tx1). Counter overflow leads to an interrupt request.

| Signal Name | Bits | Access | Default  | Description            |
|-------------|------|--------|----------|------------------------|
| ACBC(7:0)   | 7:0  | R      | 00000000 | ACB cell counter (LSB) |

### 31.4: HT1Cnt2:IUC [0D06 H / 0D07 H]

Number of transmitted Idle and Unassigned cells. Counter overflow leads to an interrupt request.

| Signal Name | Bits | Access | Default  | Description                      |
|-------------|------|--------|----------|----------------------------------|
| IUC(7:0)    | 7:0  | R      | 00000000 | Idle/unassigned cell count (LSB) |

### 31.5: HT1Cnt3:APSPE [0D08 H / 0D09 H]

Number of parity errors from Automatic Protection Switching (APS). Counter overflow leads to an interrupt request.

| Signal Name | Bits | Access | Default  | Description              |
|-------------|------|--------|----------|--------------------------|
| APSPE(7:0)  | 7:0  | R      | 00000000 | APS parity error counter |

### 31.6: HT1Th3:APSPETH [0D0A H]

Threshold for APS parity errors. Threshold overstep leads to an interrupt request.

| Signal Name  | Bits | Access | Default  | Description                            |
|--------------|------|--------|----------|--|
| APSPETH(7:0) | 7:0  | R/W    | 01111111 | Threshold for APS parity error counter |

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**31.7: HT1CntEn1 [0D02 H]**

Counter On/Off control register for ACH\_Tx1/ACB\_Tx1.

For each bit position: 0: Counter is disabled  
1: Counter is enabled

| Signal Name | Bits | Access | Default | Description                         |
|-------------|------|--------|---------|-------------------------------------|
| EN-ACBC     | 0    | R/W    | 0       | ACB cell counter enable             |
| EN-IUC      | 1    | R/W    | 0       | Idle/unassigned cell counter enable |
| EN-APSPE    | 2    | R/W    | 0       | APS parity error counter enable     |
| Reserved    | 7:3  |        |         | Not used                            |

**ACH\_Tx1 (HT1) Reset Register**
**32.1: HT1RESET [0D30 H]**

Reset chiplet control register. This register is automatically preset to the default value by the reset signal ResHT1 from the GPPINT.

For each bit position: 0: Reset not active  
1: Reset active

| Signal Name | Bits | Access | Default | Description                     |
|-------------|------|--------|---------|---------------------------------|
| Reset       | 0    | R/W    | 1       | Reset (disable) ACH_Tx1 chiplet |
| Reserved    | 7:1  |        |         | Not used                        |

## ACH\_Tx1Status Registers

### 33.1: HT1Stat1 [0D33 H]

Status register #1 of this chiplet. The bits of this register are event latches.

| Signal Name | Bits | Access | Default | Description  |
|-------------|------|--------|---------|--|
| SocMiss     | 0    | R/W    |         | Missing start of cell event  |
| sdbtxFF     | 1    | R/W    |         | FIFO Full flag from SDB_Tx1  |
| TxLpB1Fe    | 2    | R/W    |         | Transmit Loopback #1 configuration mismatch                                |
| TxLpB2Fe    | 3    | R/W    |         | Transmit Loopback #2 configuration mismatch                                |
| RxLpB2Fe    | 4    | R/W    |         | Receive Loopback #2 configuration mismatch                                 |
| IUCFErr     | 5    | R/W    |         | Unexpected state transition in FSM   |
| ApsFErr     | 6    | R/W    |         | APS fatal error detected   |
| ApsPaErr    | 7    | R/W    |         | Parity error detected at device - external APS interface (input direction) |

### 33.2: HT1Stat2 [0D34 H]

Status register #2 of this chiplet. The bits of this register immediately follow the driving signal.

| Signal Name   | Bits | Access | Default | Description  |
|---------------|------|--------|---------|--|
| acbtxEF       | 0    | R      |         | FIFO Empty flag from ACB_Tx1   |
| acbtxPAE      | 1    | R      |         | Programmable Almost Empty flag from ACB_Tx1                          |
| sdbtxPAF      | 2    | R      |         | Programmable Almost Full flag from SDB_Tx1                           |
| cellgenstatus | 3    | R      |         | 0: Idle/unassigned cell is transmitted<br>1: ACB cell is transmitted |
| Reserved      | 7:4  |        |         | Not used   |

## ACH\_Tx1 Interrupt Request and Mask Registers

### 34.1: HT1MainIRQ [0D38 H]

HT1MainIRQ: Register to indicate fatal interrupt events and to point to user IRQ registers with active requests.

For each bit position: 0: No interrupt request pending  
1: Interrupt request pending

### 34.2: HT1M\_MainIRQ [0D39 H]

HT1M\_MainIRQ: Register to mask pending interrupt requests. A masked request will not generate an outgoing IRQ to the GPPINT.

For each bit position: 0: The corresponding pending request bit is masked (DEFAULT)  
1: The corresponding pending request bit activates signal IRQHT1 to GPPINT

| Signal Name | Bits | Access | Default | Description                           |
|-------------|------|--------|---------|---------------------------------------|
| Fatal       | 0    | R/W    | 0       | Fatal event occurred                  |
| CntIRQ1     | 1    | R/W    | 0       | Active request in HT1CntIRQ1 register |
| Reserved    | 7:2  |        |         | Not used                              |

### 34.3: HT1CntIRQ1 [0D3A H]

Register to indicate active counter interrupt requests of this chiplet.

For each bit position: 0: No interrupt request pending  
1: Interrupt request pending

### 34.4: HT1M\_CntIRQ1 [0D3B H]

Register to mask pending counter interrupt requests.

For each bit position: 0: The corresponding pending request bit is masked (DEFAULT)  
1: The corresponding pending request bit activates the pointer bit in HT1MainIRQ register

| Signal Name | Bits | Access | Default | Description                                 |
|-------------|------|--------|---------|---|
| OV-ACBC     | 0    | R/W    | 0       | Overflow ACB cell counter                   |
| OV-IUC      | 1    | R/W    | 0       | Overflow idle/unassigned cell counter       |
| OV-APSPE    | 2    | R/W    | 0       | Overflow APS parity error counter           |
| TH-APSPE    | 3    | R/W    | 0       | Threshold overstep APS parity error counter |
| Reserved    | 7:4  |        |         | Not used                                    |



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**35.4: HT1Conf3-7:HEADERBYTE1/2/3/4/5 [0D4A H, 0D4B H, 0D4C H, 0D4D H, 0D4E H]**

Idle/unassigned cell header bytes, default pattern according to [I.432].

| Signal Name      | Bits | Access | Default  | Description            |
|------------------|------|--------|----------|------------------------|
| HEADERBYTE1(7:0) | 7:0  | R/W    | 00000000 | IU-cell header byte #1 |
| HEADERBYTE2(7:0) | 7:0  | R/W    | 00000000 | IU-cell header byte #2 |
| HEADERBYTE3(7:0) | 7:0  | R/W    | 00000000 | IU-cell header byte #3 |
| HEADERBYTE4(7:0) | 7:0  | R/W    | 00000001 | IU-cell header byte #4 |
| HEADERBYTE5(7:0) | 7:0  | R/W    | 01010010 | IU-cell header byte #5 |

**35.5: HT1Conf8:PAYLOADBYTE [0D4F H]**

Idle/Unassigned cell payload byte.

| Signal Name      | Bits | Access | Default  | Description          |
|------------------|------|--------|----------|----------------------|
| PAYLOADBYTE(7:0) | 7:0  | R/W    | 01101010 | IU-cell payload byte |

**35.6: HT1Conf9:HECENCTRL [0D50 H]**

HEC processing control configuration register.

| Signal Name      | Bits | Access | Default | Description   |
|------------------|------|--------|---------|---|
| HECCntIUDF1(1:0) | 1:0  | R/W    | 00      | Mode of final HEC manipulation by the UTOPIA UDF1 byte after HECOffset, HECMaskAND and HECMaskOR operations:<br>00: No manipulation<br>01: HEC XOR UDF1<br>10: HEC AND UDF1<br>11: HEC OR UDF1  |
| HECenable        | 2    | R/W    | 1       | 0: HEC calculation/manipulation disabled<br>1: HEC calculation/manipulation enabled   |
| SCRenable        | 3    | R/W    | 1       | 0: ATM cell payload scrambling disabled<br>1: ATM cell payload scrambling enabled   |
| CellType(2:0)    | 6:4  | R/W    | 000     | Payload byte control for Idle/unassigned cells:<br>000: Each PL byte is the same (default)<br>001: Increment PL byte for each ATM cell, start with default after reset; e.g., payload bytes of a cell are all set to M, the payload bytes of the next cell are all set to M+1, etc.<br>010: Increment each PL byte of a cell, start each cell with default byte.<br>011: Increment each PL byte of a cell, cross cell boundaries, start first cell after reset with default byte.<br>1xx: Each PL byte is the same. |
| Reserved         | 7    |        |         | Not used  |

### 35.7: HT1Conf10:HECOFFSET [0D51 H]

HEC offset pattern register for byte pattern used in ATM cell header HEC calculation as base offset according to [I.432].

| Signal Name    | Bits | Access | Default  | Description        |
|----------------|------|--------|----------|--------------------|
| HECOFFSET(7:0) | 7:0  | R/W    | 01010101 | HEC offset pattern |

### 35.8: HT1Conf11:HECMASKAND [0D52 H]

HEC mask pattern register for the byte pattern used in the ATM cell header HEC calculation as dedicated (ANDing) HEC error corruption mask.

| Signal Name     | Bits | Access | Default  | Description                     |
|-----------------|------|--------|----------|---------------------------------|
| HECMASKAND(7:0) | 7:0  | R/W    | 11111111 | HEC error corruption mask (AND) |

### 35.9: HT1Conf12:HECMASKOR [0D53 H]

HEC mask pattern register for the byte pattern used in the ATM cell header HEC calculation as dedicated (ORing) HEC error corruption mask.

| Signal Name    | Bits | Access | Default  | Description                    |
|----------------|------|--------|----------|--------------------------------|
| HECMASKOR(7:0) | 7:0  | R/W    | 00000000 | HEC error corruption mask (OR) |



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35.10: HT1Conf14:APSSELECT [0D55 H]

APS select matrix for transmit direction from ACH macros or APS external input port towards SONET/SDH macros (OFPs).

| Signal Name    | Bits | Access | Default | Description   |
|----------------|------|--------|---------|---|
| APSSELECT(5:0) | 5:0  | R/W    | 111111  | APS bridged:<br>000000: OFP #1: Source is ACH #2<br>000001: OFP #1: Source is ACH #3<br>000010: OFP #1: Source is ACH #4<br>000011: OFP #1: Source is APS external input port<br>000100: OFP #2: Source is ACH #1<br>000101: OFP #2: Source is ACH #3<br>000110: OFP #2: Source is ACH #4<br>000111: OFP #2: Source is APS external input port<br>001000: OFP #3: Source is ACH #1<br>001001: OFP #3: Source is ACH #2<br>001010: OFP #3: Source is ACH #4<br>001011: OFP #3: Source is APS external input port<br>001100: OFP #4: Source is ACH #1<br>001101: OFP #4: Source is ACH #2<br>001110: OFP #4: Source is ACH #3<br>001111: OFP #4: Source is APS external input port<br>010000: APS out: Source is ACH #1<br>010001: APS out: Source is ACH #2<br>010010: APS out: Source is ACH #3<br>010011: APS out: Source is ACH #4<br><br>APS switched:<br>010100: OFP #1: Source is ACH #2<br>010101: OFP #1: Source is ACH #3<br>010110: OFP #1: Source is ACH #4<br>010111: OFP #1: Source is APS external input port<br>011000: OFP #2: Source is ACH #1<br>011001: OFP #2: Source is ACH #3<br>011010: OFP #2: Source is ACH #4<br>011011: OFP #2: Source is APS external input port<br>011100: OFP #3: Source is ACH #1<br>011101: OFP #3: Source is ACH #2<br>011110: OFP #3: Source is ACH #4<br>011111: OFP #3: Source is APS external input port<br>100000: OFP #4: Source is ACH #1<br>100001: OFP #4: Source is ACH #2<br>100010: OFP #4: Source is ACH #3<br>100011: OFP #4: Source is APS external input port<br>100100: APS out: Source is ACH #1<br>100101: APS out: Source is ACH #2<br>100110: APS out: Source is ACH #3<br>100111: APS out: Source is ACH #4<br><br>101xxx: No APS activated, select macros 1:1<br>11xxxx: No APS activated, select macros 1:1 (default) |
| Reserved       | 7:6  |        |         | Not used  |

**35.11: HT1Conf15:APSCONF [0D56 H]**

APS parity processing control register.

| Signal Name | Bits | Access | Default | Description  |
|-------------|------|--------|---------|--|
| ApsOPaEn    | 0    | R/W    | 0       | APS external output parity control:<br>0: Parity generation disabled<br>1: Parity generation enabled |
| ApsOPaOdd   | 1    | R/W    | 0       | APS external output parity mode:<br>0: Even parity<br>1: Odd parity                                  |
| ApsIPaEn    | 2    | R/W    | 0       | APS external input parity control:<br>0: Parity checking disabled<br>1: Parity checking enabled      |
| ApsIPaOdd   | 3    | R/W    | 0       | APS external input parity mode:<br>0: Even parity<br>1: Odd parity                                   |
| Reserved    | 7:4  |        |         | Not used   |

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**ACH\_Tx2/3/4 Chiplet Address Map** Base Address: ACH\_Tx2 0E00 H, ACH\_Tx3 0F00 H, ACH\_Tx4 1000 H

| Register Name <sup>1</sup> | Address Offset (Hex) | Type/Width | Initial Value (Binary) | Description  | See Page |
|----------------------------|----------------------|------------|------------------------|--|----------|
| HT#ROFmid                  | 0                    | F 8        | 00000000               | Read-on-the-fly register (MidSB)                             | 191      |
| HT#ROFhi                   | 1                    | F 8        | 00000000               | Read-on-the-fly register (MSB)                               | 191      |
| HT#CntEn1                  | 2                    | X 2        | 00                     | COUNT ENABLE register  | 191      |
| HT#Cnt1:ACBC               | 4/5                  | N 24       | 000000 H               | LS byte of 24-bit ACB cell counter, no threshold             | 191      |
| HT#Cnt2:IUC                | 6/7                  | N 24       | 000000 H               | LS byte of 24-bit idle/unassigned cell counter, no threshold | 191      |
| HT#RESET                   | 30                   | R 1        | 1                      | Default RESET register                                       | 192      |
| HT#Stat1                   | 33                   | S 6        |                        | Status register #1   | 192      |
| HT#Stat2                   | 34                   | S 4        |                        | Status register #2   | 192      |
| HT#MainIRQ                 | 38                   | I 2        |                        | MAIN INTerrupt register                                      | 184      |
| HT#M_MainIRQ               | 39                   | X 2        | 00                     | INT MASK register (for HT#MainIRQ)                           | 184      |
| HT#CntIRQ1                 | 3A                   | I 2        |                        | COUNTER INTerrupt register                                   | 184      |
| HT#M_CntIRQ1               | 3B                   | X 2        | 00                     | INT MASK register (for HT#CntIRQ1)                           | 184      |
| HT#Conf1:<br>CELLTENABLE   | 48                   | C 4        | 1111                   | Chiplet configuration register                               | 194      |
| HT#Conf2:<br>ACBTXHPAE     | 49                   | C 7        | 0011011                | Programmable Almost Empty threshold                          | 194      |
| HT#Conf3:<br>HEADERBYTE1   | 4A                   | C 8        | 00000000               | IU-cell header byte 1, defaults according to [I.432]         | 195      |
| HT#Conf4:<br>HEADERBYTE2   | 4B                   | C 8        | 00000000               | IU-cell header byte 2, defaults according to [I.432]         |          |
| HT#Conf5:<br>HEADERBYTE3   | 4C                   | C 8        | 00000000               | IU-cell header byte 3, defaults according to [I.432]         |          |
| HT#Conf6:<br>HEADERBYTE4   | 4D                   | C 8        | 00000001               | IU-cell header byte 4, defaults according to [I.432]         |          |
| HT#Conf7:<br>HEADERBYTE5   | 4E                   | C 8        | 01010010               | IU-cell header byte 5, defaults according to [I.432]         |          |
| HT#Conf8:<br>PAYLOADBYTE   | 4F                   | C 8        | 01101010               | IU-cell payload byte   | 195      |
| HT#Conf9:<br>HECENCTRL     | 50                   | C 7        | 0001100                | HEC processing control                                       | 195      |
| HT#Conf10:<br>HECOFFSET    | 51                   | C 8        | 01010101               | HEC offset (i.e., coset) pattern register                    | 196      |
| HT#Conf11:<br>HECMASKAND   | 52                   | C 8        | 11111111               | HEC error corruption mask (AND)                              | 196      |
| HT#Conf12:<br>HECMASKOR    | 53                   | C 8        | 00000000               | HEC error corruption mask (OR)                               | 196      |
| HT#Conf13:<br>SDBTXHPAF    | 54                   | C 6        | 010011                 | Programmable Almost Full threshold                           | 194      |

1. # = The specific transmit direction ATM handler: 2, 3, or 4.

## ACH\_Tx (HT2/3/4) Counters

### 36.1: HT#ROFmid [0E00 H, 0F00 H, 1000 H]

Read-on-the-fly register.

| Signal Name    | Bits | Access | Default  | Description                      |
|----------------|------|--------|----------|----------------------------------|
| HT#ROFmid(7:0) | 7:0  | R      | 00000000 | Read-on-the-fly register (MidSB) |

### 36.2: HT#ROFhi [0E01 H, 0F01 H, 1001 H]

Read-on-the-fly register.

| Signal Name   | Bits | Access | Default  | Description                    |
|---------------|------|--------|----------|--------------------------------|
| HT#ROFhi(7:0) | 7:0  | R      | 00000000 | Read-on-the-fly register (MSB) |

### 36.3: HT#Cnt1:ACBC [0E04 H / 0E05 H, 0F04 H / 0F05 H, 1004 H / 1005 H]

Number of cells transmitted from the ATM Cell Buffer (ACB\_Tx2/3/4). Counter overflow leads to an interrupt request.

| Signal Name | Bits | Access | Default  | Description            |
|-------------|------|--------|----------|------------------------|
| ACBC(7:0)   | 7:0  | R      | 00000000 | ACB cell counter (LSB) |

### 36.4: HT#Cnt2:IUC [0E06 H / 0E07 H, 0F06 H / 0F07 H, 1006 H / 1007 H]

Number of transmitted Idle and Unassigned cells. Counter overflow leads to an interrupt request.

| Signal Name | Bits | Access | Default  | Description                        |
|-------------|------|--------|----------|------------------------------------|
| IUC(7:0)    | 7:0  | R      | 00000000 | Idle/unassigned cell counter (LSB) |

### 36.5: HT#CntEn1 [0E02 H, 0F02 H, 1002 H]

Counter On/Off control register for ACH\_Tx2/3/4 and ACB\_Tx2/3/4.

For each bit position: 0: Counter is disabled

1: Counter is enabled

| Signal Name | Bits | Access | Default | Description                         |
|-------------|------|--------|---------|-------------------------------------|
| EN-ACBC     | 0    | R/W    | 0       | ACB cell counter enable             |
| EN-IUC      | 1    | R/W    | 0       | Idle/unassigned cell counter enable |
| Reserved    | 7:2  |        |         | Not used                            |

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**ACH\_Tx (HT2/3/4) Reset and Status Registers**
**37.1: HT#RESET [0E30 H, 0F30 H, 1030H]**

Reset chiplet control registers. These registers are automatically preset to the default value by the reset signals ResHT2/3/4 from the GPPINT.

For each bit position: 0: Reset not active

1: Reset active

| Signal Name | Bits | Access | Default | Description                         |
|-------------|------|--------|---------|-------------------------------------|
| Reset       | 0    | R/W    | 1       | Reset (disable) ACH_Tx2/3/4 chiplet |
| Reserved    | 7:1  |        |         | Not used                            |

**37.2: HT#Stat1 [0E33 H, 0F33 H, 1033 H]**

Status register #1 of this chiplet. The bits of this register are event latches.

| Signal Name | Bits | Access | Default | Description                                 |
|-------------|------|--------|---------|---|
| SocMiss     | 0    | R/W    |         | Missed start of cell event                  |
| sdbtxFF     | 1    | R/W    |         | FIFO Full flag from SDB_Tx#                 |
| TxLpB1Fe    | 2    | R/W    |         | Transmit Loopback #1 configuration mismatch |
| TxLpB2Fe    | 3    | R/W    |         | Transmit Loopback #2 configuration mismatch |
| RxLpB2Fe    | 4    | R/W    |         | Receive Loopback #2 configuration mismatch  |
| IUCFErr     | 5    | R/W    |         | Unexpected state transition in FSM          |
| Reserved    | 7:6  |        |         | Not used                                    |

**37.3: HT#Stat2 [0E34 H, 0F34 H, 1034 H]**

Status register #2 of this chiplet. The bits of this register immediately follow the driving signal.

| Signal Name   | Bits | Access | Default | Description  |
|---------------|------|--------|---------|--|
| acbtxEF       | 0    | R      |         | FIFO Empty flag from ACB_Tx#   |
| acbtPAE       | 1    | R      |         | Programmable Almost Empty flag from ACB_Tx#                          |
| sdbtxPAF      | 2    | R      |         | Programmable Almost Full flag from SDB_Tx#                           |
| cellgenstatus | 3    | R      |         | 0: Idle/unassigned cell is transmitted<br>1: ACB cell is transmitted |
| Reserved      | 7:4  |        |         | Not used   |

## ACH\_Tx (HT2/3/4) Interrupt Request and Mask Registers

### 38.1: HT#MainIRQ [0E38 H, 0F38 H, 1038 H]

Register to indicate fatal interrupt events and to point to user IRQ registers with active requests.

For each bit position: 0: No interrupt request pending  
1: Interrupt request pending

### 38.2: HT#M\_MainIRQ [0E39 H, 0F39 H, 1039 H]

Register to mask pending interrupt requests. A masked request will not generate an outgoing IRQ to the GPPINT.

For each bit position: 0: The corresponding pending request bit is masked (DEFAULT)  
1: The corresponding pending request bit activates signal IRQHT2/3/4 to GPPINT

| Signal Name | Bits | Access | Default | Description                           |
|-------------|------|--------|---------|---------------------------------------|
| Fatal       | 0    | R/W    | 0       | Fatal event occurred                  |
| CntIRQ1     | 1    | R/W    | 0       | Active request in HT#CntIRQ1 register |
| Reserved    | 7:2  |        |         | Not used                              |

### 38.3: HT#CntIRQ1 [0E3A H, 0F3A H, 103A H]

Register to indicate active counter interrupt requests of this chiplet.

For each bit position: 0: No interrupt request pending  
1: Interrupt request pending

### 38.4: HT#M\_CntIRQ1 [0E3B H, 0F3B H, 103B H]

Register to mask pending counter interrupt requests.

For each bit position: 0: The corresponding pending request bit is masked (DEFAULT)  
1: The corresponding pending request bit activates the pointer bit in HT#MainIRQ register

| Signal Name | Bits | Access | Default | Description                           |
|-------------|------|--------|---------|---------------------------------------|
| OV-ACBC     | 0    | R/W    | 0       | Overflow ACB cell counter             |
| OV-IUC      | 1    | R/W    | 0       | Overflow idle/unassigned cell counter |
| Reserved    | 7:2  |        |         | Not used                              |



**39.4: HT#Conf3-7:HEADERBYTE1/2/3/4/5 [0E4A H, 0F4A H, 104A H; 0E4B H, 0F4B H, 104B H; 0E4C H, 0F4C H, 104C H; 0E4D H, 0F4D H, 104D H; 0E4E H, 0F4E H, 104E H]**

Idle/unassigned cell header bytes, default pattern according to [1.432].

| Signal Name      | Bits | Access | Default  | Description            |
|------------------|------|--------|----------|------------------------|
| HEADERBYTE1(7:0) | 7:0  | R/W    | 00000000 | IU-cell header byte #1 |
| HEADERBYTE2(7:0) | 7:0  | R/W    | 00000000 | IU-cell header byte #2 |
| HEADERBYTE3(7:0) | 7:0  | R/W    | 00000000 | IU-cell header byte #3 |
| HEADERBYTE4(7:0) | 7:0  | R/W    | 00000001 | IU-cell header byte #4 |
| HEADERBYTE5(7:0) | 7:0  | R/W    | 01010010 | IU-cell header byte #5 |

**39.5: HT#Conf8:PAYLOADBYTE [0E4F H, 0F4F H, 104F H]**

Idle/Unassigned cell payload byte.

| Signal Name      | Bits | Access | Default  | Description          |
|------------------|------|--------|----------|----------------------|
| PAYLOADBYTE(7:0) | 7:0  | R/W    | 01101010 | IU-cell payload byte |

**39.6: HT#Conf9:HECENCTRL [0E50 H, 0F50 H, 1050 H]**

HEC processing control configuration register.

| Signal Name      | Bits | Access | Default | Description  |
|------------------|------|--------|---------|--|
| HECCntIUDF1(1:0) | 1:0  | R/W    | 00      | Mode of final HEC manipulation by the UTOPIA UDF1 byte after HECOffset, HECMaskAND and HECMaskOR operations:<br>00: No manipulation<br>01: HEC XOR UDF1<br>10: HEC AND UDF1<br>11: HEC OR UDF1   |
| HECenable        | 2    | R/W    | 1       | 0: HEC calculation/manipulation disabled<br>1: HEC calculation/manipulation enabled  |
| SCRenable        | 3    | R/W    | 1       | 0: ATM cell payload scrambling disabled<br>1: ATM cell payload scrambling enabled  |
| CellType(2:0)    | 6:4  | R/W    | 000     | Payload byte control for Idle/Unassigned Cells:<br>000: Each PL byte is the same (default)<br>001: Increment PL byte for each ATM cell, start with default after reset<br>010: Increment each PL byte of a cell, start each cell with default byte<br>011: Increment each PL byte of a cell, cross cell boundaries, start first cell after reset with default byte<br>1xx: Each PL byte is the same. |
| Reserved         | 7    |        |         | Not used   |

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**39.7: HT#Conf10:HECOFFSET [0E51 H, 0F51 H, 1051 H]**

HEC offset pattern register for the byte pattern used in the ATM cell header HEC calculation as base offset according to [I.432].

| Signal Name    | Bits | Access | Default  | Description  |
|----------------|------|--------|----------|--|
| HECOFFSET(7:0) | 7:0  | R/W    | 01010101 | HEC offset (i.e., coset) pattern. Setting this register to 00 H has the effect of disabling the coset operation in the transmit direction. |

**39.8: HT#Conf11:HECMASKAND [0E52 H, 0F52 H, 1052 H]**

HEC mask pattern register for the byte pattern used in the ATM cell header HEC calculation as dedicated (ANDing) HEC error corruption mask.

| Signal Name     | Bits | Access | Default  | Description                     |
|-----------------|------|--------|----------|---------------------------------|
| HECMASKAND(7:0) | 7:0  | R/W    | 11111111 | HEC error corruption mask (AND) |

**39.9: HT#Conf12:HECMASKOR [0E53 H, 0F53 H, 1053 H]**

HEC mask pattern register for the byte pattern used in the ATM cell header HEC calculation as dedicated (ORing) HEC error corruption mask.

| Signal Name    | Bits | Access | Default  | Description                    |
|----------------|------|--------|----------|--------------------------------|
| HECMASKOR(7:0) | 7:0  | R/W    | 00000000 | HEC error corruption mask (OR) |

**ACH\_Rx1 Chiplet Address Map** Base Address 1100 H

| Register Name  | Address Offset (Hex) | Type/Width | Initial Value (Binary) | Description   | See Page |
|----------------|----------------------|------------|------------------------|---|----------|
| HR1ROFmid      | 0                    | F 8        | 00000000               | Read-on-the-fly register (MidSB)  | 198      |
| HR1ROFhi       | 1                    | F 8        | 00000000               | Read-on-the-fly register (MSB)  | 198      |
| HR1CntEn1      | 2                    | X 5        | 00000                  | COUNT ENABLE register   | 200      |
| HR1Cnt1:FHR    | 4/5                  | N 24       | 000000 H               | LS byte of 24-bit counter, ATM cells received from OFP, no threshold                              | 198      |
| HR1Cnt2:IHR    | 6/7                  | N 24       | 000000 H               | LS byte of 24-bit counter, received Idle cells from OFP, no threshold                             | 198      |
| HR1Cnt3:EHR1   | 8/9                  | N 16       | 0000 H                 | LS byte of 16-bit counter, uncorrected HEC errors with threshold                                  | 198      |
| HR1Th32:EHR1T2 | A                    | X 8        | 00000001               | Threshold register Byte 2 (LSB) for counter EHR1  | 199      |
| HR1Th31:EHR1T1 | B                    | X 8        | 10000000               | Threshold register Byte 1 for counter EHR1  | 198      |
| HR1Cnt4:EHR2   | C/D                  | N 16       | 0000 H                 | LS byte of 16-bit counter, corrected HEC errors with threshold                                    | 199      |
| HR1Th42:EHR2T2 | E                    | X 8        | 00000001               | Threshold register Byte 2 (LSB) for counter EHR2  | 199      |
| HR1Th41:EHR2T1 | F                    | X 8        | 10000000               | Threshold register Byte 1 for counter EHR2  | 199      |
| HR1Cnt5:BHR    | 10/11                | N 16       | 0000 H                 | LS byte of 16-bit counter, FIFO full discarded cells: (DiscPAF1=1) AND (TxLpB11=0) with threshold | 199      |
| HR1Th52:BHRTh2 | 12                   | X 8        | 00000001               | Threshold register Byte 2 (LSB) for counter BHR   | 200      |
| HR1Th51:BHRTh1 | 13                   | X 8        | 10000000               | Threshold register Byte 1 for counter BHR   | 199      |
| HR1RESET       | 30                   | R 1        | 1                      | Default RESET register  | 201      |
| HR1Stat1       | 33                   | S 3        |                        | Status register #1 (event latch)  | 201      |
| HR1Stat2       | 34                   | S 5        |                        | Status register #2 (static)   | 201      |
| HR1MainIRQ     | 38                   | I 2        |                        | MAIN INTerrupt register   | 202      |
| HR1M_MainIRQ   | 39                   | X 2        | 00                     | INT MASK register (for HR1MainIRQ)  | 202      |
| HR1CntIRQ1     | 3A                   | I 8        |                        | COUNTER INTerrupt register  | 202      |
| HR1M_CntIRQ1   | 3B                   | X 8        | 00000000               | INT MASK register (for HRCntIRQ1)   | 202      |
| HR1Conf1       | 48                   | C 2        | 11                     | Chiplet configuration register #1   | 203      |
| HR1Conf2       | 49                   | C 8        | 00000000               | Chiplet configuration register #2   | 203      |
| HR1Conf3       | 4A                   | C 8        | 01110110               | Chiplet configuration register (Alpha/Delta)  | 204      |
| HR1Conf4:ICU1  | 4B                   | C 8        | 00000000               | Configuration bytes to identify idle or unassigned cells  | 204      |
| HR1Conf5:ICU2  | 4C                   | C 8        | 00000000               | Configuration bytes to identify idle or unassigned cells  | 204      |
| HR1Conf6:ICU3  | 4D                   | C 8        | 00000000               | Configuration bytes to identify idle or unassigned cells  | 204      |
| HR1Conf7:ICU4  | 4E                   | C 8        | 00000001               | Configuration bytes to identify idle or unassigned cells  | 204      |
| HR1Conf8:MODU  | 4F                   | C 8        | 01010101               | HEC modulo pattern  | 204      |
| HR1Conf9:PL    | 50                   | C 8        | 11010000               | Dummy byte to align Payload in ACB_Rx1  | 204      |
| HR1Conf10:PAFT | 51                   | C 7        | 1100000                | ACB buffer Almost Full Threshold  | 204      |
| HR1Conf11      | 52                   | C 5        | 11111                  | APS select matrix (receive direction)   | 205      |
| HR1Conf12      | 53                   | C 4        | 0000                   | APS parity handling (receive direction)   | 206      |

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**ACH\_Rx1 (HR1) Counters**
**40.1: HR1ROFmid [1100 H]**

Read-on-the-fly register.

| Signal Name    | Bits | Access | Default  | Description                      |
|----------------|------|--------|----------|----------------------------------|
| HR1ROFmid(7:0) | 7:0  | R      | 00000000 | Read-on-the-fly register (MidSB) |

**40.2: HR1ROFhi [1101 H]**

Read-on-the-fly register.

| Signal Name   | Bits | Access | Default  | Description                    |
|---------------|------|--------|----------|--------------------------------|
| HR1ROFhi(7:0) | 7:0  | R      | 00000000 | Read-on-the-fly register (MSB) |

**40.3: HR1Cnt1:FHR [1104 H / 1105 H]**

Number of ATM cells received from OFP\_Rx. Counter overflow leads to an interrupt request.

| Signal Name | Bits | Access | Default  | Description            |
|-------------|------|--------|----------|------------------------|
| FHR(7:0)    | 7:0  | R      | 00000000 | ATM cell counter (LSB) |

**40.4: HR1Cnt2:IHR [1106 H / 1107 H]**

Number of Idle cells received from OFP\_Rx. Counter overflow leads to an interrupt request.

| Signal Name | Bits | Access | Default  | Description             |
|-------------|------|--------|----------|-------------------------|
| IHR(7:0)    | 7:0  | R      | 00000000 | Idle cell counter (LSB) |

**40.5: HR1Cnt3:EHR1 [1108 H / 1109 H]**

Number of uncorrected HEC errors. Counter overflow leads to an interrupt request.

| Signal Name | Bits | Access | Default  | Description                         |
|-------------|------|--------|----------|-------------------------------------|
| EHR1(7:0)   | 7:0  | R      | 00000000 | Uncorrected HEC error counter (LSB) |

**40.6: HR1Th31:EHR1T1 [110B H]**

Threshold for number of uncorrected HEC errors (MSB).

| Signal Name | Bits | Access | Default  | Description                                       |
|-------------|------|--------|----------|---|
| EHR1T1(7:0) | 7:0  | R/W    | 10000000 | Threshold for uncorrected HEC error counter (MSB) |

#### 40.7: HR1Th32:EHR1T2 [110A H]

Threshold for number of uncorrected HEC errors (LSB). Threshold overstep leads to an interrupt request.

| Signal Name | Bits | Access | Default  | Description                                     |
|-------------|------|--------|----------|---|
| EHR1T2(7:0) | 7:0  | R/W    | 00000001 | Threshold for uncorrected HEC error count (LSB) |

#### 40.8: HR1Cnt4:EHR2 [110C H / 110D H]

Number of corrected HEC errors. Counter overflow leads to an interrupt request.

| Signal Name | Bits | Access | Default  | Description                       |
|-------------|------|--------|----------|-----------------------------------|
| EHR2(7:0)   | 7:0  | R      | 00000000 | Corrected HEC error counter (LSB) |

#### 40.9: HR1Th41:EHR2T1 [110F H]

Threshold for number of corrected HEC errors (MSB).

| Signal Name | Bits | Access | Default  | Description                                   |
|-------------|------|--------|----------|---|
| EHR2T1(7:0) | 7:0  | R/W    | 10000000 | Threshold for corrected HEC error count (MSB) |

#### 40.10: HR1Th42:EHR2T2 [110E H]

Threshold for number of corrected HEC errors (LSB). Threshold overstep leads to an interrupt request.

| Signal Name | Bits | Access | Default  | Description                                   |
|-------------|------|--------|----------|---|
| EHR2T2(7:0) | 7:0  | R/W    | 00000001 | Threshold for corrected HEC error count (LSB) |

#### 40.11: HR1Cnt5:BHR [1110 H / 1111 H]

Number of discarded cells because of FIFO full condition. Counter overflow leads to an interrupt request.

| Signal Name | Bits | Access | Default  | Description                  |
|-------------|------|--------|----------|------------------------------|
| BHR(7:0)    | 7:0  | R      | 00000000 | Discarded cell counter (LSB) |

#### 40.12: HR1Th51:BHRTh1 [1113 H]

Threshold for number of discarded cells (MSB).

| Signal Name | Bits | Access | Default  | Description                                |
|-------------|------|--------|----------|--|
| BHRTh1(7:0) | 7:0  | R/W    | 10000000 | Threshold for discarded cell counter (MSB) |

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**40.13: HR1Th52:BHRTh2 [1112 H]**

Threshold for number of discarded cells (LSB). Threshold overstep leads to an interrupt request.

| Signal Name | Bits | Access | Default  | Description                                |
|-------------|------|--------|----------|--|
| BHRTh2(7:0) | 7:0  | R/W    | 00000001 | Threshold for discarded cell counter (LSB) |

**40.14: HR1CntEn1 [1102 H]**

Counter On/Off control register for ACH\_Rx1/ACB\_Rx1.

For each bit position: 0: Counter is disabled

1: Counter is enabled

| Signal Name | Bits | Access | Default | Description                          |
|-------------|------|--------|---------|--------------------------------------|
| EN-FHR      | 0    | R/W    | 0       | ATM cell counter enable              |
| EN-IHR      | 1    | R/W    | 0       | Idle cell counter enable             |
| EN-EHR1     | 2    | R/W    | 0       | Uncorrected HEC error counter enable |
| EN-EHR2     | 3    | R/W    | 0       | Corrected HEC error counter enable   |
| EN-BHR      | 4    | R/W    | 0       | Discarded cell counter enable        |
| Reserved    | 7:5  |        |         | Not used                             |

## ACH\_Rx1 (HR1) Reset and Status Registers

### 41.1: HR1RESET [1130 H]

Reset chiplet control register. This register is automatically preset to the default value by the reset signal ResHR1 from the GPPINT.

For each bit position: 0: Reset not active  
1: Reset active

| Signal Name | Bits | Access | Default | Description                     |
|-------------|------|--------|---------|---------------------------------|
| Reset       | 0    | R/W    | 1       | Reset (disable) ACH_Rx1 chiplet |
| Reserved    | 7:1  |        |         | Not used                        |

### 41.2: HR1Stat1 [1133 H]

Status register #1 of this chiplet. The bits of this register are event latches.

| Signal Name | Bits | Access | Default | Description  |
|-------------|------|--------|---------|--|
| APSParEr    | 0    | R/W    |         | 0: No APS parity error was detected<br>1: At least one parity error was detected |
| SyncHunt    | 1    | R/W    |         | 0: FSM still in Sync state<br>1: FSM returned from Sync to Hunt state            |
| WrFlagFF    | 2    | R/W    |         | 0: ACB FIFO did not raise the Full flag<br>1: ACB FIFO did raise the Full flag   |
| Reserved    | 7:3  |        |         | Not used   |

### 41.3: HR1Stat2 [1134 H]

Status register #2 of this chiplet. The bits of this register are static latches that follow the driving signal immediately.

| Signal Name  | Bits | Access | Default | Description  |
|--------------|------|--------|---------|--|
| CellDel(2:0) | 2:0  | R      |         | State of the cell delineation process:<br>000: Reset state<br>001: Hunt state<br>010: Presync state<br>100: Sync state |
| WrFlagPAF    | 3    | R      |         | 0: ACB FIFO is currently not almost full<br>1: ACB FIFO is currently almost full                                       |
| RdFlagEF     | 4    | R      |         | 0: SDB FIFO is currently not empty<br>1: SDB FIFO is currently empty   |
| Reserved     | 7:5  |        |         | Not used   |

## ACH\_Rx1 Interrupt Request and Mask Registers

### 42.1: HR1MainIRQ [1138 H]

Register to indicate fatal interrupt events and to point to user IRQ registers with active requests.

For each bit position: 0: No interrupt request pending  
1: Interrupt request pending

### 42.2: HR1M\_MainIRQ [1139 H]

Register to mask pending interrupt requests. A masked request will not generate an outgoing IRQ to the GPPINT.

For each bit position: 0: The corresponding pending request bit is masked (DEFAULT)  
1: The corresponding pending request bit activates signal IRQHR1 to GPPINT

| Signal Name | Bits | Access | Default | Description                           |
|-------------|------|--------|---------|---------------------------------------|
| Fatal       | 0    | R/W    | 0       | Fatal event occurred                  |
| CntIRQ1     | 1    | R/W    | 0       | Active request in HR1CntIRQ1 register |
| Reserved    | 7:2  |        |         | Not used                              |

### 42.3: HR1CntIRQ1 [113A H]

Register to indicate active counter interrupt requests of this chiplet.

For each bit position: 0: No interrupt request pending  
1: Interrupt request pending

### 42.4: HR1M\_CntIRQ1 [113B H]

Register to mask pending counter interrupt requests.

For each bit position: 0: The corresponding pending request bit is masked (DEFAULT)  
1: The corresponding pending request bit activates the pointer bit in HR1MainIRQ register

| Signal Name | Bits | Access | Default | Description                               |
|-------------|------|--------|---------|---|
| OV-FHR      | 0    | R/W    | 0       | Overflow ATM cell counter                 |
| OV-IHR      | 1    | R/W    | 0       | Overflow idle cell counter                |
| OV-EHR1     | 2    | R/W    | 0       | Overflow HEC error counter #1             |
| TH-EHR1     | 3    | R/W    | 0       | Threshold overstep HEC error counter #1   |
| OV-EHR2     | 4    | R/W    | 0       | Overflow HEC error counter #2             |
| TH-EHR2     | 5    | R/W    | 0       | Threshold overstep HEC error counter #2   |
| OV-BHR      | 6    | R/W    | 0       | Overflow discarded cell counter           |
| TH-BHR      | 7    | R/W    | 0       | Threshold overstep discarded cell counter |

## ACH\_Rx1 Configuration Registers

### 43.1: HR1Conf1 [1148 H]

Register to control auto-resetting of bits upon read access.

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| AutRst_Int  | 0    | R/W    | 1       | 0: No action on read access<br>1: Auto-reset interrupt request registers upon read access<br>Regardless of the setting of this bit, individual interrupt request bits can be cleared by writing a '1' to that bit provided that the corresponding alarm condition is removed. |
| AutRst_Sta  | 1    | R/W    | 1       | 0: No action on read access<br>1: Auto-reset all bits in the HR1Stat1 status register upon read access  |
| Reserved    | 7:2  |        |         | Not used  |

### 43.2: HR1Conf2 [1149 H]

Register to control the HEC correction modes of this chiplet.

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| CorModeHi   | 0    | R/W    | 0       | 0: FSM returns into detection mode after HEC error correction<br>1: FSM stays in correction mode until the Sync state is left |
| NCorHECEr   | 1    | R/W    | 0       | 0: Single-bit HEC errors are corrected<br>1: Single-bit HEC errors are not corrected  |
| WrIdleC     | 2    | R/W    | 0       | 0: Do not write Idle cell into ACB FIFO<br>1: Write Idle cell into ACB FIFO   |
| Ndescramb   | 3    | R/W    | 0       | 0: Descramble ATM cell payload<br>1: Do not descramble ATM cell payload   |
| WrtCHecEr   | 4    | R/W    | 0       | 0: Do not write ATM cell with HEC errors<br>1: Write ATM cell with HEC errors   |
| NotDetHecEr | 5    | R/W    | 0       | 0: Detect ATM cell with HEC error<br>1: Do not detect ATM cell with HEC error   |
| NWrToFifo   | 6    | R/W    | 0       | 0: Write into ACB FIFO<br>1: Do not write into ACB FIFO; all received cells are discarded                                     |
| DetStartOC  | 7    | R/W    | 0       | 0: Do not detect start of cell<br>1: Detect start of cell   |



**43.8: HR1Conf11 [1152 H]**

APS select matrix for receive direction from SONET/SDH macros or APS external input port towards ACH.

| Signal Name    | Bits | Access | Default | Description   |
|----------------|------|--------|---------|---|
| ApsSource(4:0) | 4:0  | R/W    | 11111   | 00000: ACH #1: Source is SONET/SDH macro #2<br>00001: ACH #1: Source is SONET/SDH macro #3<br>00010: ACH #1: Source is SONET/SDH macro #4<br>00011: ACH #1: Source is APS external input port<br>00100: ACH #2: Source is SONET/SDH macro #1<br>00101: ACH #2: Source is SONET/SDH macro #3<br>00110: ACH #2: Source is SONET/SDH macro #4<br>00111: ACH #2: Source is APS external input port<br>01000: ACH #3: Source is SONET/SDH macro #1<br>01001: ACH #3: Source is SONET/SDH macro #2<br>01010: ACH #3: Source is SONET/SDH macro #4<br>01011: ACH #3: Source is APS external input port<br>01100: ACH #4: Source is SONET/SDH macro #1<br>01101: ACH #4: Source is SONET/SDH macro #2<br>01110: ACH #4: Source is SONET/SDH macro #3<br>01111: ACH #4: Source is APS external input port<br>10000: APS out: Source is SDH macro # 1<br>10001: APS out: Source is SDH macro # 2<br>10010: APS out: Source is SDH macro # 3<br>10011: APS out: Source is SDH macro # 4<br>10100: ACH #1: Source is SONET/SDH macro #2<br>10100: ACH #2: not switched, not used<br>10100: ACH #3: Source is SONET/SDH macro #4<br>10100: ACH #4: not switched, not used<br>10101: ACH #1: not switched, not used<br>10101: ACH #2: Source is SONET/SDH macro #1<br>10101: ACH #3: Source is SONET/SDH macro #4<br>10101: ACH #4: not switched, not used<br>10110: ACH #1: Source is SONET/SDH macro #2<br>10110: ACH #2: not switched, not used<br>10110: ACH #3: not switched, not used<br>10110: ACH #4: Source is SONET/SDH macro #3<br>10111: ACH #1: not switched, not used<br>10111: ACH #2: Source is SONET/SDH macro #1<br>10111: ACH #3: not switched, not used<br>10111: ACH #4: Source is SONET/SDH macro #3<br>11xxx: No APS is activated, select macros 1:1 (transparent) |
| Reserved       | 7:5  |        |         | Not used  |

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**43.9: HR1Conf12 [1153 H]**

Controls APS parity handling (receive direction).

| Signal Name | Bits | Access | Default | Description  |
|-------------|------|--------|---------|--|
| ApsOPaEn    | 0    | R/W    | 0       | APS external output parity control:<br>0: Parity generation disabled<br>1: Parity generation enabled |
| ApsOPaOdd   | 1    | R/W    | 0       | APS external output parity:<br>0: Even parity<br>1: Odd parity                                       |
| ApsIPaEn    | 2    | R/W    | 0       | APS external input parity control:<br>0: Parity checking disabled<br>1: Parity checking enabled      |
| ApsIPaOdd   | 3    | R/W    | 0       | APS external input parity:<br>0: Even parity<br>1: Odd parity  |
| Reserved    | 7:4  | R/W    |         | Not used   |



### ACH\_Rx2/3/4 Chiplet Address Map

Base Address: ACH\_Rx2 1200 H, ACH\_Rx3 1300 H,  
ACH\_Rx4 1400 H

| Register Name  | Address Offset (Hex) | Type/Width | Initial Value (Binary) | Description   | See Page |
|----------------|----------------------|------------|------------------------|---|----------|
| HR#ROFmid      | 0                    | F 8        | 00000000               | Read-on-the-fly register (MidSB)  | 208      |
| HR#ROFhi       | 1                    | F 8        | 00000000               | Read-on-the-fly register (MSB)  | 208      |
| HR#CntEn1      | 2                    | X 5        | 00000                  | COUNT ENABLE register   | 210      |
| HR#Cnt1:FHR    | 4/5                  | N 24       | 000000 H               | LS byte of 24-bit counter, ATM cells received from OFF, no threshold                              | 208      |
| HR#Cnt2:IHR    | 6/7                  | N 24       | 000000 H               | LS byte of 24-bit counter, received Idle cells from OFF, no threshold                             | 208      |
| HR#Cnt3:EHR1   | 8/9                  | N 16       | 0000 H                 | LS byte of 16-bit counter, uncorrected HEC errors with threshold                                  | 208      |
| HR#Th32:EHR1T2 | A                    | X 8        | 00000001               | Threshold register Byte2 (LSB) for counter EHR1   | 209      |
| HR#Th31:EHR1T1 | B                    | X 8        | 10000000               | Threshold register Byte1 for counter EHR1   | 208      |
| HR#Cnt4:EHR2   | C/D                  | N 16       | 0000 H                 | LS byte of 16-bit counter, corrected HEC errors with threshold                                    | 209      |
| HR#Th42:EHR2T2 | E                    | X 8        | 00000001               | Threshold register Byte2 (LSB) for counter EHR2   | 209      |
| HR#Th41:EHR2T1 | F                    | X 8        | 10000000               | Threshold register Byte1 for counter EHR2   | 209      |
| HR#Cnt5:BHR    | 10/11                | N 16       | 0000 H                 | LS byte of 16-bit counter, FIFO full discarded cells: (DiscPAF1=1) AND (TxLpB11=0) with threshold | 209      |
| HR#Th52:BHRTh2 | 12                   | X 8        | 00000001               | Threshold register Byte2 (LSB) for counter BHR  | 210      |
| HR#Th51:BHRTh1 | 13                   | X 8        | 10000000               | Threshold register Byte1 for counter BHR  | 209      |
| HR#RESET       | 30                   | R 1        | 1                      | Default RESET register  | 211      |
| HR#Stat1       | 33                   | S 2        |                        | Status register #1 (event latch)  | 211      |
| HR#Stat2       | 34                   | S 5        |                        | Status register #2 (static)   | 211      |
| HR#MainIRQ     | 38                   | I 2        |                        | MAIN INTerrupt register   | 212      |
| HR#M_MainIRQ   | 39                   | X 2        | 00                     | INT MASK register (for MainIRQ)   | 212      |
| HR#CntIRQ1     | 3A                   | I 8        |                        | COUNTER INTerrupt register  | 212      |
| HR#M_CntIRQ1   | 3B                   | X 8        | 00000000               | INT MASK register (for HR#CntIRQ1)  | 212      |
| HR#Conf1       | 48                   | C 2        | 11                     | Chiplet configuration register #1   | 213      |
| HR#Conf2       | 49                   | C 8        | 00000000               | Chiplet configuration register #2   | 213      |
| HR#Conf3       | 4A                   | C 8        | 01110110               | Chiplet configuration register (Alpha/Delta)  | 213      |
| HR#Conf4:ICU1  | 4B                   | C 8        | 00000000               | Configuration bytes to identify idle or unassigned cells  | 214      |
| HR#Conf5:ICU2  | 4C                   | C 8        | 00000000               | Configuration bytes to identify idle or unassigned cells  |          |
| HR#Conf6:ICU3  | 4D                   | C 8        | 00000000               | Configuration bytes to identify idle or unassigned cells  |          |
| HR#Conf7:ICU4  | 4E                   | C 8        | 00000001               | Configuration bytes to identify idle or unassigned cells  |          |
| HR#Conf8:MODU  | 4F                   | C 8        | 01010101               | HEC modulo pattern (i.e., coset)  | 214      |
| HR#Conf9:PL    | 50                   | C 8        | 11010000               | Dummy byte to align Payload in ACB_Rx2/3/4  | 214      |
| HR#Conf10:PAFT | 51                   | C 7        | 1100000                | ACB buffer Almost Full threshold  | 214      |

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**ACH\_Rx2/3/4 (HR2/3/4) Counters**
**44.1: HR#ROFmid [1200 H, 1300 H, 1400 H]**

Read-on-the-fly register.

| Signal Name    | Bits | Access | Default  | Description                      |
|----------------|------|--------|----------|----------------------------------|
| HR#ROFmid(7:0) | 7:0  | R      | 00000000 | Read-on-the-fly register (MidSB) |

**44.2: HR#ROFhi [1201 H, 1301 H, 1401 H]**

Read-on-the-fly register.

| Signal Name   | Bits | Access | Default  | Description                    |
|---------------|------|--------|----------|--------------------------------|
| HR#ROFhi(7:0) | 7:0  | R      | 00000000 | Read-on-the-fly register (MSB) |

**44.3: HR#Cnt1:FHR [1204 H / 1205 H, 1304 H / 1305 H, 1404 H / 1405 H]**

Number of ATM cells received from OFP\_Rx. Counter overflow leads to an interrupt request.

| Signal Name | Bits | Access | Default  | Description            |
|-------------|------|--------|----------|------------------------|
| FHR(7:0)    | 7:0  | R      | 00000000 | ATM cell counter (LSB) |

**44.4: HR#Cnt2:IHR [1206 H / 1207 H, 1306 H / 1307 H, 1406 H / 1407 H]**

Number of Idle cells received from OFP\_Rx. Counter overflow leads to an interrupt request.

| Signal Name | Bits | Access | Default  | Description             |
|-------------|------|--------|----------|-------------------------|
| IHR(7:0)    | 7:0  | R      | 00000000 | Idle cell counter (LSB) |

**44.5: HR#Cnt3:EHR1 [1208 H / 1209 H, 1308 H / 1309 H, 1408 H / 1409 H]**

Number of uncorrected HEC errors. Counter overflow leads to an interrupt request.

| Signal Name | Bits | Access | Default  | Description                         |
|-------------|------|--------|----------|-------------------------------------|
| EHR1(7:0)   | 7:0  | R      | 00000000 | Uncorrected HEC error counter (LSB) |

**44.6: HR#Th31:EHR1T1 [120B H, 130B H, 140B H]**

Threshold for number of uncorrected HEC errors (MSB).

| Signal Name | Bits | Access | Default  | Description                                       |
|-------------|------|--------|----------|---|
| EHR1T1(7:0) | 7:0  | R/W    | 10000000 | Threshold for uncorrected HEC error counter (MSB) |

#### 44.7: HR#Th32:EHR1T2 [120A H, 130A H, 140A H]

Threshold for number of uncorrected HEC errors (LSB). Threshold overstep leads to an interrupt request.

| Signal Name | Bits | Access | Default  | Description                                       |
|-------------|------|--------|----------|---|
| EHR1T2(7:0) | 7:0  | R/W    | 00000001 | Threshold for uncorrected HEC error counter (LSB) |

#### 44.8: HR#Cnt4:EHR2 [120C H / 120D H, 130C H / 130D H, 140C H / 140D H]

Number of corrected HEC errors. Counter overflow leads to an interrupt request.

| Signal Name | Bits | Access | Default  | Description                       |
|-------------|------|--------|----------|-----------------------------------|
| EHR2(7:0)   | 7:0  | R      | 00000000 | Corrected HEC error counter (LSB) |

#### 44.9: HR#Th41:EHR2T1 [120F H, 130F H, 140F H]

Threshold for number of corrected HEC errors (MSB).

| Signal Name | Bits | Access | Default  | Description                                     |
|-------------|------|--------|----------|---|
| EHR2T1(7:0) | 7:0  | R/W    | 10000000 | Threshold for corrected HEC error counter (MSB) |

#### 44.10: HR#Th42:EHR2T2 [120E H, 130E H, 140E H]

Threshold for number of corrected HEC errors (LSB). Threshold overstep leads to an interrupt request.

| Signal Name | Bits | Access | Default  | Description                                     |
|-------------|------|--------|----------|---|
| EHR2T2(7:0) | 7:0  | R/W    | 00000001 | Threshold for corrected HEC error counter (LSB) |

#### 44.11: HR#Cnt5:BHR [1210 H / 1211 H, 1310 H / 1311 H, 1410 H / 1411 H]

Number of discarded cells because of FIFO full condition. Counter overflow leads to an interrupt request.

| Signal Name | Bits | Access | Default  | Description                  |
|-------------|------|--------|----------|------------------------------|
| BHR(7:0)    | 7:0  | R      | 00000000 | Discarded cell counter (LSB) |

#### 44.12: HR#Th51:BHRTh1 [1213 H, 1313 H, 1413 H]

Threshold for number of discarded cells (MSB).

| Signal Name | Bits | Access | Default  | Description                              |
|-------------|------|--------|----------|--|
| BHRTh1(7:0) | 7:0  | R/W    | 10000000 | Threshold for discarded cell count (MSB) |

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**44.13: HR#Th52:BHRTh2 [1212 H, 1312 H, 1412 H]**

Threshold for number of discarded cells (LSB). Threshold overstep leads to an interrupt request.

| Signal Name | Bits | Access | Default  | Description                                |
|-------------|------|--------|----------|--|
| BHRTh2(7:0) | 7:0  | R/W    | 00000001 | Threshold for discarded cell counter (LSB) |

**44.14: HR#CntEn1 [1202 H, 1302 H, 1402 H]**

Counter On/Off control register for ACH\_Rx2/3/4 and ACB\_Rx2/3/4.

For each bit position: 0: Counter is disabled

1: Counter is enabled

| Signal Name | Bits | Access | Default | Description                          |
|-------------|------|--------|---------|--------------------------------------|
| EN-FHR      | 0    | R/W    | 0       | ATM cell counter enable              |
| EN-IHR      | 1    | R/W    | 0       | Idle cell counter enable             |
| EN-EHR1     | 2    | R/W    | 0       | Uncorrected HEC error counter enable |
| EN-EHR2     | 3    | R/W    | 0       | Corrected HEC error counter enable   |
| EN-BHR      | 4    | R/W    | 0       | Discarded cell counter enable        |
| Reserved    | 7:5  |        |         | Not used                             |

## ACH\_Rx2/3/4 (HR2/3/4) Reset and Status Registers

### 45.1: HR#RESET [1230 H, 1330 H, 1430 H]

Reset chiplet control registers. These registers are automatically preset to the default value by the reset signals ResHR2/3/4 from the GPPINT.

For each bit position: 0: Reset not active

1: Reset active

| Signal Name | Bits | Access | Default | Description                         |
|-------------|------|--------|---------|-------------------------------------|
| Reset       | 0    | R/W    | 1       | Reset (disable) ACH_Rx2/3/4 chiplet |
| Reserved    | 7:1  |        |         | Not used                            |

### 45.2: HR#Stat1 [1233 H, 1333 H, 1433 H]

Status register #1 of this chiplet. The bits of this register are event latches.

| Signal Name | Bits | Access | Default | Description  |
|-------------|------|--------|---------|--|
| SyncHunt    | 0    | R/W    |         | 0: FSM still in Sync state<br>1: FSM returned from Sync to Hunt state          |
| WrFlagFF    | 1    | R/W    |         | 0: ACB FIFO did not raise the Full flag<br>1: ACB FIFO did raise the Full flag |
| Reserved    | 7:2  |        |         | Not used   |

### 45.3: HR#Stat2 [1234 H, 1334 H, 1434 H]

Status register #2 of this chiplet. The bits of this register are static latches that follow the driving signal immediately.

| Signal Name  | Bits | Access | Default | Description  |
|--------------|------|--------|---------|--|
| CellDel(2:0) | 2:0  | R      |         | State of the cell delineation process:<br>000: Reset state<br>001: Hunt state<br>010: Presync state<br>100: Sync state |
| WrFlagPAF    | 3    | R      |         | 0: ACB FIFO is currently not almost full<br>1: ACB FIFO is currently almost full                                       |
| RdFlagEF     | 4    | R      |         | 0: SDB FIFO is currently not empty<br>1: SDB FIFO is currently empty   |
| Reserved     | 7:5  |        |         | Not used   |

## ACH\_Rx2/3/4 Interrupt Request and Mask Registers

### 46.1: HR#MainIRQ [1238 H, 1338 H, 1438 H]

Register to indicate fatal interrupt events and to point to user IRQ registers with active requests.

For each bit position: 0: No interrupt request pending  
1: Interrupt request pending

### 46.2: HR#M\_MainIRQ [1239 H, 1339 H, 1439 H]

Register to mask pending interrupt requests. A masked request will not generate an outgoing IRQ to the GPPINT.

For each bit position: 0: The corresponding pending request bit is masked (DEFAULT)  
1: The corresponding pending request bit activates signal IRQHR2/3/4 to GPPINT

| Signal Name | Bits | Access | Default | Description                           |
|-------------|------|--------|---------|---------------------------------------|
| Fatal       | 0    | R/W    | 0       | Fatal event occurred                  |
| CntIRQ1     | 1    | R/W    | 0       | Active request in HR#CntIRQ1 register |
| Reserved    | 7:2  |        |         | Not used                              |

### 46.3: HR#CntIRQ1 [123A H, 133A H, 143A H]

Register to indicate active counter interrupt requests of this chiplet.

For each bit position: 0: No interrupt request pending  
1: Interrupt request pending

### 46.4: HR#M\_CntIRQ1 [123B H, 133B H, 143B H]

Register to mask pending counter interrupt requests.

For each bit position: 0: The corresponding pending request bit is masked (DEFAULT)  
1: The corresponding pending request bit activates the pointer bit in HR#MainIRQ register

| Signal Name | Bits | Access | Default | Description                               |
|-------------|------|--------|---------|---|
| OV-FHR      | 0    | R/W    | 0       | Overflow ATM cell counter                 |
| OV-IHR      | 1    | R/W    | 0       | Overflow idle cell counter                |
| OV-EHR1     | 2    | R/W    | 0       | Overflow HEC error counter #1             |
| TH-EHR1     | 3    | R/W    | 0       | Threshold overstep HEC error counter #1   |
| OV-EHR2     | 4    | R/W    | 0       | Overflow HEC error counter #2             |
| TH-EHR2     | 5    | R/W    | 0       | Threshold overstep HEC error counter #2   |
| OV-BHR      | 6    | R/W    | 0       | Overflow discarded cell counter           |
| TH-BHR      | 7    | R/W    | 0       | Threshold overstep discarded cell counter |

## ACH\_Rx2/3/4 Configuration Registers

### 47.1: HR#Conf1 [1248 H, 1348 H, 1448 H]

Register to control auto-resetting of bits upon read access.

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| AutRst_Int  | 0    | R/W    | 1       | 0: No action on read access<br>1: Auto-reset interrupt request registers upon read access<br>Regardless of the setting of this bit, individual interrupt request bits can be cleared by writing a '1' to that bit provided that the corresponding alarm condition is removed. |
| AutRst_Sta  | 1    | R/W    | 1       | 0: No action on read access<br>1: Auto-reset all bits in the HR#Stat1 status register upon read access  |
| Reserved    | 7:2  |        |         | Not used  |

### 47.2: HR#Conf2 [1249 H, 1349 H, 1449 H]

Register to control the HEC correction modes of this chiplet.

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| CorModeHi   | 0    | R/W    | 0       | 0: FSM returns into detection mode after HEC error correction<br>1: FSM stays in correction mode until the Sync state is left |
| NCorHECEr   | 1    | R/W    | 0       | 0: Single-bit HEC errors are corrected<br>1: Single-bit HEC errors are not corrected  |
| WrIdleC     | 2    | R/W    | 0       | 0: Do not write Idle cell into ACB FIFO<br>1: Write Idle cell into ACB FIFO   |
| Ndescramb   | 3    | R/W    | 0       | 0: Descramble ATM cell payload<br>1: Do not descramble ATM cell payload   |
| WrtCHecEr   | 4    | R/W    | 0       | 0: Do not write ATM cell with HEC errors<br>1: Write ATM cell with HEC errors   |
| NotDetHecEr | 5    | R/W    | 0       | 0: Detect ATM cell with HEC error<br>1: Do not detect ATM cell with HEC error   |
| NWrToFifo   | 6    | R/W    | 0       | 0: Write into ACB FIFO<br>1: Do not write into ACB FIFO; all received cells are discarded                                     |
| DetStartOC  | 7    | R/W    | 0       | 0: Do not detect start of cell<br>1: Detect start of cell   |

### 47.3: HR#Conf3 [124A H, 134A H, 144A H]

Register to control ATM cell synchronization in this chiplet.

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| Delta(3:0)  | 3:0  | R/W    | 0110    | Required number of consecutive good HECs detected to jump from PRESYNC to SYNC state. |
| Alpha(3:0)  | 7:4  | R/W    | 0111    | Required number of consecutive false HECs detected to return from SYNC to HUNT state. |



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**47.4: HR#Conf4-7:ICU1/2/3/4 [124B H, 134B H, 144B H; 124C H, 134C H, 144C H; 124D H, 134D H, 144D H; 124E H, 134E H, 144E H]**

Header pattern to identify Idle/Unassigned cells.

| Signal Name | Bits | Access | Default  | Description    |
|-------------|------|--------|----------|----------------|
| ICU1(7:0)   | 7:0  | R/W    | 00000000 | Header byte #1 |
| ICU2(7:0)   | 7:0  | R/W    | 00000000 | Header byte #2 |
| ICU3(7:0)   | 7:0  | R/W    | 00000000 | Header byte #3 |
| ICU4(7:0)   | 7:0  | R/W    | 00000001 | Header byte #4 |

**47.5: HR#Conf8:MODU [124F H, 134F H, 144F H]**

Pattern to do last modulo operation in HEC (i.e., coset).

| Signal Name | Bits | Access | Default  | Description   |
|-------------|------|--------|----------|---|
| MODU(7:0)   | 7:0  | R/W    | 01010101 | HEC modulo pattern. This is also known as the coset pattern. Setting this register to 00 H disables the coset operation in the receive direction. |

**47.6: HR#Conf9:PL [1250 H, 1350 H, 1450 H]**

Dummy byte to align the Payload in the ACB\_Rx2/3/4 buffer.

| Signal Name | Bits | Access | Default  | Description            |
|-------------|------|--------|----------|------------------------|
| PL(7:0)     | 7:0  | R/W    | 11010000 | Payload alignment byte |

**47.7: HR#Conf10:PAFT [1251 H, 1351 H, 1451 H]**

Threshold for Programmable Almost Full flag (ACB\_Rx2/3/4).

| Signal Name | Bits | Access | Default | Description  |
|-------------|------|--------|---------|--|
| PAFT(6:0)   | 6:0  | R/W    | 1100000 | Threshold for Programmable Almost Full flag, ACB_Rx2/3/4. This register should be set according to mode as follows:<br><br>ATM:<br>STM-4c/STS-12c 74 H<br>STM-1/STS-3c/STM-4/STS-12 60 H<br><br>PPP: For PPP mode, this register should be set to 7B H |
| Reserved    | 7    |        |         | Not used   |

**PPP Chiplet Address Map** Base Address: 1500 H

| Register Name  | Address Offset (Hex) | Type/Width | Initial Value (Binary) | Description  | See Page |
|----------------|----------------------|------------|------------------------|--|----------|
| PPPCntEn1      | 2                    | X 6        | 000000                 | COUNT ENABLE register #1   | 217      |
| PPPCntEn2      | 3                    | X 6        | 000000                 | COUNT ENABLE register #2   | 217      |
| PPPCnt1:FCSE1  | 4/5                  | N 8        | 00000000               | FCS error counter macro #1, no threshold   | 216      |
| PPPCnt2:MFLE1  | 6/7                  | N 8        | 00000000               | MFLE ( <u>M</u> aximum <u>E</u> rame <u>L</u> ength <u>E</u> xceeded) event counter macro #1, no threshold | 216      |
| PPPCnt3:BMFL1  | 8/9                  | N 8        | 00000000               | BMFL ( <u>B</u> elow <u>M</u> inimum <u>E</u> rame <u>L</u> ength) event counter macro #1, no threshold    | 216      |
| PPPCnt4:FCSE2  | A/B                  | N 8        | 00000000               | FCS error counter macro #2, no threshold   | 216      |
| PPPCnt5:MFLE2  | C/D                  | N 8        | 00000000               | MFLE event counter macro #2, no threshold  | 216      |
| PPPCnt6:BMFL2  | E/F                  | N 8        | 00000000               | BMFL event counter macro #2, no threshold  | 216      |
| PPPCnt7:FCSE3  | 10/11                | N 8        | 00000000               | FCS error counter macro #3, no threshold   | 216      |
| PPPCnt8:MFLE3  | 12/13                | N 8        | 00000000               | MFLE event counter macro #3, no threshold  | 216      |
| PPPCnt9:BMFL3  | 14/15                | N 8        | 00000000               | BMFL event counter macro #3, no threshold  | 216      |
| PPPCnt10:FCSE4 | 16/17                | N 8        | 00000000               | FCS error counter macro #4, no threshold   | 216      |
| PPPCnt11:MFLE4 | 18/19                | N 8        | 00000000               | MFLE event counter macro #4, no threshold  | 216      |
| PPPCnt12:BMFL4 | 1A/1B                | N 8        | 00000000               | BMFL event counter macro #4, no threshold  | 216      |
| PPPRESET       | 30                   | R 1        | 1                      | Default RESET register (PPP_Tx and PPP_Rx)   | 218      |
| PPPMMainIRQ    | 38                   | I 5        |                        | MAIN INTerrupt register  | 218      |
| PPPM_MainIRQ   | 39                   | X 5        | 00000                  | INT MASK register (for PPPMainIRQ)   | 218      |
| PPPCntIRQ1     | 3A                   | I 6        |                        | COUNTER INTerrupt register #1  | 219      |
| PPPM_CntIRQ1   | 3B                   | X 6        | 000000                 | INT MASK register (for PPCntIRQ1)  | 219      |
| PPPCntIRQ2     | 3C                   | I 6        |                        | COUNTER INTerrupt register #2  | 219      |
| PPPM_CntIRQ2   | 3D                   | X 6        | 000000                 | INT MASK register (for PPCntIRQ2)  | 219      |
| PPPIRQ1        | 3E                   | I 8        |                        | USER INTerrupt register #1   | 220      |
| PPPM_IRQ1      | 3F                   | X 8        | 00000000               | INT MASK register (for PPPIRQ1)  |          |
| PPPIRQ2        | 40                   | I 8        |                        | USER INTerrupt register #2   | 220      |
| PPPM_IRQ2      | 41                   | X 8        | 00000000               | INT MASK register (for PPPIRQ2)  | 221      |
| PPPConf1       | 48                   | C 2        | 11                     | Chiplet configuration register #1 (general A)  | 222      |
| PPPConf2       | 49                   | C 8        | 00000000               | Configuration register #2 (general B)  | 222      |
| PPPConf3       | 4A                   | C 8        | 00000000               | Configuration register #3 (minimum frame length)   | 223      |
| PPPConf4       | 4B                   | C 8        | 11111111               | Configuration register #4 (maximum frame length, LSByte)   | 223      |
| PPPConf5       | 4C                   | C 8        | 11111111               | Configuration register #5 (maximum frame length, MSByte)   | 223      |
| PPPConf6       | 4D                   | C 8        | 00000000               | Configuration register #6 (PPP control)  | 224      |



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**PPP Counters**

**48.1: PPCnt1..3:FCSE1/MFLE1/BMFL1 [1504 H / 1505 H, 1506 H / 1507 H, 1508 H / 1509 H]**

Counters for PPP macro #1. Counter overflow leads to an interrupt request.

| Signal Name | Bits | Access | Default  | Description                       |
|-------------|------|--------|----------|-----------------------------------|
| FCSE1(7:0)  | 7:0  | R      | 00000000 | FCS/Abort error counter, macro #1 |
| MFLE1(7:0)  | 7:0  | R      | 00000000 | MFLE event counter, macro #1      |
| BMFL1(7:0)  | 7:0  | R      | 00000000 | BMFL event counter, macro #1      |

**48.2: PPCnt4..6:FCSE2/MFLE2/BMFL2 [150A H / 150B H, 150C H / 150D H, 150E H / 150F H]**

Counters for PPP macro #2. Counter overflow leads to an interrupt request.

| Signal Name | Bits | Access | Default  | Description                       |
|-------------|------|--------|----------|-----------------------------------|
| FCSE2(7:0)  | 7:0  | R      | 00000000 | FCS/Abort error counter, macro #2 |
| MFLE2(7:0)  | 7:0  | R      | 00000000 | MFLE event counter, macro #2      |
| BMFL2(7:0)  | 7:0  | R      | 00000000 | BMFL event counter, macro #2      |

**48.3: PPCnt7..9:FCS3/MFLE3/BMFL3 [1510 H / 1511 H, 1512 H / 1513 H, 1514 H / 1515 H]**

Counters for PPP macro #3. Counter overflow leads to an interrupt request.

| Signal Name | Bits | Access | Default  | Description                       |
|-------------|------|--------|----------|-----------------------------------|
| FCSE3(7:0)  | 7:0  | R      | 00000000 | FCS/Abort error counter, macro #3 |
| MFLE3(7:0)  | 7:0  | R      | 00000000 | MFLE event counter, macro #3      |
| BMFL3(7:0)  | 7:0  | R      | 00000000 | BMFL event counter, macro #3      |

**48.4: PPCnt10..12:FCSE4/MFLE4/BMFL4 [1516 H / 1517 H, 1518 H / 1519 H, 151A H / 151B H]**

Counters for PPP macro #4. Counter overflow leads to an interrupt request.

| Signal Name | Bits | Access | Default  | Description                       |
|-------------|------|--------|----------|-----------------------------------|
| FCSE4(7:0)  | 7:0  | R      | 00000000 | FCS/Abort error counter, macro #4 |
| MFLE4(7:0)  | 7:0  | R      | 00000000 | MFLE event counter, macro #4      |
| BMFL4(7:0)  | 7:0  | R      | 00000000 | BMFL event counter, macro #4      |

#### 48.5: PPCntEn1 [1502 H]

Counter On/Off control register #1 for PPP.

For each bit position: 0: Counter is disabled  
1: Counter is enabled

| Signal Name | Bits | Access | Default | Description                        |
|-------------|------|--------|---------|------------------------------------|
| EN-BMFL2    | 0    | R/W    | 0       | BMFL event counter macro #2 enable |
| EN-MFLE2    | 1    | R/W    | 0       | MFLE event counter macro #2 enable |
| EN-FCSE2    | 2    | R/W    | 0       | FCS error counter macro #2 enable  |
| EN-BMFL1    | 3    | R/W    | 0       | BMFL event counter macro #1 enable |
| EN-MFLE1    | 4    | R/W    | 0       | MFLE event counter macro #1 enable |
| EN-FCSE1    | 5    | R/W    | 0       | FCS error counter macro #1 enable  |
| Reserved    | 7:6  |        |         | Not used                           |

#### 48.6: PPCntEn2 [1503 H]

Counter On/Off control register #2 for PPP.

For each bit position: 0: Counter is disabled  
1: Counter is enabled

| Signal Name | Bits | Access | Default | Description                        |
|-------------|------|--------|---------|------------------------------------|
| EN-BMFL4    | 0    | R/W    | 0       | BMFL event counter macro #4 enable |
| EN-MFLE4    | 1    | R/W    | 0       | MFLE event counter macro #4 enable |
| EN-FCSE4    | 2    | R/W    | 0       | FCS error counter macro #4 enable  |
| EN-BMFL3    | 3    | R/W    | 0       | BMFL event counter macro #3 enable |
| EN-MFLE3    | 4    | R/W    | 0       | MFLE event counter macro #3 enable |
| EN-FCSE3    | 5    | R/W    | 0       | FCS error counter macro #3 enable  |
| Reserved    | 7:6  |        |         | Not used                           |

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**PPP Reset Register**
**49.1: PPPRESET [1530 H]**

Reset chiplet control register. This register is automatically preset to the default value by the reset signal ResPPP from the GPPINT.

For each bit position: 0: Reset not active

1: Reset active

| Signal Name | Bits | Access | Default | Description  |
|-------------|------|--------|---------|--|
| Reset       | 0    | R/W    | 1       | Reset (disable) PPP_Tx and PPP_Rx chiplets:<br>1: Disables the receive and transmit PPP chiplets. Flags (7E H) are transmitted in the transmit direction if transparent mode is turned off in the transmit direction else all '1's are transmitted.<br>0: Enables the receive and transmit PPP chiplets. If transparent mode is not enabled, then the SONET/SDH framer looks for a flag followed by a non-flag before writing data into the receive ACB FIFO. Also it waits for a TXSOFl indication before it starts transmitting data. If transparent mode is enabled, receive and transmit data are transferred immediately. |
| Reserved    | 7:1  |        |         | Not used   |

**PPP Interrupt Request and Mask Registers**
**50.1: PPPMainIRQ [1538 H]**

Register to indicate fatal interrupt events and to point to user IRQ registers with active requests.

For each bit position: 0: No interrupt request pending

1: Interrupt request pending

**50.2: PPPM\_MainIRQ [1539 H]**

Register to mask pending interrupt requests. A masked request will not generate an outgoing IRQ to the GPPINT.

For each bit position: 0: The corresponding pending request bit is masked (DEFAULT)

1: The corresponding pending request bit activates signal IRQPPP to GPPINT

| Signal Name | Bits | Access | Default | Description                           |
|-------------|------|--------|---------|---------------------------------------|
| Fatal       | 0    | R/W    | 0       | Fatal event occurred                  |
| CntIRQ1     | 1    | R/W    | 0       | Active request in PPPCntIRQ1 register |
| CntIRQ2     | 2    | R/W    | 0       | Active request in PPPCntIRQ2 register |
| IRQ1        | 3    | R/W    | 0       | Active request in PPPIRQ1 register    |
| IRQ2        | 4    | R/W    | 0       | Active request in PPPIRQ2 register    |
| Reserved    | 7:5  |        |         | Not used                              |

### 50.3: PPCntIRQ1 [153A H]

Register #1 to indicate active counter interrupt requests of this chiplet.

For each bit position: 0: No interrupt request pending  
1: Interrupt request pending

### 50.4: PPPM\_CntIRQ1 [153B H]

Register #1 to mask pending counter interrupt requests.

For each bit position: 0: The corresponding pending request bit is masked (DEFAULT)  
1: The corresponding pending request bit activates the pointer bit in PPPMainIRQ register

| Signal Name | Bits | Access | Default | Description                          |
|-------------|------|--------|---------|--------------------------------------|
| OV-BMFL2    | 0    | R/W    | 0       | Overflow BMFL event counter macro #2 |
| OV-MFLE2    | 1    | R/W    | 0       | Overflow MFLE event counter macro #2 |
| OV-FCSE2    | 2    | R/W    | 0       | Overflow FCS error counter macro #2  |
| OV-BMFL1    | 3    | R/W    | 0       | Overflow BMFL event counter macro #1 |
| OV-MFLE1    | 4    | R/W    | 0       | Overflow MFLE event counter macro #1 |
| OV-FCSE1    | 5    | R/W    | 0       | Overflow FCS error counter macro #1  |
| Reserved    | 7:6  |        |         | Not used                             |

### 50.5: PPCntIRQ2 [153C H]

Register #2 to indicate active counter interrupt requests of this chiplet.

For each bit position: 0: No interrupt request pending  
1: Interrupt request pending

### 50.6: PPPM\_CntIRQ2 [153D H]

Register #2 to mask pending counter interrupt requests.

For each bit position: 0: The corresponding pending request bit is masked (DEFAULT)  
1: The corresponding pending request bit activates the pointer bit in PPPMainIRQ register

| Signal Name | Bits | Access | Default | Description                          |
|-------------|------|--------|---------|--------------------------------------|
| OV-BMFL4    | 0    | R/W    | 0       | Overflow BMFL event counter macro #4 |
| OV-MFLE4    | 1    | R/W    | 0       | Overflow MFLE event counter macro #4 |
| OV-FCSE4    | 2    | R/W    | 0       | Overflow FCS error counter macro #4  |
| OV-BMFL3    | 3    | R/W    | 0       | Overflow BMFL event counter macro #3 |
| OV-MFLE3    | 4    | R/W    | 0       | Overflow MFLE event counter macro #3 |
| OV-FCSE3    | 5    | R/W    | 0       | Overflow FCS error counter macro #3  |
| Reserved    | 7:6  |        |         | Not used                             |

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**50.7: PPIRQ1 [153E H]**

Register #1 to indicate active user interrupt requests of this chiplet.

For each bit position: 0: No interrupt request pending

1: Interrupt request pending

**50.8: PPPM\_IRQ1 [153F H]**

Register #1 to mask pending user interrupt requests.

For each bit position: 0: The corresponding pending request bit is masked (DEFAULT)

1: The corresponding pending request bit activates the pointer bit in PPPMainIRQ register

| Signal Name | Bits | Access | Default | Description  |
|-------------|------|--------|---------|--|
| ABT2        | 0    | R/W    | 0       | Abort character (7D7E H) detected in macro #2.   |
| BMFL2       | 1    | R/W    | 0       | Below minimum frame length, macro #2. This bit is set when a packet is received that is shorter than the size set in MINFL(6:0).                           |
| MFLE2       | 2    | R/W    | 0       | Maximum frame length exceeded in macro #2. This bit is set when a packet is received that is longer than or equal to the size set in the MAXFL(15:0) bits. |
| FCS2        | 3    | R/W    | 0       | Received bad frame in macro #2. This bit is set when an FCS error is detected in the received packet.  |
| ABT1        | 4    | R/W    | 0       | Abort character (7D7E H) detected in macro #1.   |
| BMFL1       | 5    | R/W    | 0       | Below minimum frame length, macro #1. This bit is set when a packet is received that is shorter than the size set in MINFL(6:0).                           |
| MFLE1       | 6    | R/W    | 0       | Maximum frame length exceeded in macro #1. This bit is set when a packet is received that is longer than or equal to the size set in the MAXFL(15:0) bits. |
| FCS1        | 7    | R/W    | 0       | Received bad frame in macro #1. This bit is set when an FCS error is detected in the received packet.  |

**50.9: PPIRQ2 [1540 H]**

Register #2 to indicate active user interrupt requests of this chiplet.

For each bit position: 0: No interrupt request pending

1: Interrupt request pending

### 50.10: PPPM\_IRQ2 [1541 H]

Register #2 to mask pending user interrupt requests.

For each bit position: 0: The corresponding pending request bit is masked (DEFAULT)

1: The corresponding pending request bit activates the pointer bit in PPPMainIRQ register

| Signal Name | Bits | Access | Default | Description  |
|-------------|------|--------|---------|--|
| ABT4        | 0    | R/W    | 0       | Abort character (7D7E H) detected in macro #4.   |
| BMFL4       | 1    | R/W    | 0       | Below minimum frame length, macro #4. This bit is set when a packet is received that is shorter than the size set in MINFL(6:0).                           |
| MFLE4       | 2    | R/W    | 0       | Maximum frame length exceeded in macro #4. This bit is set when a packet is received that is longer than or equal to the size set in the MAXFL(15:0) bits. |
| FCS4        | 3    | R/W    | 0       | Received bad frame in macro #4. This bit is set when an FCS error is detected in the received packet.  |
| ABT3        | 4    | R/W    | 0       | Abort character (7D7E H) detected in macro #3.   |
| BMFL3       | 5    | R/W    | 0       | Below minimum frame length, macro #3. This bit is set when a packet is received that is shorter than the size set in MINFL(6:0).                           |
| MFLE3       | 6    | R/W    | 0       | Maximum frame length exceeded in macro #3. This bit is set when a packet is received that is longer than or equal to the size set in the MAXFL(15:0) bits. |
| FCS3        | 7    | R/W    | 0       | Received bad frame in macro #3. This bit is set when an FCS error is detected in the received packet.  |



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PPP Configuration Registers

51.1: PPPConf1 [1548 H]

Configuration register #1. General PPP configuration signals A.

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| AutRst_Int  | 0    | R/W    | 1       | 0: No action on read access<br>1: Auto-reset interrupt request registers upon read access<br>Regardless of the setting of this bit, individual interrupt request bits can be cleared by writing a '1' to that bit provided that the corresponding alarm condition is removed. |
| Reserved    | 1    | R/W    | 1       | Reserved  |
| Reserved    | 7:2  |        |         | Not used  |

51.2: PPPConf2 [1549 H]

Configuration register #2. General PPP configuration signals B.

| Signal Name | Bits | Access | Default | Description  |
|-------------|------|--------|---------|--|
| MFLAG       | 0    | R/W    | 0       | Multiple flag:<br>0: At least one 7E H flag will be inserted between transmitted frames.<br>1: At least two 7E H flags will be inserted between transmitted frames.                |
| SCRAM       | 1    | R/W    | 0       | Scrambler enable:<br>0: Scrambler/descrambler is bypassed.<br>1: The PPP Scrambler/descrambler is active. The scrambler operates over all bytes inserted into the SONET/SDH frame. |
| FCSABT      | 2    | R/W    | 0       | FCS abort: use of RXFCSE pin:<br>0: Only active if FCS error detected.<br>1: Active if FCS or ABORT error detected, RXABTO pin remains at '0'.                                     |
| DMINF       | 3    | R/W    | 0       | Discard minimum frame:<br>0: All received frames are output.<br>1: Received frames that are less than the minimum size as indicated by the MINFL(6:0) bits are aborted.            |
| TFCS(1:0)   | 5:4  | R/W    | 00      | Calculation of FCS in PPP_Tx:<br>00: Transparent mode<br>01: No FCS is used<br>10: 16-bit FCS is used<br>11: 32-bit FCS is used  |
| RFCS(1:0)   | 7:6  | R/W    | 00      | Calculation of FCS in PPP_Rx:<br>00: Transparent mode<br>01: No FCS is used<br>10: 16-bit FCS is used<br>11: 32-bit FCS is used  |

### 51.3: PPPConf3 [154A H]

Configuration register #3. Minimum frame length, used to monitor the received frames.

| Signal Name | Bits | Access | Default | Description  |
|-------------|------|--------|---------|--|
| MINFL(6:0)  | 6:0  | R/W    | 0000000 | Minimum frame length: min. frame size to monitor received frames. Received frames that are less than the length indicated by MINFL(6:0) are discarded. |
| Reserved    | 7    | R/W    | 0       | Not used   |

### 51.4: PPPConf4-5 [154B H, 154C H]

Configuration registers #4 - #5. Maximum frame length, used to monitor the received frames.

| Signal Name | Bits | Access | Default  | Description   |
|-------------|------|--------|----------|---|
| MAXFL(7:0)  | 7:0  | R/W    | 11111111 | PPPConf4: Max. frame length (LS Byte) frame size to monitor received frames. Received frames that are equal to or greater than the length indicated by MAXFL(15:0) are discarded. |
| MAXFL(15:8) | 7:0  | R/W    | 11111111 | PPPConf5: Max. frame length (MS Byte) frame size to monitor received frames. Received frames that are equal to or greater than the length indicated by MAXFL(15:0) are discarded. |

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**51.5: PPPConf6 [154D H]**

Configuration register #6. PPP control signals.

For all TXEN# bits, if transparent mode is disabled and a TXEN# bit is set to '0' while in the middle of a frame transfer for that PHY, an illegal sequence (7D7E H) is transmitted, followed by flags. The TXABTO pin will also be asserted when that PHY is selected. Otherwise flags (7E H) are transmitted. If transparent mode is enabled and a TXEN# bit is set to '0', an all '1's pattern is inserted into the transmit data stream. When transparent mode is disabled and a TXEN# bit is set to '1', flags (7E H) are transmitted until the start of a new frame is read out of the transmit ACB FIFO. If transparent mode is enabled and a TXEN# bit is set to '1', then data is just read out of the transmit ACB FIFO at the point where it left off.

For all RXEN# bits, if transparent mode is enabled or if transparent mode is disabled and the SONET/SDH framer is in the middle of a frame transfer and a RXEN# bit is set to '0', operation will continue normally until the end of the current chunk, then the RXABTO (or RXFCSEO pin if enabled by the FCSABT bit), RXMSO and RXEFO signals will be asserted when that PHY is selected. If transparent mode is enabled, data received for the receive PPP macro # is immediately written into the receive ACB, otherwise the SONET/SDH framer looks for a flag (7E H) followed by a non-flag character before writing data into the receive ACB FIFO.

| Signal Name | Bits | Access | Default | Description  |
|-------------|------|--------|---------|--|
| TXEN4       | 0    | R/W    | 0       | Transmit enable:<br>0: Transmit PPP macro #4 is held in reset after completion of current chunk<br>1: Transmit PPP macro #4 is enabled |
| TXEN3       | 1    | R/W    | 0       | Transmit enable:<br>0: Transmit PPP macro #3 is held in reset after completion of current chunk<br>1: Transmit PPP macro #3 is enabled |
| TXEN2       | 2    | R/W    | 0       | Transmit enable:<br>0: Transmit PPP macro #2 is held in reset after completion of current chunk<br>1: Transmit PPP macro #2 is enabled |
| TXEN1       | 3    | R/W    | 0       | Transmit enable:<br>0: Transmit PPP macro #1 is held in reset after completion of current chunk<br>1: Transmit PPP macro #1 is enabled |
| RXEN4       | 4    | R/W    | 0       | Receive enable:<br>0: Receive PPP macro #4 is held in reset after completion of current chunk<br>1: Receive PPP macro #4 is enabled    |
| RXEN3       | 5    | R/W    | 0       | Receive enable:<br>0: Receive PPP macro #3 is held in reset after completion of current chunk<br>1: Receive PPP macro #3 is enabled    |
| RXEN2       | 6    | R/W    | 0       | Receive enable:<br>0: Receive PPP macro #2 is held in reset after completion of current chunk<br>1: Receive PPP macro #2 is enabled    |
| RXEN1       | 7    | R/W    | 0       | Receive enable:<br>0: Receive PPP macro #1 is held in reset after completion of current chunk<br>1: Receive PPP macro #1 is enabled    |



**OFF\_Tx1/2/3/4 Chiplet Address Mapping** Base Address: OFF\_Tx1 1800 H, OFF\_Tx2 1C00 H, OFF\_Tx3 2000 H, OFF\_Tx4 2400 H

| Register Name <sup>1</sup> | Address Offset (Hex) | Type/Width | Initial Value (Binary) | Description                                     | See Page |
|----------------------------|----------------------|------------|------------------------|---|----------|
| OT#CntEn1                  | 2                    | X 4        | 0000                   | COUNT ENABLE register                           | 227      |
| OT#Cnt1:PTRINC             | 4/5                  | N 8        | 00000000               | Pointer increment event counter, no threshold   | 226      |
| OT#Cnt2:PTRDEC             | 6/7                  | N 8        | 00000000               | Pointer decrement event counter, no threshold   | 226      |
| OT#Cnt3:ND_EVC             | 8/9                  | N 8        | 00000000               | New data event counter, no threshold            | 226      |
| OT#Cnt4:JUSC               | A/B                  | N 8        | 00000000               | Justification error counter with threshold      | 227      |
| OT#Th4:JUSCTh              | C                    | X 8        | 10000000               | Threshold register for counter JUSC             | 227      |
| OT#RESET                   | 30                   | R 1        | 1                      | Default RESET register                          | 227      |
| OT#CMD1                    | 31                   | O 3        | 000                    | Njus, Pjus, NDF                                 | 228      |
| OT#Stat1                   | 33                   | S 5        |                        | Init, HUG, Mode(2:0) (event)                    | 228      |
| OT#Stat2                   | 34                   | S 3        |                        | Njus, Pjus, NDF (event)                         | 228      |
| OT#Stat3                   | 35                   | S 8        |                        | K1 byte from STM-1 (static)                     | 229      |
| OT#Stat4                   | 36                   | S 8        |                        | K2 byte from STM-1 (static)                     | 229      |
| OT#Stat5                   | 37                   | S 8        |                        | K3 byte from STM-1 (static)                     | 229      |
| OT#MainIRQ                 | 38                   | I 4        |                        | MAIN INTerrupt register                         | 230      |
| OT#M_MainIRQ               | 39                   | X 4        | 0000                   | INT MASK register (for OT#MainIRQ)              | 230      |
| OT#CntIRQ1                 | 3A                   | I 5        |                        | COUNTER INTerrupt register                      | 230      |
| OT#M_CntIRQ1               | 3B                   | X 5        | 00000                  | INT MASK register (for OT#CntIRQ1)              | 230      |
| OT#IRQ1                    | 3C                   | I 7        |                        | USER INTerrupt register #1                      | 231      |
| OT#M_IRQ1                  | 3D                   | X 7        | 0000000                | INT MASK register (for OT#IRQ1)                 | 231      |
| OT#IRQ2                    | 3E                   | I 6        |                        | USER INTerrupt register #2                      | 231      |
| OT#M_IRQ2                  | 3F                   | X 6        | 000000                 | INT MASK register (for OT#IRQ2)                 | 231      |
| OT#Conf1                   | 48                   | C 8        | 00000011               | Chiplet configuration register #1 (general A)   | 233      |
| OT#Conf2                   | 49                   | C 8        | 00000000               | Configuration register #2 (general B)           | 233      |
| OT#Conf3                   | 4A                   | C 8        | 11111110               | Configuration register #3 (fscr reload pattern) | 234      |
| OT#Conf4                   | 4B                   | C 8        | 00000000               | Configuration register #4 (errmask)             |          |
| OT#Conf5                   | 4C                   | C 8        | 00000000               | Configuration register #5 (erraddress)          |          |
| OT#Conf6                   | 4D                   | C 8        | 00000001               | Configuration register #6 (fscr control)        | 234      |
| OT#Conf7                   | 4E                   | C 4        | 0000                   | Configuration register #7 (DCC control)         | 234      |
| OT#Conf8                   | 4F                   | C 6        | 000011                 | Configuration register #8 (ThrLoW)              | 235      |
| OT#Conf9                   | 50                   | C 6        | 010001                 | Configuration register #9 (ThrNoW)              | 235      |
| OT#Conf10                  | 51                   | C 6        | 100000                 | Configuration register #10 (ThrHiW)             | 235      |
| OT#Conf11                  | 52                   | C 5        | 00000                  | Configuration register #11 (Telecom Bus)        | 235      |
| GRA                        | 100-3FF              |            |                        | Growable Register Array (TOH)                   | 235      |

1. # = A specific Overhead Frame Processor macro in the transmit direction: 1, 2, 3, or 4.

## OFF\_Tx1/2/3/4 (OT1/2/3/4) Counters

### 52.1: OT#Cnt1:PTRINC [1804 H / 1805 H, 1C04 H / 1C05 H, 2004 H / 2005 H, 2404 H / 2405 H]

Number of pointer increment events. Counter overflow leads to an interrupt request.

| Signal Name | Bits | Access | Default  | Description               |
|-------------|------|--------|----------|---------------------------|
| PTRINC(7:0) | 7:0  | R      | 00000000 | Pointer increment counter |

### 52.2: OT#Cnt2:PTRDEC [1806 H / 1807 H, 1C06 H / 1C07 H, 2006 H / 2007 H, 2406 H / 2407 H]

Number of pointer decrement events. Counter overflow leads to an interrupt request.

| Signal Name | Bits | Access | Default  | Description               |
|-------------|------|--------|----------|---------------------------|
| PTRDEC(7:0) | 7:0  | R      | 00000000 | Pointer decrement counter |

### 52.3: OT#Cnt3:ND\_EVC [1808 H / 1809 H, 1C08 H / 1C09 H, 2008 H / 2009 H, 2408 H / 2409 H]

Number of new data events. Counter overflow leads to an interrupt request.

| Signal Name | Bits | Access | Default  | Description            |
|-------------|------|--------|----------|------------------------|
| ND_EVC(7:0) | 7:0  | R      | 00000000 | New data event counter |

#### 52.4: OT#Cnt4:JUSC [180A H / 180B H, 1C0A H / 1C0B H, 200A H / 200B H, 240A H / 240B H]

Number of justification errors detected. Counter overflow leads to an interrupt request.

| Signal Name | Bits | Access | Default  | Description                 |
|-------------|------|--------|----------|-----------------------------|
| JUSC(7:0)   | 7:0  | R      | 00000000 | Justification error counter |

#### 52.5: OT#Th4:JUSCTh [180C H, 1C0C H, 200C H, 240C H]

Threshold for number of justification errors. Threshold overstep leads to an interrupt request.

| Signal Name | Bits | Access | Default  | Description                               |
|-------------|------|--------|----------|---|
| JUSCTh(7:0) | 7:0  | R/W    | 10000000 | Threshold for justification error counter |

#### 52.6: OT#CntEn1 [1802 H, 1C02 H, 2002 H, 2402 H]

Counter On/Off control register for OFP\_Tx1/2/3/4

For each bit position: 0: Counter is disabled  
1: Counter is enabled

| Signal Name | Bits | Access | Default | Description                        |
|-------------|------|--------|---------|------------------------------------|
| EN-PTRINC   | 0    | R/W    | 0       | Pointer increment counter enable   |
| EN-PTRDEC   | 1    | R/W    | 0       | Pointer decrement counter enable   |
| EN-ND_EVCNT | 2    | R/W    | 0       | New data event counter enable      |
| EN-JUSCNT   | 3    | R/W    | 0       | Justification error counter enable |
| Reserved    | 7:4  |        |         | Not used                           |

### OFF\_Tx1/2/3/4 (OT1/2/3/4) Reset Registers

#### 53.1: OT#RESET [1830 H, 1C30 H, 2030 H, 2430 H]

Reset chiplet control registers. These registers are automatically preset to the default value by the reset signals ResOT1/2/3/4 from the GPPINT.

For each bit position: 0: Reset not active  
1: Reset active

| Signal Name | Bits | Access | Default | Description                           |
|-------------|------|--------|---------|---------------------------------------|
| Reset       | 0    | R/W    | 1       | Reset (disable) OFF_Tx1/2/3/4 chiplet |
| Reserved    | 7:1  |        |         | Not used                              |

**IBM SONET/SDH Framer**
**OFF\_Tx1/2/3/4 (OT1/2/3/4) Command Register**
**54.1: OT#CMD1 [1831 H, 1C31 H, 2031 H, 2431 H]**

Command register for the chiplet. Single-cycle active if '1' is written into bit position.

| Signal Name | Bits | Access | Default | Description                                |
|-------------|------|--------|---------|--|
| Njus        | 0    | R/W    | 0       | Perform a negative frequency justification |
| Pjus        | 1    | R/W    | 0       | Perform a positive frequency justification |
| NDF         | 2    | R/W    | 0       | Force a start-of-new-VC-4 event            |
| Reserved    | 7:3  |        |         | Not used                                   |

**OFF\_Tx1/2/3/4 Status Registers**
**55.1: OT#Stat1 [1833 H, 1C33 H, 2033 H, 2433 H]**

Status register #1 of the chiplet. This is an event latch register.

| Signal Name | Bits | Access | Default | Description  |
|-------------|------|--------|---------|--|
| Init        | 0    | R/W    |         | 0: Default GRA initialization not completed<br>1: Default GRA initialization completed       |
| HUG         | 1    | R/W    |         | 0: Higher-order unequipped generator inactive<br>1: Higher-order unequipped generator active |
| Mode(2:0)   | 4:2  | R/W    |         | Mode:<br>000: Single macro<br>001: Multi-macro<br>010: Concatenated<br>100: Multi-device     |
| Reserved    | 7:5  |        |         | Not used   |

**55.2: OT#Stat2 [1834 H, 1C34 H, 2034 H, 2434 H]**

Status register #2 of the chiplet. This is an event latch register.

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| Njus        | 0    | R/W    |         | 0: No negative frequency justification transmitted<br>1: Negative frequency justification transmitted |
| Pjus        | 1    | R/W    |         | 0: No positive frequency justification transmitted<br>1: Positive frequency justification transmitted |
| NDF         | 2    | R/W    |         | 0: No NDF transmitted<br>1: NDF transmitted   |
| Reserved    | 7:3  |        |         | Not used  |

### 55.3: OT#Stat3 [1835 H, 1C35 H, 2035 H, 2435 H]

Status register #3 of the chiplet. This is a static latch register; the bit values follow the driving signals immediately.

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| K1byte(7:0) | 7:0  | R      |         | This is the K1 byte received from the ring port when the RING control bit is set to '1', otherwise it is the debounced K1 byte from OFP_Rx #. |

### 55.4: OT#Stat4 [1836 H, 1C36 H, 2036 H, 2436 H]

Status register #4 of the chiplet. This is a static latch register; the bit values follow the driving signals immediately.

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| K2byte(7:0) | 7:0  | R      |         | This is the K2 byte received from the ring port when the RING control bit is set to '1', otherwise it is the debounced K2 byte from OFP_Rx #. |

### 55.5: OT#Stat5 [1837 H, 1C37 H, 2037 H, 2437 H]

Status register #5 of the chiplet. This is a static latch register; the bit values follow the driving signals immediately.

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| K3byte(7:0) | 7:0  | R      |         | This is the K3 byte received from the ring port when the RING control bit is set to '1', otherwise it is the debounced K3 byte from OFP_Rx #. |



## OFF\_Tx1/2/3/4 Interrupt Request and Mask Registers

### 56.1: OT#MainIRQ [1838 H, 1C38 H, 2038 H, 2438 H]

Register to indicate fatal interrupt events and to point to user IRQ registers with active requests.

For each bit position: 0: No interrupt request pending  
 1: Interrupt request pending

### 56.2: OT#M\_MainIRQ [1839 H, 1C39 H, 2039 H, 2439 H]

Register to mask pending interrupt requests. A masked request will not generate an outgoing IRQ to the GPPINT.

For each bit position: 0: The corresponding pending request bit is masked (DEFAULT)  
 1: The corresponding pending request bit activates signal IRQOT1/2/3/4 to GPPINT

| Signal Name | Bits | Access | Default | Description                           |
|-------------|------|--------|---------|---------------------------------------|
| Fatal       | 0    | R/W    | 0       | Fatal event occurred                  |
| CntIRQ1     | 1    | R/W    | 0       | Active request in OT#CntIRQ1 register |
| IRQ1        | 2    | R/W    | 0       | Active request in OT#IRQ1 register    |
| IRQ2        | 3    | R/W    | 0       | Active request in OT#IRQ2 register    |
| Reserved    | 7:4  |        |         | Not used                              |

### 56.3: OT#CntIRQ1 [183A H, 1C3A H, 203A H, 243A H]

Register to indicate active counter interrupt requests of this chiplet.

For each bit position: 0: No interrupt request pending  
 1: Interrupt request pending

### 56.4: OT#M\_CntIRQ1 [183B H, 1C3B H, 203B H, 243B H]

Register to mask pending counter interrupt requests.

For each bit position: 0: The corresponding pending request bit is masked (DEFAULT)  
 1: The corresponding pending request bit activates the pointer bit in OT#MainIRQ register

| Signal Name | Bits | Access | Default | Description                                    |
|-------------|------|--------|---------|--|
| OV-PTRINC   | 0    | R/W    | 0       | Overflow pointer increment counter             |
| OV-PTRDEC   | 1    | R/W    | 0       | Overflow pointer decrement counter             |
| OV-ND_EVCNT | 2    | R/W    | 0       | Overflow new data event counter                |
| OV-JUSCNT   | 3    | R/W    | 0       | Overflow justification error counter           |
| TH-JUSCNT   | 4    | R/W    | 0       | Threshold overstep justification error counter |
| Reserved    | 7:5  |        |         | Not used                                       |

### 56.5: OT#IRQ1 [183C H, 1C3C H, 203C H, 243C H]

Register to indicate active user interrupt requests of this chiplet.

For each bit position: 0: No interrupt request pending  
1: Interrupt request pending

### 56.6: OT#M\_IRQ1 [183D H, 1C3D H, 203D H, 243D H]

Register to mask pending user interrupt requests.

For each bit position: 0: The corresponding pending request bit is masked (DEFAULT)  
1: The corresponding pending request bit activates the pointer bit in OT#MainIRQ register

| Signal Name | Bits | Access | Default | Description  |
|-------------|------|--------|---------|--|
| TxLPow      | 0    | R/W    | 0       | Low Power indication from O/E module. This interrupt request bit is activated via the TXLPOW# input pin. |
| SPCIR       | 1    | R/W    | 0       | SPC FSM interrupt request  |
| FrmErr      | 2    | R/W    | 0       | Framing error detected   |
| FHigh       | 3    | R/W    | 0       | FIFO high threshold overstep   |
| FLow        | 4    | R/W    | 0       | FIFO low threshold understep   |
| DLoss       | 5    | R/W    | 0       | Data loss = Data FIFO empty  |
| FPwarn      | 6    | R/W    | 0       | Frame pulse out of sync  |
| Reserved    | 7    |        |         | Not used   |

### 56.7: OT#IRQ2 [183E H, 1C3E H, 203E H, 243E H]

Register to indicate active user interrupt requests of this chiplet.

For each bit position: 0: No interrupt request pending  
1: Interrupt request pending

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**56.8: OT#M\_IRQ2 [183F H, 1C3F H, 203F H, 243F H]**

Register to mask pending user interrupt requests.

For each bit position: 0: The corresponding pending request bit is masked (DEFAULT)

1: The corresponding pending request bit activates the pointer bit in OT#MainIRQ register

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| NewAPS      | 0    | R/W    | 0       | New debounced K1/K2 APS bytes. When the ring port is enabled, this bit is set to indicate that a New APS indication was received from the ring port. When the ring port is disabled, this bit indicates that new debounced K1/K2 APS bytes have been received from the receive line.  |
| NewK3       | 1    | R/W    | 0       | New debounced K3 byte. When the ring port is enabled, this bit is set to indicate that a New K3 indication was received from the ring port. When the ring port is disabled, this bit indicates that a new debounced K3 byte has been received from the receive line.  |
| MS_LRDI     | 2    | R/W    | 0       | MS/Line RDI in corresponding receive section. This bit is set to indicate that a MS RDI indication was received from the ring port.   |
| AIP_DLoss   | 3    | R/W    | 0       | Loss of Transmit Ring Port Data. This bit will become set if the start sequence is not detected for 1 to 2 transmit frame times. Only the interrupt and interrupt mask bits in OT1IRQ2 and OT1M_IRQ2 are used for this alarm. The corresponding mask bits in OT2M_IRQ2, OT3M_IRQ2 and OT4M_IRQ2 should always be set to 0 to avoid multiple requests. |
| APS_Fail    | 4    | R/W    | 0       | APS failure   |
| PAR_ERR     | 5    | R/W    | 0       | Telecom Bus parity error  |
| Reserved    | 7:6  |        |         | Not used  |

## OFF\_Tx1/2/3/4 Configuration Registers

### 57.1: OT#Conf1 [1848 H, 1C48 H, 2048 H, 2448 H]

Configuration register #1. General OFF\_Tx configuration signals A.

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| AutRst_Int  | 0    | R/W    | 1       | 0: No action on read access<br>1: Auto-reset interrupt request registers upon read access<br>Regardless of the setting of this bit, individual interrupt request bits can be cleared by writing a '1' to that bit provided that the corresponding alarm condition is removed. |
| AutRst_Sta  | 1    | R/W    | 1       | 0: No action on read access<br>1: Auto-reset all bits in the OT#Stat1 and OT#Stat2 status registers upon read access  |
| JusFrm      | 2    | R/W    | 0       | 0: Allow pointer modification to be performed on frame-to-frame basis<br>1: Enforces three frames being interleaved between two pointer modification operations   |
| J1Mode      | 3    | R/W    | 0       | 0: Transmit 16-byte J1 path trace<br>1: Transmit 64-byte J1 path trace  |
| SPCI(3:0)   | 7:4  | R/W    | 0000    | Specifies STM-N row number in which an interrupt request will be issued.  |

### 57.2: OT#Conf2 [1849 H, 1C49 H, 2049 H, 2449 H]

Configuration register #2. General OFF\_Tx configuration signals B.

| Signal Name | Bits | Access | Default | Description  |
|-------------|------|--------|---------|--|
| MsAIS       | 0    | R/W    | 0       | 0: No multiplex section AIS<br>1: Enforce multiplex section AIS. The MSOH and AU-4 are set to all '1's.  |
| HUG         | 1    | R/W    | 0       | 0: No unequipped STM-N signal<br>1: Enforce unequipped STM-N signal. An unequipped signal is generated by setting the C-4 and C2 POH bytes to all '0's. The other POH bytes are processed normally. The C2 value in the GRA has no effect. |
| TxSDown     | 2    | R/W    | 0       | Directly connected to output pin:<br>0: The corresponding TXSDOWN# pin is set to '0'.<br>1: The corresponding TXSDOWN# pin is set to '1'.  |
| P_AIS       | 3    | R/W    | 0       | 0: No Path AIS<br>1: Enforce Path AIS from microprocessor  |
| P_RDI(1:0)  | 5:4  | R/W    | 00      | 00: No Path RDI<br>XX: Path RDI pattern, microprocessor-enforced insertion in G1 byte  |
| MS_RDI      | 6    | R/W    | 0       | 0: No MS RDI<br>1: Enforce MS RDI from microprocessor  |
| ExtSync     | 7    | R/W    | 0       | 0: Do <b>not</b> use external frame pulse synchronization.<br>1: Use device-external frame pulse for frame synchronization   |



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**57.3: OT#Conf3-5 [184A H, 1C4A H, 204A H, 244A H; 184B H, 1C4B H, 244B H; 184C H, 1C4C H, 244C H]**

Configuration registers #3 - #5.

| Signal Name  | Bits | Access | Default  | Description   |
|--------------|------|--------|----------|---|
| FSCR(7:0)    | 7:0  | R/W    | 11111110 | OT#Conf3: Reload pattern for frame scrambler; setting this register to all-zeros results in an unmodified data stream. Setting this register to FE H enables the scrambler. Any other values are illegal. |
| ErrMask(7:0) | 7:0  | R/W    | 00000000 | OT#Conf4: Mask register forcing bit error insertion; XOR-ed with retrieved SOH/POH.   |
| ErrAddr(7:0) | 7:0  | R/W    | 00000000 | OT#Conf5: Error mask address register; indicates address of SOH/POH byte to be corrupted.   |

**57.4: OT#Conf6 [184D H, 1C4D H, 204D H, 244D H]**

Configuration register #6. Frame scrambling control register.

| Signal Name | Bits | Access | Default | Description  |
|-------------|------|--------|---------|--|
| ScrEn       | 0    | R/W    | 1       | Scramble Enable. This bit should always be set to 1.<br>0: Scrambler generator pattern is output to the line<br>1: Data from scrambler is output to line |
| CIDEn       | 1    | R/W    | 0       | CID Insertion Enable:<br>0: No CID insertion<br>1: Perform CID insertion   |
| CIDnum(5:0) | 7:2  | R/W    | 000000  | Number of all - '1'/0' bytes   |

**57.5: OT#Conf7 [184E H, 1C4E H, 204E H, 244E H]**

Configuration register #7. DCC control register.

| Signal Name | Bits | Access | Default | Description  |
|-------------|------|--------|---------|--|
| Enable      | 0    | R/W    | 0       | 0: Disable DCC processing<br>1: Enable DCC processing          |
| OpMode      | 1    | R/W    | 0       | 0: DCC1 channel (D1 - D3)<br>1: DCC2 channel (D4 - D12)        |
| ClkMode     | 2    | R/W    | 0       | 0: Continuous clock<br>1: Strobed clock (do not use this mode) |
| EdgeMode    | 3    | R/W    | 0       | 0: Active falling edge<br>1: Active rising edge                |
| Reserved    | 7:4  |        |         | Not used   |

**57.6: OT#Conf8-10 [184F H, 1C4F H, 204F H, 244F H; 1850 H, 1C50 H, 2050 H, 2450 H; 1851 H, 1C51 H, 2051 H, 2451 H]**

Configuration registers #8 - #10. FIFO threshold registers.

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| ThrLoW(5:0) | 5:0  | R/W    | 000011  | OT#Conf8: Low Water FIFO threshold, default = 3 H     |
| Reserved    | 7:6  |        |         | Not used  |
| ThrNoW(5:0) | 5:0  | R/W    | 010001  | OT#Conf9: Normal Water FIFO threshold, default = 11 H |
| Reserved    | 7:6  |        |         | Not used  |
| ThrHiW(5:0) | 5:0  | R/W    | 100000  | OT#Conf10: High Water FIFO threshold, default = 20 H  |
| Reserved    | 7:6  |        |         | Not used  |

**57.7: OT#Conf11 [1852 H, 1C52 H, 2052 H, 2452 H]**

Configuration register #11. Telecom Bus control signals.

| Signal Name       | Bits | Access | Default | Description  |
|-------------------|------|--------|---------|--|
| FRM_SLT_SEL (1:0) | 1:0  | R/W    | 00      | Slot selection for C1 pulse: These bits are used when transmit retiming is turned off and indicate which slot the C1 pulse is in.<br>00: Do not use C1 (no delay compensation)<br>01: C1 pulse on slot 1<br>10: C1 pulse on slot 2<br>11: C1 pulse on slot 3 |
| PAR_FULL          | 2    | R/W    | 0       | 0: Parity over data only<br>1: Parity over data, C1J1, SPE, FAIL   |
| PAR_EN            | 3    | R/W    | 0       | 0: No parity checking<br>1: Parity checking enabled  |
| PAR_EVEN          | 4    | R/W    | 0       | 0: Odd parity<br>1: Even parity  |
| Reserved          | 7:5  |        |         | Not used   |

**IBM SONET/SDH Framer**
**OFF\_Tx1/2/3/4 Growable Register Array (GRA) Address Map** Base Address: 1900 H - 19BF H,  
 1D00 H - 1DBF H, 2100 H - 21BF H, 2500 H - 25BF H (Sheet 1 of 4)

| Address Offset (Hex) | Byte Name <sup>1</sup> | Default (Hex) | Description |
|----------------------|------------------------|---------------|-------------|
| 00                   | A1                     | F6            | First A1    |
| 01                   | A1                     | F6            | Second A1   |
| 02                   | A1                     | F6            | Third A1    |
| 03                   | A2                     | 28            | First A2    |
| 04                   | A2                     | 28            | Second A2   |
| 05                   | A2                     | 28            | Third A2    |
| 06                   | J0                     | 55            | (C1)        |
| 07                   | X*                     | 55            | (C1)        |
| 08                   | X*                     | 55            | (C1)        |
| 09                   | B1                     | 55            |             |
| 0A                   | #                      | 55            |             |
| 0B                   | #                      | 55            |             |
| 0C                   | E1                     | 55            |             |
| 0D                   | #                      | 55            |             |
| 0E                   |                        | 55            |             |
| 0F                   | F1                     | 55            |             |
| 10                   | X                      | 55            |             |
| 11                   | X                      | 55            |             |
| 12                   | D1                     | 55            |             |
| 13                   | #                      | 55            |             |
| 14                   | #                      | 55            |             |
| 15                   | D2                     | 55            |             |
| 16                   | #                      | 55            |             |
| 17                   |                        | 55            |             |
| 18                   | D3                     | 55            |             |
| 19                   |                        | 55            |             |
| 1A                   |                        | 55            |             |
| 1B                   | H1                     | 68            |             |
| 1C                   | Y                      | 9F            |             |
| 1D                   | Y                      | 9F            |             |
| 1E                   | H2                     | 00            |             |

1. Bytes marked as "X" are reserved for national use. The "\*" character indicates bytes that are not included in frame scrambling. Therefore, care should be taken with their content. Bytes marked as "#" are media dependent bytes. All unmarked bytes are reserved for future international standardization.

**OFF\_Tx1/2/3/4 Growable Register Array (GRA) Address Map** Base Address: 1900 H - 19BF H,  
1D00 H - 1DBF H, 2100 H - 21BF H, 2500 H - 25BF H (Sheet 2 of 4)

| Address Offset (Hex) | Byte Name <sup>1</sup> | Default (Hex) | Description |
|----------------------|------------------------|---------------|-------------|
| 1F                   | 1s                     | FF            |             |
| 20                   | 1s                     | FF            |             |
| 21                   | H3                     | 55            |             |
| 22                   | H3                     | 55            |             |
| 23                   | H3                     | 55            |             |
| 24                   | B2                     | 55            |             |
| 25                   | B2                     | 55            |             |
| 26                   | B2                     | 55            |             |
| 27                   | K1                     | 00            |             |
| 28                   |                        | 55            |             |
| 29                   |                        | 55            |             |
| 2A                   | K2                     | 00            |             |
| 2B                   |                        | 55            |             |
| 2C                   |                        | 55            |             |
| 2D                   | D4                     | 55            |             |
| 2E                   |                        | 55            |             |
| 2F                   |                        | 55            |             |
| 30                   | D5                     | 55            |             |
| 31                   |                        | 55            |             |
| 32                   |                        | 55            |             |
| 33                   | D6                     | 55            |             |
| 34                   |                        | 55            |             |
| 35                   |                        | 55            |             |
| 36                   | D7                     | 55            |             |
| 37                   |                        | 55            |             |
| 38                   |                        | 55            |             |
| 39                   | D8                     | 55            |             |
| 3A                   |                        | 55            |             |
| 3B                   |                        | 55            |             |
| 3C                   | D9                     | 55            |             |
| 3D                   |                        | 55            |             |
| 3E                   |                        | 55            |             |

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**OFF\_Tx1/2/3/4 Growable Register Array (GRA) Address Map** Base Address: 1900 H - 19BF H, 1D00 H - 1DBF H, 2100 H - 21BF H, 2500 H - 25BF H (Sheet 3 of 4)

| Address Offset (Hex) | Byte Name <sup>1</sup> | Default (Hex) | Description  |
|----------------------|------------------------|---------------|--|
| 3F                   | D10                    | 55            |  |
| 40                   |                        | 55            |  |
| 41                   |                        | 55            |  |
| 42                   | D11                    | 55            |  |
| 43                   |                        | 55            |  |
| 44                   |                        | 55            |  |
| 45                   | D12                    | 55            |  |
| 46                   |                        | 55            |  |
| 47                   |                        | 55            |  |
| 48                   | S1                     | 00            |  |
| 49                   |                        | 55            |  |
| 4A                   |                        | 55            |  |
| 4B                   | M1                     | 00            | for STM-4 (STM-4c , STS-12c) in macro # 3 only and for STS-1 in the enabled macros |
| 4C                   |                        | 55            |  |
| 4D                   | M1                     | 00            | for STS-3 only in macro #3 and for STM-1 (STS-3c) in the enabled macros            |
| 4E                   | E2                     | 55            |  |
| 4F                   |                        | 55            |  |
| 50                   |                        | 55            |  |
| 51                   |                        | 55            | Reserved   |
| 52                   |                        | 55            |  |
| 53                   |                        | 55            |  |
| 54                   | J1                     | 55            | Reserved   |
| 55                   | B3                     | 55            |  |
| 56                   | C2                     | 13            |  |
| 57                   | G1                     | 00            |  |
| 58                   | F2                     | 00            |  |
| 59                   | H4                     | 00            |  |
| 5A                   | F3                     | 00            |  |
| 5B                   | K3                     | 00            |  |
| 5C                   | N1                     | 00            |  |
| 5D                   | Reserved               | 55            | Reserved   |

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**OFF\_Tx1/2/3/4 Growable Register Array (GRA) Address Map** Base Address: 1900 H - 19BF H, 1D00 H - 1DBF H, 2100 H - 21BF H, 2500 H - 25BF H (Sheet 4 of 4)

| Address Offset (Hex) | Byte Name <sup>1</sup> | Default (Hex) | Description  |
|----------------------|------------------------|---------------|--|
| 5E                   | Reserved               | 55            | Reserved   |
| 5F                   | Reserved               | 55            | Reserved   |
| 60                   | J0                     | 55            | Expected 16-byte J0 section trace                                  |
| ...                  | ..                     | ..            |  |
| 6F                   | J0                     | 55            |  |
| 70                   | J0                     | 55            | Received 16-byte J0 section trace                                  |
| ...                  | ..                     | ..            |  |
| 7F                   | J0                     | 55            |  |
| 80                   | J1                     | 55            | J1 path trace in 16-byte format                                    |
| ...                  | ..                     | ..            |  |
| 8F                   | J1                     | 55            |  |
| 90                   | J1                     | 55            | Additional registers used for 64-byte J1 path trace in free format |
| ...                  | ..                     | ..            |  |
| 1BF                  | J1                     | 55            |  |

1. Bytes marked as "X" are reserved for national use. The "\*" character indicates bytes that are not included in frame scrambling. Therefore, care should be taken with their content. Bytes marked as "#" are media dependent bytes. All unmarked bytes are reserved for future international standardization.



**IBM SONET/SDH Framer**

**OFF\_Rx1/2/3/4 Chiplet Address Map** Base Address: OFF\_Rx1 2800 H, OFF\_Rx2 2C00 H, OFF\_Rx3 3000 H, OFF\_Rx4 3400 H (Sheet 1 of 2)

| Register Name <sup>1</sup> | Address Offset (Hex) | Type/Width | Initial Value (Binary) | Description   | See Page |
|----------------------------|----------------------|------------|------------------------|---|----------|
| OR#ROFmid                  | 0                    | F 8        | 00000000               | Read-on-the-fly register  | 242      |
| OR#CntEn1                  | 2                    | X 8        | 00000000               | COUNT ENABLE register #1  | 245      |
| OR#CntEn2                  | 3                    | X 3        | 000                    | COUNT ENABLE register #2  | 245      |
| OR#Cnt1:B1BITC             | 4/5                  | N 16       | 0000 H                 | LS byte of 16-bit BIP-8 B1 bit error counter                        | 242      |
| OR#Th12:B1BITCTh2          | 6                    | X 8        | 00000000               | Threshold register Byte 2 (LSByte) for B1BITC                       | 242      |
| OR#Th11:B1BITCTh1          | 7                    | X 8        | 01111101               | Threshold register Byte 1 for counter B1BITC                        | 242      |
| OR#Cnt2:B1BLKC             | 8/9                  | N 16       | 0000 H                 | LS byte of 16-bit BIP-8 B1 block error counter                      | 242      |
| OR#Th22:B1BLKCTh2          | A                    | X 8        | 00000000               | Threshold register Byte 2 (LSByte) for B1BLKC                       | 242      |
| OR#Th21:B1BLKCTh1          | B                    | X 8        | 01111101               | Threshold register Byte 1 for counter B1BLKC                        | 242      |
| OR#Cnt3:B2BITC             | C/D                  | N 16       | 0000 H                 | LS byte of 16-bit BIP-24 B2 bit error counter, two thresholds       | 242      |
| OR#Th32d:B2BITCTh2d        | E                    | X 8        | 00100000               | Signal degradation threshold Byte 2 (LSByte) for B2BITC             | 242      |
| OR#Th31d:B2BITCTh1d        | F                    | X 8        | 01001110               | Signal degradation threshold Byte 1 for B2BITC                      | 242      |
| OR#Th32f:B2BITCTh2f        | 10                   | X 8        | 00000000               | Failure threshold Byte 2 (LSByte) for B2BITC                        | 242      |
| OR#Th31f:B2BITCTh1f        | 11                   | X 8        | 01111101               | Failure threshold Byte 1 for B2BITC                                 | 242      |
| OR#Cnt4:B2BLKC             | 12/13                | N 16       | 0000 H                 | LS byte of 16-bit BIP-24 B2 block error counter, two thresholds     | 243      |
| OR#Th42d:B2BLKCTh2d        | 14                   | X 8        | 00100000               | Signal degradation threshold Byte 2 (LSByte) for B2BLKC             | 243      |
| OR#Th41d:B2BLKCTh1d        | 15                   | X 8        | 01001110               | Signal degradation threshold Byte 1 for B2BLKC                      | 243      |
| OR#Th42f:B2BLKCTh2f        | 16                   | X 8        | 00000000               | Failure threshold Byte 2 (LSByte) for B2BLKC                        | 243      |
| OR#Th41f:B2BLKCTh1f        | 17                   | X 8        | 01111101               | Failure threshold Byte 1 for B2BLKC                                 | 243      |
| OR#Cnt5:B3BITC             | 18/19                | N 16       | 0000 H                 | LS byte of 16-bit BIP-8 B3 bit error counter                        | 243      |
| OR#Th52:B3BITCTh2          | 1A                   | X 8        | 00000000               | Threshold register Byte 2 (LSByte) for B3BITC                       | 243      |
| OR#Th51:B3BITCTh1          | 1B                   | X 8        | 01111101               | Threshold register Byte 1 for counter B3BITC                        | 243      |
| OR#Cnt6:B3BLKC             | 1C/1D                | N 16       | 0000 H                 | LS byte of 16-bit BIP-8 B3 block error counter                      | 243      |
| OR#Th62:B3BLKCTh2          | 1E                   | X 8        | 00000000               | Threshold register Byte 2 (LSByte) for B3BLKC                       | 243      |
| OR#Th61:B3BLKCTh1          | 1F                   | X 8        | 01111101               | Threshold register Byte 1 for counter B3BLKC                        | 243      |
| OR#Cnt7:MSREIC             | 20/21                | N 16       | 0000 H                 | LS byte of 16-bit multiplex section remote error indication counter | 243      |
| OR#Th72:MSREICTh2          | 22                   | X 8        | 00000000               | Threshold register Byte 2 (LSByte) for MSREIC                       | 243      |
| OR#Th71:MSREICTh1          | 23                   | X 8        | 01111101               | Threshold register Byte 1 for counter MSREIC                        | 243      |
| OR#Cnt8:HPREIC             | 24/25                | N 16       | 0000 H                 | LS byte of 16-bit higher-order path remote error indication counter | 244      |
| OR#Th82:HPREICTh2          | 26                   | X 8        | 00000000               | Threshold register Byte 2 (LSByte) for HPREIC                       | 244      |
| OR#Th81:HPREICTh1          | 27                   | X 8        | 01111101               | Threshold register Byte 1 for counter HPREIC                        | 244      |

1. # = A specific Overhead Frame Processor macro in the receive direction: 1, 2, 3, or 4.



**OFF\_Rx1/2/3/4 Chiplet Address Map** Base Address: OFF\_Rx1 2800 H, OFF\_Rx2 2C00 H, OFF\_Rx3 3000 H, OFF\_Rx4 3400 H (Sheet 2 of 2)

| Register Name <sup>1</sup> | Address Offset (Hex) | Type/Width | Initial Value (Binary) | Description                                      | See Page |
|----------------------------|----------------------|------------|------------------------|--|----------|
| OR#Cnt9:PJ_EVCNT           | 28/29                | N 8        | 00000000               | Positive justification counter, no threshold     | 244      |
| OR#Cnt10:NJ_EVCNT          | 2A/2B                | N 8        | 00000000               | Negative justification counter, no threshold     | 244      |
| OR#Cnt11:ND_EVCNT          | 2C/2D                | N 8        | 00000000               | New data event counter, no threshold             | 244      |
| OR#RESET                   | 30                   | R 1        | 1                      | Default RESET register                           | 246      |
| OR#Stat1                   | 33                   | S 3        |                        | Status register #1 (Mode; event)                 | 246      |
| OR#Stat2                   | 34                   | S 6        |                        | Status register #2 (AU pointer; event)           | 246      |
| OR#MainIRQ                 | 38                   | I 7        |                        | MAIN INTerrupt register                          | 247      |
| OR#M_MainIRQ               | 39                   | X 7        | 00000000               | INT MASK register (for OR#MainIRQ)               | 247      |
| OR#CntIRQ1                 | 3A                   | I 8        |                        | COUNTER INTerrupt register                       | 247      |
| OR#M_CntIRQ1               | 3B                   | X 8        | 00000000               | INT MASK register (for OR#CntIRQ1)               | 248      |
| OR#CntIRQ2                 | 3C                   | I 8        |                        | COUNTER INTerrupt register                       | 248      |
| OR#M_CntIRQ2               | 3D                   | X 8        | 00000000               | INT MASK register (for OR#CntIRQ2)               | 248      |
| OR#CntIRQ3                 | 3E                   | I 5        |                        | COUNTER INTerrupt register                       | 249      |
| OR#M_CntIRQ3               | 3F                   | X 5        | 00000                  | INT MASK register (for OR#CntIRQ3)               | 249      |
| OR#IRQ1                    | 40                   | I 5        |                        | USER INTerrupt register                          | 250      |
| OR#M_IRQ1                  | 41                   | X 5        | 00000                  | INT MASK register (for OR#IRQ1)                  | 250      |
| OR#IRQ2                    | 42                   | I 8        |                        | USER INTerrupt register                          | 250      |
| OR#M_IRQ2                  | 43                   | X 8        | 00000000               | INT MASK register (for OR#IRQ2)                  | 251      |
| OR#IRQ3                    | 44                   | I 8        |                        | USER INTerrupt register                          | 251      |
| OR#M_IRQ3                  | 45                   | X 8        | 00000000               | INT MASK register (for OR#IRQ3)                  | 252      |
| OR#Conf1                   | 48                   | C 8        | 00111111               | Configuration register #1 (general)              | 253      |
| OR#Conf2                   | 49                   | C 8        | 01000000               | Configuration register #2 (SOH processing)       | 254      |
| OR#Conf3                   | 4A                   | C 8        | 00100000               | Configuration register #3 (POH byte processing)  | 254      |
| OR#Conf4                   | 4B                   | C 8        | 00000000               | Configuration register #4 (APS processing)       | 255      |
| OR#Conf5                   | 4C                   | C 8        | 00000000               | Configuration register #5 (K1 shadow)            | 255      |
| OR#Conf6                   | 4D                   | C 8        | 00000000               | Configuration register #6 (K2 shadow)            | 255      |
| OR#Conf7                   | 4E                   | C 8        | 00100000               | Configuration register #7 (miscellaneous)        | 255      |
| OR#Conf8                   | 4F                   | C 8        | 11111110               | Configuration register #8 (FSCR)                 | 256      |
| OR#Conf9                   | 50                   | C 8        | 00010011               | Configuration register #9 (SL)                   | 256      |
| OR#Conf10                  | 51                   | C 8        | 00000000               | Configuration register #10 (SM)                  | 256      |
| OR#Conf11                  | 52                   | C 8        | 00000000               | Configuration register #11 (H4)                  | 256      |
| OR#Conf12                  | 53                   | C 7        | 0010101                | Configuration register #12 (RDI control)         | 256      |
| OR#Conf13                  | 54                   | C 3        | 000                    | Configuration register #13 (Telecom Bus control) | 257      |
| GRA                        | 100-3FF              |            |                        | Growable Register Array (TOH)                    | 236      |

1. # = A specific Overhead Frame Processor macro in the receive direction: 1, 2, 3, or 4.

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## OFF\_Rx1/2/3/4 (OR1/2/3/4) Counters

### 58.1: OR#ROFmid [2800 H, 2C00 H, 3000 H, 3400 H]

Read-on-the-fly register.

| Signal Name    | Bits | Access | Default  | Description                    |
|----------------|------|--------|----------|--------------------------------|
| OR#ROFmid(7:0) | 7:0  | R      | 00000000 | Read-on-the-fly register (MSB) |

### 58.2: OR#Cnt1:B1BITC, OR#Th11:B1BITCTh1, OR#Th12:B1BITCTh2

[2804 H / 2805 H, 2C04 H / 2C05 H, 3004 H / 3005 H, 3404 H / 3405 H; 2807 H, 2C07 H, 3007 H, 3407 H; 2806 H, 2C06 H, 3006 H, 3406 H]

| Signal Name    | Bits | Access | Default  | Description   |
|----------------|------|--------|----------|---|
| B1BITC(7:0)    | 7:0  | R      | 00000000 | BIP-8 B1 bit error counter (LSByte).<br>Number of BIP-8 B1 bit errors counted since last counter reset. Counter overflow leads to an interrupt request. |
| B1BITCTh1(7:0) | 7:0  | R/W    | 01111101 | Threshold for number of BIP-8 B1 bit errors (MSByte).   |
| B1BITCTh2(7:0) | 7:0  | R/W    | 00000000 | Threshold for number of BIP-8 B1 bit errors (LSByte).<br>Threshold overstep leads to an interrupt request.  |

### 58.3: OR#Cnt2:B1BLKC, OR#Th21:B1BLKCTh1, OR#Th22:B1BLKCTh2

[2808 H / 2809 H, 2C08 H / 2C09 H, 3008 H / 3009 H, 3408 H / 3409 H; 280B H, 2C0B H, 300B H, 340B H; 280A H, 2C0A H, 300A H, 340A H]

| Signal Name    | Bits | Access | Default  | Description   |
|----------------|------|--------|----------|---|
| B1BLKC(7:0)    | 7:0  | R      | 00000000 | BIP-8 B1 block error counter (LSByte).<br>Number of BIP-8 B1 block errors counted since last counter reset. Counter overflow leads to an interrupt request. |
| B1BLKCTh1(7:0) | 7:0  | R/W    | 01111101 | Threshold for number of BIP-8 B1 block errors (MSByte).   |
| B1BLKCTh2(7:0) | 7:0  | R/W    | 00000000 | Threshold for number of BIP-8 B1 block errors (LSByte).<br>Threshold overstep leads to an interrupt request.  |

### 58.4: OR#Cnt3:B2BITC, OR#Th31d:B2BITCTh1d, OR#Th32d:B2BITCTh2d, OR#Th31f:B2BITCTh1f, OR#Th32f:B2BITCTh2f [280C H / 280D H, 2C0C H / 2C0D H, 300C H / 300D H, 340C H / 340D H; 280F H, 2C0F H, 300F H, 340F H; 280E H, 2C0E H, 300E H, 340E H; 2811 H, 2C11 H, 3011 H, 3411 H; 2810 H, 2C10 H, 3010 H, 3410 H]

| Signal Name     | Bits | Access | Default  | Description   |
|-----------------|------|--------|----------|---|
| B2BITC(7:0)     | 7:0  | R      | 00000000 | Number of BIP-24 B2 bit errors counted since last counter reset (LSByte). Counter overflow leads to an interrupt request.   |
| B2BITCTh1d(7:0) | 7:0  | R/W    | 01001110 | Signal Degradation threshold for number of BIP-24 B2 bit errors (MSByte).   |
| B2BITCTh2d(7:0) | 7:0  | R/W    | 00100000 | Signal Degradation threshold for number of BIP-24 B2 bit errors (LSByte). Threshold overstep leads to an interrupt request. |
| B2BITCTh1f(7:0) | 7:0  | R/W    | 01111101 | Signal Failure threshold for number of BIP-24 B2 bit errors (MSByte).   |
| B2BITCTh2f(7:0) | 7:0  | R/W    | 00000000 | Signal Failure threshold for number of BIP-24 B2 bit errors (LSByte).<br>Threshold overstep leads to an interrupt request.  |

**58.5: OR#Cnt4:B2BLKC, OR#Th41d:B2BLKCTh1d, OR#Th42d:B2BLKCTh2d, OR#Th41f:B2BLKCTh1f, OR#Th42f:B2BLKCTh2f [2812 H / 2813 H, 2C12 H / 2C13 H, 3012 H / 3013 H, 3412 H / 3413 H; 2815 H, 2C15 H, 3015 H, 3415 H; 2814 H, 2C14 H, 3014 H, 3414 H; 2817 H, 2C17 H, 3017 H, 3417 H; 2816 H, 2C16 H, 3016 H, 3416 H]**

| Signal Name     | Bits | Access | Default  | Description   |
|-----------------|------|--------|----------|---|
| B2BLKC(7:0)     | 7:0  | R      | 00000000 | Number of BIP-24 B2 block errors counted since last counter reset (LSByte). Counter overflow leads to an interrupt request.   |
| B2BLKCTh1d(7:0) | 7:0  | R/W    | 01001110 | Signal Degradation threshold for number of BIP-24 B2 block errors (MSByte).   |
| B2BLKCTh2d(7:0) | 7:0  | R/W    | 00100000 | Signal Degradation threshold for number of BIP-24 B2 block errors (LSByte). Threshold overstep leads to an interrupt request. |
| B2BLKCTh1f(7:0) | 7:0  | R/W    | 01111101 | Signal Failure threshold for number of BIP-24 B2 block errors (MSByte).   |
| B2BLKCTh2f(7:0) | 7:0  | R/W    | 00000000 | Signal Failure threshold for number of BIP-24 B2 block errors (LSByte). Threshold overstep leads to an interrupt request.     |

**58.6: OR#Cnt5:B3BITC, OR#Th51:B3BITCTh1, OR#Th52:B3BITCTh2 [2818 H / 2819 H, 2C18 H / 2C19 H, 3018 H / 3019 H, 3418 H / 3419 H; 281B H, 2C1B H, 301B H, 341B H; 281A H, 2C1A H, 301A H, 341A H]**

| Signal Name    | Bits | Access | Default  | Description  |
|----------------|------|--------|----------|--|
| B3BITC(7:0)    | 7:0  | R      | 00000000 | Number of BIP-8 B3 bit errors counted since last counter reset (LSByte). Counter overflow leads to an interrupt request. |
| B3BITCTh1(7:0) | 7:0  | R/W    | 01111101 | Threshold for BIP-8 B3 bit error counter (MSByte).   |
| B3BITCTh2(7:0) | 7:0  | R/W    | 00000000 | Threshold for number of BIP-8 B3 bit errors (LSByte). Threshold overstep leads to an interrupt request.                  |

**58.7: OR#Cnt6:B3BLKC, OR#Th61:B3BLKCTh1, OR#Th62:B3BLKCTh2 [281C H / 281D H, 2C1C H / 2C1D H, 301C H / 301D H, 341C H / 341D H; 281F H, 2C1F H, 301F H, 341F H; 281E H, 2C1E H, 301E H, 341E H]**

| Signal Name    | Bits | Access | Default  | Description  |
|----------------|------|--------|----------|--|
| B3BLKC(7:0)    | 7:0  | R      | 00000000 | Number of BIP-8 B3 block errors counted since last counter reset (LSByte). Counter overflow leads to an interrupt request. |
| B3BLKCTh1(7:0) | 7:0  | R/W    | 01111101 | Threshold for BIP-8 B3 block error counter (MSByte).   |
| B3BLKCTh2(7:0) | 7:0  | R/W    | 00000000 | Threshold for number of BIP-8 B3 block errors (LSByte). Threshold overstep leads to an interrupt request.                  |

**58.8: OR#Cnt7:MSREIC, OR#Th71:MSREICTh1, OR#Th72:MSREICTh2 [2820 H / 2821 H, 2C20 H / 2C21 H, 3020 H / 3021 H, 3420 H / 3421 H; 2823 H, 2C23 H, 3023 H, 3423 H; 2822 H, 2C22 H, 3022 H, 3422 H]**

| Signal Name    | Bits | Access | Default  | Description   |
|----------------|------|--------|----------|---|
| MSREIC(7:0)    | 7:0  | R      | 00000000 | Multiplex Section Remote Error Indication counter (LSByte). Counter overflow leads to an interrupt request.         |
| MSREICTh1(7:0) | 7:0  | R/W    | 01111101 | Threshold for number of Multiplex Section Remote Errors (MSByte).   |
| MSREICTh2(7:0) | 7:0  | R/W    | 00000000 | Threshold for number of Multiplex Section Remote Errors (LSByte). Threshold overstep leads to an interrupt request. |

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**58.9: OR#Cnt8:HPREIC, OR#Th81:HPREICTh1, OR#Th82:HPREICTh2**

**[2824 H / 2825 H, 2C24 H / 2C25 H, 3024 H / 3025 H, 3424 H / 3425 H; 2827 H, 2C27 H, 3027 H, 3427 H; 2826 H, 2C26 H, 3026 H, 3426 H]**

| Signal Name    | Bits | Access | Default  | Description   |
|----------------|------|--------|----------|---|
| HPREIC(7:0)    | 7:0  | R      | 00000000 | Higher-Order Path Remote Error Indication counter (LSByte). Counter overflow leads to an interrupt request.         |
| HPREICTh1(7:0) | 7:0  | R/W    | 01111101 | Threshold for number of Higher-Order Path Remote Errors (MSByte).   |
| HPREICTh2(7:0) | 7:0  | R/W    | 00000000 | Threshold for number of Higher-Order Path Remote Errors (LSByte). Threshold overstep leads to an interrupt request. |

**58.10: OR#Cnt9:PJ\_EVCNT [2828 H / 2829 H, 2C28 H / 2C29 H, 3028 H / 3029 H, 3428 H / 3429 H]**

Positive Justification Event counter. Counter overflow leads to an interrupt request.

| Signal Name   | Bits | Access | Default  | Description                          |
|---------------|------|--------|----------|--------------------------------------|
| PJ_EVCNT(7:0) | 7:0  | R      | 00000000 | Positive Justification Event counter |

**58.11: OR#Cnt10:NJ\_EVCNT [282A H / 282B H, 2C2A H / 2C2B H, 302A H / 302B H, 342A H / 342B H]**

Negative Justification Event counter. Counter overflow leads to an interrupt request.

| Signal Name   | Bits | Access | Default  | Description                          |
|---------------|------|--------|----------|--------------------------------------|
| NJ_EVCNT(7:0) | 7:0  | R      | 00000000 | Negative Justification Event counter |

**58.12: OR#Cnt11:ND\_EVCNT [282C H / 282D H, 2C2C H / 2C2D H, 302C H / 302D H, 342C H / 342D H]**

New Data Event counter. Counter overflow leads to an interrupt request.

| Signal Name   | Bits | Access | Default  | Description            |
|---------------|------|--------|----------|------------------------|
| ND_EVCNT(7:0) | 7:0  | R      | 00000000 | New Data Event counter |

**58.13: OR#CntEn1 [2802 H, 2C02 H, 3002 H, 3402 H]**

Counter On/Off control register #1 for OFP\_Rx1/2/3/4.

For each bit position: 0: Counter is disabled

1: Counter is enabled

| Signal Name | Bits | Access | Default | Description  |
|-------------|------|--------|---------|--|
| EN-B1BITCNT | 0    | R/W    | 0       | BIP-8 B1 bit error counter enable                        |
| EN-B1BLKCNT | 1    | R/W    | 0       | BIP-8 B1 block error counter enable                      |
| EN-B2BITCNT | 2    | R/W    | 0       | BIP-24 B2 bit error counter enable                       |
| EN-B2BLKCNT | 3    | R/W    | 0       | BIP-24 B2 block error counter enable                     |
| EN-B3BITCNT | 4    | R/W    | 0       | BIP-8 B3 bit error counter enable                        |
| EN-B3BLKCNT | 5    | R/W    | 0       | BIP-8 B3 block error counter enable                      |
| EN-MSREICNT | 6    | R/W    | 0       | Multiplex Section Remote Error Indication counter enable |
| EN-HPREICNT | 7    | R/W    | 0       | Higher-Order Path Remote Error Indication counter enable |

**58.14: OR#CntEn2 [2803 H, 2C03 H, 3003 H, 3403 H]**

Counter On/Off control register #2 for OFP\_Rx1/2/3/4.

For each bit position: 0: Counter is disabled

1: Counter is enabled

| Signal Name | Bits | Access | Default | Description                                 |
|-------------|------|--------|---------|---|
| EN-PJ_EVCNT | 0    | R/W    | 0       | Positive Justification Event counter enable |
| EN-NJ_EVCNT | 1    | R/W    | 0       | Negative Justification Event counter enable |
| EN-ND_EVCNT | 2    | R/W    | 0       | New Data Event counter enable               |
| Reserved    | 7:3  |        |         | Not used                                    |



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**OFF\_Rx1/2/3/4 (OR1/2/3/4) Reset and Status Registers**

**59.1: OR#RESET [2830 H, 2C30 H, 3030 H, 3430 H]**

Reset chiplet control registers. These registers are automatically preset to the default value by the reset signals ResOR1/2/3/4 from the GPPINT.

For each bit position: 0: Reset not active  
1: Reset active

| Signal Name | Bits | Access | Default | Description                           |
|-------------|------|--------|---------|---------------------------------------|
| Reset       | 0    | R/W    | 1       | Reset (disable) OFF_Rx1/2/3/4 chiplet |
| Reserved    | 7:1  |        |         | Not used                              |

**59.2: OR#Stat1 [2833 H, 2C33 H, 3033 H, 3433 H]**

Status register #1 of the chiplet. OFF\_Rx Mode status information. This is an event latch register.

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| Mode(2:0)   | 2:0  | R/W    |         | Mode was active:<br>000: Single macro<br>001: Multi-macro<br>010: Concatenated<br>100: Multi-device |
| Reserved    | 7:3  |        |         | Not used  |

**59.3: OR#Stat2 [2834 H, 2C34 H, 3034 H, 3434 H]**

Status register #2 of the chiplet. AU pointer status information of OFF\_Rx. This is an event latch register.

| Signal Name | Bits | Access | Default | Description  |
|-------------|------|--------|---------|--|
| Njus        | 0    | R/W    |         | Negative frequency justification received.   |
| Pjus        | 1    | R/W    |         | Positive frequency justification received.   |
| NDF         | 2    | R/W    |         | NDF received.  |
| InvPtr      | 3    | R/W    |         | Invalid Pointer received.  |
| NewPtr      | 4    | R/W    |         | Valid New Pointer received.  |
| CONCRx      | 5    | R/W    |         | Concatenation indication received. This bit indicates that a concatenation indication was received for this macro. |
| Reserved    | 7:6  |        |         | Not used   |

## OFF\_Rx1/2/3/4 Interrupt Request and Mask Registers

### 60.1: OR#MainIRQ [2838 H, 2C38 H, 3038 H, 3438 H]

Register to indicate fatal interrupt events and to point to user IRQ registers with active requests.

For each bit position: 0: No interrupt request pending  
1: Interrupt request pending

### 60.2: OR#M\_MainIRQ [2839 H, 2C39 H, 3039 H, 3439 H]

Register to mask pending interrupt requests. A masked request will not generate an outgoing IRQ to the GPPINT.

For each bit position: 0: The corresponding pending request bit is masked (DEFAULT)  
1: The corresponding pending request bit activates signal IRQOR1/2/3/4 to GPPINT

| Signal Name | Bits | Access | Default | Description                           |
|-------------|------|--------|---------|---------------------------------------|
| Fatal       | 0    | R/W    | 0       | Fatal event occurred                  |
| CntIRQ1     | 1    | R/W    | 0       | Active request in OR#CntIRQ1 register |
| CntIRQ2     | 2    | R/W    | 0       | Active request in OR#CntIRQ2 register |
| CntIRQ3     | 3    | R/W    | 0       | Active request in OR#CntIRQ3 register |
| IRQ1        | 4    | R/W    | 0       | Active request in OR#IRQ1 register    |
| IRQ2        | 5    | R/W    | 0       | Active request in OR#IRQ2 register    |
| IRQ3        | 6    | R/W    | 0       | Active request in OR#IRQ3 register    |
| Reserved    | 7    |        |         | Not used                              |

### 60.3: OR#CntIRQ1[283A H, 2C3A H, 303A H, 343A H]

Register #1 to indicate active counter interrupt requests of this chiplet.

For each bit position: 0: No interrupt request pending  
1: Interrupt request pending

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**60.4: OR#M\_CntIRQ1 [283B H, 2C3B H, 303B H, 343B H]**

Register to mask pending counter interrupt requests.

For each bit position: 0: The corresponding pending request bit is masked (DEFAULT)  
 1: The corresponding pending request bit activates the pointer bit in OR#MainIRQ register

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| OV-B1BITCNT | 0    | R/W    | 0       | Overflow BIP-8 B1 bit error counter                               |
| TH-B1BITCNT | 1    | R/W    | 0       | Threshold overstep BIP-8 B1 bit error counter                     |
| OV-B1BLKCNT | 2    | R/W    | 0       | Overflow BIP-8 B1 block error counter                             |
| TH-B1BLKCNT | 3    | R/W    | 0       | Threshold overstep BIP-8 B1 block error counter                   |
| OV-B2BITCNT | 4    | R/W    | 0       | Overflow BIP-24 B2 bit error counter                              |
| TH-B2BITCNT | 5    | R/W    | 0       | Signal Degradation threshold overstep BIP-24 B2 bit error counter |
| T2-B2BITCNT | 6    | R/W    | 0       | Signal Failure threshold overstep BIP-24 B2 bit error counter     |
| OV-B2BLKCNT | 7    | R/W    | 0       | Overflow BIP-24 B2 block error counter                            |

**60.5: OR#CntIRQ2 [283C H, 2C3C H, 303C H, 343C H]**

Register #2 to indicate active counter interrupt requests of this chiplet.

For each bit position: 0: No interrupt request pending  
 1: Interrupt request pending

**60.6: OR#M\_CntIRQ2 [283D H, 2C3D H, 303D H, 343D H]**

Register to mask pending counter interrupt requests.

For each bit position: 0: The corresponding pending request bit is masked (DEFAULT)  
 1: The corresponding pending request bit activates the pointer bit in OR#MainIRQ register

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| TH-B2BLKCNT | 0    | R/W    | 0       | Signal Degradation threshold overstep BIP-24 B2 block error counter |
| T2-B2BLKCNT | 1    | R/W    | 0       | Failure threshold overstep BIP-24 B2 block error counter            |
| OV-B3BITCNT | 2    | R/W    | 0       | Overflow BIP-8 B3 bit error counter                                 |
| TH-B3BITCNT | 3    | R/W    | 0       | Threshold overstep BIP-8 B3 bit error counter                       |
| OV-B3BLKCNT | 4    | R/W    | 0       | Overflow BIP-8 B3 block error counter                               |
| TH-B3BLKCNT | 5    | R/W    | 0       | Threshold overstep BIP-8 B3 block error counter                     |
| OV-MSREICNT | 6    | R/W    | 0       | Overflow MS Remote Error Indication counter                         |
| TH-MSREICNT | 7    | R/W    | 0       | Threshold overstep MS Remote Error Indication counter               |

**60.7: OR#CntIRQ3 [283E H, 2C3E H, 303E H, 343E H]**

Register #3 to indicate active counter interrupt requests of this chiplet.

For each bit position: 0: No interrupt request pending

1: Interrupt request pending

**60.8: OR#M\_CntIRQ3 [283F H, 2C3F H, 303F H, 343F H]**

Register to mask pending counter interrupt requests.

For each bit position: 0: The corresponding pending request bit is masked (DEFAULT)

1: The corresponding pending request bit activates the pointer bit in OR#MainIRQ register

| Signal Name | Bits | Access | Default | Description  |
|-------------|------|--------|---------|--|
| OV-HPREICNT | 0    | R/W    | 0       | Overflow HPR error indication counter                                |
| TH-HPREICNT | 1    | R/W    | 0       | Threshold overstep Higher-Order Path Remote Error Indication counter |
| OV-PJ_EVCNT | 2    | R/W    | 0       | Overflow Positive Justification event counter                        |
| OV-NJ_EVCNT | 3    | R/W    | 0       | Overflow Negative Justification event counter                        |
| OV-ND_EVCNT | 4    | R/W    | 0       | Overflow New Data event counter                                      |
| Reserved    | 7:5  |        |         | Not used   |



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**60.9: OR#IRQ1 [2840 H, 2C40 H, 3040 H, 3440 H]**

Register to indicate active user interrupt requests of this chiplet.

For each bit position: 0: No interrupt request pending  
 1: Interrupt request pending

**60.10: OR#M\_IRQ1 [2841 H, 2C41 H, 3041 H, 3441 H]**

Register to mask pending user interrupt requests.

For each bit position: 0: The corresponding pending request bit is masked (DEFAULT)  
 1: The corresponding pending request bit activates the pointer bit in OR#MainIRQ register

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| HPREI       | 0    | R/W    | 0       | Higher-Order Path Remote Error Indication. Received HP-REI values larger than 8 do not cause this bit to become set.  |
| S1chg       | 1    | R/W    | 0       | Synchronization Status changed. If the received S1 byte differs from the expected S1 byte in OR#Conf10 for 5 (Bellcore Standard) or 3 (ITU-T Standard) consecutive frames, then this interrupt bit becomes set. When the received S1 byte matches the expected S1 byte in OR#Conf10 for 5 (Bellcore Standard) or 3 (ITU-T Standard) consecutive frames, then the interrupt signal to set this bit is removed. Note that all 8 bits of the receive S1 byte and all 8 bits of the SMexpct(7:0) register are used in the comparison. |
| FrmErr      | 2    | R/W    | 0       | Interrupt from ORxAUG FSM   |
| SDBfull     | 3    | R/W    | 0       | SDB_Rx FIFO full  |
| H4chg       | 4    | R/W    | 0       | Unexpected H4 byte received. If the received H4 byte differs from the expected H4 byte in OR#Conf11 for 5 consecutive frames, then this interrupt bit becomes set. When the received H4 byte matches the expected H4 byte in OR#Conf11 for 5 consecutive frames, then the interrupt signal to set this bit is removed.  |
| Reserved    | 7:5  |        |         | Not used  |

**60.11: OR#IRQ2 [2842 H, 2C42 H, 3042 H, 3442 H]**

Register to indicate active user interrupt requests of this chiplet.

For each bit position: 0: No interrupt request pending  
 1: Interrupt request pending

**60.12: OR#M\_IRQ2 [2843 H, 2C43 H, 3043 H, 3443 H]**

Register to mask pending user interrupt requests.

For each bit position: 0: The corresponding pending request bit is masked (DEFAULT)

1: The corresponding pending request bit activates the pointer bit in OR#MainIRQ register

| Signal Name | Bits | Access | Default | Description  |
|-------------|------|--------|---------|--|
| SLM         | 0    | R/W    | 0       | Signal label mismatch alarm. When the received C2 byte does not match the expected C2 value in the OR#Conf9 register or 01 H for 5 consecutive frames, then this bit is asserted. When the received C2 byte equals the expected C2 value in OR#Conf9 or 01 H for 5 consecutive frames, then the signal label mismatch condition is terminated. 00 H is not regarded as a signal label mismatch regardless of the setting of the OR#Conf9 register. |
| UNEQ        | 1    | R/W    | 0       | Unequipped signal. When the received C2 byte equals 00 H for 5 consecutive frames, then this bit is asserted. When the received C2 byte equals any non-zero value for 5 consecutive frames, then the unequipped signal condition is detected.  |
| HPRDI       | 2    | R/W    | 0       | Higher-order path RDI:<br>ITU mode: This bit is set when either a 1XX or 010 is received in the RDI bits. No persistency check is performed.<br>Bellcore mode: This bit is set when either 1XX or 01X is received in the RDI bit positions for 5 consecutive frames. The HPRDI condition is terminated when an 00X is detected in the RDI bits for 5 consecutive frames. The HPRDI condition is terminated when an HPAIS condition is received.    |
| HPAIS       | 3    | R/W    | 0       | Higher-order path AIS. When an STM-4c/STS-12c is being processed, in macros 2-4, this bit indicates an AISc [annex C of G.783]. Otherwise, for STM-4/STS-12 or for 4 x STM-1/STS-3c, this bit indicates AIS for its respective AU-4.   |
| LOP         | 4    | R/W    | 0       | Loss of pointer alarm. When an STM-4c/STS-12c is being processed, in macros 2-4, this bit indicates a LOPC [annex C of G.783]. Otherwise, for STM-4/STS-12 or for 4 x STM-1/STS-3c, this bit indicates LOP for its respective AU-4.  |
| LOF         | 5    | R/W    | 0       | Loss of frame alarm. This bit becomes set when a loss-of-frame condition, according to ITU-T G.707 or Bellcore GR-253, is detected.  |
| LOS         | 6    | R/W    | 0       | Loss of signal alarm. This bit is set when the corresponding LOSSIG# pin is asserted.  |
| OOF         | 7    | R/W    | 0       | Out of frame alarm.  |

**60.13: OR#IRQ3 [2844 H, 2C44 H, 3044 H, 3444 H]**

Register to indicate active user interrupt requests of this chiplet.

For each bit position: 0: No interrupt request pending

1: Interrupt request pending

**IBM SONET/SDH Framer**
**60.14: OR#M\_IRQ3 [2845 H, 2C45 H, 3045 H, 3445 H]**

Register to mask pending user interrupt requests.

For each bit position: 0: The corresponding pending request bit is masked (DEFAULT)

1: The corresponding pending request bit activates the pointer bit in OR#MainIRQ register

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| PtrErr      | 0    | R/W    | 0       | Pointer processing error.   |
| HPTIM       | 1    | R/W    | 0       | Higher-order path trace identifier mismatch.  |
| STIM        | 2    | R/W    | 0       | Section trace identifier mismatch.  |
| MSPRR       | 3    | R/W    | 0       | Multiplex Section protection release request. This bit signals a request to the external microprocessor interface to release the switch. i.e., the data stream is no longer received on the protection channel. This bit is set when the received K2 byte does not match the shadow K1 byte (K1shdrx(7:0)). Once this interrupt request is cleared by reading this bit or writing a '1' to it, it will not become set if the original condition that caused the interrupt is still present.   |
| MSPSR       | 4    | R/W    | 0       | Multiplex Section protection switch request. This bit signals a request to the external microprocessor to read the K2 byte to find the working channel (number) which must be switched to protection. This bit is set when the channel number in the corresponding K1 shadow register (K1shdrx(7:0)) matches the channel number in the received K2 byte and bit 3 of the transmitted K2 byte matches bit 3 of the received K2 byte, and the channel in the received K2 byte is not '0' and the protection channel is fail free. Once this interrupt request is cleared by reading this bit or writing a '1' to it, it will not become set if the original condition that caused the interrupt is still present. |
| MSPBR       | 5    | R/W    | 0       | Multiplex Section protection bridge request. This bit signals a request to the external microprocessor to read the K1 byte to find the working channel (number) which must be bridged to protection. This interrupt is set when the received K1 request is of a higher priority than that in the corresponding shadow register (K1shdrx(7:0) in register OR#Conf5). Once this interrupt request is cleared by reading this bit or writing a '1' to it, it will not become set if the original condition that caused the interrupt is still present.   |
| MSRDI       | 6    | R/W    | 0       | Multiplex Section RDI   |
| MSAIS       | 7    | R/W    | 0       | Multiplex Section AIS   |

## OFF\_Rx1/2/3/4 Configuration Registers

### 61.1: OR#Conf1 [2848 H, 2C48 H, 3048 H, 3448 H]

Configuration register #1. General OFF\_Rx configuration signals.

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| AutRst_Int  | 0    | R/W    | 1       | 0: No action on read access<br>1: Auto-reset interrupt request registers upon read access<br>Regardless of the setting of this bit, individual interrupt request bits can be cleared by writing a '1' to that bit provided that the corresponding alarm condition is removed. |
| AutRst_Sta  | 1    | R/W    | 1       | 0: No action on read access<br>1: Auto-reset all bits in the OR#Stat1 and OR#Stat2 status registers upon read access  |
| GRAen       | 2    | R/W    | 1       | 0: Do not write SOH/POH to GRA<br>1: Write received SOH/POH to GRA  |
| FIFOen      | 3    | R/W    | 1       | 0: Do not write C4 payload to FIFO<br>1: Write C4 payload to FIFO   |
| J0GRA       | 4    | R/W    | 1       | 0: Do not write J0 section trace to GRA<br>1: Write J0 section trace to GRA   |
| J1GRA       | 5    | R/W    | 1       | 0: Do not write J1 section trace to GRA<br>1: Write J1 section trace to GRA   |
| Bellcore    | 6    | R/W    | 0       | 0: Operate according to ITU standard<br>1: Operate according to Bellcore specs  |
| ResHunt     | 7    | R/W    | 0       | 0: Hunt free running<br>1: Reset Hunt to PIM  |

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**61.2: OR#Conf2 [2849 H, 2C49 H, 3049 H, 3449 H]**

Configuration register #2. SOH processing configuration signals.

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| J0proc      | 0    | R/W    | 0       | 0: Disable J0 section trace processing<br>1: Enable J0 section trace processing   |
| M1en        | 1    | R/W    | 0       | 0: Disable M1 REI processing<br>1: Enable M1 REI processing   |
| S1en        | 2    | R/W    | 0       | 0: Disable S1 synchronization status processing<br>1: Enable S1 synchronization status processing   |
| K2en        | 3    | R/W    | 0       | 0: Disable K2 AIS processing<br>1: Enable K2 AIS processing   |
| K1en        | 4    | R/W    | 0       | 0: Disable K1 APS processing<br>1: Enable K1 APS processing   |
| Pchan       | 5    | R/W    | 0       | This bit is used to indicate which channel is the protection channel as follows:<br>0: OFP_Rx# is working channel(#=1...4)<br>1: OFP_Rx# is protection channel (#=1...4)<br>The K1 bytes of the working channels are ignored. |
| All1En      | 6    | R/W    | 1       | 0: Disable all '1's data path forwarding<br>1: Enable all '1's data path forwarding   |
| M1BitBlk    | 7    | R/W    | 0       | 0: MS-REI bit error counting<br>1: MS-REI block error counting  |

**61.3: OR#Conf3 [284A H, 2C4A H, 304A H, 344A H]**

Configuration register #3. POH byte processing configuration signals.

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| J1proc      | 0    | R/W    | 0       | 0: Disable J1 path trace processing<br>1: Enable J1 path trace processing     |
| J1mode64    | 1    | R/W    | 0       | 0: 16-byte J1 trace<br>1: 64-byte J1 trace                                    |
| G1en        | 2    | R/W    | 0       | 0: Disable G1 path status processing<br>1: Enable G1 path status processing   |
| C2en        | 3    | R/W    | 0       | 0: Disable C2 signal label processing<br>1: Enable C2 signal label processing |
| G1BitBlk    | 4    | R/W    | 0       | 0: P-REI bit error counting<br>1: P-REI block error counting                  |
| JusITU      | 5    | R/W    | 1       | Perform Inc/Dec decoding based on:<br>0: 8-of-10<br>1: ITU-T G.707            |
| H4en        | 6    | R/W    | 0       | 0: Disable H4 byte processing<br>1: Enable H4 byte processing                 |
| K3en        | 7    | R/W    | 0       | 0: Disable K3 byte processing<br>1: Enable K3 byte processing                 |

#### 61.4: OR#Conf4 [284B H, 2C4B H, 304B H, 344B H]

Configuration register #4. APS processing configuration signals.

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| ChNum(3:0)  | 3:0  | R/W    | 0000    | Channel number  |
| Prior       | 4    | R/W    | 0       | Priority level  |
| SDFen       | 5    | R/W    | 0       | 0: Disable automatic SDF K1 processing<br>1: Enable automatic SDF K1 processing             |
| AAen        | 6    | R/W    | 0       | 0: Disable automatic Alarm processing for K2<br>1: Enable automatic Alarm processing for K2 |
| SFen        | 7    | R/W    | 0       | 0: Disable Signal Fail K2 MS_RDI processing<br>1: Enable Signal Fail K2 MS_RDI processing   |

#### 61.5: OR#Conf5-6 [284C H, 2C4C H, 304C H, 344C H; 284D H, 2C4D H, 304D H, 344D H]

Configuration registers #5/6. Shadow registers.

| Signal Name  | Bits | Access | Default  | Description   |
|--------------|------|--------|----------|---|
| K1shdrx(7:0) | 7:0  | R/W    | 00000000 | OR#Conf5: Shadows the K1 byte of the protection channel. This register is updated by the microprocessor to reflect the transmit K1 byte of the protection channel (i.e., after the microprocessor updates the transmit K1 byte, a copy of that K1 byte is written to this register).                          |
| K2shdrx(7:0) | 7:0  | R/W    | 00000000 | OR#Conf6: Shadows the K2 byte of the protection channel. This register is updated by the microprocessor to reflect the transmit K2 byte of the protection channel after a bridge operation (i.e., after the microprocessor updates the transmit K2 byte, a copy of that K2 byte is written to this register). |

#### 61.6: OR#Conf7 [284E H, 2C4E H, 304E H, 344E H]

Configuration register #7. Miscellaneous OFP\_Rx configuration signals.

| Signal Name | Bits | Access | Default | Description  |
|-------------|------|--------|---------|--|
| INnum(1:0)  | 1:0  | R/W    | 00      | Number of ms for loss-of-frame to in-frame transition                    |
| OUTnum(1:0) | 3:2  | R/W    | 00      | Number of ms for in-frame to loss-of-frame transition                    |
| DCCen       | 4    | R/W    | 0       | 0: Disable DCC processing<br>1: Enable DCC processing                    |
| OpMode      | 5    | R/W    | 1       | 0: DCC 1 channel selected<br>1: DCC 2 channel selected                   |
| ClkMode     | 6    | R/W    | 0       | 0: Continuous clock mode<br>1: Strobed clock mode (do not use this mode) |
| EdgeMode    | 7    | R/W    | 0       | 0: Active falling edge<br>1: Active rising edge                          |



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**61.7: OR#Conf8-11 [284F H, 2C4F H, 304F H, 344F H; 2850 H, 2C50 H, 3050 H, 3450 H; 2851 H, 2C51 H, 3051 H, 3451 H; 2852 H, 2C52 H, 3052 H, 3452 H]**

Configuration registers #8 - #11. Pattern registers.

| Signal Name  | Bits | Access | Default  | Description   |
|--------------|------|--------|----------|---|
| FSCRrx(7:0)  | 7:0  | R/W    | 11111110 | OR#Conf8: Frame descrambling reload pattern. Setting this register to 00 H turns off the SONET/SDH descrambler. Setting this register to FE H enables the SONET/SDH descrambler. Any values other than 00 H or FE H are not allowed.                              |
| SLexpct(7:0) | 7:0  | R/W    | 00010011 | OR#Conf9: Expected signal label. The received C2 byte is compared to the value in this register in determining if a SLM alarm has occurred.   |
| SMexpct(7:0) | 7:0  | R/W    | 00000000 | OR#Conf10: Expected synchronization message. The received S1 byte is compared to the value in this register in determining if a S1chg alarm has occurred. Note that all 8 bits of the receive S1 byte and all 8 bits of this register are used in the comparison. |
| H4expct(7:0) | 7:0  | R/W    | 00000000 | OR#Conf11: Expected H4 byte. The received H4 byte is compared to the value in this register in determining if a H4chg alarm has occurred.   |

**61.8: OR#Conf12 [2853 H, 2C53 H, 3053 H, 3453 H]**

Configuration register #12. RDI control bits.

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| SLM_RDI     | 0    | R/W    | 1       | 0: Exclude SLM defect from P-RDI<br>1: Include SLM defect in P-RDI                |
| SLM_uP      | 1    | R/W    | 0       | 0: No microprocessor-enforced SLM defect<br>1: Microprocessor-enforced SLM defect |
| TIM_RDI     | 2    | R/W    | 1       | 0: Exclude TIM defect from P-RDI<br>1: Include TIM defect in P-RDI                |
| TIM_uP      | 3    | R/W    | 0       | 0: No microprocessor-enforced TIM defect<br>1: Microprocessor-enforced TIM defect |
| LCD_RDI     | 4    | R/W    | 1       | 0: Exclude LCD defect from P-RDI<br>1: Include LCD defect in P-RDI                |
| LCD_uP      | 5    | R/W    | 0       | 0: No microprocessor-enforced LCD defect<br>1: Microprocessor-enforced LCD defect |
| EED_uP      | 6    | R/W    | 0       | 0: No microprocessor-enforced EED defect<br>1: Microprocessor-enforced EED defect |
| Reserved    | 7    |        |         | Not used  |

**61.9: OR#Conf13 [2854 H, 2C54 H, 3054 H, 3454 H]**

Configuration register #13. Telecom Bus control signals.

| Signal Name | Bits | Access | Default | Description   |
|-------------|------|--------|---------|---|
| PAR_FULL    | 0    | R/W    | 0       | 0: Parity over data only<br>1: Parity over data, C1, SPE, FAIL                      |
| PAR_EVEN    | 1    | R/W    | 0       | 0: Odd parity<br>1: Even parity   |
| CPOS        | 2    | R/W    | 0       | 0: RXTB#C1J1 pin indicates A2#3 and no J1<br>1: RXTB#C1J1 pin indicates C1#1 and J1 |
| Reserved    | 7:3  |        |         | Not used  |



**IBM SONET/SDH Framer**

**OFF\_Rx1/2/3/4 Growable Register Array (GRA) Address Map** Base Address: 2900 H - 29BF H, 2D00 H - 2DBF H, 3100 H - 31BF H, 3500 H - 35BF H (Sheet 1 of 4)

| Address Offset (Hex) | Byte Name <sup>1</sup> | Default (Hex) | Description |
|----------------------|------------------------|---------------|-------------|
| 00                   | A1                     |               | First A1    |
| 01                   | A1                     |               | Second A1   |
| 02                   | A1                     |               | Third A1    |
| 03                   | A2                     |               | First A2    |
| 04                   | A2                     |               | Second A2   |
| 05                   | A2                     |               | Third A2    |
| 06                   | J0                     |               | (C1)        |
| 07                   | X*                     |               | (C1)        |
| 08                   | X*                     |               | (C1)        |
| 09                   | B1                     |               |             |
| 0A                   | #                      |               |             |
| 0B                   | #                      |               |             |
| 0C                   | E1                     |               |             |
| 0D                   | #                      |               |             |
| 0E                   |                        |               |             |
| 0F                   | F1                     |               |             |
| 10                   | X                      |               |             |
| 11                   | X                      |               |             |
| 12                   | D1                     |               |             |
| 13                   | #                      |               |             |
| 14                   | #                      |               |             |
| 15                   | D2                     |               |             |
| 16                   | #                      |               |             |
| 17                   |                        |               |             |
| 18                   | D3                     |               |             |
| 19                   |                        |               |             |
| 1A                   |                        |               |             |
| 1B                   | H1                     |               |             |
| 1C                   | Y                      |               |             |
| 1D                   | Y                      |               |             |
| 1E                   | H2                     |               |             |

1. Bytes marked as "X" are reserved for national use. The "\*" character indicates bytes that are not included in frame scrambling. Therefore, care should be taken with their content. Bytes marked as "#" are media dependent bytes. All unmarked bytes are reserved for future international standardization.

**OFF\_Rx1/2/3/4 Growable Register Array (GRA) Address Map** Base Address: 2900 H - 29BF H, 2D00 H - 2DBF H, 3100 H - 31BF H, 3500 H - 35BF H (Sheet 2 of 4)

| Address Offset (Hex) | Byte Name <sup>1</sup> | Default (Hex) | Description |
|----------------------|------------------------|---------------|-------------|
| 1F                   | 1s                     |               |             |
| 20                   | 1s                     |               |             |
| 21                   | H3                     |               |             |
| 22                   | H3                     |               |             |
| 23                   | H3                     |               |             |
| 24                   | B2                     |               |             |
| 25                   | B2                     |               |             |
| 26                   | B2                     |               |             |
| 27                   | K1                     |               |             |
| 28                   |                        |               |             |
| 29                   |                        |               |             |
| 2A                   | K2                     |               |             |
| 2B                   |                        |               |             |
| 2C                   |                        |               |             |
| 2D                   | D4                     |               |             |
| 2E                   |                        |               |             |
| 2F                   |                        |               |             |
| 30                   | D5                     |               |             |
| 31                   |                        |               |             |
| 32                   |                        |               |             |
| 33                   | D6                     |               |             |
| 34                   |                        |               |             |
| 35                   |                        |               |             |
| 36                   | D7                     |               |             |
| 37                   |                        |               |             |
| 38                   |                        |               |             |
| 39                   | D8                     |               |             |
| 3A                   |                        |               |             |
| 3B                   |                        |               |             |
| 3C                   | D9                     |               |             |
| 3D                   |                        |               |             |
| 3E                   |                        |               |             |

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**IBM SONET/SDH Framer**

**OFF\_Rx1/2/3/4 Growable Register Array (GRA) Address Map** Base Address: 2900 H - 29BF H, 2D00 H - 2DBF H, 3100 H - 31BF H, 3500 H - 35BF H (Sheet 3 of 4)

| Address Offset (Hex) | Byte Name <sup>1</sup> | Default (Hex) | Description  |
|----------------------|------------------------|---------------|--|
| 3F                   | D10                    |               |  |
| 40                   |                        |               |  |
| 41                   |                        |               |  |
| 42                   | D11                    |               |  |
| 43                   |                        |               |  |
| 44                   |                        |               |  |
| 45                   | D12                    |               |  |
| 46                   |                        |               |  |
| 47                   |                        |               |  |
| 48                   | S1                     |               |  |
| 49                   |                        |               |  |
| 4A                   |                        | 55            |  |
| 4B                   | M1                     | 00            | for STM-4 (STM-4c , STS-12c) in macro # 3 only and for STS-1 in the enabled macros |
| 4C                   |                        | 55            |  |
| 4D                   | M1                     | 00            | for STS-3 only in macro #3 and for STM-1 (STS-3c) in the enabled macros            |
| 4E                   | E2                     | 55            |  |
| 4F                   |                        |               |  |
| 50                   |                        |               |  |
| 51                   |                        |               | Reserved   |
| 52                   |                        |               |  |
| 53                   |                        |               |  |
| 54                   | J1                     |               | Reserved   |
| 55                   | B3                     |               |  |
| 56                   | C2                     |               |  |
| 57                   | G1                     |               |  |
| 58                   | F2                     |               |  |
| 59                   | H4                     |               |  |
| 5A                   | F3                     |               |  |
| 5B                   | K3                     |               |  |
| 5C                   | N1                     |               |  |
| 5D                   | Reserved               |               | Reserved   |

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**OFF\_Rx1/2/3/4 Growable Register Array (GRA) Address Map** Base Address: 2900 H - 29BF H, 2D00 H - 2DBF H, 3100 H - 31BF H, 3500 H - 35BF H (Sheet 4 of 4)

| Address Offset (Hex) | Byte Name <sup>1</sup> | Default (Hex) | Description                                   |
|----------------------|------------------------|---------------|---|
| 5E                   | Reserved               |               | Reserved                                      |
| 5F                   | Reserved               |               | Reserved                                      |
| 60                   | J0                     |               | Expected 16-byte J0 section trace             |
| ...                  | ..                     |               |   |
| 6F                   | J0                     |               |   |
| 70                   | J0                     |               | Received 16-byte J0 section trace             |
| ...                  | ..                     |               |   |
| 7F                   | J0                     |               |   |
| 80                   | J1                     |               | Expected J1 path trace in 16-byte format      |
| ...                  | ..                     |               |   |
| 8F                   | J1                     |               |   |
| 90                   | J1                     |               | Received J1 path trace in 16-byte format      |
| ...                  | ..                     |               |   |
| 9F                   | J1                     |               |   |
| 80                   | J1                     |               | Received J1 path trace in 64-byte free format |
| ...                  | ..                     |               |   |
| BF                   | J1                     |               |   |

1. Bytes marked as "X" are reserved for national use. The "\*" character indicates bytes that are not included in frame scrambling. Therefore, care should be taken with their content. Bytes marked as "#" are media dependent bytes. All unmarked bytes are reserved for future international standardization.

## Parallel Interface Module (PIM)

The PIM module has no dynamic configuration nor interrupt request signals. It therefore has no handshaking interface with the GPPINT.

## SIM Module

The SIM module has no dynamic configuration nor interrupt request signals. It therefore has no handshaking interface with the GPPINT.

## Boundary Scan

### Boundary Scan Introduction

The IEEE 1149.1 Standard defines the requirements of a boundary scan architecture that has been specified by the IEEE Joint Test Action Group (JTAG). Boundary scan is a specialized scan architecture that provides observability and controllability for the interface pins of the device. The TAP block, which implements the boundary scan functions, consists of a TAP controller, instruction and test data registers, and a boundary scan register path bordering the input and output pins, as illustrated in Boundary Scan Schematic on page 263. The boundary scan test bus interface consists of four input signals (i.e., the Test Clock (TCK), Test Mode Select (TMS), Test Data Input (TDI) and Test Reset ( $\overline{\text{TRST}}$ ) input signals) and a Test Data Output (TDO) output signal. A brief description of boundary scan operation is provided below; further information is available in the IEEE Standard document.

The TAP controller receives external control information via a TCK, a TMS, and a  $\overline{\text{TRST}}$  signal, and it sends control signals to the internal scan paths. The scan path architecture consists of a two-bit serial instruction register, a one-bit bypass register and a 361-bit boundary scan register. The instruction and data registers are connected in parallel between the serial TDI and TDO signals. The TDI signal is routed to the instruction, bypass and boundary scan registers and is used to transfer serial data into a register during a scan operation. The data to the TDO signal is selected from either register during a scan operation. When boundary scan testing is not being performed, the boundary scan register is transparent, allowing the input and output signals at the device pins to pass to and from the SONET/SDH framer's internal logic, as illustrated in Boundary Scan Schematic on page 263. During boundary scan testing, the boundary scan register disables the normal flow of input and output signals to allow the device to be controlled and observed via scan operations. A timing diagram for the boundary scan feature is provided in Boundary Scan Timing on page 74.

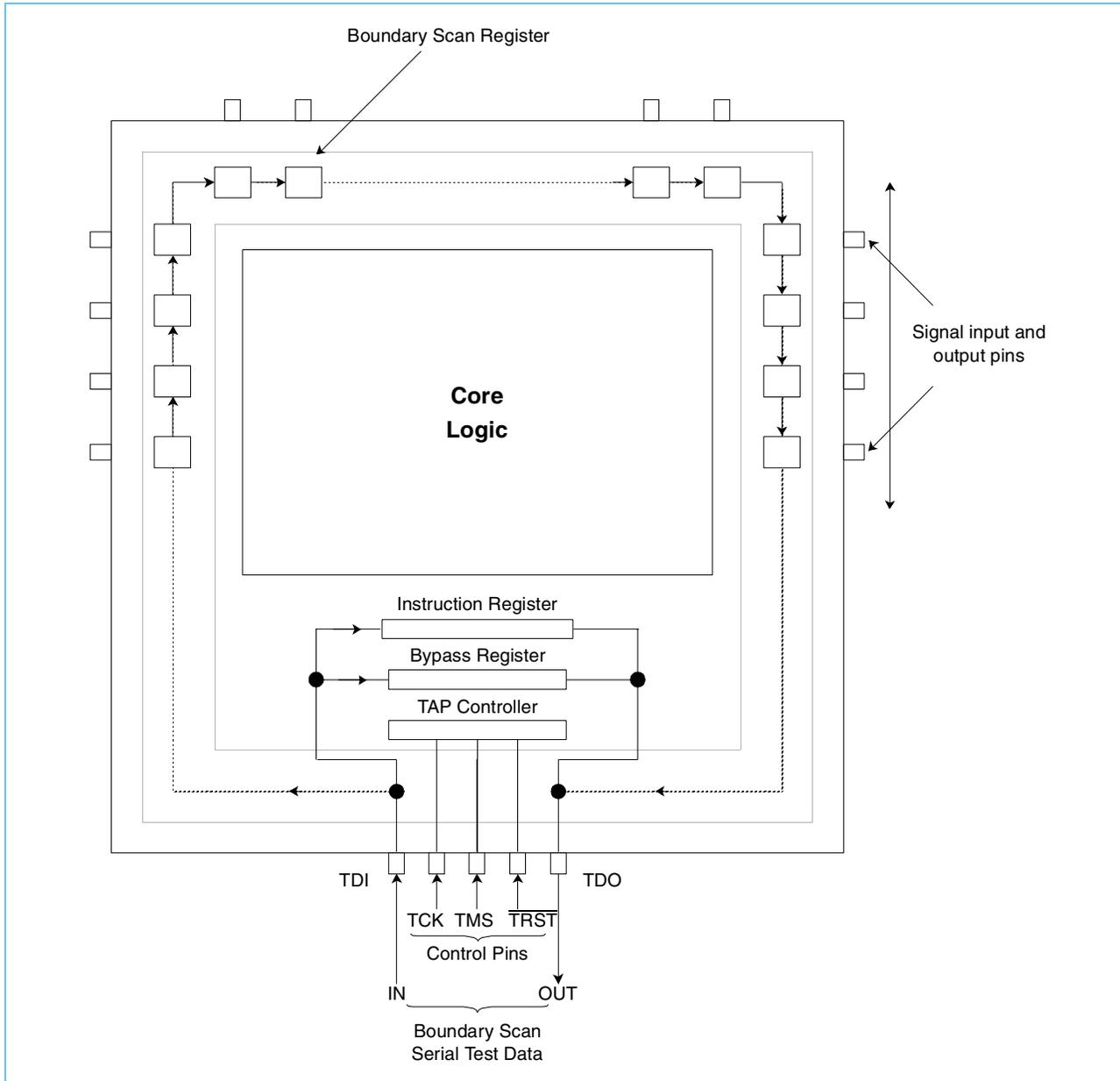
### Boundary Scan Support

The maximum frequency the SONET/SDH framer will support for boundary scan is 20 MHz. The SONET/SDH framer performs the following boundary scan test instructions (ID commands and ID Register are not supported):

- EXTEST (00)** One of the required boundary scan tests is the external boundary test (EXTEST) instruction. When this instruction is shifted in, the SONET/SDH framer is forced into an off-line test mode. While in this test mode, the test bus can shift data through the boundary scan registers to control the external SONET/SDH framer input and output pins.
- SAMPLE/PRELOAD (01)** When the SAMPLE/PRELOAD instruction is shifted in, the SONET/SDH framer remains fully operational. While in this test mode, SONET/SDH framer input data, and data destined for device outputs, can be captured and shifted out for inspection. The data is captured in response to control signals sent to the TAP controller.
- BYPASS (11)** When the BYPASS instruction is shifted in, the SONET/SDH framer remains fully operational. While in this test mode, a scan operation will transfer serial data from the TDI input, through an internal scan cell, to the TDO pin. The purpose of this instruction is to abbreviate the scan path through the circuits that are not being tested to only a single clock delay.
- Boundary Scan Reset** Specific control of the  $\overline{\text{TRST}}$  pin is required in order to ensure that the boundary scan logic does not interfere with normal device operation. This pin should be held low whenever boundary scan operations are not being performed.

**Note:** The CAPTURE - IR State (INSTRUCTION\_CAPTURE attribute of BSDL) is "01".

### Boundary Scan Schematic



**IBM SONET/SDH Framer**
**Boundary Scan Chain**

There are 361 scan cells in the SONET/SDH framer boundary scan chain. Bidirectional device pins have combined input/output scan cells. Additional scan cells are used for direction control as needed. The following table shows the listed order of the scan cells and their functions. Cells that are not associated with a pin are marked "NA" in the "Pin No." column. A '1' written to a control cell will cause the outputs that it controls to be enabled. A '0' written to a control cell will cause the outputs that it controls to go to the tri-state condition.

**Scan Cells** (Sheet 1 of 11)

| Scan Cell No. | I/O | Pin No. | Symbol    | Comments     |
|---------------|-----|---------|-----------|--------------|
|               | I   | T17     | TDI       | [SCAN Input] |
| 360           | O   | D11     | MUXDIVCLK | Output2      |
| 359           | O   | P10     | ALARM4(4) | Output2      |
| 358           | O   | N09     | ALARM4(3) | Output2      |
| 357           | O   | M10     | ALARM4(2) | Output2      |
| 356           | O   | L09     | ALARM4(1) | Output2      |
| 355           | O   | J11     | ALARM4(0) | Output2      |
| 354           | O   | E07     | ALARM3(4) | Output2      |
| 353           | O   | C05     | ALARM3(3) | Output2      |
| 352           | O   | T05     | ALARM3(2) | Output2      |
| 351           | O   | T03     | ALARM3(1) | Output2      |
| 350           | O   | T01     | ALARM3(0) | Output2      |
| 349           | O   | P05     | ALARM2(4) | Output2      |
| 348           | O   | P03     | ALARM2(3) | Output2      |
| 347           | O   | P01     | ALARM2(2) | Output2      |
| 346           | O   | M03     | ALARM2(1) | Output2      |
| 345           | O   | M01     | ALARM2(0) | Output2      |
| 344           | O   | K05     | ALARM1(4) | Output2      |
| 343           | O   | K03     | ALARM1(3) | Output2      |
| 342           | O   | K01     | ALARM1(2) | Output2      |
| 341           | O   | H03     | ALARM1(1) | Output2      |
| 340           | O   | H01     | ALARM1(0) | Output2      |
| 339           | O   | V15     | RXRINGCLK | Output2      |
| 338           | O   | V14     | RXRINGD   | Output2      |
| 337           | I   | V13     | TXRINGCLK | Input        |
| 336           | I   | V12     | TXRINGD   | Input        |
| 335           | O   | T14     | TXFRMOUT  | Output2      |
| 334           | I   | T13     | TXFRMIN   | Input        |
| 333           | O   | U13     | RXEXPOUT  | Output2      |
| 332           | I   | T12     | RXEXPIN   | Input        |
| 331           | O   | R11     | TXEXPOUT  | Output2      |

**Scan Cells** (Sheet 2 of 11)

| Scan Cell No. | I/O | Pin No. | Symbol      | Comments  |
|---------------|-----|---------|-------------|---|
| 330           | I   | R09     | TXEXPIN     | Input   |
| 329           | --  | --      | Control     | Control. This is not a pin. This cell controls the RXAPSDAVA, RXAPSPAR, and RXAPSDAT(0:2) pins. |
| 328           | --  | --      | Control     | Control. This is not a pin. This cell controls the RXAPSDAT(3:8) pins.                          |
| 327           | I/O | G15     | RXAPSDAVA   | Bidirectional   |
| 326           | I/O | H15     | RXAPSPAR    | Bidirectional   |
| 325           | I/O | H14     | RXAPSDAT(0) | Bidirectional   |
| 324           | I/O | J15     | RXAPSDAT(1) | Bidirectional   |
| 323           | I/O | J13     | RXAPSDAT(2) | Bidirectional   |
| 322           | I/O | K14     | RXAPSDAT(3) | Bidirectional   |
| 321           | I/O | K13     | RXAPSDAT(4) | Bidirectional   |
| 320           | I/O | K12     | RXAPSDAT(5) | Bidirectional   |
| 319           | I/O | K11     | RXAPSDAT(6) | Bidirectional   |
| 318           | I/O | L15     | RXAPSDAT(7) | Bidirectional   |
| 317           | I/O | L13     | RXAPSDAT(8) | Bidirectional   |
| 316           | --  | --      | Control     | Control. This is not a pin. This cell controls the TXAPSDARQ pin.                               |
| 315           | I/O | L11     | TXAPSDARQ   | Bidirectional   |
| 314           | --  | --      | Control     | Control. This is not a pin. This cell controls the TXAPSDAVA, TXAPSPAR, and TXAPSDAT(0:2) pins. |
| 313           | --  | --      | Control     | Control. This is not a pin. This cell controls the TXAPSDAT(3:8) pins.                          |
| 312           | I/O | M14     | TXAPSDAVA   | Bidirectional   |
| 311           | I/O | M13     | TXAPSPAR    | Bidirectional   |
| 310           | I/O | M12     | TXAPSDAT(0) | Bidirectional   |
| 309           | I/O | N15     | TXAPSDAT(1) | Bidirectional   |
| 308           | I/O | N13     | TXAPSDAT(2) | Bidirectional   |
| 307           | I/O | N11     | TXAPSDAT(3) | Bidirectional   |
| 306           | I/O | P14     | TXAPSDAT(4) | Bidirectional   |
| 305           | I/O | P13     | TXAPSDAT(5) | Bidirectional   |
| 304           | I/O | P12     | TXAPSDAT(6) | Bidirectional   |
| 303           | I/O | R15     | TXAPSDAT(7) | Bidirectional   |
| 302           | I/O | R13     | TXAPSDAT(8) | Bidirectional   |
| 301           | O   | AE15    | R1DCLK4     | Output2   |
| 300           | O   | AE13    | R1DCLK3     | Output2   |
| 299           | O   | AE09    | R1DCLK2     | Output2   |
| 298           | O   | AE07    | R1DCLK1     | Output2   |
| 297           | O   | AC15    | R1DATA4     | Output2   |

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## Scan Cells (Sheet 3 of 11)

| Scan Cell No. | I/O | Pin No. | Symbol  | Comments  |
|---------------|-----|---------|---|---|
| 296           | O   | AC13    | R1DATA3   | Output2   |
| 295           | O   | AC11    | R1DATA2   | Output2   |
| 294           | O   | AC09    | R1DATA1   | Output2   |
| 293           | O   | AA13    | T1DCLK4   | Output2   |
| 292           | O   | AA11    | T1DCLK3   | Output2   |
| 291           | O   | AA09    | T1DCLK2   | Output2   |
| 290           | O   | AA07    | T1DCLK1   | Output2   |
| 289           | I   | Y19     | T1DATA4   | Input   |
| 288           | I   | AA19    | T1DATA3   | Input   |
| 287           | I   | AB19    | T1DATA2   | Input   |
| 286           | I   | AC19    | T1DATA1   | Input   |
| 285           | I   | W13     | INTFSELECT  | Input   |
| 284           | I   | AD19    | INTFMODE  | Input   |
| 283           | --  | --      | Control   | Control. This is not a pin. This cell controls the $\overline{\text{GPINT}}$ pin.                               |
| 282           | I/O | W15     | $\overline{\text{GPINT}}$                                   | Bidirectional   |
| 281           | I   | AB13    | $\overline{\text{GPSEL}}$                                   | Input   |
| 280           | --  | --      | Control   | Control. This is not a pin. This cell controls the $\overline{\text{GPDTACK}}$ , $\overline{\text{GPRDY}}$ pin. |
| 279           | I/O | Y12     | $\overline{\text{GPDTACK}}$ , $\overline{\text{GPRDY}}$     | Bidirectional   |
| 278           | I   | AD13    | $\overline{\text{GPDS}}$ , $\overline{\text{GPRD}}$         | Input   |
| 277           | I   | AE12    | $\text{GPR}/\overline{\text{W}}$ , $\overline{\text{GPWR}}$ | Input   |
| 276           | I   | Y16     | GPADDR(0)   | Input   |
| 275           | I   | AA16    | GPADDR(1)   | Input   |
| 274           | I   | AB16    | GPADDR(2)   | Input   |
| 273           | I   | AD16    | GPADDR(3)   | Input   |
| 272           | I   | AE16    | GPADDR(4)   | Input   |
| 271           | I   | Y15     | GPADDR(5)   | Input   |
| 270           | I   | AA15    | GPADDR(6)   | Input   |
| 269           | I   | AB15    | GPADDR(7)   | Input   |
| 268           | I   | AD15    | GPADDR(8)   | Input   |
| 267           | I   | Y14     | GPADDR(9)   | Input   |
| 266           | I   | AB14    | GPADDR(10)  | Input   |
| 265           | I   | AC14    | GPADDR(11)  | Input   |
| 264           | I   | AE14    | GPADDR(12)  | Input   |
| 263           | I   | Y13     | GPADDR(13)  | Input   |
| 262           | --  | --      | Control   | Control. This is not a pin. This cell controls the GPDATA(7:0) pins.  |
| 261           | I/O | AB18    | GPDATA(0)   | Bidirectional   |

**Scan Cells** (Sheet 4 of 11)

| Scan Cell No. | I/O | Pin No. | Symbol       | Comments  |
|---------------|-----|---------|--------------|---|
| 260           | I/O | AC18    | GPDATA(1)    | Bidirectional   |
| 259           | I/O | AD18    | GPDATA(2)    | Bidirectional   |
| 258           | I/O | AE18    | GPDATA(3)    | Bidirectional   |
| 257           | I/O | AB17    | GPDATA(4)    | Bidirectional   |
| 256           | I/O | AC17    | GPDATA(5)    | Bidirectional   |
| 255           | I/O | AD17    | GPDATA(6)    | Bidirectional   |
| 254           | I/O | AE17    | GPDATA(7)    | Bidirectional   |
| 253           | I   | AE11    | GPPCLK       | Input   |
| 252           | --  | --      | Control      | Control. This is not a pin. This cell controls the RXTB4FAIL, RXTB4PAR, RXTB4SPE, and RXTB4C1J1 pins. |
| 251           | I/O | Y06     | RXTB4FAIL    | Bidirectional   |
| 250           | I/O | AA05    | RXTB4PAR     | Bidirectional   |
| 249           | I/O | AB05    | RXTB4SPE     | Bidirectional   |
| 248           | I/O | AA04    | RXTB4C1J1    | Bidirectional   |
| 247           | I/O | AB04    | RXTB4CLK     | Bidirectional   |
| 246           | --  | --      | Control      | Control. This is not a pin. This cell controls the RXTB4DATA(7:0) pins.                               |
| 245           | I/O | AD04    | RXTB4DATA(0) | Bidirectional   |
| 244           | I/O | AE04    | RXTB4DATA(1) | Bidirectional   |
| 243           | I/O | AC03    | RXTB4DATA(2) | Bidirectional   |
| 242           | I/O | AD03    | RXTB4DATA(3) | Bidirectional   |
| 241           | I/O | AE03    | RXTB4DATA(4) | Bidirectional   |
| 240           | I/O | AD02    | RXTB4DATA(5) | Bidirectional   |
| 239           | I/O | AE02    | RXTB4DATA(6) | Bidirectional   |
| 238           | I/O | AD01    | RXTB4DATA(7) | Bidirectional   |
| 237           | --  | --      | Control      | Control. This is not a pin. This cell controls the RXTB3FAIL, RXTB3PAR, RXTB3SPE, and RXTB3C1J1 pins. |
| 236           | I/O | AC02    | RXTB3FAIL    | Bidirectional   |
| 235           | I/O | AC01    | RXTB3PAR     | Bidirectional   |
| 234           | I/O | AB03    | RXTB3SPE     | Bidirectional   |
| 233           | I/O | AB02    | RXTB3C1J1    | Bidirectional   |
| 232           | I/O | AB01    | RXTB3CLK     | Bidirectional   |
| 231           | --  | --      | Control      | Control. This is not a pin. This cell controls the RXTB3DATA(7:0) pins.                               |
| 230           | I/O | AA03    | RXTB3DATA(0) | Bidirectional   |
| 229           | I/O | AA01    | RXTB3DATA(1) | Bidirectional   |
| 228           | I/O | Y05     | RXTB3DATA(2) | Bidirectional   |
| 227           | I/O | Y04     | RXTB3DATA(3) | Bidirectional   |

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## Scan Cells (Sheet 5 of 11)

| Scan Cell No. | I/O | Pin No. | Symbol       | Comments  |
|---------------|-----|---------|--------------|---|
| 226           | I/O | Y03     | RXTB3DATA(4) | Bidirectional   |
| 225           | I/O | Y02     | RXTB3DATA(5) | Bidirectional   |
| 224           | I/O | Y01     | RXTB3DATA(6) | Bidirectional   |
| 223           | I/O | W05     | RXTB3DATA(7) | Bidirectional   |
| 222           | --  | --      | Control      | Control. This is not a pin. This cell controls the RXTB2FAIL, RXTB2PAR, RXTB2SPE, and RXTB2C1J1 pins. |
| 221           | I/O | W03     | RXTB2FAIL    | Bidirectional   |
| 220           | I/O | W02     | RXTB2PAR     | Bidirectional   |
| 219           | I/O | W01     | RXTB2SPE     | Bidirectional   |
| 218           | I/O | V07     | RXTB2C1J1    | Bidirectional   |
| 217           | I/O | V06     | RXTB2CLK     | Bidirectional   |
| 216           | --  | --      | Control      | Control. This is not a pin. This cell controls the RXTB2DATA(7:0) pins.                               |
| 215           | I/O | V05     | RXTB2DATA(0) | Bidirectional   |
| 214           | I/O | V04     | RXTB2DATA(1) | Bidirectional   |
| 213           | I/O | V02     | RXTB2DATA(2) | Bidirectional   |
| 212           | I/O | U07     | RXTB2DATA(3) | Bidirectional   |
| 211           | I/O | U05     | RXTB2DATA(4) | Bidirectional   |
| 210           | I/O | U03     | RXTB2DATA(5) | Bidirectional   |
| 209           | I/O | U01     | RXTB2DATA(6) | Bidirectional   |
| 208           | I/O | T07     | RXTB2DATA(7) | Bidirectional   |
| 207           | --  | --      | Control      | Control. This is not a pin. This cell controls the RXTB1FAIL, RXTB1PAR, RXTB1SPE, and RXTB1C1J1 pins. |
| 206           | I/O | T06     | RXTB1FAIL    | Bidirectional   |
| 205           | I/O | T04     | RXTB1PAR     | Bidirectional   |
| 204           | I/O | T02     | RXTB1SPE     | Bidirectional   |
| 203           | I/O | R07     | RXTB1C1J1    | Bidirectional   |
| 202           | I/O | R05     | RXTB1CLK     | Bidirectional   |
| 201           | --  | --      | Control      | Control. This is not a pin. This cell controls the RXTB1DATA(7:0) pins.                               |
| 200           | I/O | R03     | RXTB1DATA(0) | Bidirectional   |
| 199           | I/O | R02     | RXTB1DATA(1) | Bidirectional   |
| 198           | I/O | R01     | RXTB1DATA(2) | Bidirectional   |
| 197           | I/O | P08     | RXTB1DATA(3) | Bidirectional   |
| 196           | I/O | P07     | RXTB1DATA(4) | Bidirectional   |
| 195           | I/O | P06     | RXTB1DATA(5) | Bidirectional   |
| 194           | I/O | P04     | RXTB1DATA(6) | Bidirectional   |
| 193           | I/O | P02     | RXTB1DATA(7) | Bidirectional   |

**Scan Cells** (Sheet 6 of 11)

| Scan Cell No. | I/O | Pin No. | Symbol       | Comments |
|---------------|-----|---------|--------------|----------|
| 192           | I   | M04     | TXTB4FAIL    | Input    |
| 191           | I   | M02     | TXTB4PAR     | Input    |
| 190           | I   | N07     | TXTB4SPE     | Input    |
| 189           | I   | N05     | TXTB4C1J1    | Input    |
| 188           | I   | N03     | TXTB4CLK     | Input    |
| 187           | I   | L07     | TXTB4DATA(0) | Input    |
| 186           | I   | L05     | TXTB4DATA(1) | Input    |
| 185           | I   | L03     | TXTB4DATA(2) | Input    |
| 184           | I   | L02     | TXTB4DATA(3) | Input    |
| 183           | I   | L01     | TXTB4DATA(4) | Input    |
| 182           | I   | M08     | TXTB4DATA(5) | Input    |
| 181           | I   | M07     | TXTB4DATA(6) | Input    |
| 180           | I   | M06     | TXTB4DATA(7) | Input    |
| 179           | I   | J01     | TXTB3FAIL    | Input    |
| 178           | I   | K07     | TXTB3PAR     | Input    |
| 177           | I   | K06     | TXTB3SPE     | Input    |
| 176           | I   | K04     | TXTB3C1J1    | Input    |
| 175           | I   | K02     | TXTB3CLK     | Input    |
| 174           | I   | H07     | TXTB3DATA(0) | Input    |
| 173           | I   | H06     | TXTB3DATA(1) | Input    |
| 172           | I   | H05     | TXTB3DATA(2) | Input    |
| 171           | I   | H04     | TXTB3DATA(3) | Input    |
| 170           | I   | H02     | TXTB3DATA(4) | Input    |
| 169           | I   | J07     | TXTB3DATA(5) | Input    |
| 168           | I   | J05     | TXTB3DATA(6) | Input    |
| 167           | I   | J03     | TXTB3DATA(7) | Input    |
| 166           | I   | F01     | TXTB2FAIL    | Input    |
| 165           | I   | G05     | TXTB2PAR     | Input    |
| 164           | I   | G03     | TXTB2SPE     | Input    |
| 163           | I   | G02     | TXTB2C1J1    | Input    |
| 162           | I   | G01     | TXTB2CLK     | Input    |
| 161           | I   | C02     | TXTB2DATA(0) | Input    |
| 160           | I   | C01     | TXTB2DATA(1) | Input    |
| 159           | I   | D02     | TXTB2DATA(2) | Input    |
| 158           | I   | D01     | TXTB2DATA(3) | Input    |
| 157           | I   | E01     | TXTB2DATA(4) | Input    |

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## Scan Cells (Sheet 7 of 11)

| Scan Cell No. | I/O | Pin No. | Symbol                     | Comments  |
|---------------|-----|---------|----------------------------|---|
| 156           | I   | F04     | TXTB2DATA(5)               | Input   |
| 155           | I   | F03     | TXTB2DATA(6)               | Input   |
| 154           | I   | F02     | TXTB2DATA(7)               | Input   |
| 153           | I   | E03     | TXTB1FAIL                  | Input   |
| 152           | I   | D03     | TXTB1PAR                   | Input   |
| 151           | I   | C03     | TXTB1SPE                   | Input   |
| 150           | I   | B02     | TXTB1C1J1                  | Input   |
| 149           | I   | B01     | TXTB1CLK                   | Input   |
| 148           | I   | F05     | TXTB1DATA(0)               | Input   |
| 147           | I   | E04     | TXTB1DATA(1)               | Input   |
| 146           | I   | D04     | TXTB1DATA(2)               | Input   |
| 145           | I   | B04     | TXTB1DATA(3)               | Input   |
| 144           | I   | A04     | TXTB1DATA(4)               | Input   |
| 143           | I   | B03     | TXTB1DATA(5)               | Input   |
| 142           | I   | A03     | TXTB1DATA(6)               | Input   |
| 141           | I   | A02     | TXTB1DATA(7)               | Input   |
| 140           | O   | F06     | TXCFRM                     | Output2   |
| 139           | O   | E05     | $\overline{\text{TXCCLK}}$ | Output2   |
| 138           | O   | D05     | TXCCLK                     | Output2   |
| 137           | --  | --      | Control                    | Control. This is not a pin. This cell controls the RXABTO pin.    |
| 136           | I/O | T11     | RXABTO                     | Bidirectional   |
| 135           | --  | --      | Control                    | Control. This is not a pin. This cell controls the RXFCSEO pin.   |
| 134           | I/O | U11     | RXFCSEO                    | Bidirectional   |
| 133           | --  | --      | Control                    | Control. This is not a pin. This cell controls the RXMSO pin.     |
| 132           | I/O | T10     | RXMSO                      | Bidirectional   |
| 131           | --  | --      | Control                    | Control. This is not a pin. This cell controls the RXEOFO pin.    |
| 130           | I/O | T09     | RXEOFO                     | Bidirectional   |
| 129           | --  | --      | Control                    | Control. This is not a pin. This cell controls the RXCLAV(3) pin. |
| 128           | --  | --      | Control                    | Control. This is not a pin. This cell controls the RXCLAV(2) pin. |
| 127           | --  | --      | Control                    | Control. This is not a pin. This cell controls the RXCLAV(1) pin. |
| 126           | --  | --      | Control                    | Control. This is not a pin. This cell controls the RXCLAV(0) pin. |
| 125           | I/O | V11     | RXCLAV(3)                  | Bidirectional   |
| 124           | I/O | W11     | RXCLAV(2)                  | Bidirectional   |
| 123           | I/O | Y11     | RXCLAV(1)                  | Bidirectional   |
| 122           | I/O | AB12    | RXCLAV(0)                  | Bidirectional   |
| 121           | I   | AE06    | $\overline{\text{RXENB}}$  | Input   |

**Scan Cells** (Sheet 8 of 11)

| Scan Cell No. | I/O | Pin No. | Symbol      | Comments   |
|---------------|-----|---------|-------------|--|
| 120           | --  | --      | Control     | Control. This is not a pin. This cell controls the RXSOFO, RXSOC, and RXPRTY pins. |
| 119           | I/O | U09     | RXSOFO      | Bidirectional  |
| 118           | I/O | AD12    | RXSOC       | Bidirectional  |
| 117           | I/O | V10     | RXPRTY      | Bidirectional  |
| 116           | I   | AD11    | RXUADDR(0)  | Input  |
| 115           | I   | AB11    | RXUADDR(1)  | Input  |
| 114           | I   | AB10    | RXUADDR(2)  | Input  |
| 113           | I   | AC10    | RXUADDR(3)  | Input  |
| 112           | I   | AE10    | RXUADDR(4)  | Input  |
| 111           | --  | --      | Control     | Control. This is not a pin. This cell controls the RXUDATA(7:0) pins.              |
| 110           | --  | --      | Control     | Control. This is not a pin. This cell controls the RXUDATA(15:8) pins.             |
| 109           | I/O | Y10     | RXUDATA(0)  | Bidirectional  |
| 108           | I/O | V09     | RXUDATA(1)  | Bidirectional  |
| 107           | I/O | W09     | RXUDATA(2)  | Bidirectional  |
| 106           | I/O | Y09     | RXUDATA(3)  | Bidirectional  |
| 105           | I/O | AB09    | RXUDATA(4)  | Bidirectional  |
| 104           | I/O | AD09    | RXUDATA(5)  | Bidirectional  |
| 103           | I/O | V08     | RXUDATA(6)  | Bidirectional  |
| 102           | I/O | Y08     | RXUDATA(7)  | Bidirectional  |
| 101           | I/O | AB08    | RXUDATA(8)  | Bidirectional  |
| 100           | I/O | AD08    | RXUDATA(9)  | Bidirectional  |
| 99            | I/O | AE08    | RXUDATA(10) | Bidirectional  |
| 98            | I/O | Y07     | RXUDATA(11) | Bidirectional  |
| 97            | I/O | AB07    | RXUDATA(12) | Bidirectional  |
| 96            | I/O | AD07    | RXUDATA(13) | Bidirectional  |
| 95            | I/O | AB06    | RXUDATA(14) | Bidirectional  |
| 94            | I/O | AC06    | RXUDATA(15) | Bidirectional  |
| 93            | I   | AD05    | RXUCLK2     | Input  |
| 92            | I   | AE05    | RXUCLK1     | Input  |
| 91            | --  | --      | Control     | Control. This is not a pin. This cell controls the TXABTO pin.                     |
| 90            | I/O | F12     | TXABTO      | Bidirectional  |
| 89            | I   | K10     | TXMSI       | Input  |
| 88            | I   | H11     | TXEOF1      | Input  |
| 87            | --  | --      | Control     | Control. This is not a pin. This cell controls the TXCLAV(3) pin.                  |
| 86            | --  | --      | Control     | Control. This is not a pin. This cell controls the TXCLAV(2) pin.                  |

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## Scan Cells (Sheet 9 of 11)

| Scan Cell No. | I/O | Pin No. | Symbol                    | Comments  |
|---------------|-----|---------|---------------------------|---|
| 85            | --  | --      | Control                   | Control. This is not a pin. This cell controls the TXCLAV(1) pin. |
| 84            | --  | --      | Control                   | Control. This is not a pin. This cell controls the TXCLAV(0) pin. |
| 83            | I/O | G07     | TXCLAV(3)                 | Bidirectional   |
| 82            | I/O | F07     | TXCLAV(2)                 | Bidirectional   |
| 81            | I/O | D07     | TXCLAV(1)                 | Bidirectional   |
| 80            | I/O | A06     | TXCLAV(0)                 | Bidirectional   |
| 79            | I   | K09     | $\overline{\text{TXENB}}$ | Input   |
| 78            | I   | G11     | TXSOFI                    | Input   |
| 77            | I   | D12     | TXSOC                     | Input   |
| 76            | I   | D13     | TXPRTY                    | Input   |
| 75            | I   | B12     | TXUADDR(0)                | Input   |
| 74            | I   | B11     | TXUADDR(1)                | Input   |
| 73            | I   | C10     | TXUADDR(2)                | Input   |
| 72            | I   | A10     | TXUADDR(3)                | Input   |
| 71            | I   | B09     | TXUADDR(4)                | Input   |
| 70            | I   | F11     | TXUDATA(0)                | Input   |
| 69            | I   | H10     | TXUDATA(1)                | Input   |
| 68            | I   | F10     | TXUDATA(2)                | Input   |
| 67            | I   | D10     | TXUDATA(3)                | Input   |
| 66            | I   | J09     | TXUDATA(4)                | Input   |
| 65            | I   | H09     | TXUDATA(5)                | Input   |
| 64            | I   | G09     | TXUDATA(6)                | Input   |
| 63            | I   | F09     | TXUDATA(7)                | Input   |
| 62            | I   | D09     | TXUDATA(8)                | Input   |
| 61            | I   | K08     | TXUDATA(9)                | Input   |
| 60            | I   | H08     | TXUDATA(10)               | Input   |
| 59            | I   | F08     | TXUDATA(11)               | Input   |
| 58            | I   | D08     | TXUDATA(12)               | Input   |
| 57            | I   | B08     | TXUDATA(13)               | Input   |
| 56            | I   | A08     | TXUDATA(14)               | Input   |
| 55            | I   | B07     | TXUDATA(15)               | Input   |
| 54            | I   | C06     | TXUCLK2                   | Input   |
| 53            | I   | A05     | TXUCLK1                   | Input   |
| 52            | O   | H19     | RSTCREC1                  | Output2   |
| 51            | I   | A12     | FP1                       | Input   |
| 50            | --  | --      | Control                   | Control. This is not a pin. This cell controls the OOF1 pin.      |

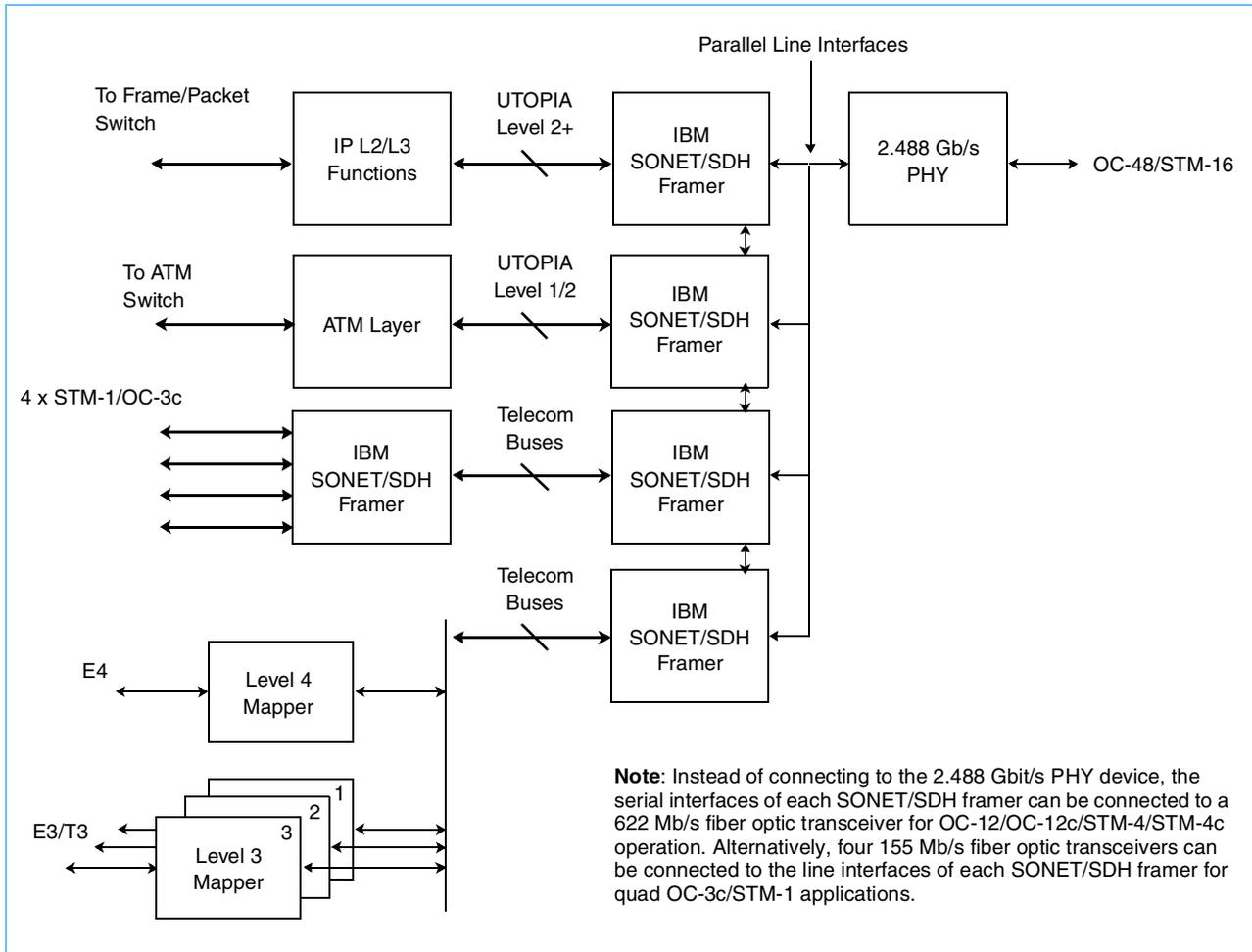
**Scan Cells** (Sheet 10 of 11)

| Scan Cell No. | I/O | Pin No. | Symbol         | Comments   |
|---------------|-----|---------|----------------|--|
| 49            | I/O | D17     | OOF1           | Bidirectional  |
| 48            | I   | H12     | LOSSIG4        | Input  |
| 47            | I   | H13     | LOSSIG3        | Input  |
| 46            | I   | G13     | LOSSIG2        | Input  |
| 45            | I   | F13     | LOSSIG1        | Input  |
| 44            | I   | D19     | LOCKDET1       | Input  |
| 43            | --  | --      | Control        | Control. This is not a pin. This cell controls the RXDCLKT4 pin. |
| 42            | I/O | AA17    | RXDCLKT4       | Bidirectional  |
| 41            | --  | --      | Control        | Control. This is not a pin. This cell controls the RXDCLKT3 pin. |
| 40            | I/O | Y17     | RXDCLKT3       | Bidirectional  |
| 39            | --  | --      | Control        | Control. This is not a pin. This cell controls the RXDCLKT2 pin. |
| 38            | I/O | C18     | RXDCLKT2       | Bidirectional  |
| 37            | --  | --      | Control        | Control. This is not a pin. This cell controls the RXDCLKT1 pin. |
| 36            | I/O | E16     | RXDCLKT1       | Bidirectional  |
| 35            | I   | A09     | RXBYCLK1       | Input  |
| 34            | I   | B13     | RXPDAT(0)      | Input  |
| 33            | I   | C14     | RXPDAT(1)      | Input  |
| 32            | I   | D14     | RXPDAT(2)      | Input  |
| 31            | I   | A14     | RXPDAT(3)      | Input  |
| 30            | I   | D15     | RXPDAT(4)      | Input  |
| 29            | I   | B15     | RXPDAT(5)      | Input  |
| 28            | I   | F15     | RXPDAT(6)      | Input  |
| 27            | I   | D16     | RXPDAT(7)      | Input  |
| 26            | O   | C07     | TXSDOWN4       | Output2  |
| 25            | O   | P15     | TXSDOWN3       | Output2  |
| 24            | O   | M15     | TXSDOWN2       | Output2  |
| 23            | O   | K15     | TXSDOWN1       | Output2  |
| 22            | I   | T16     | TXLPOW4        | Input  |
| 21            | I   | P16     | TXLPOW3        | Input  |
| 20            | I   | M16     | TXLPOW2        | Input  |
| 19            | I   | K16     | TXLPOW1        | Input  |
| 18            | I   | F14     | TX_BYCLKINE(0) | Input  |
| 17            | I   | A15     | TX_BYCLKINT    | Input  |
| 16            | --  | --      | Control        | Control. This is not a pin. This cell controls the TXDCLKT pin.  |
| 15            | I/O | E17     | TXDCLKT        | Bidirectional  |
| 14            | I   | D18     | REFCLKE(0)     | Input  |

**IBM SONET/SDH Framer**
**Scan Cells** (Sheet 11 of 11)

| Scan Cell No. | I/O     | Pin No. | Symbol     | Comments  |
|---------------|---------|---------|------------|---|
| 13            | I       | M19     | REFCLKT    | Input   |
| 12            | --      | --      | Control    | Control. This is not a pin. This cell controls the TXPDAT1(7:0) pins. |
| 11            | I/O     | A17     | TXPDAT1(0) | Bidirectional   |
| 10            | I/O     | B17     | TXPDAT1(1) | Bidirectional   |
| 9             | I/O     | B18     | TXPDAT1(2) | Bidirectional   |
| 8             | I/O     | A18     | TXPDAT1(3) | Bidirectional   |
| 7             | I/O     | B19     | TXPDAT1(4) | Bidirectional   |
| 6             | I/O     | C19     | TXPDAT1(5) | Bidirectional   |
| 5             | I/O     | B16     | TXPDAT1(6) | Bidirectional   |
| 4             | I/O     | A16     | TXPDAT1(7) | Bidirectional   |
| 3             | I       | U17     | ADDR(0)    | Input   |
| 2             | I       | V16     | ADDR(1)    | Input   |
| 1             | I       | U15     | ADDR(2)    | Input   |
| 0             | I       | N01     | ACHCLK     | Input   |
|               | 2-STATE | P17     | TDO        | [SCAN Output]   |

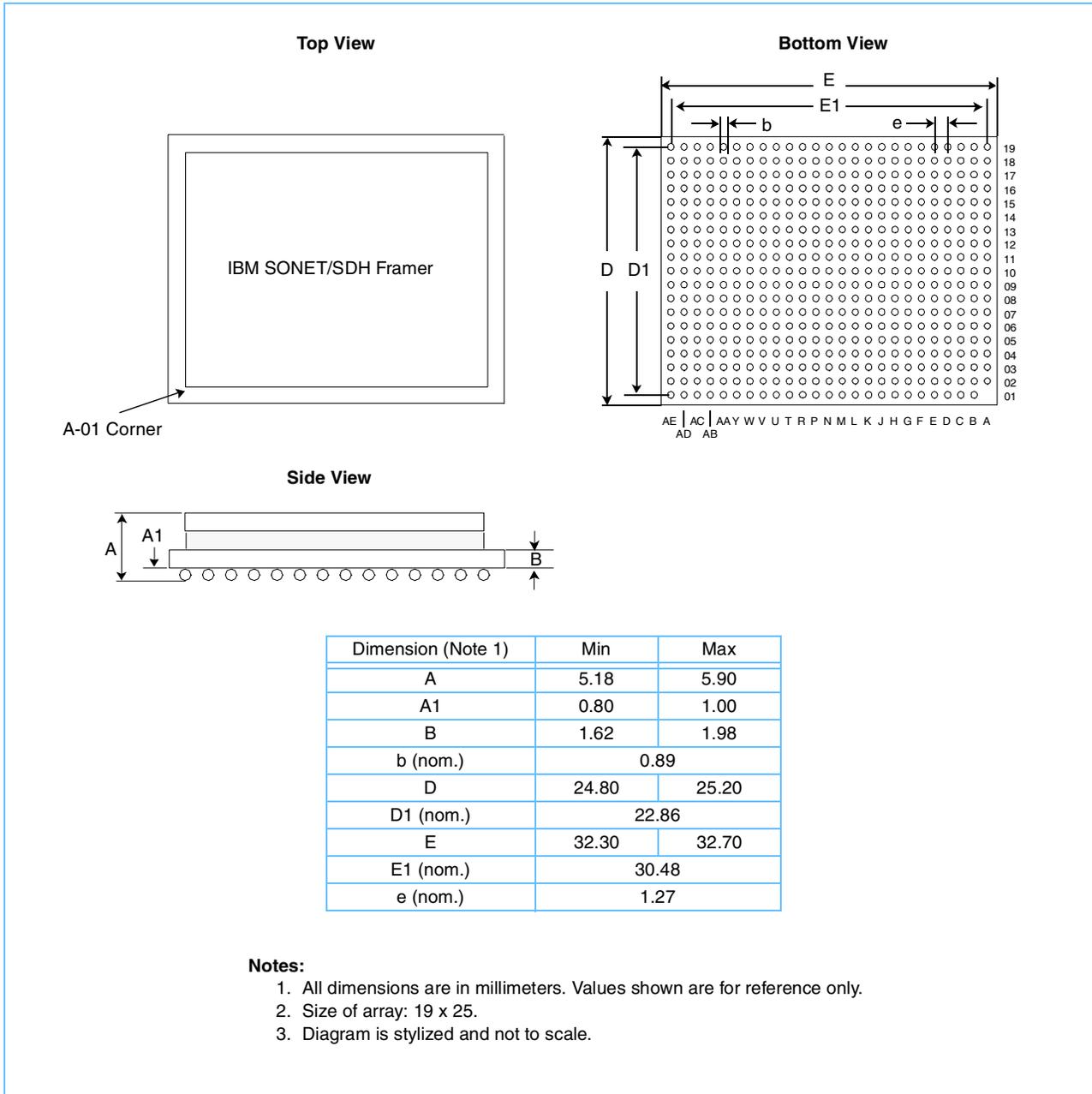
## Example SONET/SDH Framer Applications



IBM SONET/SDH Framer

### Package Diagram

474-pin Ceramic Ball Grid Array with Direct Lid Attach (CBGA-DLA), suitable for surface mounting.



## Standards Documentation Sources

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

**ANSI (U.S.A.):**

American National Standards Institute (ANSI)  
11 West 42nd Street  
New York, New York 10036  
Tel: 212-642-4900  
Fax:212-302-1286

**The ATM Forum (U.S.A.):**

ATM Forum World Headquarters  
303 Vintage Park Drive  
Foster City, CA 94404-1138

Tel: 415-578-6860  
Fax:415-525-0182

ATM Forum European Office  
14 Place Marie - Jeanne Bassot  
Levallois Perret Cedex  
92593 Paris France  
Tel: 33 1 46 39 56 26  
Fax:33 1 46 39 56 99

**Bellcore (U.S.A.):**

Bellcore  
Attention - Customer Service  
8 Corporate Place  
Piscataway, NJ 08854  
Tel: 800-521-CORE (In U.S.A.)  
Tel: 908-699-5800  
Fax:908-336-2559

**EIA - Electronic Industries Association (U.S.A.):**

Global Engineering Documents  
Suite 407  
7730 Carondelet Avenue  
Clayton, MO 63105  
Tel: 800-854-7179 (In U.S.A.)  
Fax:314-726-6418

**ETSI (Europe):**

European Telecommunications Standards Institute  
ETSI, 06921 Sophia - Antipolis  
Cedex France  
Tel: 33 92 94 42 00  
Fax:33 93 65 47 16

**IBM SONET/SDH Framer**

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ITU-T (International):

Publication Services of International Telecommunication Union (ITU)  
Telecommunication Standardization Sector (T)  
Place des Nations  
CH 1211  
Geneve 20, Switzerland  
Tel: 41-22-730-5285  
Fax:41-22-730-5991

MIL-STD Military Standard (U.S.A.):

Standardization Documents Order Desk  
700 Robbins Avenue  
Building 4D  
Philadelphia, PA 19111-5094  
Tel: 212-697-1187  
Fax:215-697-2978

TTC (Japan):

TTC Standard Publishing Group of the  
Telecommunications Technology Committee  
2nd Floor, Hamamatsucho - Suzuki Building,  
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo  
Tel:81-3-3432-1551  
Fax:81-3-3432-1553

## Revision Log

| Date    | Description   |
|---------|---|
| 5/7/99  | Preliminary draft of version 00, for limited distribution.  |
| 5/25/99 | Second preliminary draft of version 00, for limited distribution.   |
| 7/27/99 | Initial public release (version 00).  |
| 8/27/99 | First revision (version 01). Refined GPDTACK waveform on pages 75, 77, 79, and 81.<br>Modified descriptions in table 27.4 (p. 176) and table 30.2 (p. 179). |