



### Description

The ICS501A LOCO™ is the most cost effective way to generate a high quality, high frequency clock output from a lower frequency crystal or clock input. The name LOCO stands for Low Cost Oscillator, as it is designed to replace crystal oscillators in most electronic systems. Using Phase-Locked Loop (PLL) techniques, the device uses a standard fundamental mode, inexpensive crystal to produce output clocks up to 200 MHz.

Stored in the chip's ROM is the ability to generate nine different multiplication factors, allowing one chip to output many common frequencies (see table on page 2).

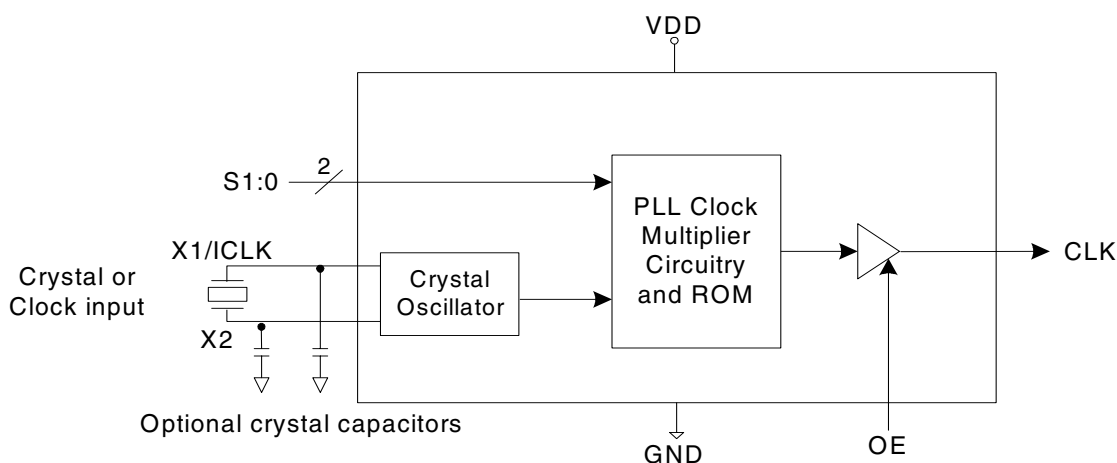
The device also has an output enable pin which tri-states the clock output when the OE pin is taken low.

This product is intended for clock generation. It has low output jitter (variation in the output period), but input to output skew and jitter are not defined or guaranteed. For applications which require defined input to output skew, use the ICS570B.

### Features

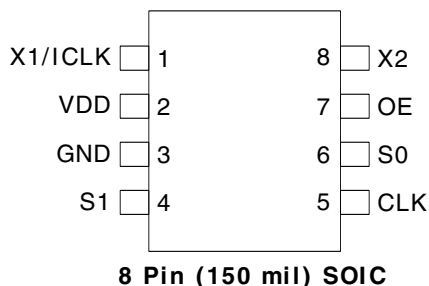
- Packaged as 8-pin SOIC or die
- ICS' lowest cost PLL clock
- Zero ppm multiplication error
- Input crystal frequency of upto 27 MHz
- Input clock frequency of upto 50 MHz
- Output clock frequencies up to 200 MHz
- Extremely low jitter of 25 ps (one sigma)
- Compatible with all popular CPUs
- Duty cycle of 45/55 up to 200 MHz
- Nine selectable frequencies
- Operating voltage of 3.3V
- Tri-state output for board level testing
- 25mA drive capability at TTL levels
- Ideal for oscillator replacement
- Optimized for output frequencies of upto to 200 MHz
- Industrial temperature version available
- Advanced, low power CMOS process

### Block Diagram





## Pin Assignment



## Clock Output Table

| S1 | S0 | CLK          | Minimum Input (MHz) |
|----|----|--------------|---------------------|
| 0  | 0  | 4X input     | 15                  |
| 0  | M  | 5.333X input | 12                  |
| 0  | 1  | 5X input     | 12                  |
| M  | 0  | 10X input    | 6                   |
| M  | M  | 2X input     | 30                  |
| M  | 1  | 12X input    | 5                   |
| 1  | 0  | 6X input     | 10                  |
| 1  | M  | 3X input     | 20                  |
| 1  | 1  | 8X input     | 10                  |

0 = connect directly to ground

1 = connect directly to VDD

M = leave unconnected (floating)

## Pin Descriptions

| Pin Number | Pin Name | Pin Type        | Pin Description                                                           |
|------------|----------|-----------------|---------------------------------------------------------------------------|
| 1          | XI/ICLK  | Input           | Crystal connection or clock input.                                        |
| 2          | VDD      | Power           | Connect to +3.3 V.                                                        |
| 3          | GND      | Power           | Connect to ground.                                                        |
| 4          | S1       | Tri-level Input | Select 1 for output clock. Connect to GND or VDD or float.                |
| 5          | CLK      | Output          | Clock output per table above.                                             |
| 6          | S0       | Tri-level Input | Select 0 for output clock. Connect to GND or VDD or float.                |
| 7          | OE       | Input           | Output enable. Tri-states CLK output when low. Internal pull-up resistor. |
| 8          | X2       | Output          | Crystal connection. Leave unconnected for clock input.                    |



## External Components

### Decoupling Capacitor

As with any high-performance mixed-signal IC, the ICS501A must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of 0.01 $\mu$ F must be connected between VDD and the GND. It must be connected close to the ICS501A to minimize lead inductance. No external power supply filtering is required for the ICS501A.

### Series Termination Resistor

A 33 $\Omega$  terminating resistor can be used next to the CLK pin for trace lengths over one inch.

### Crystal Load Capacitors

The total on-chip capacitance is approximately 12 pF. A parallel resonant, fundamental mode crystal should be used. The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors, if needed, must be connected from each of the pins X1 and X2 to ground.

The value (in pF) of these crystal caps should equal  $(C_L - 12 \text{ pF}) \times 2$ . In this equation,  $C_L$  = crystal load capacitance in pF. Example: For a crystal with a 16 pF load capacitance, each crystal capacitor would be 8 pF  $[(16 - 12) \times 2] = 8$ .



## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS501A. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item                          | Rating            |
|-------------------------------|-------------------|
| Supply Voltage, VDD           | 7V                |
| All Inputs and Outputs        | -0.5V to VDD+0.5V |
| Ambient Operating Temperature | -40 to +85°C      |
| Storage Temperature           | -65 to +150°C     |
| Soldering Temperature         | 260°C             |

## Recommended Operation Conditions

| Parameter                                         | Min. | Typ. | Max. | Units |
|---------------------------------------------------|------|------|------|-------|
| Ambient Operating Temperature                     | 0    |      | +70  | °C    |
| Power Supply Voltage (measured in respect to GND) | +3.0 |      | +3.6 | V     |

## DC Electrical Characteristics

VDD=3.3 V  $\pm 10\%$  , Ambient temperature 0 to +70°C, unless stated otherwise

| Parameter                        | Symbol          | Conditions               | Min.      | Typ.     | Max.      | Units |
|----------------------------------|-----------------|--------------------------|-----------|----------|-----------|-------|
| Operating Voltage                | VDD             |                          | 3.0       |          | 3.6       | V     |
| Input High Voltage, ICLK only    | V <sub>IH</sub> | ICLK (pin 1)             | (VDD/2)+1 |          |           | V     |
| Input Low Voltage, ICLK only     | V <sub>IL</sub> | ICLK (pin 1)             |           |          | (VDD/2)-1 | V     |
| Input High Voltage               | V <sub>IH</sub> | OE (pin 7)               | 2.0       |          |           | V     |
| Input Low Voltage                | V <sub>IL</sub> | OE (pin 7)               |           |          | 0.8       | V     |
| Input High Voltage               | V <sub>IH</sub> | S0, S1                   | VDD-0.5   |          |           | V     |
| Input Low Voltage                | V <sub>IL</sub> | S0, S1                   |           |          | 0.5       | V     |
| Output High Voltage              | V <sub>OH</sub> | I <sub>OH</sub> = -12 mA | 2.4       |          |           | V     |
| Output Low Voltage               | V <sub>OL</sub> | I <sub>OL</sub> = 12 mA  |           |          | 0.4       | V     |
| IDD Operating Supply Current, 20 |                 | No load, 100M            |           | 20       |           | mA    |
| Short Circuit Current            |                 | CLK output               |           | $\pm 70$ |           | mA    |



| Parameter                         | Symbol | Conditions   | Min. | Typ. | Max. | Units      |
|-----------------------------------|--------|--------------|------|------|------|------------|
| On-Chip Pull-up Resistor          |        | Pin 7        |      | 270  |      | k $\Omega$ |
| Input Capacitance, S1, S0, and OE |        | Pins 4, 6, 7 |      | 4    |      | pF         |
| Nominal Output Impedance          |        |              |      | 20   |      | $\Omega$   |

## AC Electrical Characteristics

**VDD = 3.3 V  $\pm$ 10%**, Ambient Temperature 0 to +70° C, unless stated otherwise

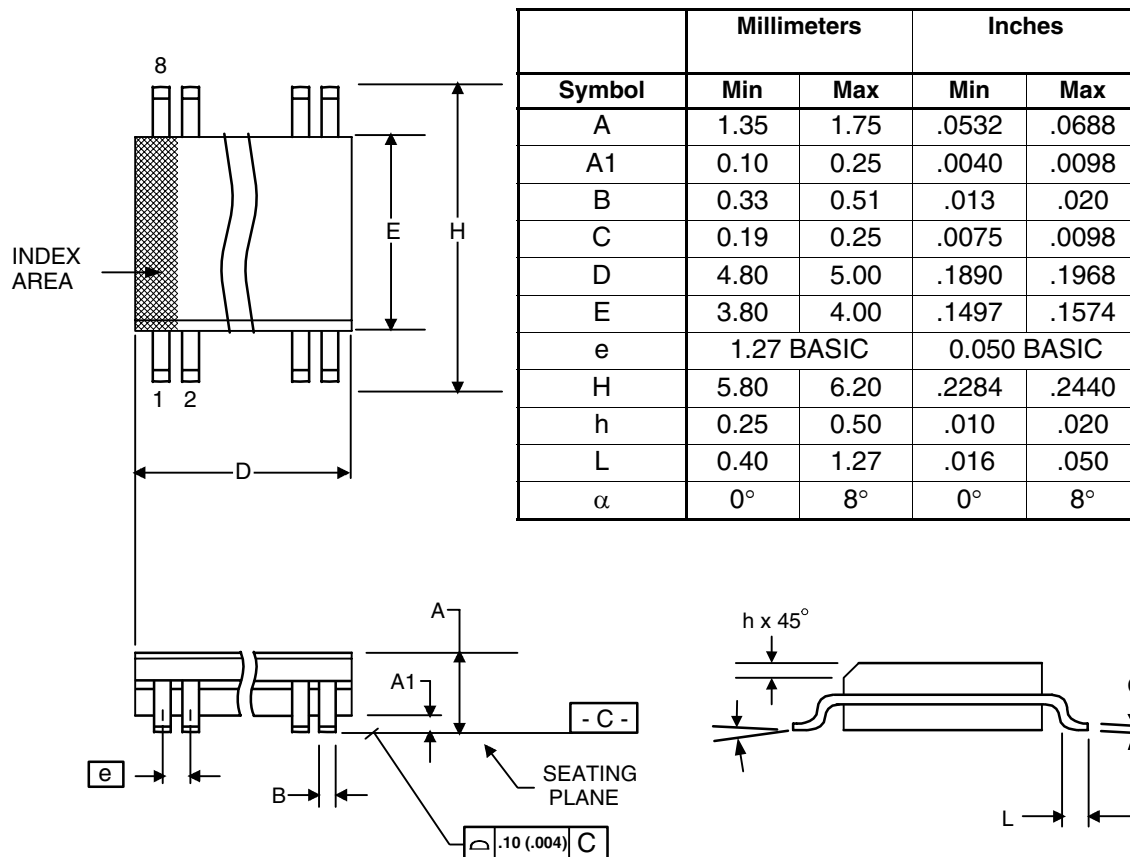
| Parameter                                | Symbol           | Conditions           | Min. | Typ.     | Max. | Units |
|------------------------------------------|------------------|----------------------|------|----------|------|-------|
| Input Frequency, crystal input           | F <sub>IN</sub>  | see page 2           |      |          | 27   | MHz   |
| Input Frequency, clock input             | F <sub>IN</sub>  | see page 2           |      |          | 50   | MHz   |
| Output Frequency, VDD = 3.0 to 3.6V      | F <sub>OUT</sub> | 0°C to +70°C         |      |          | 200  | MHz   |
|                                          |                  | -40°C to +85°C       |      |          | TBD  | MHz   |
| Output Clock Rise Time                   | t <sub>OR</sub>  | 0.8 to 2.0 V, Note 1 |      | 1        |      | ns    |
| Output Clock Fall Time                   | t <sub>OF</sub>  | 2.0 to 8.0 V, Note 1 |      | 1        |      | ns    |
| Output Clock Duty Cycle                  | t <sub>OD</sub>  | 1.5 V, up to 160 MHz | 45   | 49-51    | 55   | %     |
| PLL Bandwidth                            |                  |                      | 120  |          |      | kHz   |
| Output Enable Time, OE high to output on |                  |                      |      | 50       |      | ns    |
| Output Disable Time, OE low to tri-state |                  |                      |      | 50       |      | ns    |
| Absolute Clock Period Jitter             | t <sub>ja</sub>  | Deviation from mean  |      | $\pm$ 70 |      | ps    |
| One Sigma Clock Period Jitter            | t <sub>js</sub>  |                      |      | 25       |      | ps    |

Note 1: Measured with 15 pF load.



## Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



## Ordering Information

| Part / Order Number | Marking | Shipping Packaging          | Package    | Temperature   |
|---------------------|---------|-----------------------------|------------|---------------|
| ICS501AM            | 501AM   | Tubes                       | 8-pin SOIC | 0 to +70° C   |
| ICS501AMT           | 501AM   | Tape and Reel               | 8-pin SOIC | 0 to +70° C   |
| ICS501AMI           | 501AI   | Tubes                       | 8-pin SOIC | -40 to +85° C |
| ICS501AMIT          | 501AI   | Tape and Reel               | 8-pin SOIC | -40 to +85° C |
| ICS501A-DWF         | -       | Die on uncut, probed wafers |            | 0 to +70° C   |
| ICS501A-DPK         | -       | Tested die in waffle pack   |            | 0 to +70° C   |

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