FEMTOCLOCKS™ CRYSTAL-TO-HSTL FREQUENCY SYNTHESIZER

ICS842256-24

General Description

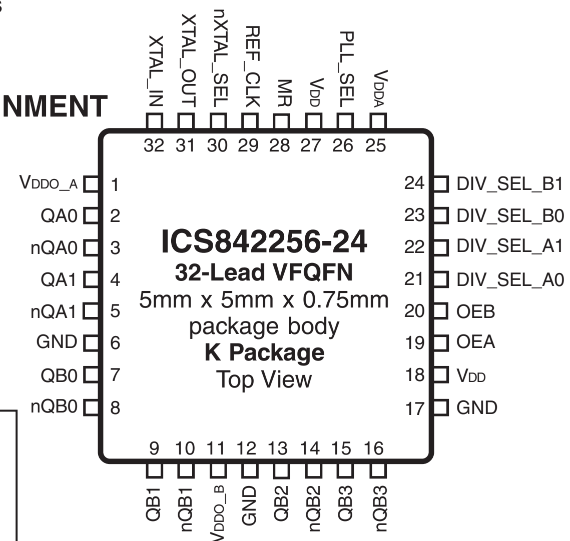
The ICS842256-24 is a 6 differential HSTL output Synthesizer designed to generate reference clocks for SPI-4.2 and XAUI/XGMII 10Gb Ethernet interfaces and is a member of the HiPerClocks™ family of high performance clock solutions from IDT. Using a 31.25MHz, 18pF parallel resonant crystal, the following frequencies can be generated based on the settings of frequency select pins: 390.625MHz, 312.5MHz, 195.3125MHz and 156.25MHz.

The two banks have their own dedicated frequency select pins and can be independently set for the frequencies mentioned above. The ICS842256-24, with low phase noise VCO tech-nology, can achieve 1ps or lower typical rms phase jitter, easily meeting SPI-4.2 and 10Gb Ethernet jitter requirements. The ICS842256-24 is packaged in a small 32-pin VFQFN package.

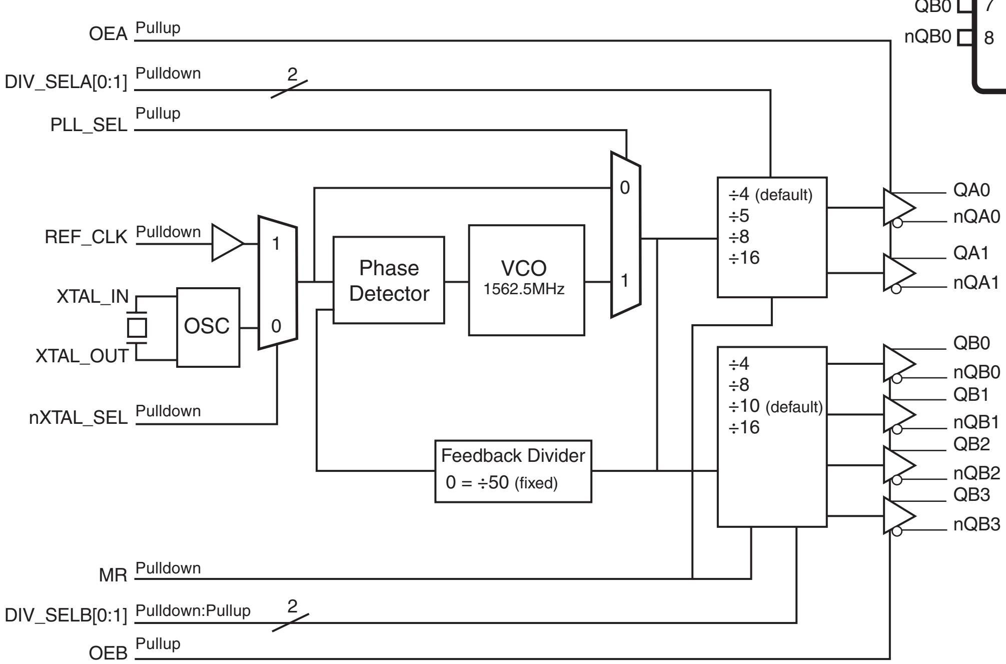
Features

- Six differential HSTL output pairs
- Using a 31.25MHz crystal, the two output banks can be independently set for 390.625MHz, 312.5MHz, 195.3125MHz or 156.25MHz
- Crystal oscillator interface
- VCO: 1562.5MHz
- RMS phase jitter @ 156.25MHz (1.875MHz - 20MHz): 0.56ps (typical)
- Full 3.3V supply mode
- 0°C to 70°C ambient operating temperature
- Industrial temperature available upon request
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Pin Assignment



Block Diagram



The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V_{DDO_A}	Power		Output supply pin for Bank A outputs.
2, 3 4, 5	QA0, nQA0 QA1, nQA1	Output		Differential clock outputs. HSTL interface levels.
6, 12, 17	GND	Power		Power supply ground.
7, 8 9, 10 13, 14 15, 16	QB0, nQB0 QB1, nQB1 QB2, nQB2 QB3, nQB3	Output		Differential clock outputs. HSTL interface levels.
11	V_{DDO_B}	Power		Output supply pins for Bank B outputs.
18, 27	V_{DD}	Power		Core supply pin.
19	OEA	Input	Pullup	Output enable pin for Bank A outputs. LVCMOS/LVTTL interface levels.
20	OEB	Input	Pullup	Output enable pin for Bank B outputs. LVCMOS/LVTTL interface levels.
21, 22	DIV_SEL_A0, DIV_SEL_A1	Input	Pulldown	Divide select pins for Bank A outputs. See Table 3A. LVCMOS/LVTTL interface levels.
23	DIV_SEL_B0	Input	Pulldown	Divide select pin for Bank B outputs. See Table 3B. LVCMOS/LVTTL interface levels.
24	DIV_SEL_B1	Input	Pullup	Divide select pin for Bank B outputs. See Table 3B. LVCMOS/LVTTL interface levels.
25	V_{DDA}	Power		Analog supply pin.
26	PLL_SEL	Input	Pullup	LVCMOS/LVTTL interface levels.
28	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs (QAx, QBx) to go low and the inverted outputs (nQAx, nQBx) to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
29	REF_CLK	Input	Pulldown	Single-ended LVCMOS/LVTTL reference clock input.
30	nXTAL_SEL	Input	Pulldown	Selects between the crystal or REF_CLK inputs as the PLL reference source. When HIGH, selects REF_CLK. When LOW, selects XTAL inputs. LVCMOS/LVTTL interface levels.
31, 32	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_OUT is the output. XTAL_IN is the input.

NOTE: *Pulldown and Pullup* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

TABLE 3A. BANK A FREQUENCY TABLE

Inputs			Feedback Divider	Bank A Output Divider	QA/nQA Output Frequency (MHz)
Crystal Frequency (MHz)	DIV_SEL_A1	DIV_SEL_A0			
31.25	0	0	25	4	390.625 (default)
31.25	0	1	25	5	312.5
31.25	1	0	25	8	195.3125
31.25	1	1	25	16	97.65625

TABLE 3B. BANK B FREQUENCY TABLE

Inputs			Feedback Divider	Bank B Output Divider	QB/nQB Output Frequency (MHz)
Crystal Frequency (MHz)	DIV_SEL_B1	DIV_SEL_B0			
31.25	0	0	25	2	390.625
31.25	0	1	25	4	195.3125
31.25	1	0	25	5	156.25 (default)
31.25	1	1	25	8	97.65625

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, θ_{JA}	37°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO\_A,}$ V_{DDO_B} = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.10	3.3	V_{DD}	V
V_{DDO_A}, V_{DDO_B}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			160		mA
I_{DDA}	Analog Supply Current			10		mA
I_{DDO_A}, I_{DDO_B}	Output Supply Current	No Load		0		mA

Table 4B. LVCMOS / LVTTL DC Characteristics, $V_{DD} = V_{DDO\_A} = V_{DDO\_B}$ = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	REF_CLK, MR, DIV_SELA[0:1], DIV_SELB0, nXTAL_SEL	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		OEA, OEB, PLL_SEL, DIV_SELB1	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	REF_CLK, MR, DIV_SELA[0:1], DIV_SELB0, nXTAL_SEL	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		OEA, OEB, PLL_SEL, DIV_SELB1	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA

Table 4C. HSTL DC Characteristics, $V_{DD} = V_{DDO\_A} = V_{DDO\_B}$ = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		1		1.4	V
V_{OL}	Output Low Voltage; NOTE 1		0		0.4	V
V_{OX}	Output Crossover Voltage; NOTE 2		40		60	%
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.4	V

NOTE 1: Outputs terminated with 50Ω to GND.
NOTE 2: Defined with respect to output voltage swing at a given condition.

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			31.25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

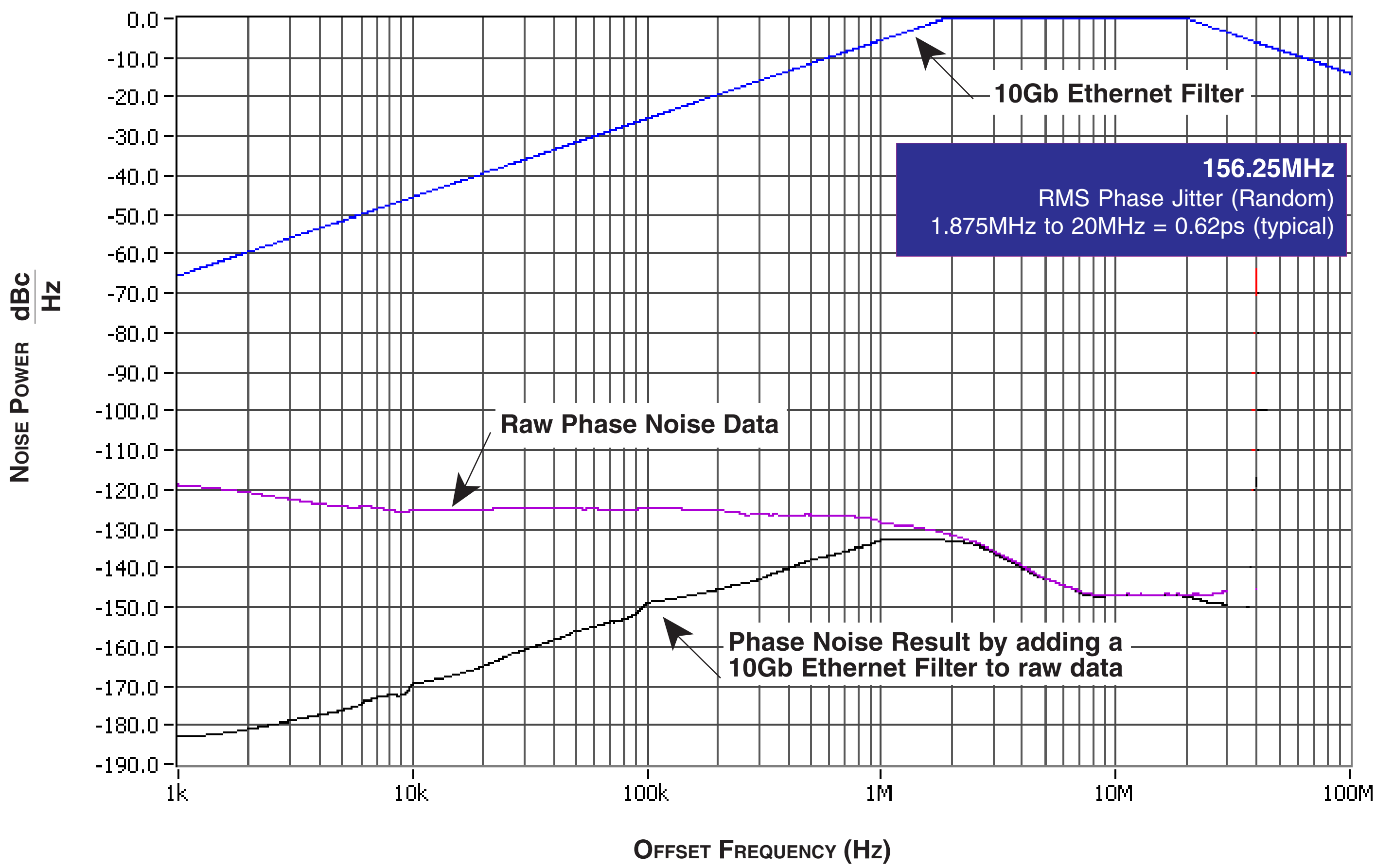
NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 6. AC CHARACTERISTICS, $V_{DD} = V_{DDO\_A}, V_{DDO\_B}$ = 3.3V±5%, TA = 0°C TO 70°C

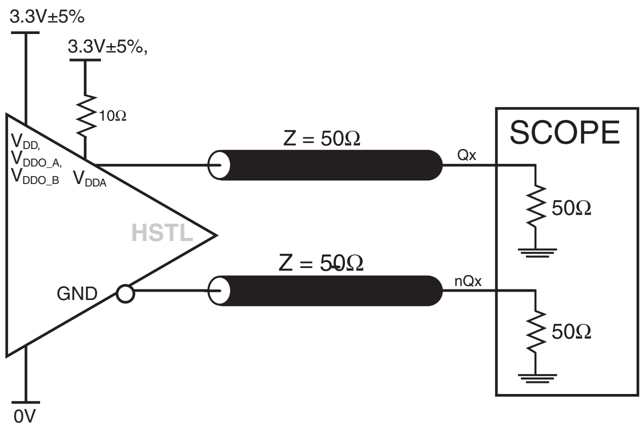
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	QAx/nQAx		97.65625		390.625	MHz
		QBx/nQBx		97.65625		390.625	MHz
*t*sk(o)	Output Skew; NOTE 1, 2		Outputs @ Same Frequency		TBD		ps
			Outputs @ Different Frequencies		TBD		ps
*t*sk(b)	Bank Skew; NOTE 2, 3				TBD		ps
*t*jit(Ø)	RMS Phase Jitter, Random; NOTE 4		390.625MHz (1.875MHz-20MHz)		0.60		ps
			312.5MHz (1.875MHz-20MHz)		0.58		ps
			195.3125MHz (1.875MHz-20MHz)		0.58		ps
			156.25MHz (1.875MHz-20MHz)		0.56		ps
t_R / t_F	Rise/Fall Time		20% to 80%		400		ps
odc	Output Duty Cycle				50		%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at the output differential cross points.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.
NOTE 4: Please refer to Phase Noise Plots.

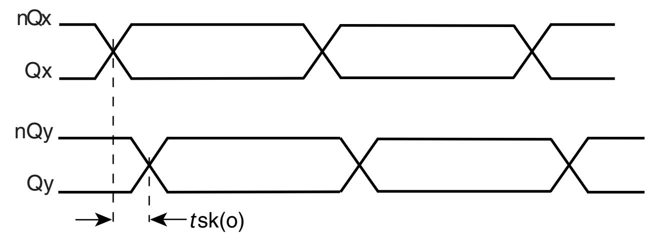
TYPICAL PHASE NOISE AT 156.25MHZ



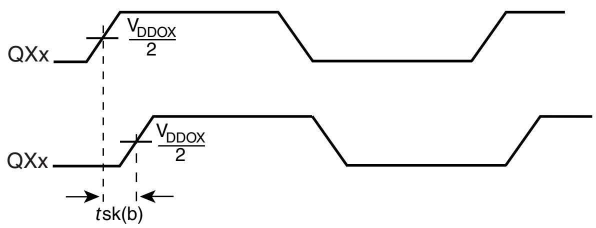
Parameter Measurement Information



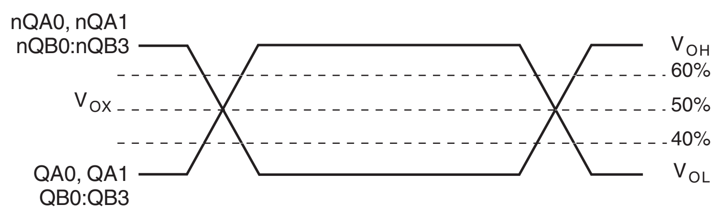
3.3V Core/3.3V Output Load AC Test Circuit



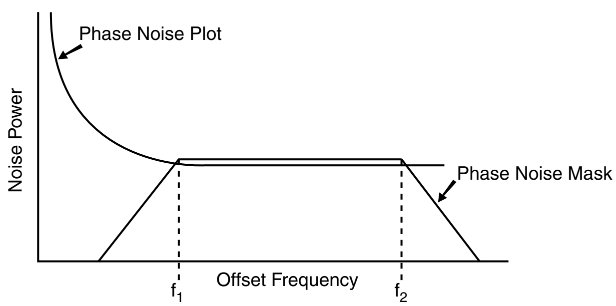
Output Skew



Bank Skew (where X denotes outputs in the same bank)

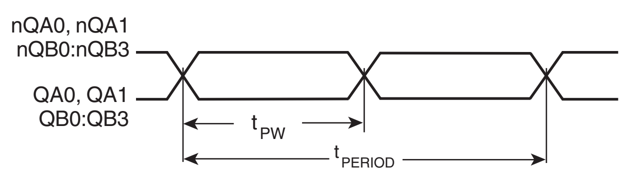


Output Crossover Voltage



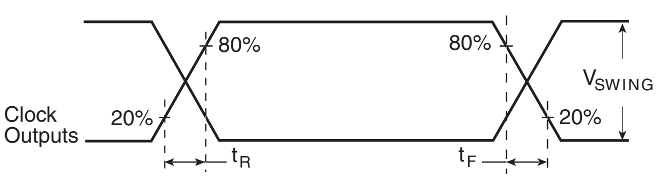
RMS Jitter = $\sqrt{\text{Area Under the Masked Phase Noise Plot}}$

RMS Phase Jitter



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

Application Information

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS842256-24 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, V_{DDO_A} and V_{DDO_B} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA} pin.

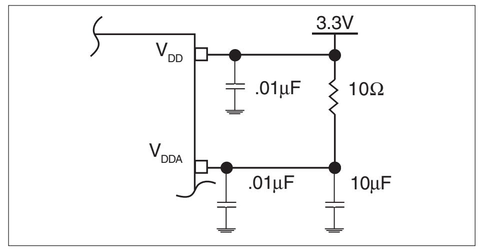


FIGURE 1. POWER SUPPLY FILTERING

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Input:
For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_CLK Input:
For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

LVCMOS Control Pins:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

HSTL Output
All unused LVHSTL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Crystal Input Interface

The ICS842256-24 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 31.25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

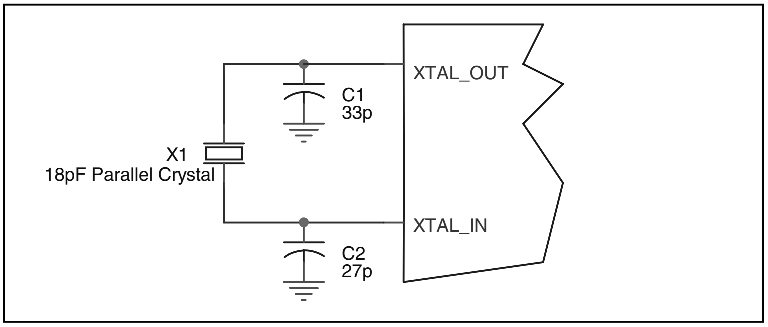


Figure 2. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

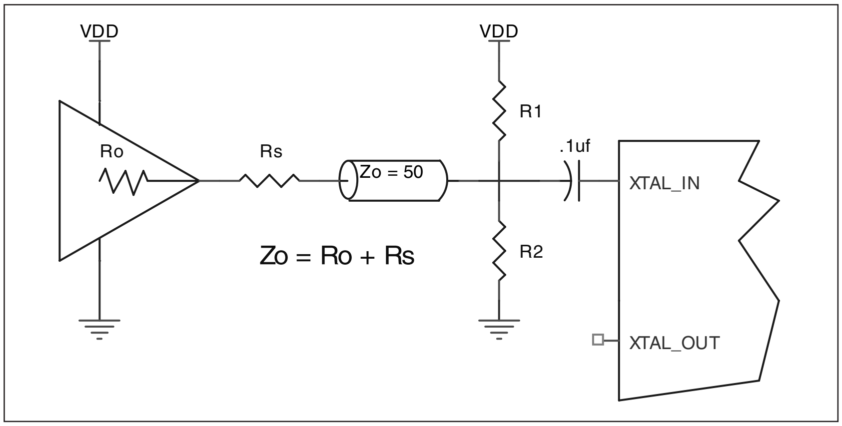


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

Thermal Release Path

The expose metal pad provides heat transfer from the device to the P.C. board. The expose metal pad is ground pad connected to ground plane through thermal via. The exposed pad on the device to the exposed metal pad on the PCB is contacted through solder as shown in *Figure 4*. For further information, please refer to the Application Note on Surface Mount Assembly of Amkor's Thermally /Electrically Enhance Leadframe Base Package, Amkor Technology.

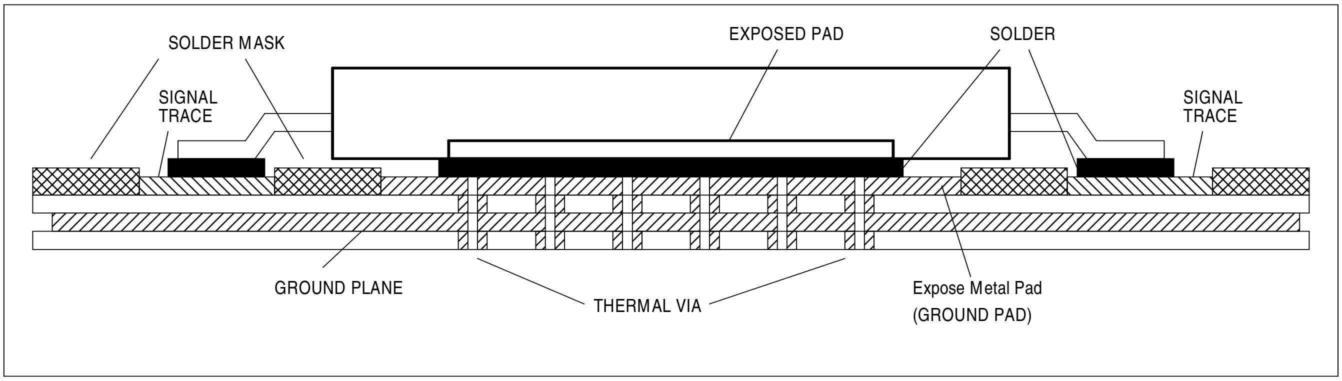


Figure 4. P.C. Board for Exposed Pad Thermal Release Path Example

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS842256-24. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS842256-24 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 3.465V * 160mA = **554.40mW**
- Power (outputs)$_{MAX}$ = **82.34mW/Loaded Output pair**
  If all outputs are loaded, the total power is 6 x 82.34mW = **494.04mW**

Total Power $_{\_MAX}$ (3.465V, with all outputs switching) = 554.40mW + 494.04mW = **1048.44mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 37°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 1.048W * 37°C/W = 108.8°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

Table 7. Thermal Resistance θ_{JA} for 32-pin VFQFN, Forced Convection

θ_{JA} vs. Air Flow (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

HSTL output driver circuit and termination are shown in *Figure 5.*

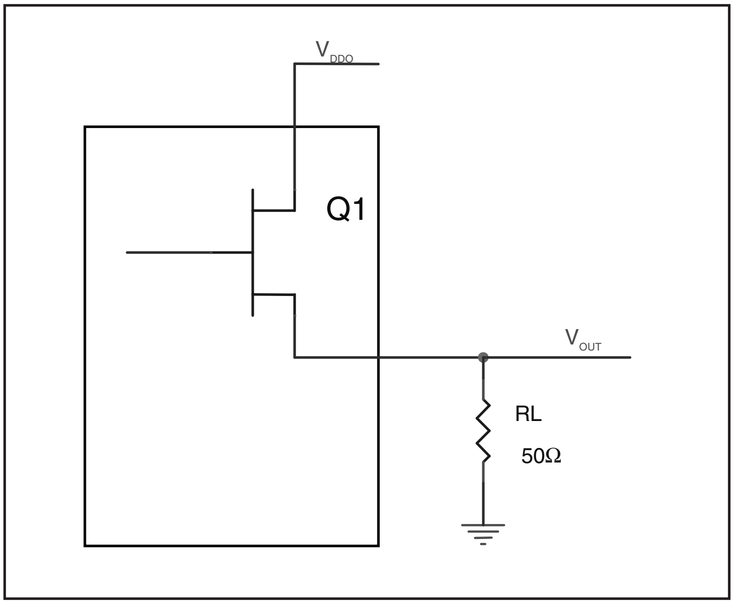


FIGURE 5. HSTL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load.

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$$Pd\_H = (V_{OH\_MAX}/R_L) * (V_{DD\_MAX} - V_{OH\_MAX})$$

$$Pd\_L = (V_{OL\_MAX}/R_L) * (V_{DD\_MAX} - V_{OL\_MAX})$$

Pd_H = (1.4V/50Ω) * (3.465 - 1.4V) = 57.82mW
Pd_L = 0.4V (50Ω) * (3.465 - 0.4V) = 24.52mW

Total Power Dissipation per output pair = Pd_H + Pd_L = **82.34mW**

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for 32 Lead VFQFN

θ_{JA} vs. Air Flow (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

Transistor Count

The transistor count for ICS842256-24 is: 2364

Package Outline - K Suffix for 32 Lead VFQFN

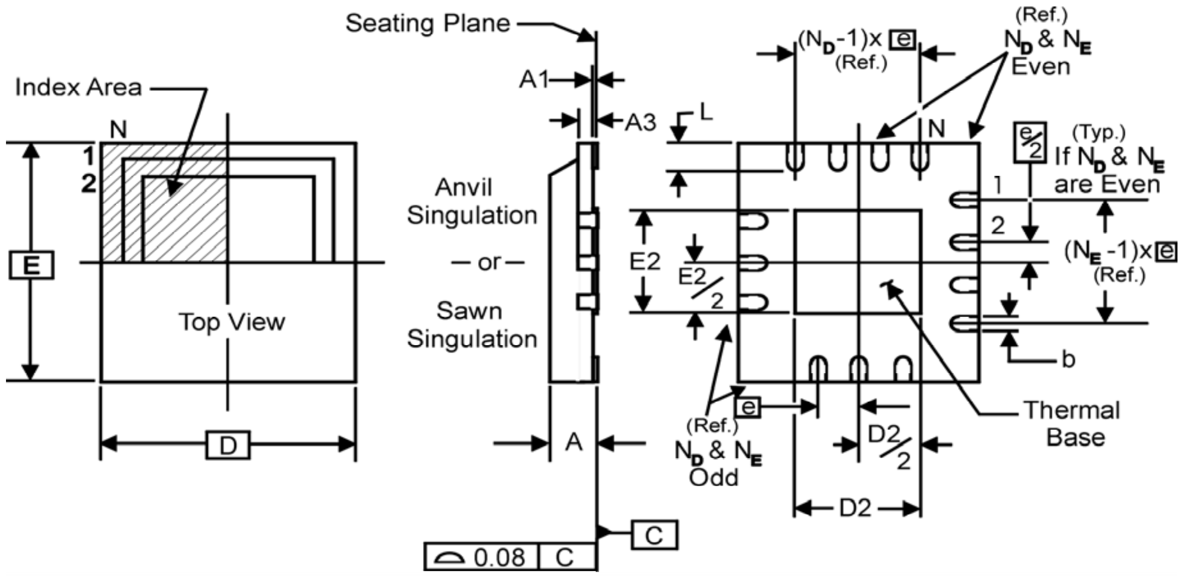


Table 9. Package Dimensions

SYMBOL	JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
	VHHD-2		
	MINIMUM	NOMINAL	MAXIMUM
N	32		
A	0.80	--	1.00
A1	0	--	0.05
A3	0.25 Ref.		
b	0.18	0.25	0.30
N_D			8
N_E			8
D	5.00 BASIC		
D2	1.25	2.25	3.25
E	5.00 BASIC		
E2	1.25	2.25	3.25
e	0.50 BASIC		
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
842256CK-24	ICS42256C24	32 Lead VFQFN	Tray	0°C to 70°C
842256CK-24T	ICS42256C24	32 Lead VFQFN	1000 Tape & Reel	0°C to 70°C
842256CK-24LF	ICS2256C24L	32 Lead "Lead-Free" VFQFN	Tray	0°C to 70°C
842256CK-24LFT	ICS2256C24L	32 Lead "Lead-Free" VFQFN	1000 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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