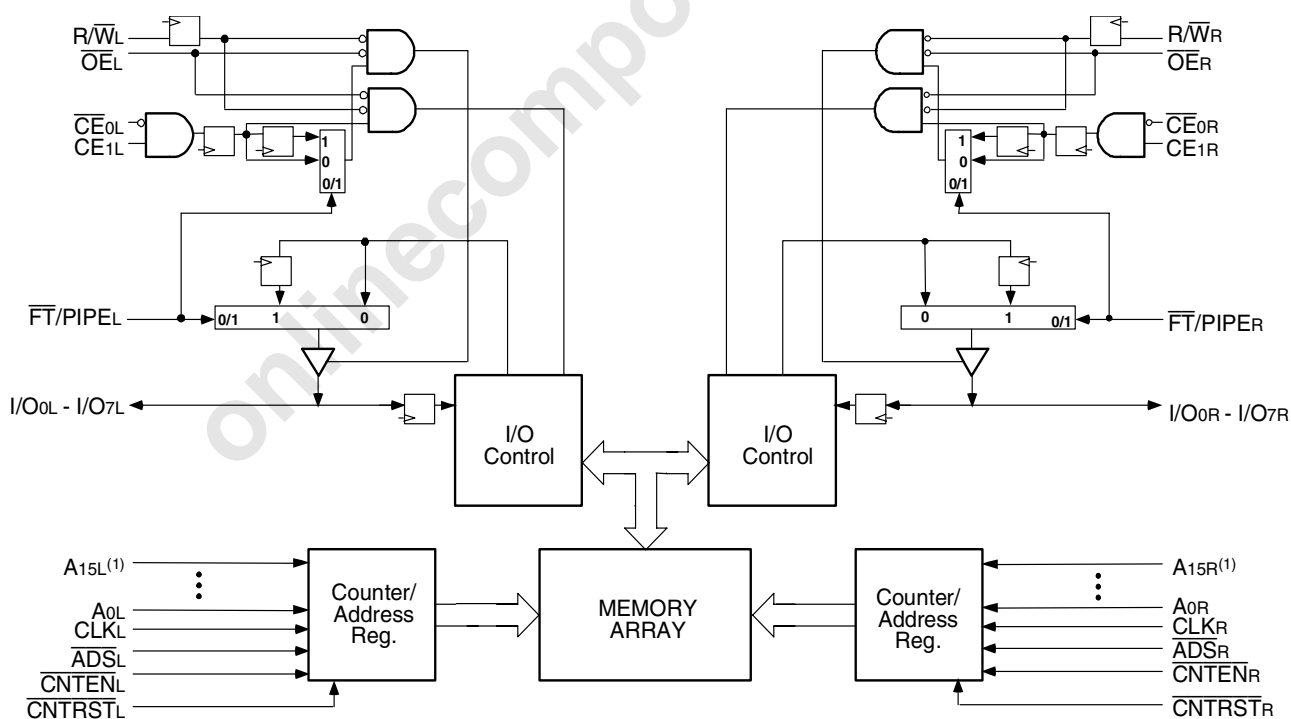# HIGH-SPEED 64/32K x 8 SYNCHRONOUS DUAL-PORT STATIC RAM

IDT709089/79S/L

Features:

- True Dual-Ported memory cells which allow simultaneous access of the same memory location
- High-speed clock to data access
  - *Commercial: 6/7/9/12/15ns (max.)*
  - *Industrial: 12ns (max.)*
- Low-power operation
  - *IDT709089/79S*
    Active: 950mW (typ.)
    Standby: 5mW (typ.)
  - *IDT709089/79L*
    Active: 950mW (typ.)
    Standby: 1mW (typ.)
- Flow-Through or Pipelined output mode on either port via the $\overline{FT}$/PIPE pin
- Counter enable and reset features
- Dual chip enables allow for depth expansion without additional logic
- Full synchronous operation on both ports
  - *4ns setup to clock and 1ns hold on all control, data, and address inputs*
  - *Data input, address, and control registers*
  - *Fast 6.5ns clock to data out in the Pipelined output mode*
  - *Self-timed write allows fast cycle time*
  - *10ns cycle time, 100MHz operation in the Pipelined output mode*
- TTL- compatible, single 5V (±10%) power supply
- Industrial temperature range (–40°C to +85°C) is available for selected speeds
- Available in 100-pin Thin Quad Flatpack (TQFP) package
- Green parts available, see ordering information

Functional Block Diagram

3242 drw 01

NOTE:
1. A_{15X} is a NC for IDT709079.

DSC-3242/14

Description:

The IDT709089/79 is a high-speed 64/32K x 8 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times.

With an input data register, the IDT709089/79 has been optimized for applications having unidirectional or bidirectional data flow in bursts. An automatic power down feature, controlled by $\overline{CE}_0$ and CE_1, permits the on-chip circuitry of each port to enter a very low standby power mode. Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 950mW of power.

Pin Configuration[1,2,3]

08/19/03

Index

IDT709089/79PF
PN100-1[5]

100-PIN TQFP
TOP VIEW[6]

3242 drw 02

Top pins (left to right, pins 100–76): NC, NC, A6L, A5L, A4L, A3L, A2L, A1L, A0L, $\overline{CNTEN}$L, CLKL, $\overline{ADS}$L, GND, $\overline{ADS}$R, CLKR, $\overline{CNTEN}$R, A0R, A1R, A2R, A3R, A4R, A5R, A6R, NC, NC

Left side (pins 1–25):
Pin	Signal
1	NC
2	NC
3	A7L
4	A8L
5	A9L
6	A10L
7	A11L
8	A12L
9	A13L
10	A14L
11	A15L
12	NC
13	VCC
14	NC
15	NC
16	NC
17	NC
18	$\overline{CE}$0L
19	CE1L
20	$\overline{CNTRST}$L
21	R/$\overline{W}$L
22	$\overline{OE}$L
23	$\overline{FT}$/PIPEL
24	NC
25	NC

Right side (pins 75–51):
Pin	Signal
75	NC
74	NC
73	A7R
72	A8R
71	A9R
70	A10R
69	A11R
68	A12R
67	A13R
66	A14R
65	A15R
64	NC
63	GND
62	NC
61	NC
60	NC
59	NC
58	$\overline{CE}$0R
57	CE1R
56	$\overline{CNTRST}$R
55	R/$\overline{W}$R
54	$\overline{OE}$R
53	$\overline{FT}$/PIPER
52	GND
51	NC

Bottom pins (left to right, pins 26–50): GND, NC, I/O7L, I/O6L, I/O5L, I/O4L, I/O3L, I/O2L, GND, I/O1L, I/O0L, VCC, GND, I/O0R, I/O1R, I/O2R, VCC, I/O3R, I/O4R, I/O5R, I/O6R, I/O7R, NC, NC, NC

NOTES:
1. A15X is a NC for IDT709079.
2. All VCC pins must be connected to power supply.
3. All GND pins must be connected to ground supply.
4. Package body is approximately 14mm x 14mm x 1.4mm.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

Pin Names

Left Port	Right Port	Names
$\overline{CE}_{0L}$, CE_{1L}	$\overline{CE}_{0R}$, CE_{1R}	Chip Enables
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A_{0L} - A_{15L}[1]	A_{0R} - A_{15R}[1]	Address
I/O_{0L} - I/O_{7L}	I/O_{0R} - I/O_{7R}	Data Input/Output
CLK_L	CLK_R	Clock
$\overline{ADS}_L$	$\overline{ADS}_R$	Address Strobe
$\overline{CNTEN}_L$	$\overline{CNTEN}_R$	Counter Enable
$\overline{CNTRST}_L$	$\overline{CNTRST}_R$	Counter Reset
$\overline{FT}/PIPE_L$	$\overline{FT}/PIPE_R$	Flow-Through/Pipeline
V_{CC}		Power
GND		Ground

3242 tbl 01

NOTE:
1. A_{15X} is a NC for IDT709079.

Truth Table I—
Read/Write and Enable Control[1,2,3]

$\overline{OE}$	CLK	$\overline{CE}_0$	CE_1	$R/\overline{W}$	I/O_{0-7}	Mode
X	↑	H	X	X	High-Z	Deselected
X	↑	X	L	X	High-Z	Deselected
X	↑	L	H	L	D_{IN}	Write
L	↑	L	H	H	D_{OUT}	Read
H	X	L	H	X	High-Z	Outputs Disabled

3242 tbl 02

NOTES:
1. "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
2. $\overline{ADS}$, $\overline{CNTEN}$, $\overline{CNTRST}$ = X.
3. $\overline{OE}$ is an asynchronous input signal.

Truth Table II—Address Counter Control[1,2]

External Address	Previous Internal Address	Internal Address Used	CLK	$\overline{ADS}$	$\overline{CNTEN}$	$\overline{CNTRST}$	I/O[3]	MODE
An	X	An	↑	L[4]	X	H	$D_{I/O}$ (n)	External Address Used
X	An	An + 1	↑	H	L[5]	H	$D_{I/O}$(n+1)	Counter Enabled—Internal Address generation
X	An + 1	An + 1	↑	H	H	H	$D_{I/O}$(n+1)	External Address Blocked—Counter disabled (An + 1 reused)
X	X	A0	↑	X	X	L[4]	$D_{I/O}$(0)	Counter Reset to Address 0

5640 tbl 03

NOTES:
1. "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
2. $\overline{CE}_0$ and $\overline{OE}$ = V_{IL}; CE_1 and $R/\overline{W}$ = V_{IH}.
3. Outputs configured in Flow-Through Output mode; if outputs are in Pipelined mode the data out will be delayed by one cycle.
4. $\overline{ADS}$ is independent of all other signals including $\overline{CE}_0$ and CE_1.
5. The address counter advances if $\overline{CNTEN}$ = V_{IL} on the rising edge of CLK, regardless of all other signals including $\overline{CE}_0$ and CE_1.

Recommended Operating Temperature and Supply Voltage[1]

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%

3242 tbl 04

NOTES:
1. This is the parameter T_A. This is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0[1]	V
V_{IL}	Input Low Voltage	-0.5[2]	—	0.8	V

3242 tbl 05

NOTES:
1. V_{TERM} must not exceed V_{CC} + 10%.
2. $V_{IL} \geq$ -1.5V for pulse width less than 10ns.

Absolute Maximum Ratings[1]

Symbol	Rating	Commercial & Industrial	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
T_{JN}	Junction Temperature	+150	°C
I_{OUT}	DC Output Current	50	mA

3242 tbl 06

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC}+ 10% for more than 25% of the cycle time or 10ns maximum, and is limited to $\leq$ 20mA for the period of $V_{TERM} \geq V_{CC}$ + 10%.
3. Ambient Temperature Under DC Bias. No AC Conditions. Chip Deselected.

Capacitance[1]
(T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions[2]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	9	pF
C_{OUT}[3]	Output Capacitance	V_{OUT} = 3dV	10	pF

3242 tbl 07

NOTES:
1. These parameters are determined by device characterization, but are not production tested.
2. 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
3. C_{OUT} also references $C_{I/O}$.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	709089/79S/L Min.	709089/79S/L Max.	Unit
$|I_{LI}|$	Input Leakage Current[1]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	μA
$|I_{LO}|$	Output Leakage Current	$\overline{CE}_0$ = V_{IH} or CE_1 = V_{IL}, V_{OUT} = 0V to V_{CC}	—	10	μA
V_{OL}	Output Low Voltage	I_{OL} = +4mA	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	V

3242 tbl 08

NOTE:
1. At $V_{CC} \leq$ 2.0V input leakages are undefined.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[6] (V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Version		709089/79X6 Com'l Only		709089/79X7 Com'l Only		709089/79X9 Com'l Only		Unit
					Typ.[4]	Max.	Typ.[4]	Max.	Typ.[4]	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R$ = V_{IL} Outputs Disabled f = f$_{MAX}$[1]	COM'L S		270	585	250	490	210	390	mA
			L		270	525	250	440	210	350	
			IND S		—	—	—	—	—	—	
			L		—	—	—	—	—	—	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ = $\overline{CE}_R$ = V_{IH} f = f$_{MAX}$[1]	COM'L S		80	205	65	170	50	135	mA
			L		80	175	65	145	50	115	
			IND S		—	—	—	—	—	—	
			L		—	—	—	—	—	—	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}$"A" = V_{IL} and $\overline{CE}$"B" = V_{IH}[3] Active Port Outputs Disabled, f=f$_{MAX}$[1]	COM'L S		180	405	160	340	140	270	mA
			L		180	360	160	295	140	240	
			IND S		—	—	—	—	—	—	
			L		—	—	—	—	—	—	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_R$ and $\overline{CE}_L \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V, f = 0[2]	COM'L S		1.0	15	1.0	15	1.0	15	mA
			L		0.2	5	0.2	5	0.2	5	
			IND S		—	—	—	—	—	—	
			L		—	—	—	—	—	—	
I_{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}$"A" $\leq$ 0.2V and $\overline{CE}$"B" $\geq V_{CC}$ - 0.2V[5] $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V, Active Port Outputs Disabled, f = f$_{MAX}$[1]	COM'L S		170	395	150	330	130	245	mA
			L		170	340	150	290	130	225	
			IND S		—	—	—	—	—	—	
			L		—	—	—	—	—	—	

3242 tbl 09

NOTES:
1. At f = f$_{MAX}$, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of 1/t$_{CYC}$, using "AC TEST CONDITIONS" at input levels of GND to 3V.
2. f = 0 means no address, clock, or control lines change. Applies only to input at CMOS level standby.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
4. V_{CC} = 5V, T$_A$ = 25°C for Typ, and are not production tested. I_{CC} $_{DC}$(f=0) = 150mA (Typ).
5. $\overline{CE}_X = V_{IL}$ means $\overline{CE}_{0X} = V_{IL}$ and CE$_{1X} = V_{IH}$
   $\overline{CE}_X = V_{IH}$ means $\overline{CE}_{0X} = V_{IH}$ or CE$_{1X} = V_{IL}$
   $\overline{CE}_X \leq$ 0.2V means $\overline{CE}_{0X} \leq$ 0.2V and CE$_{1X} \geq V_{CC}$ - 0.2V
   $\overline{CE}_X \geq V_{CC}$ - 0.2V means $\overline{CE}_{0X} \geq V_{CC}$ - 0.2V or CE$_{1X} \leq$ 0.2V
   "X" represents "L" for left port or "R" for right port.
6. 'X' in part numbers indicate power (S or L).

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[6] (V_{CC} = 5V ± 10%)(cont'd)

Symbol	Parameter	Test Condition	Version		709089/79X12 Com'l & Ind		709089/79X15 Com'l Only		Unit
					Typ.[4]	Max.	Typ.[4]	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R$= V_{IL} Outputs Disabled f = f$_{MAX}$[1]	COM'L	S L	200 200	345 305	190 190	325 285	mA
			IND	S L	200 200	380 340	— —	— —	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ = $\overline{CE}_R$ = V_{IH} f = f$_{MAX}$[1]	COM'L	S L	50 50	110 90	50 50	110 90	mA
			IND	S L	50 50	125 105	— —	— —	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}$"A" = V_{IL} and $\overline{CE}$"B" = V_{IH}[3] Active Port Outputs Disabled, f=f$_{MAX}$[1]	COM'L	S L	130 130	230 200	120 120	220 190	mA
			IND	S L	130 130	245 215	— —	— —	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_R$ and $\overline{CE}_L \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V, f = 0[2]	COM'L	S L	1.0 0.2	15 5	1.0 0.2	15 5	mA
			IND	S L	1.0 0.2	15 5	— —	— —	
I_{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}$"A" $\leq$ 0.2V and $\overline{CE}$"B" $\geq V_{CC}$ - 0.2V[5] $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V, Active Port Outputs Disabled, f = f$_{MAX}$[1]	COM'L	S L	120 120	205 185	110 110	195 175	mA
			IND	S L	120 120	220 200	— —	— —	

3242 tbl 09a

NOTES:
1. At f = f$_{MAX}$, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of 1/t$_{CYC}$, using "AC TEST CONDITIONS" at input levels of GND to 3V.
2. f = 0 means no address, clock, or control lines change. Applies only to input at CMOS level standby.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
4. V_{CC} = 5V, T_A = 25°C for Typ, and are not production tested. I_{CC} DC(f=0) = 150mA (Typ).
5. $\overline{CE}_X$ = V_{IL} means $\overline{CE}_{0X}$ = V_{IL} and CE_{1X} = V_{IH}
   $\overline{CE}_X$ = V_{IH} means $\overline{CE}_{0X}$ = V_{IH} or CE_{1X} = V_{IL}
   $\overline{CE}_X \leq$ 0.2V means $\overline{CE}_{0X} \leq$ 0.2V and $CE_{1X} \geq V_{CC}$ - 0.2V
   $\overline{CE}_X \geq V_{CC}$ - 0.2V means $\overline{CE}_{0X} \geq V_{CC}$ - 0.2V or $CE_{1X} \leq$ 0.2V
   "X" represents "L" for left port or "R" for right port.
6. 'X' in part numbers indicate power (S or L).

AC Test Conditions

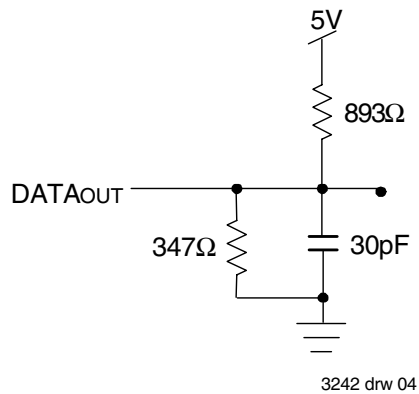|	
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1,2 and 3

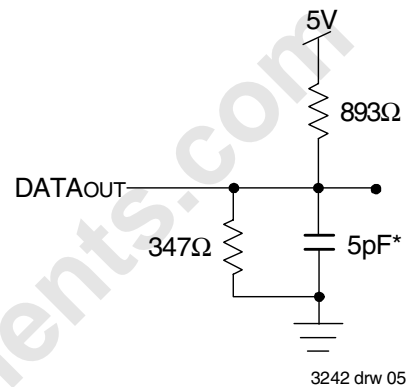3242 tbl 10

Figure 1. AC Output Test load.

3242 drw 04

Figure 2. Output Test Load
(**For** t$_{CKLZ}$, t$_{CKHZ}$, t$_{OLZ}$, **and** t$_{OHZ}$).
*Including scope and jig.

3242 drw 05

Figure 3. Typical Output Derating (Lumped Capacitive Load).

3242 drw 06

AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)[3,4] (V_{CC} = 5V ± 10%)

Symbol	Parameter	709089/79X6 Com'l Only Min.	Max.	709089/79X7 Com'l Only Min.	Max.	709089/79X9 Com'l Only Min.	Max.	709089/79X12 Com'l & Ind Min.	Max.	709089/79X15 Com'l Only Min.	Max.	Unit
t_{CYC1}	Clock Cycle Time (Flow-Through)[2]	19	—	22	—	25	—	30	—	35	—	ns
t_{CYC2}	Clock Cycle Time (Pipelined)[2]	10	—	12	—	15	—	20	—	25	—	ns
t_{CH1}	Clock High Time (Flow-Through)[2]	6.5	—	7.5	—	12	—	12	—	12	—	ns
t_{CL1}	Clock Low Time (Flow-Through)[2]	6.5	—	7.5	—	12	—	12	—	12	—	ns
t_{CH2}	Clock High Time (Pipelined)[2]	4	—	5	—	6	—	8	—	10	—	ns
t_{CL2}	Clock Low Time (Pipelined)[2]	4	—	5	—	6	—	8	—	10	—	ns
t_R	Clock Rise Time	—	3	—	3	—	3	—	3	—	3	ns
t_F	Clock Fall Time	—	3	—	3	—	3	—	3	—	3	ns
t_{SA}	Address Setup Time	3.5	—	4	—	4	—	4	—	4	—	ns
t_{HA}	Address Hold Time	0	—	0	—	1	—	1	—	1	—	ns
t_{SC}	Chip Enable Setup Time	3.5	—	4	—	4	—	4	—	4	—	ns
t_{HC}	Chip Enable Hold Time	0	—	0	—	1	—	1	—	1	—	ns
t_{SW}	R/$\overline{W}$ Setup Time	3.5	—	4	—	4	—	4	—	4	—	ns
t_{HW}	R/$\overline{W}$ Hold Time	0	—	0	—	1	—	1	—	1	—	ns
t_{SD}	Input Data Setup Time	3.5	—	4	—	4	—	4	—	4	—	ns
t_{HD}	Input Data Hold Time	0	—	0	—	1	—	1	—	1	—	ns
t_{SAD}	$\overline{ADS}$ Setup Time	3.5	—	4	—	4	—	4	—	4	—	ns
t_{HAD}	$\overline{ADS}$ Hold Time	0	—	0	—	1	—	1	—	1	—	ns
t_{SCN}	$\overline{CNTEN}$ Setup Time	3.5	—	4	—	4	—	4	—	4	—	ns
t_{HCN}	$\overline{CNTEN}$ Hold Time	0	—	0	—	1	—	1	—	1	—	ns
t_{SRST}	$\overline{CNTRST}$ Setup Time	3.5	—	4	—	4	—	4	—	4	—	ns
t_{HRST}	$\overline{CNTRST}$ Hold Time	0	—	0	—	1	—	1	—	1	—	ns
t_{OE}	Output Enable to Data Valid	—	6.5	—	7.5	—	9	—	12	—	15	ns
t_{OLZ}	Output Enable to Output Low-Z[1]	2	—	2	—	2	—	2	—	2	—	ns
t_{OHZ}	Output Enable to Output High-Z[1]	1	7	1	7	1	7	1	7	1	7	ns
t_{CD1}	Clock to Data Valid (Flow-Through)[2]	—	15	—	18	—	20	—	25	—	30	ns
t_{CD2}	Clock to Data Valid (Pipelined)[2]	—	6.5	—	7.5	—	9	—	12	—	15	ns
t_{DC}	Data Output Hold After Clock High	2	—	2	—	2	—	2	—	2	—	ns
t_{CKHZ}	Clock High to Output High-Z[1]	2	9	2	9	2	9	2	9	2	9	ns
t_{CKLZ}	Clock High to Output Low-Z[1]	2	—	2	—	2	—	2	—	2	—	ns
Port-to-Port Delay												
t_{CWDD}	Write Port Clock High to Read Data Delay	—	24	—	28	—	35	—	40	—	50	ns
t_{CCS}	Clock-to-Clock Setup Time	—	9	—	10	—	15	—	15	—	20	ns

3242 tbl 11

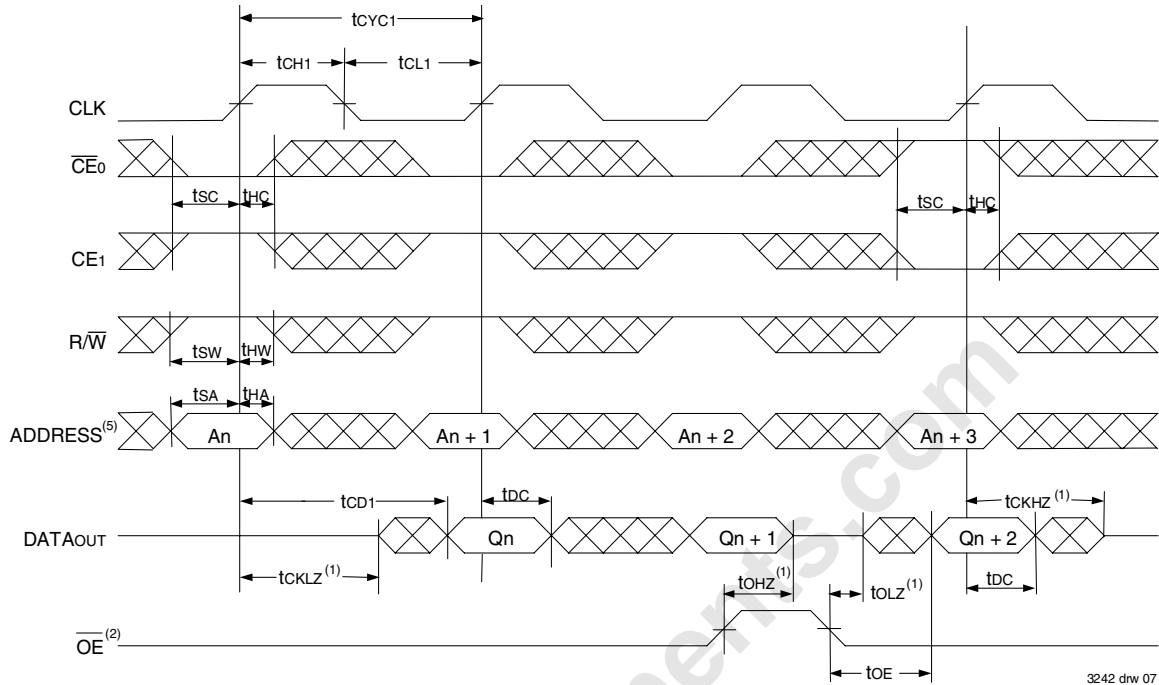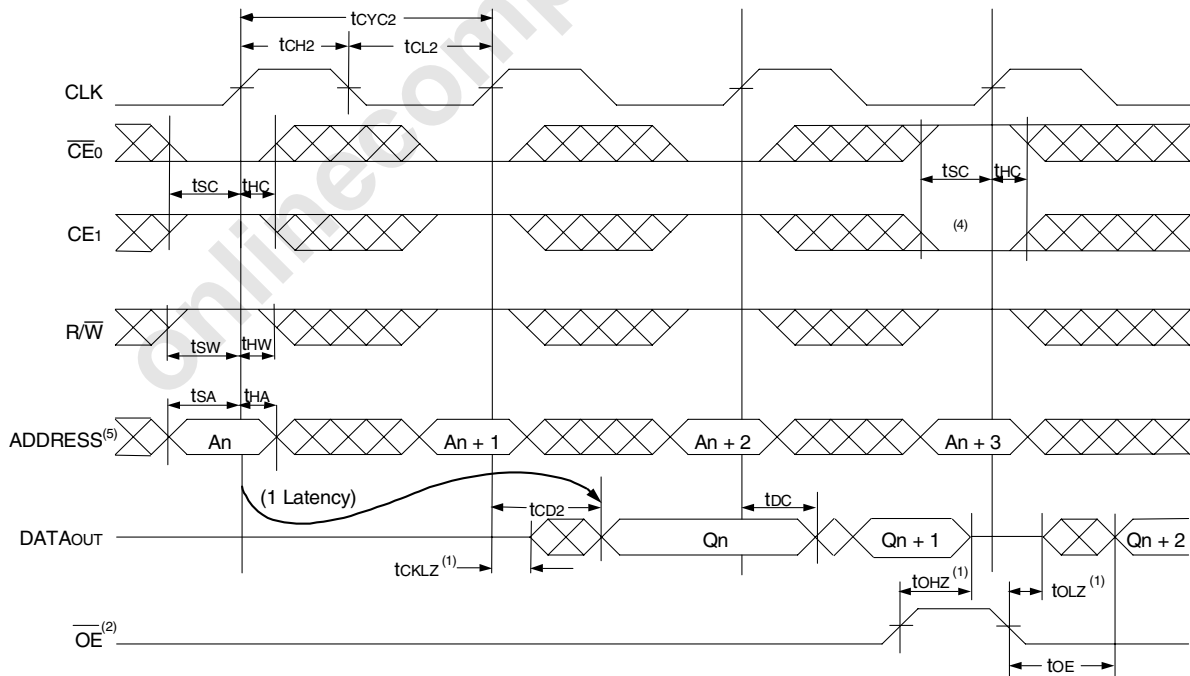**NOTES:**

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2). This parameter is guaranteed by device characterization, but is not production tested.
2. The Pipelined output parameters (t_{CYC2}, t_{CD2}) apply to either or both left and right ports when $\overline{FT}$/PIPE = V_{IH}. Flow-through parameters (t_{CYC1}, t_{CD1}) apply when $\overline{FT}$/PIPE = V_{IL} for that port.
3. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable ($\overline{OE}$) and $\overline{FT}$/PIPE. $\overline{FT}$/PIPE should be treated as a DC signal, i.e. steady state during operation.
4. 'X' in part number indicates power rating (S or L).

Timing Waveform of Read Cycle for Flow-Through Output ($\overline{FT}$/PIPE"x" = V_{IL})[3,6]

3242 drw 07

Timing Waveform of Read Cycle for Pipelined Output ($\overline{FT}$/PIPE"x" = V_{IH})[3,6]

3242 drw 08

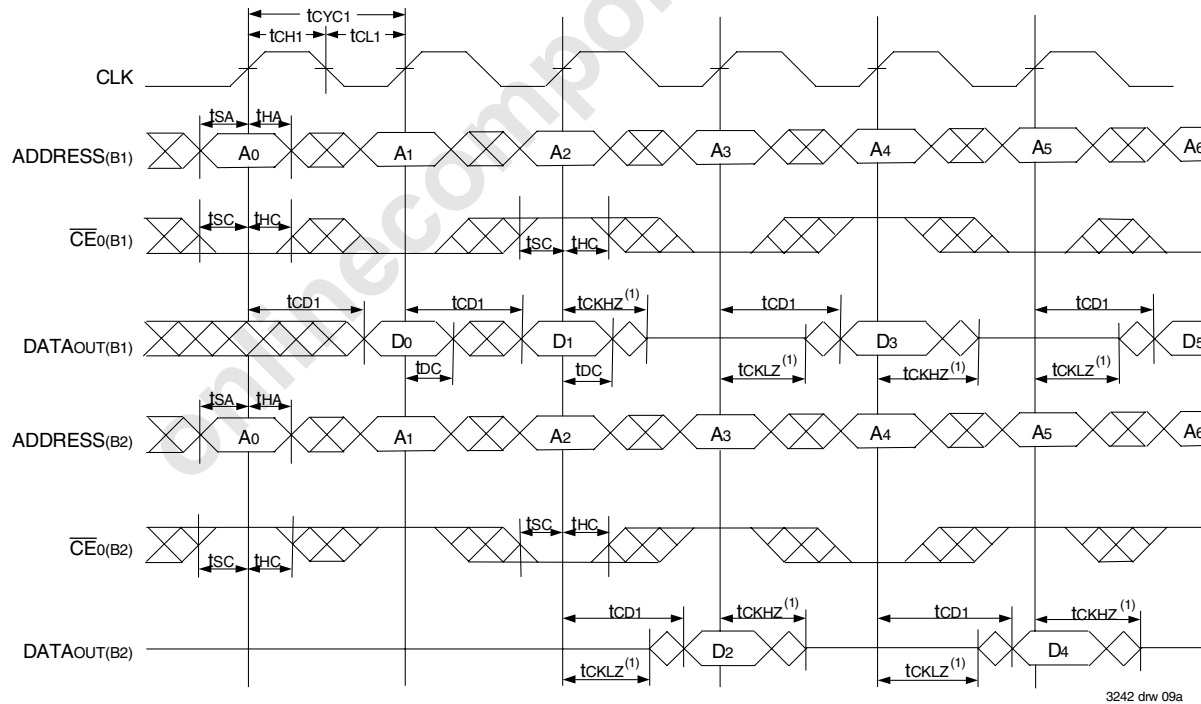**NOTES:**
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. $\overline{OE}$ is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
3. $\overline{ADS}$ = V_{IL} and $\overline{CNTRST}$ = V_{IH}.
4. The output is disabled (High-Impedance state) by $\overline{CE}_0$ = V_{IH} or CE_1 = V_{IL} following the next rising edge of clock. Refer to Truth Table 1.
5. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
6. "x" denotes Left or Right port. The diagram is with respect to that port.
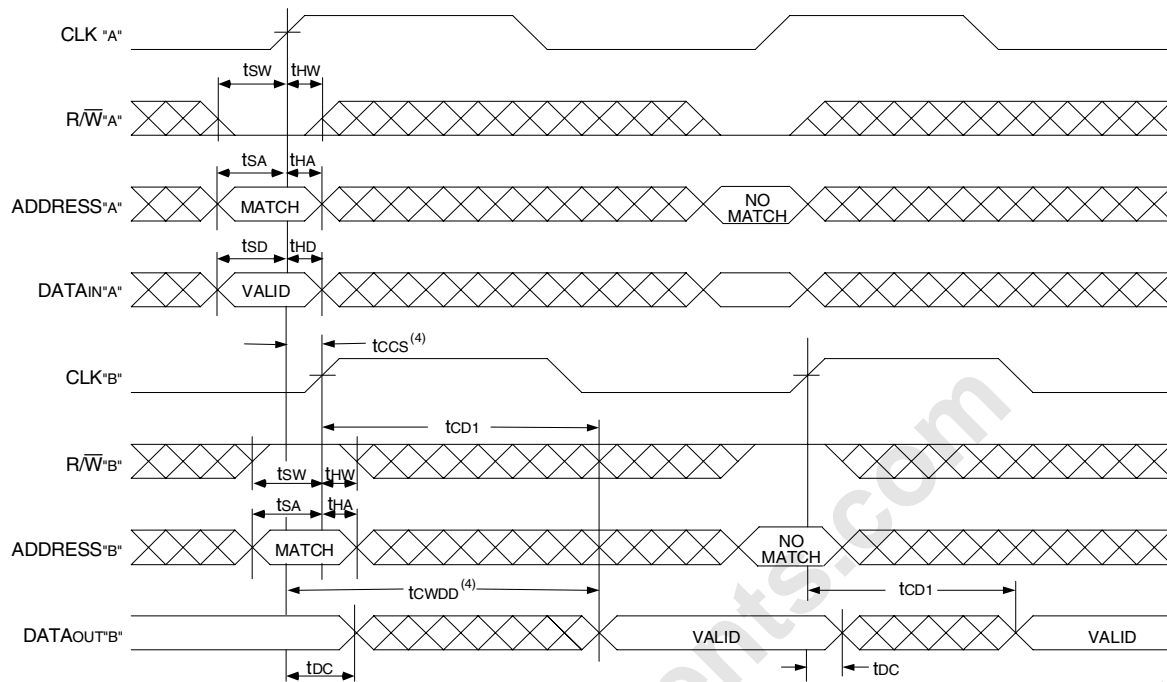
Timing Waveform of a Bank Select Pipelined Read[1,2]

3242 drw 09

Timing Waveform of a Bank Select Flow-Through Read[6,7]

3242 drw 09a

NOTES:

1. B1 Represents Bank #1; B2 Represents Bank #2. Each Bank consists of one IDT709089/79 for this waveform, and are setup for depth expansion in this example. ADDRESS(B1) = ADDRESS(B2) in this situation.

2. $\overline{OE}$ and $\overline{ADS}$ = V_{IL}; CE1(B1), CE1(B2), R/$\overline{W}$ and $\overline{CNTRST}$ = V_{IH}.

3. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).

4. $\overline{CE}0$ and $\overline{ADS}$ = V_{IL}; CE1 and $\overline{CNTRST}$ = V_{IH}.

5. $\overline{OE}$ = V_{IL} for the Right Port, which is being read from. $\overline{OE}$ = V_{IH} for the Left Port, which is being written to.

6. If $t_{CCS} \leq$ maximum specified, then data from right port READ is not valid until the maximum specified for t_{CWDD}.
   If $t_{CCS} >$ maximum specified, then data from right port READ is not valid until $t_{CCS} + t_{CD1}$. t_{CWDD} does not apply in this case.

7. All timing is the same for both Left and Right ports. Port "A" may be either Left or Right port. Port "B" is the opposite of Port "A".

Timing Waveform with Port-to-Port Flow-Through Read[1,2,3,5]

3242 drw 10

NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. $\overline{CE}_0$ and $\overline{ADS}$ = V_{IL}; CE₁ and $\overline{CNTRST}$ = V_{IH}.
3. $\overline{OE}$ = V_{IL} for the Right Port, which is being read from. $\overline{OE}$ = V_{IH} for the Left Port, which is being written to.
4. If $t_{CCS} \leq$ maximum specified, then data from right port READ is not valid until the maximum specified for t_{CWDD}.
   If $t_{CCS} >$ maximum specified, then data from right port READ is not valid until $t_{CCS} + t_{CD1}$. t_{CWDD} does not apply in this case.
5. All timing is the same for both Left and Right ports. Port "A" may be either Left or Right port. Port "B" is the opposite of Port "A".

Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{\text{OE}}$ = V$_{IL}$)[3]

3242 drw 11

Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{\text{OE}}$ Controlled)[3]

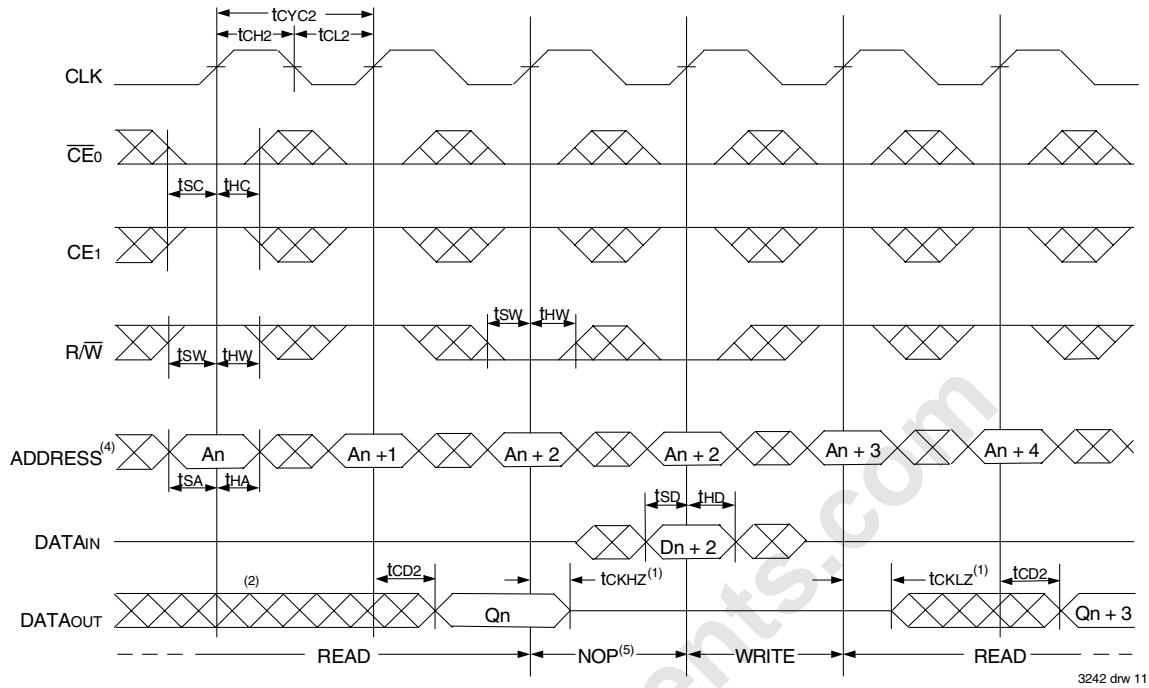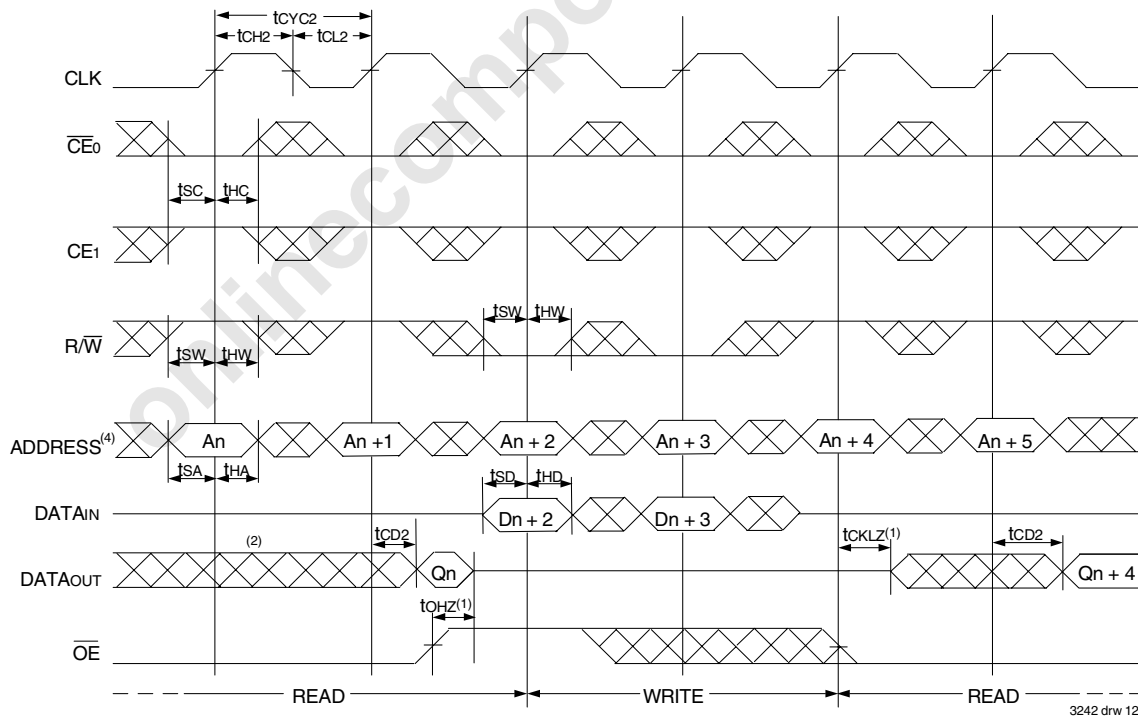

3242 drw 12

NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
3. $\overline{\text{CE}}_0$ and $\overline{\text{ADS}}$ = V$_{IL}$; CE$_1$ and $\overline{\text{CNTRST}}$ = V$_{IH}$.
4. Addresses do not have to be accessed sequentially since $\overline{\text{ADS}}$ = V$_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

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IDT709089/79S/L
High-Speed 64/32K x 8 Synchronous Dual-Port Static RAM   **Industrial and Commercial Temperature Ranges**

Timing Waveform Flow-Through Read-to-Write-to-Read ($\overline{OE}$ = V$_{IL}$)[3]

CLK

$\overline{CE}_0$

CE$_1$

R/$\overline{W}$

ADDRESS[4]

DATA$_{IN}$

DATA$_{OUT}$

tCYC1, tCH1, tCL1, tSC, tHC, tSW, tHW, tSA, tHA, tSD, tHD, tCD1, tDC, tCKHZ[1], tCKLZ[1]

An, An +1, An + 2, An + 2, An + 3, An + 4

Dn + 2

Qn, Qn + 1, Qn + 3

READ — NOP[5] — WRITE — READ

3242 drw 13

Timing Waveform of Flow-Through Read-to-Write-to-Read ($\overline{OE}$ Controlled)[3]

CLK

$\overline{CE}_0$

CE$_1$

R/$\overline{W}$

ADDRESS[4]

DATA$_{IN}$

DATA$_{OUT}$

$\overline{OE}$

tCYC1, tCH1, tCL1, tSC, tHC, tSW, tHW, tSA, tHA, tSD, tHD, tCD1, tDC, tOE, tOHZ[1], tCKLZ[1], tDC

An, An +1, An + 2, An + 3, An + 4, An + 5

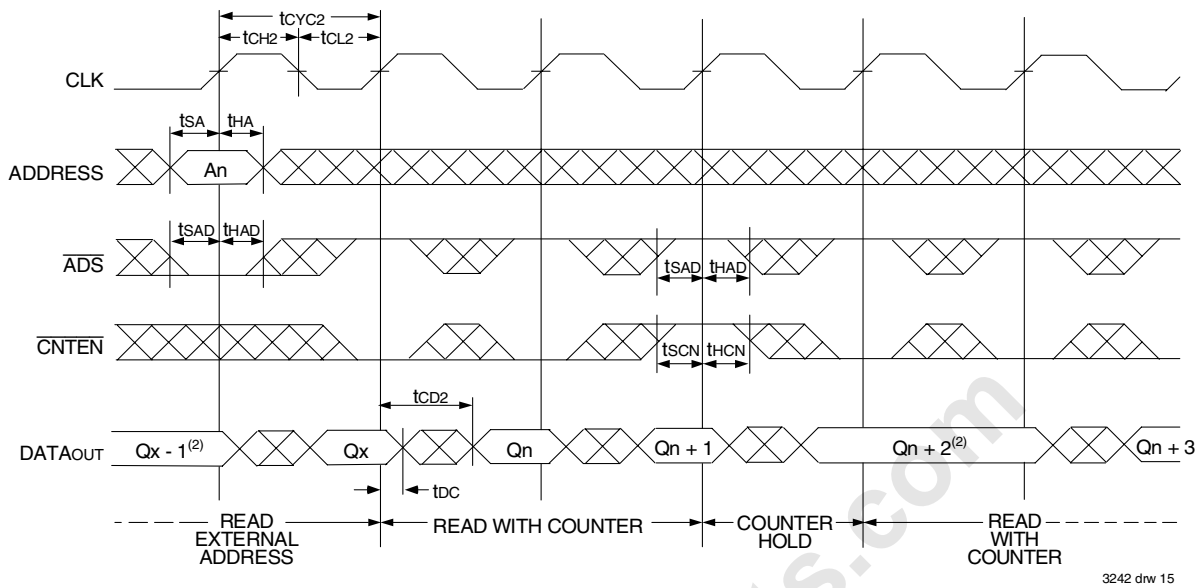Dn + 2, Dn + 3
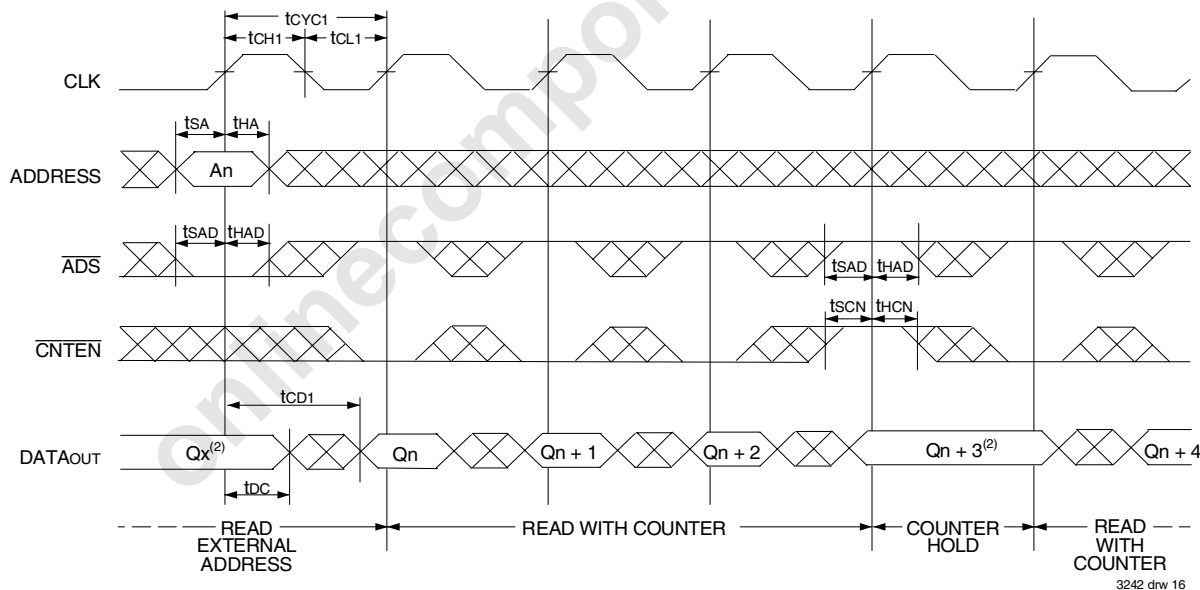
Qn, Qn + 4

READ — WRITE — READ

3242 drw 14

NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance is determined by the previous cycle control signals.
3. $\overline{CE}_0$ and $\overline{ADS}$ = V$_{IL}$; CE$_1$ and $\overline{CNTRST}$ = V$_{IH}$.
4. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V$_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

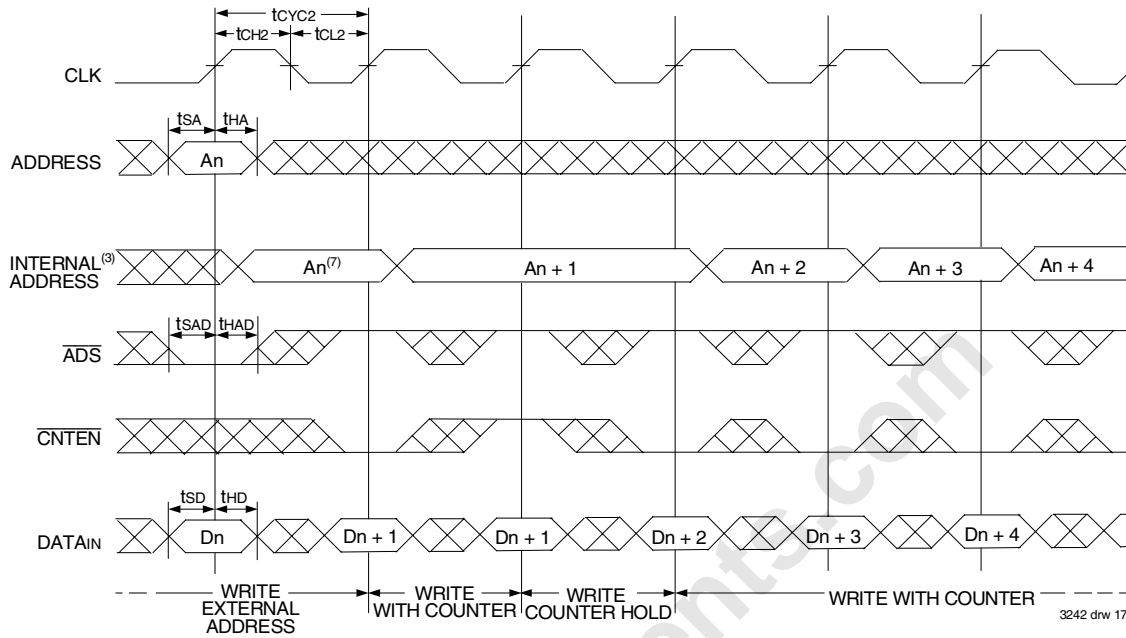## Timing Waveform of Pipelined Read with Address Counter Advance[1]

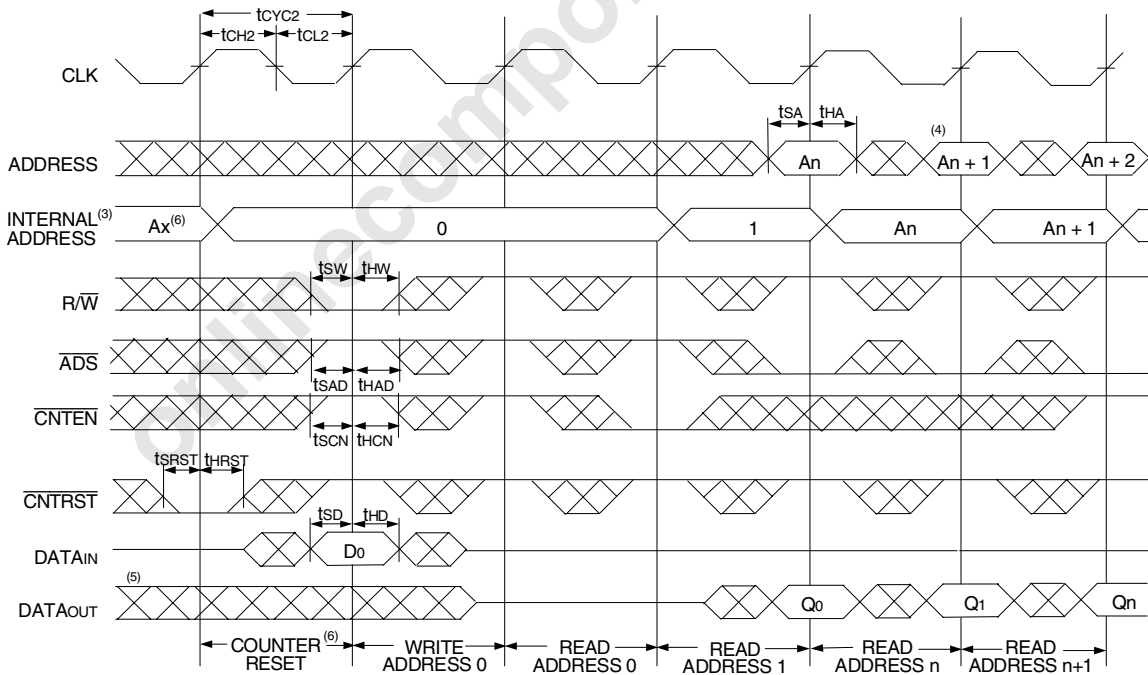## Timing Waveform of Flow-Through Read with Address Counter Advance[1]

NOTES:

1. $\overline{CE}_0$ and $\overline{OE}$ = V_{IL}; CE_1, R/$\overline{W}$, and $\overline{CNTRST}$ = V_{IH}.

2. If there is no address change via $\overline{ADS}$ = V_{IL} (loading a new address) or $\overline{CNTEN}$ = V_{IL} (advancing the address), i.e. $\overline{ADS}$ = V_{IH} and $\overline{CNTEN}$ = V_{IH}, then the data output remains constant for subsequent clocks.

Timing Waveform of Write with Address Counter Advance (Flow-Through or Pipelined Outputs)[1]

3242 drw 17

Timing Waveform of Counter Reset (Pipelined Outputs)[2]

3242 drw 18

NOTES:

1. $\overline{CE_0}$ and R/$\overline{W}$ = V_{IL}; CE_1 and $\overline{CNTRST}$ = V_{IH}.
2. $\overline{CE_0}$ = V_{IL}; CE_1 = V_{IH}.
3. The "Internal Address" is equal to the "External Address" when $\overline{ADS}$ = V_{IL} and equals the counter output when $\overline{ADS}$ = V_{IH}.
4. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
6. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset. $ADDR_0$ will be accessed. Extra cycles are shown here simply for clarification.
7. $\overline{CNTEN}$ = V_{IL} advances Internal Address from 'An' to 'An +1'. The transition shown indicates the time required for the counter to advance. The 'An +1'Address is written to during this cycle.

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Functional Description

The IDT709089/79 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse is independent of the LOW to HIGH transition of the clock signal.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

A HIGH on $\overline{CE}_0$ or a LOW on CE_1 for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT709089/79's for depth expansion configurations. When the Pipelined output mode is enabled, two cycles are required with $\overline{CE}_0$ LOW and CE_1 HIGH to re-activate the outputs.

Depth and Width Expansion

The IDT709089/79 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT709089/79 can also be used in applications requiring expanded width, as indicated in Figure 4. Since the banks are allocated at the discretion of the user, the external controller can be set up to drive the input signals for the various devices as required to allow for 16-bit or wider applications.
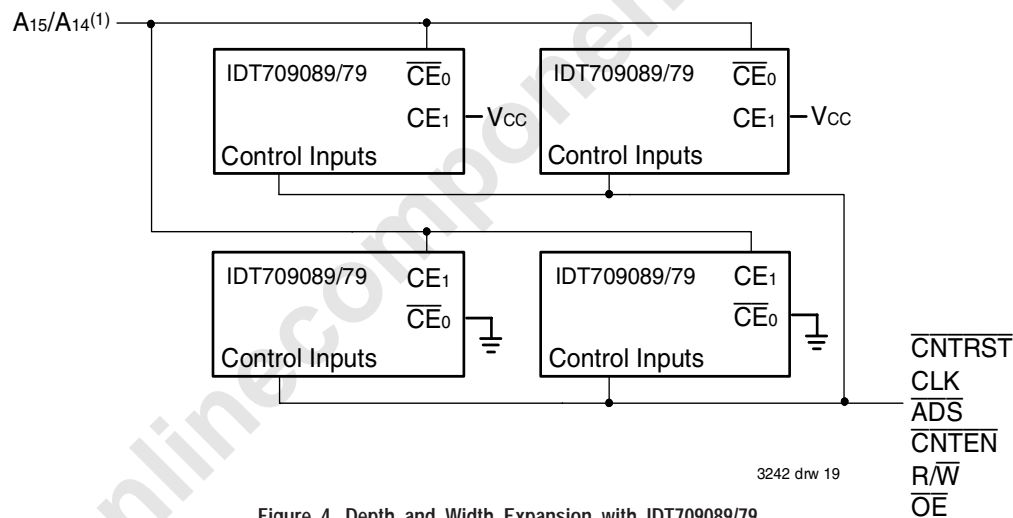

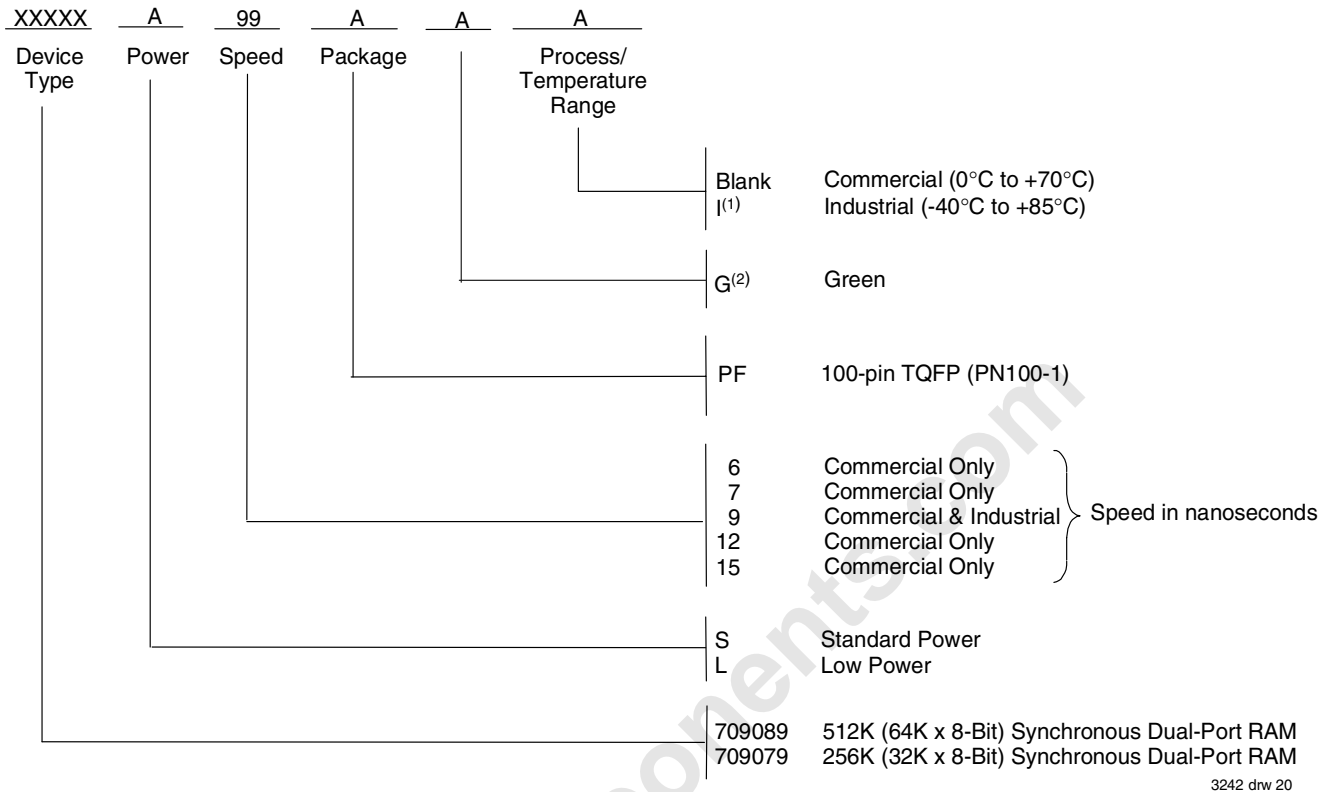Figure 4. Depth and Width Expansion with IDT709089/79

NOTE:

1. A_{15} is for IDT709089, A_{14} is for IDT709079.

Ordering Information

```
XXXXX     A     99     A     A     A
Device   Power  Speed  Package     Process/
Type                               Temperature
                                   Range
```

Blank	Commercial (0°C to +70°C)
I[1]	Industrial (-40°C to +85°C)

G[2]	Green

PF	100-pin TQFP (PN100-1)

6	Commercial Only	
7	Commercial Only	
9	Commercial & Industrial	Speed in nanoseconds
12	Commercial Only	
15	Commercial Only	

S	Standard Power
L	Low Power

709089	512K (64K x 8-Bit) Synchronous Dual-Port RAM
709079	256K (32K x 8-Bit) Synchronous Dual-Port RAM

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NOTE:
1. Contact your local sales office for industrial temp range for other speeds, packages and powers.
2. Green parts available. For specific speeds, packages and powers contact your sales office.

Ordering Information for Flow-through Devices

Old Flow-through Part	New Combined Part
70908S/L20	709089S/L9
70908S/L25	709089S/L12
70908S/L30	709089S/L15

3242 tbl 12

IDT Clock Solution for IDT709089/79 Dual-Port

IDT Dual-Port Part Number	Dual-Port I/O Specifications		Clock Specifications				IDT PLL Clock Device	IDT Non-PLL Clock Device
	Voltage	I/O	Input Capacitance	Input Duty Cycle Requirement	Maximum Frequency	Jitter Tolerance		
709089/79	5	TTL	9pF	40%	100	150ps	FCT88915TT	49FCT805T 49FCT806T 74FCT807T

3242 tbl 13

Datasheet Document History

1/12/99:		Initiated datasheet document history
		Converted to new format
		Cosmetic and typographical corrections
		Added additional notes to pin configurations
	Page 15	Added Depth and Width Expansion note
6/7/99:		Changed drawing format
	Page 4	Deleted note 6 for Table II
11/10/99:		Replaced IDT logo
12/22/99:	Page 1	Removed "Separate upper-byte..." line
1/12/00:		Combined Pipelined 709089 family and Flow-through 70908 family offerings into one data sheet
		Changed ±200mV in waveform notes to 0mV
		Added corresponding part chart with ordering information
2/18/00:	Pages 8 & 9	Changed ±220mV waveform notes to 0mV
	Page 9	Changed "Operation" in heading to "Pipelined Output", fixed drawing 08
		Removed PGA package
5/24/00:	Page 3	Changed information in Truth Table II
	Page 4	Increased storage temperature parameters
		Clarified T_A parameter
	Page 5	DC Electrical parameters–changed wording from "open" to "disabled"
		Added Industrial Temperature Ranges and removed related notes
01/10/02:	Page 2	Added date revision for pin configuration
	Page 5 & 7	Removed industrial temp from column headings and values for 15ns from AC & DC Electrical Characteristics
	Page 16	Removed industrial offering from 15ns ordering info and added industrial temp footnote
	Page 1 & 17	Replaced IDT ™ logo with ® logo
06/21/04:		Consolidated multiple devices into one datasheet
		Removed Preliminary status from datasheet
	Page 4	Added Junction Temperature to Absolute Maximum Ratings Table
		Added Ambient Temperature footnote
	Page 5	Added 6ns & 7ns speed DC timing numbers to the DC Electrical Characteristics Table
	Page 8	Added 6ns & 7ns speed AC timing numbers to the AC Electrical Characteristics Table
	Page 17	Added 6ns & 7ns speed grades to ordering information
		Added IDT Clock Solution Table
	Page 1 & 18	Replaced old ® logo with new ™ logo
01/29/09:	Page 17	Removed "IDT" from orderable part number
07/26/10:	Page 1	Added green parts availability to features
	Page 17	Added green indicator to ordering information
	Page 8	In order to correct the header notes of the AC Elect Chars Table and align them with the Industrial temp range values located in the table, the commercial T_A header note has been removed
	Pages 9-13	In order to correct the footnotes of timing diagrams, $\overline{CNTEN}$ has been removed to reconcile the footnotes with the $\overline{CNTEN}$ logic definition found in Truth Table II - Address Counter Control