



## CMOS Static RAM 256K (32K x 8-Bit)

**IDT71256S**  
**IDT71256L**

### Features

- ♦ **High-speed address/chip select time**
  - Military: 25/35/45/55/70/85/100ns (max.)
  - Industrial: 25/35ns (max.)
  - Commercial: 20/25/35ns (max.) low power only
- ♦ **Low-power operation**
- ♦ **Battery Backup operation – 2V data retention**
- ♦ **Produced with advanced high-performance CMOS technology**
- ♦ **Input and output directly TTL-compatible**
- ♦ **Available in standard 28-pin (300 or 600 mil) ceramic DIP, 28-pin (600 mil) plastic DIP, 28-pin (300 mil) SOJ and 32-pin LCC**
- ♦ **Military product compliant to MIL-STD-883, Class B**

### Description

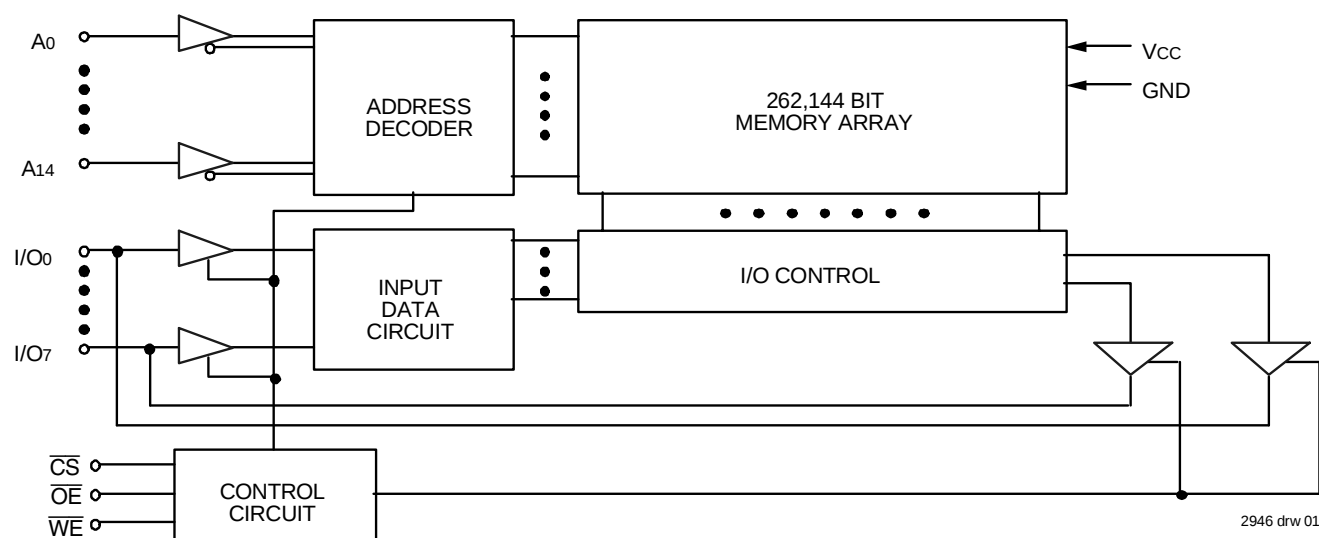
The IDT 71256 is a 262,144-bit high-speed static RAM organized as 32K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology.

Address access times as fast as 20ns are available with power consumption of only 350mW (typ.). The circuit also offers a reduced power standby mode. When  $\overline{CS}$  goes HIGH, the circuit will automatically go to and remain in, a low-power standby mode as long as  $\overline{CS}$  remains HIGH. In the full standby mode, the low-power device consumes less than 15 $\mu$ W, typically. This capability provides significant system level power and cooling savings. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 5 $\mu$ W when operating off a 2V battery.

The IDT71256 is packaged in a 28-pin (300 or 600 mil) ceramic DIP, a 28-pin 300 mil SOJ, a 28-pin (600 mil) plastic DIP, and a 32-pin LCC providing high board level packing densities.

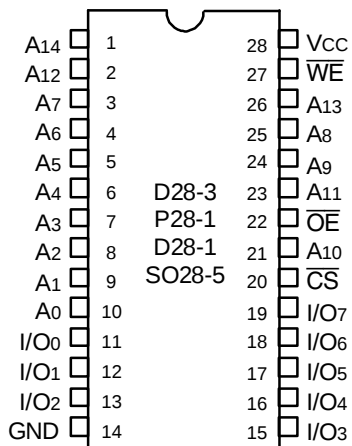
The IDT71256 military RAM is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

### Functional Block Diagram



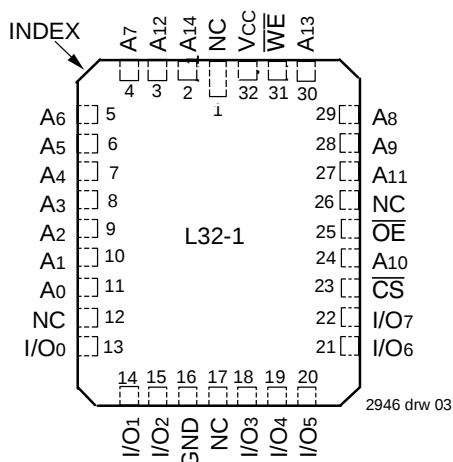
NOVEMBER 2008

## Pin Configurations



2946 drw 02

DIP/SOJ  
Top View



2946 drw 03

32-Pin LCC  
Top View

## Pin Descriptions

| Name            | Description       |
|-----------------|-------------------|
| A0 - A14        | Address Inputs    |
| I/O0 - I/O7     | Data Input/Output |
| $\overline{CS}$ | Chip Select       |
| $\overline{WE}$ | Write Enable      |
| $\overline{OE}$ | Output Enable     |
| GND             | Ground            |
| Vcc             | Power             |

2946 tbl 01

## Truth Table<sup>(1)</sup>

| $\overline{WE}$ | $\overline{CS}$ | $\overline{OE}$ | I/O    | Function              |
|-----------------|-----------------|-----------------|--------|-----------------------|
| X               | H               | X               | High-Z | Standby ( $IS_B$ )    |
| X               | $V_{HC}$        | X               | High-Z | Standby ( $IS_{B1}$ ) |
| H               | L               | H               | High-Z | Output Disabled       |
| H               | L               | L               | DOUT   | Read Data             |
| L               | L               | X               | DIN    | Write Data            |

2946 tbl 02

### NOTE:

1. H =  $V_{IH}$ , L =  $V_{IL}$ , X = Don't care.

## Absolute Maximum Ratings<sup>(1)</sup>

| Symbol     | Rating                               | Com'l.       | Ind.         | Mil.         | Unit |
|------------|--------------------------------------|--------------|--------------|--------------|------|
| $V_{TERM}$ | Terminal Voltage with Respect to GND | -0.5 to +7.0 | -0.5 to +7.0 | -0.5 to +7.0 | V    |
| $T_A$      | Operating Temperature                | 0 to +70     | -40 to +85   | -55 to +125  | °C   |
| $T_{BIAS}$ | Temperature Under Bias               | -55 to +125  | -55 to +125  | -65 to +135  | °C   |
| $T_{STG}$  | Storage Temperature                  | -55 to +125  | -55 to +125  | -65 to +150  | °C   |
| $P_T$      | Power Dissipation                    | 1.0          | 1.0          | 1.0          | W    |
| $I_{OUT}$  | DC Output Current                    | 50           | 50           | 50           | mA   |

2946 tbl 03

### NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Capacitance ( $T_A = +25^\circ\text{C}$ , $f = 1.0\text{MHz}$ )

| Symbol   | Parameter <sup>(1)</sup> | Conditions     | Max. | Unit |
|----------|--------------------------|----------------|------|------|
| $C_{IN}$ | Input Capacitance        | $V_{IN} = 0V$  | 11   | pF   |
| $C_{VO}$ | I/O Capacitance          | $V_{OUT} = 0V$ | 11   | pF   |

2946 tbl 04

### NOTE:

1. This parameter is determined by device characterization, but is not production tested.

## Recommended Operating Temperature and Supply Voltage

| Grade      | Temperature     | GND | Vcc      |
|------------|-----------------|-----|----------|
| Military   | -55°C to +125°C | 0V  | 5V ± 10% |
| Industrial | -40°C to +85°C  | 0V  | 5V ± 10% |
| Commercial | 0°C to +70°C    | 0V  | 5V ± 10% |

2946 tbl 05

## Recommended DC Operating Conditions

| Symbol          | Parameter          | Min.                | Typ. | Max. | Unit |
|-----------------|--------------------|---------------------|------|------|------|
| Vcc             | Supply Voltage     | 4.5                 | 5.0  | 5.5  | V    |
| GND             | Ground             | 0                   | 0    | 0    | V    |
| V <sub>IH</sub> | Input High Voltage | 2.2                 | —    | 6.0  | V    |
| V <sub>IL</sub> | Input Low Voltage  | -0.5 <sup>(1)</sup> | —    | 0.8  | V    |

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### NOTE:

- V<sub>IL</sub> (min.) = -3.0V for pulse width less than 20ns, once per cycle.

## DC Electrical Characteristics<sup>(1,2)</sup> (V<sub>CC</sub> = 5.0V ± 10%, V<sub>LC</sub> = 0.2V, V<sub>HC</sub> = V<sub>CC</sub> - 0.2V)

| Symbol | Parameter                                                                                                                                        | Power | 71256S/L20   |      | 71256S/L25   |      | 71256S/L35   |      | 71256S/L45 |      | Unit |
|--------|--------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------------|------|--------------|------|--------------|------|------------|------|------|
|        |                                                                                                                                                  |       | Com'l. & Ind | Mil. | Com'l. & Ind | Mil. | Com'l. & Ind | Mil. | Com'l.     | Mil. |      |
| ICC    | Dynamic Operating Current<br>CS ≤ V <sub>IL</sub> , Outputs Open<br>V <sub>CC</sub> = Max., f <sub>MAX</sub> <sup>(2)</sup>                      | S     | —            | —    | —            | 150  | —            | 140  | —          | 135  | mA   |
|        |                                                                                                                                                  | L     | 135          | —    | 125          | 130  | 115          | 120  | —          | 115  |      |
| ISB    | Standby Power Supply Current<br>(TTL Level), CS ≥ V <sub>IH</sub> , V <sub>CC</sub> = Max.,<br>Outputs Open, f = f <sub>MAX</sub> <sup>(2)</sup> | S     | —            | —    | —            | 20   | —            | 20   | —          | 20   | mA   |
|        |                                                                                                                                                  | L     | 3            | —    | 3            | 3    | 3            | 3    | —          | 3    |      |
| ISB1   | Full Standby Power Supply Current<br>(CMOS Level), CS ≥ V <sub>HC</sub> ,<br>V <sub>CC</sub> = Max., f = 0                                       | S     | —            | —    | —            | 20   | —            | 20   | —          | 20   | mA   |
|        |                                                                                                                                                  | L     | 0.6          | —    | 0.6          | 1.5  | 0.6          | 1.5  | —          | 1.5  |      |

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| Symbol | Parameter                                                                                                                                        | Power | 71256S/L55 | 71256S/L70 | 71256S/L85 | 71256S/L100 | Unit |
|--------|--------------------------------------------------------------------------------------------------------------------------------------------------|-------|------------|------------|------------|-------------|------|
|        |                                                                                                                                                  |       | Mil.       | Mil.       | Mil.       | Mil.        |      |
| ICC    | Dynamic Operating Current<br>CS ≤ V <sub>IL</sub> , Outputs Open<br>V <sub>CC</sub> = Max., f <sub>MAX</sub> <sup>(2)</sup>                      | S     | 135        | 135        | 135        | 135         | mA   |
|        |                                                                                                                                                  | L     | 115        | 115        | 115        | 115         |      |
| ISB    | Standby Power Supply Current<br>(TTL Level), CS ≥ V <sub>IH</sub> , V <sub>CC</sub> = Max.,<br>Outputs Open, f = f <sub>MAX</sub> <sup>(2)</sup> | S     | 20         | 20         | 20         | 20          | mA   |
|        |                                                                                                                                                  | L     | 3          | 3          | 3          | 3           |      |
| ISB1   | Full Standby Power Supply Current<br>(CMOS Level), CS ≥ V <sub>HC</sub> ,<br>V <sub>CC</sub> = Max., f = 0                                       | S     | 20         | 20         | 20         | 20          | mA   |
|        |                                                                                                                                                  | L     | 1.5        | 1.5        | 1.5        | 1.5         |      |

2946 tbl 08

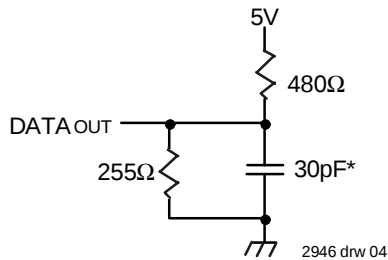
### NOTES:

- All values are maximum guaranteed values.
- f<sub>MAX</sub> = 1/TRC, all address inputs are cycling at f<sub>MAX</sub>; f = 0 means no address pins are cycling.

## AC Test Conditions

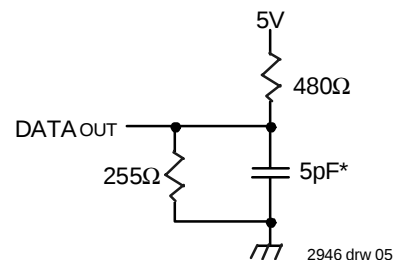
|                               |                     |
|-------------------------------|---------------------|
| Input Pulse Levels            | GND to 3.0V         |
| Input Rise/Fall Times         | 5ns                 |
| Input Timing Reference Levels | 1.5V                |
| Output Reference Levels       | 1.5V                |
| AC Test Load                  | See Figures 1 and 2 |

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2946 drw 04

Figure 1. AC Test Load



2946 drw 05

Figure 2. AC Test Load

(for tCLZ, tOLZ, tCHZ, tOHZ, tOW, and tWHZ)

\*Includes scope and jig capacitances

## DC Electrical Characteristics (V<sub>CC</sub> = 5.0V ± 10%)

| Symbol          | Parameter              | Test Conditions                                                                                          |                      | IDT71256S |        |         | IDT71256L |        |        | Unit |
|-----------------|------------------------|----------------------------------------------------------------------------------------------------------|----------------------|-----------|--------|---------|-----------|--------|--------|------|
|                 |                        |                                                                                                          |                      | Min.      | Typ.   | Max.    | Min.      | Typ.   | Max.   |      |
| I <sub>LI</sub> | Input Leakage Current  | V <sub>CC</sub> = Max.,<br>V <sub>IN</sub> = GND to V <sub>CC</sub>                                      | MIL.<br>COM"L & IND. | —<br>—    | —<br>— | 10<br>5 | —<br>—    | —<br>— | 5<br>2 | μA   |
| I <sub>LO</sub> | Output Leakage Current | V <sub>CC</sub> = Max., $\overline{CS}$ = V <sub>IH</sub> ,<br>V <sub>OUT</sub> = GND to V <sub>CC</sub> | MIL.<br>COM"L & IND. | —<br>—    | —<br>— | 10<br>5 | —<br>—    | —<br>— | 5<br>2 | μA   |
| V <sub>OL</sub> | Output Low Voltage     | I <sub>OL</sub> = 8mA, V <sub>CC</sub> = Min.                                                            |                      | —         | —      | 0.4     | —         | —      | 0.4    | V    |
|                 |                        | I <sub>OL</sub> = 10mA, V <sub>CC</sub> = Min.                                                           |                      | —         | —      | 0.5     | —         | —      | 0.5    |      |
| V <sub>OH</sub> | Output High Voltage    | I <sub>OH</sub> = -4mA, V <sub>CC</sub> = Min.                                                           |                      | 2.4       | —      | —       | 2.4       | —      | —      | V    |

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## Data Retention Characteristics Over All Temperature Ranges

(L Version Only) (V<sub>LC</sub> = 0.2V, V<sub>HC</sub> = V<sub>CC</sub> - 0.2V)

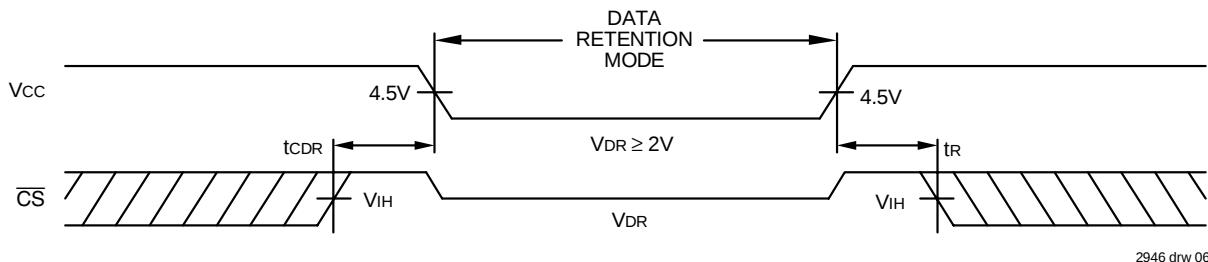
| Symbol                         | Parameter                            | Test Condition              | Min.                           | Typ. <sup>(1)</sup><br>V <sub>CC</sub> @ |        | Max.<br>V <sub>CC</sub> @ |            | Unit |
|--------------------------------|--------------------------------------|-----------------------------|--------------------------------|------------------------------------------|--------|---------------------------|------------|------|
|                                |                                      |                             |                                | 2.0V                                     | 3.0V   | 2.0V                      | 3.0V       |      |
| V <sub>DR</sub>                | V <sub>CC</sub> for Data Retention   | —                           | 2.0                            | —                                        | —      | —                         | —          | V    |
| I <sub>CDR</sub>               | Data Retention Current               | MIL.<br>COM"L & IND.        | —<br>—                         | —<br>—                                   | —<br>— | 500<br>120                | 800<br>200 | μA   |
| t <sub>CDR</sub>               | Chip Deselect to Data Retention Time | $\overline{CS} \geq V_{HC}$ | 0                              | —                                        | —      | —                         | —          | ns   |
| t <sub>tr</sub> <sup>(3)</sup> | Operation Recovery Time              |                             | t <sub>RC</sub> <sup>(2)</sup> | —                                        | —      | —                         | —          | ns   |

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### NOTES:

- T<sub>A</sub> = +25°C.
- t<sub>RC</sub> = Read Cycle Time.
- This parameter is guaranteed by device characterization, but is not production tested.

## Low Vcc Data Retention Waveform



## AC Electrical Characteristics (Vcc = 5.0V ± 10%, All Temperature Ranges)

| Symbol              | Parameter                          | 71256L20 <sup>(1)</sup> |      | 71256S25<br>71256L25 |      | 71256S35<br>71256L35 |      | 71256S45 <sup>(3)</sup><br>71256L45 <sup>(3)</sup> |      | Unit |
|---------------------|------------------------------------|-------------------------|------|----------------------|------|----------------------|------|----------------------------------------------------|------|------|
|                     |                                    | Min.                    | Max. | Min.                 | Max. | Min.                 | Max. | Min.                                               | Max. |      |
| Read Cycle          |                                    |                         |      |                      |      |                      |      |                                                    |      |      |
| tRC                 | Read Cycle Time                    | 20                      | —    | 25                   | —    | 35                   | —    | 45                                                 | —    | ns   |
| tAA                 | Address Access Time                | —                       | 20   | —                    | 25   | —                    | 35   | —                                                  | 45   | ns   |
| tACS                | Chip Select Access Time            | —                       | 20   | —                    | 25   | —                    | 35   | —                                                  | 45   | ns   |
| tOLZ <sup>(2)</sup> | Chip Select to Output in Low-Z     | 5                       | —    | 5                    | —    | 5                    | —    | 5                                                  | —    | ns   |
| tCHZ <sup>(2)</sup> | Chip Deselect to Output in High-Z  | —                       | 10   | —                    | 11   | —                    | 15   | —                                                  | 20   | ns   |
| tOE                 | Output Enable to Output Valid      | —                       | 10   | —                    | 11   | —                    | 15   | —                                                  | 20   | ns   |
| tOLZ <sup>(2)</sup> | Output Enable to Output in Low-Z   | 2                       | —    | 2                    | —    | 2                    | —    | 0                                                  | —    | ns   |
| tOHZ <sup>(2)</sup> | Output Disable to Output in High-Z | 2                       | 8    | 2                    | 10   | 2                    | 15   | —                                                  | 20   | ns   |
| tOH                 | Output Hold from Address Change    | 5                       | —    | 5                    | —    | 5                    | —    | 5                                                  | —    | ns   |
| Write Cycle         |                                    |                         |      |                      |      |                      |      |                                                    |      |      |
| tWC                 | Write Cycle Time                   | 20                      | —    | 25                   | —    | 35                   | —    | 45                                                 | —    | ns   |
| tCW                 | Chip Select to End-of-Write        | 15                      | —    | 20                   | —    | 30                   | —    | 40                                                 | —    | ns   |
| tAW                 | Address Valid to End-of-Write      | 15                      | —    | 20                   | —    | 30                   | —    | 40                                                 | —    | ns   |
| tAS                 | Address Set-up Time                | 0                       | —    | 0                    | —    | 0                    | —    | 0                                                  | —    | ns   |
| tWP                 | Write Pulse Width                  | 15                      | —    | 20                   | —    | 30                   | —    | 35                                                 | —    | ns   |
| tWR                 | Write Recovery Time                | 0                       | —    | 0                    | —    | 0                    | —    | 0                                                  | —    | ns   |
| tDW                 | Data to Write Time Overlap         | 11                      | —    | 13                   | —    | 15                   | —    | 20                                                 | —    | ns   |
| tWHZ <sup>(2)</sup> | Write Enable to Output in High-Z   | —                       | 10   | —                    | 11   | —                    | 15   | —                                                  | 20   | ns   |
| tDH                 | Data Hold from Write Time          | 0                       | —    | 0                    | —    | 0                    | —    | 0                                                  | —    | ns   |
| tOW <sup>(2)</sup>  | Output Active from End-of-Write    | 5                       | —    | 5                    | —    | 5                    | —    | 5                                                  | —    | ns   |

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## NOTES:

- 0° to +70°C temperature range only.
- This parameter is guaranteed by device characterization, but is not production tested.
- 55°C to +125°C temperature range only.

# AC Electrical Characteristics (V<sub>CC</sub> = 5.0V ± 10%, Military Temperature Ranges)

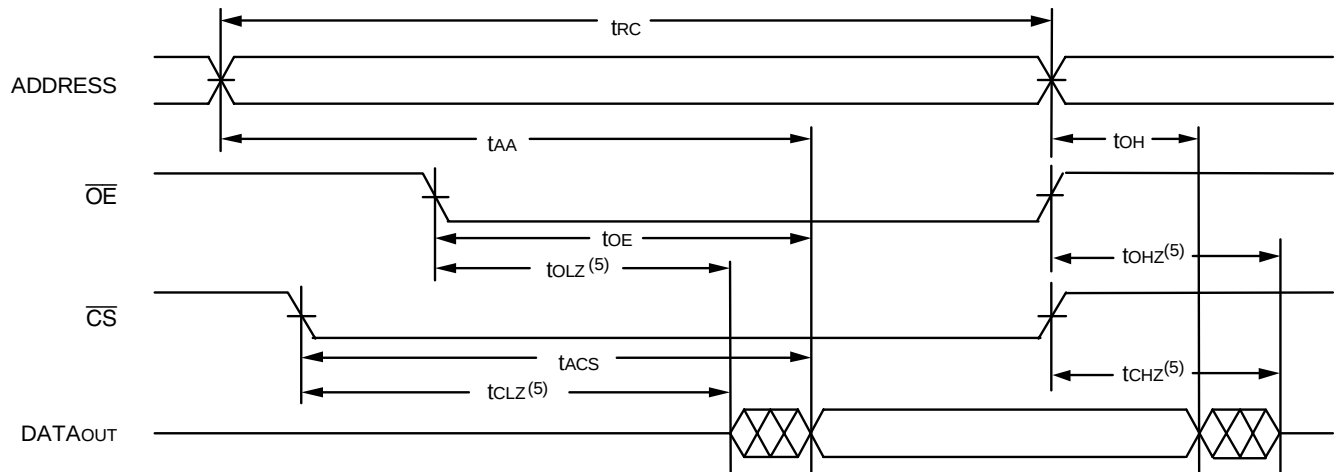
| Symbol              | Parameter                                     | 71256S55 <sup>(1)</sup><br>71256L55 <sup>(1)</sup> |      | 71256S70 <sup>(1)</sup><br>71256L70 <sup>(1)</sup> |      | 71256S85 <sup>(1)</sup><br>71256L85 <sup>(1)</sup> |      | 71256S100 <sup>(1)</sup><br>71256L100 <sup>(1)</sup> |      | Unit |
|---------------------|-----------------------------------------------|----------------------------------------------------|------|----------------------------------------------------|------|----------------------------------------------------|------|------------------------------------------------------|------|------|
|                     |                                               | Min.                                               | Max. | Min.                                               | Max. | Min.                                               | Max. | Min.                                                 | Max. |      |
| Read Cycle          |                                               |                                                    |      |                                                    |      |                                                    |      |                                                      |      |      |
| tRC                 | Read Cycle Time                               | 55                                                 | —    | 70                                                 | —    | 85                                                 | —    | 100                                                  | —    | ns   |
| tAA                 | Address Access Time                           | —                                                  | 55   | —                                                  | 70   | —                                                  | 85   | —                                                    | 100  | ns   |
| tACS                | Chip Select Access Time                       | —                                                  | 55   | —                                                  | 70   | —                                                  | 85   | —                                                    | 100  | ns   |
| tOLZ <sup>(2)</sup> | Chip Select to Output in Low-Z                | 5                                                  | —    | 5                                                  | —    | 5                                                  | —    | 5                                                    | —    | ns   |
| tCHZ <sup>(2)</sup> | Chip Deselect to Output in High-Z             | —                                                  | 25   | —                                                  | 30   | —                                                  | 35   | —                                                    | 40   | ns   |
| tOE                 | Output Enable to Output Valid                 | —                                                  | 25   | —                                                  | 30   | —                                                  | 35   | —                                                    | 40   | ns   |
| tOLZ <sup>(2)</sup> | Output Enable to Output in Low-Z              | 0                                                  | —    | 0                                                  | —    | 0                                                  | —    | 0                                                    | —    | ns   |
| tOHZ <sup>(2)</sup> | Output Disable to Output in High-Z            | 0                                                  | 25   | 0                                                  | 30   | —                                                  | 35   | —                                                    | 40   | ns   |
| tOH                 | Output Hold from Address Change               | 5                                                  | —    | 5                                                  | —    | 5                                                  | —    | 5                                                    | —    | ns   |
| Write Cycle         |                                               |                                                    |      |                                                    |      |                                                    |      |                                                      |      |      |
| tWC                 | Write Cycle Time                              | 55                                                 | —    | 70                                                 | —    | 85                                                 | —    | 100                                                  | —    | ns   |
| tCW                 | Chip Select to End-of-Write                   | 50                                                 | —    | 60                                                 | —    | 70                                                 | —    | 80                                                   | —    | ns   |
| tAW                 | Address Valid to End-of-Write                 | 50                                                 | —    | 60                                                 | —    | 70                                                 | —    | 80                                                   | —    | ns   |
| tAS                 | Address Set-up Time                           | 0                                                  | —    | 0                                                  | —    | 0                                                  | —    | 0                                                    | —    | ns   |
| tWP                 | Write Pulse Width                             | 40                                                 | —    | 45                                                 | —    | 50                                                 | —    | 55                                                   | —    | ns   |
| tWR                 | Write Recovery Time                           | 0                                                  | —    | 0                                                  | —    | 0                                                  | —    | 0                                                    | —    | ns   |
| tDW                 | Data to Write Time Overlap                    | 25                                                 | —    | 30                                                 | —    | 35                                                 | —    | 40                                                   | —    | ns   |
| tWHZ <sup>(2)</sup> | Write Enable to Output in High-Z              | —                                                  | 25   | —                                                  | 30   | —                                                  | 35   | —                                                    | 40   | ns   |
| tDH                 | Data Hold from Write Time ( $\overline{WE}$ ) | 0                                                  | —    | 0                                                  | —    | 0                                                  | —    | 0                                                    | —    | ns   |
| tOW <sup>(2)</sup>  | Output Active from End-of-Write               | 5                                                  | —    | 5                                                  | —    | 5                                                  | —    | 5                                                    | —    | ns   |

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## NOTES:

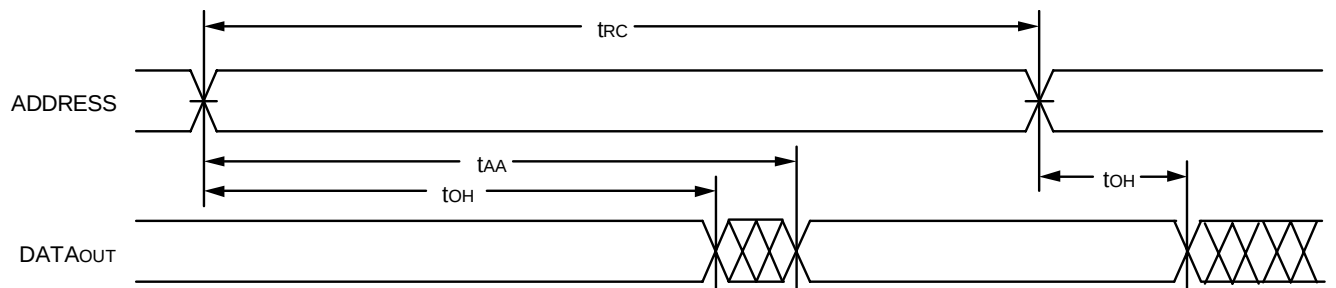
- 55° to +125°C temperature range only.
- This parameter is guaranteed by device characterization, but is not production tested.

## Timing Waveform of Read Cycle No. 1<sup>(1)</sup>



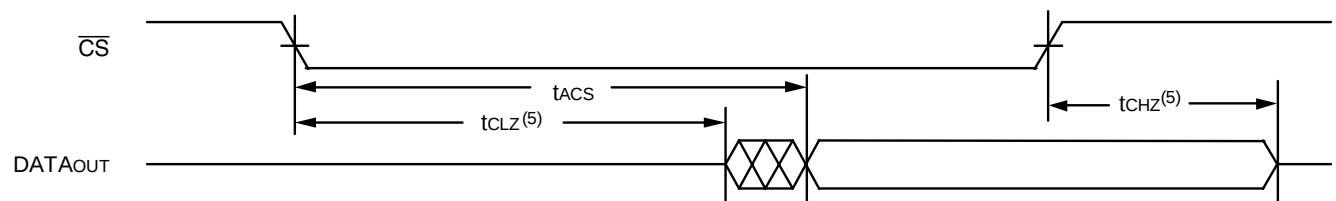
2946 drw 07

## Timing Waveform of Read Cycle No. 2<sup>(1,2,4)</sup>



2946 drw 08

## Timing Waveform of Read Cycle No. 2<sup>(1,3,4)</sup>

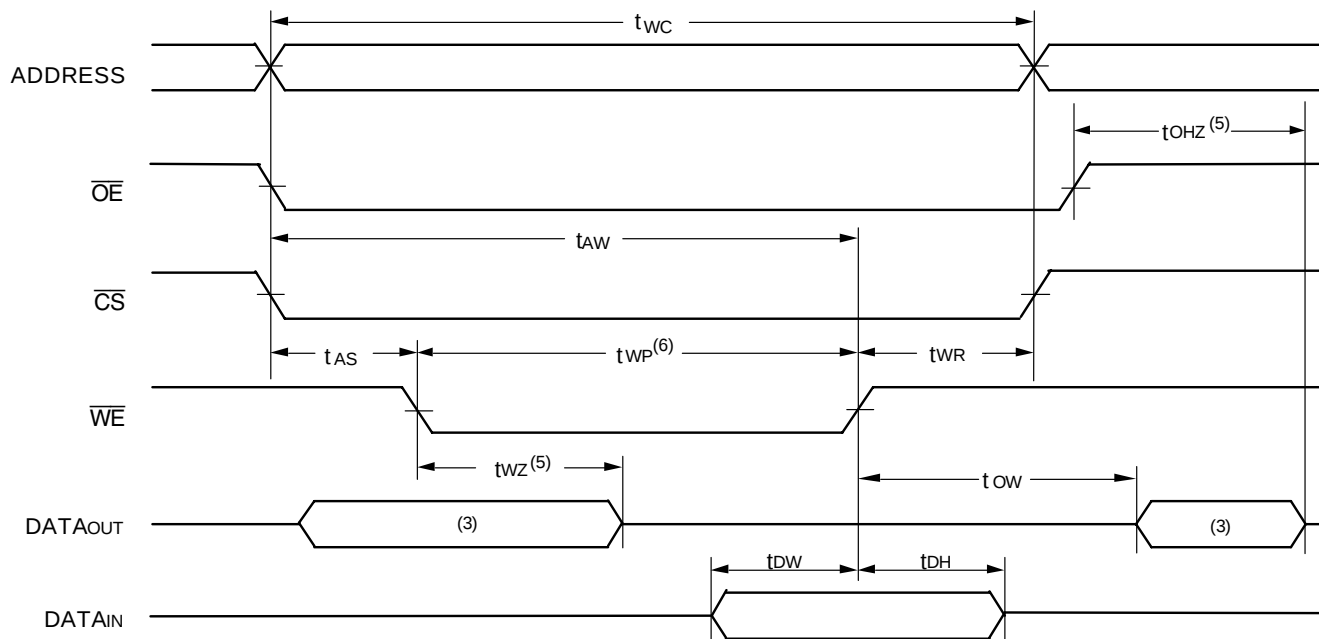


2946 drw 09

### NOTES:

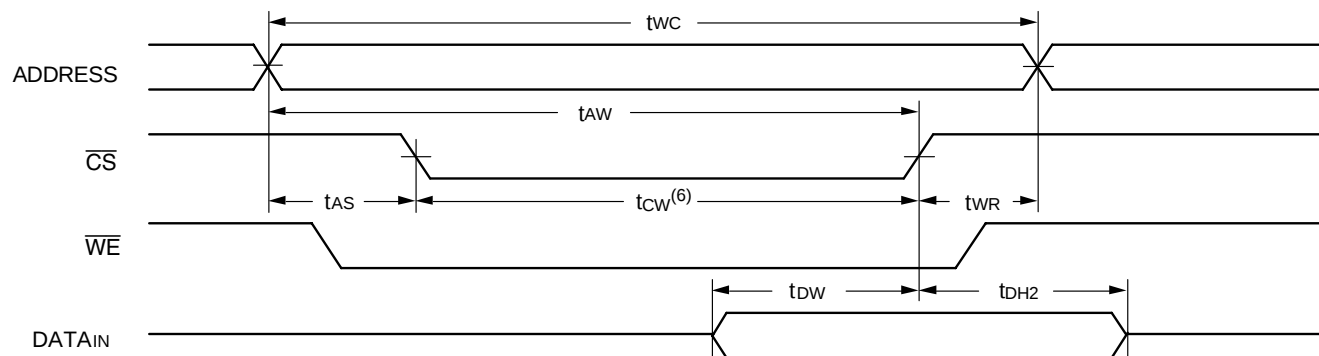
1.  $\overline{WE}$  is HIGH for Read Cycle.
2. Device is continuously selected,  $\overline{CS}$  is LOW.
3. Address valid prior to or coincident with  $\overline{CS}$  transition LOW.
4.  $\overline{OE}$  is LOW.
5. Transition is measured  $\pm 200\text{mV}$  from steady state.

## Timing Waveform of Write Cycle No. 1 ( $\overline{WE}$ Controlled Timing)<sup>(1,2,4,6)</sup>



2946 drw 10

## Timing Waveform of Write Cycle No. 2 ( $\overline{CS}$ Controlled Timing)<sup>(1,2,4)</sup>

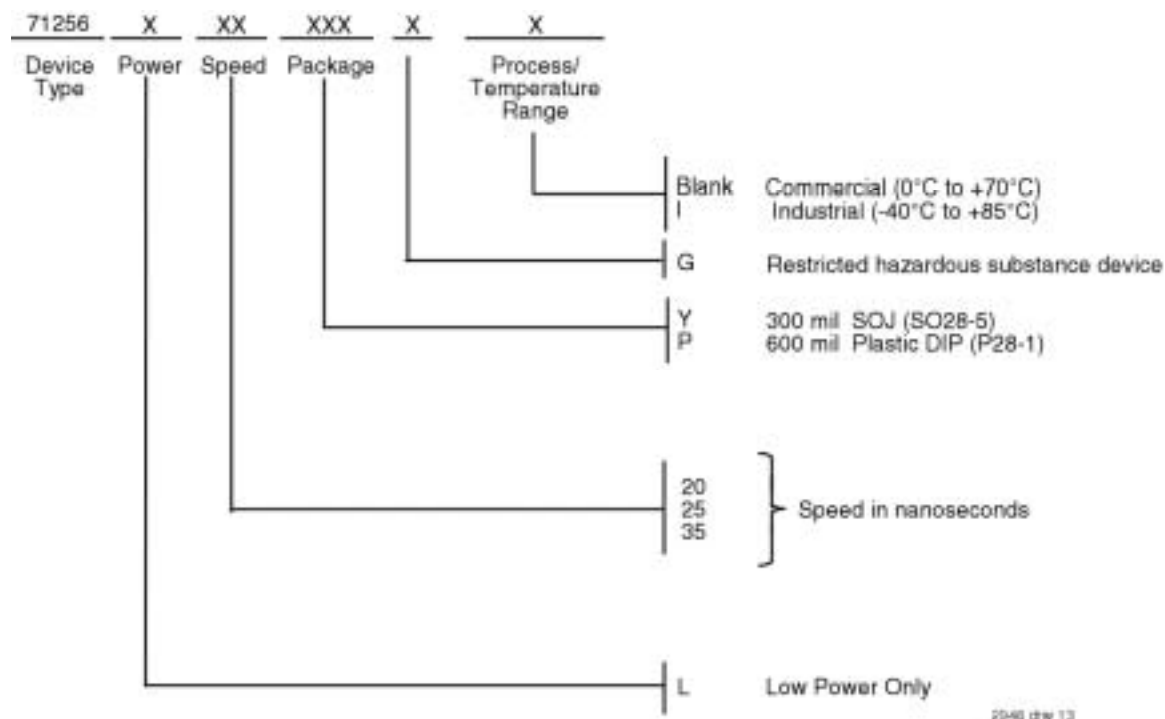


2946 drw 11

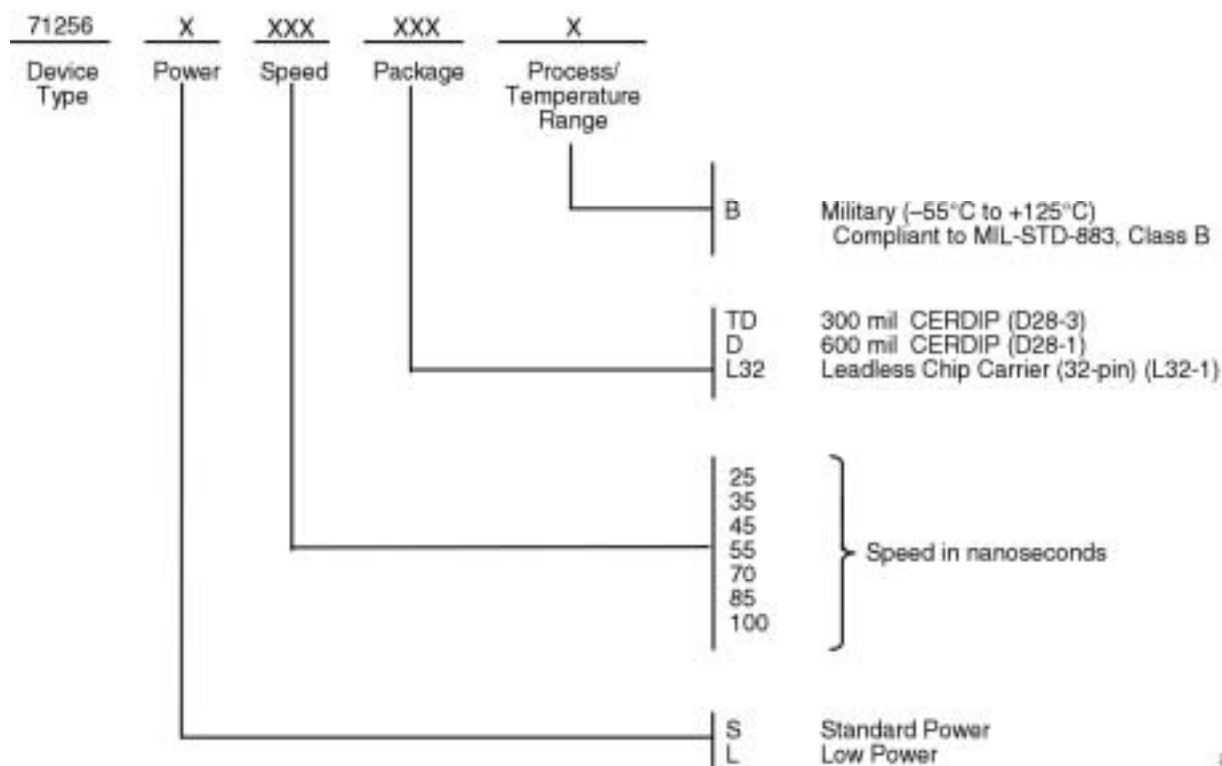
### NOTES:

1. A write occurs during the overlap of a LOW  $\overline{CS}$  and a LOW  $\overline{WE}$ .
2.  $t_{WR}$  is measured from the earlier of  $\overline{CS}$  or  $\overline{WE}$  going HIGH to the end of the write cycle.
3. During this period, I/O pins are in the output state so that the input signals must not be applied.
4. If the  $\overline{CS}$  LOW transition occurs simultaneously with or after the  $\overline{WE}$  LOW transition, the outputs remain in a high-impedance state.
5. Transition is measured  $\pm 200\text{mV}$  from steady state.
6. If  $\overline{OE}$  is LOW during a  $\overline{WE}$  controlled write cycle, the write pulse width must be the larger of  $t_{WP}$  or  $(t_{WHZ} + t_{DW})$  to allow the I/O drivers to turn off and data to be placed on the bus for the required  $t_{DW}$ . If  $\overline{OE}$  is HIGH during a  $\overline{WE}$  controlled write cycle, this requirement does not apply and the minimum write pulse width can be as short as the specified  $t_{WP}$ . For a  $\overline{CS}$  controlled write cycle,  $\overline{OE}$  may be LOW with no degradation to  $t_{CW}$ .

## Ordering Information — Commercial & Industrial



## Ordering Information — Military



## Datasheet Document History

|          |            |                                                                                                                                                   |
|----------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| 11/4/99  |            | Updated to new format                                                                                                                             |
|          | Pp. 1–5, 9 | Added Industrial Temperature Range offerings                                                                                                      |
|          | Pg. 1      | Removed 30, 120, and 150ns military and 45ns commercial speed grade offerings.                                                                    |
|          | Pg. 2      | Removed P28-2 package from DIP/SOJ Top View                                                                                                       |
|          | Pg. 3      | Removed 30ns and 45ns (Commercial only) speed grade offerings from DC Electrical table                                                            |
|          |            | Revised notes and footnotes                                                                                                                       |
|          | Pg. 5      | Removed 30ns speed grade offering from AC Electrical table                                                                                        |
|          |            | Revised notes and footnotes                                                                                                                       |
|          | Pg. 6      | Expressed Military Temperature range on AC Electrical table                                                                                       |
|          |            | Revised notes and footnotes                                                                                                                       |
|          | Pg. 8      | Removed Note 1 and renumbered notes and footnotes                                                                                                 |
|          | Pg. 9      | Revised Ordering Information and presented by temperature range offering                                                                          |
|          | Pg. 10     | Added Datasheet Document History                                                                                                                  |
| 08/09/00 |            | Not recommended for new designs                                                                                                                   |
| 02/01/01 |            | Remove "Not recommended for new designs"                                                                                                          |
| 11/15/06 | Pg.3       | Changed power limits for commercial and industrial. Refer to PCN SR-0602-03. Added Restricted hazardous substance device to ordering information. |
| 11/01/08 | Pg.2,9     | Corrected typo on pin 21 in 32-Pin LCC diagram. Updated the ordering information by removing the "IDT" notation.                                  |



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