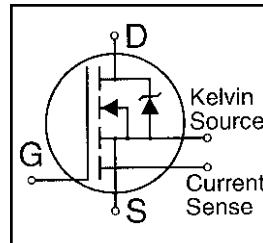


HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Current Sense
- 175°C Operating Temperature
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements

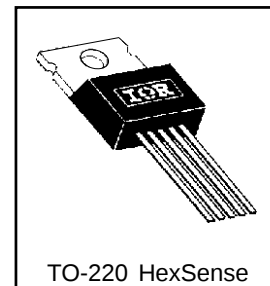


$V_{DS} = 60V$
$R_{DS(on)} = 0.050\Omega$
$I_D = 30A$

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device, low on-resistance and cost-effectiveness.

The HEXSense device provides an accurate fraction of the drain current through the additional two leads to be used for control or protection of the device. These devices exhibit similar electrical and thermal characteristics as their IRF-series equivalent part numbers. The provision of a kelvin source connection effectively eliminates problems of common source inductance when the HEXSense is used as a fast, high-current switch in non current-sensing applications.



Absolute Maximum Ratings

Parameter	Max.	Units
I_D @ $T_C = 25^\circ C$	30	A
I_D @ $T_C = 100^\circ C$	21	
I_{DM}	120	
P_D @ $T_C = 25^\circ C$	88	W
	0.59	W/°C
V_{GS}	±20	V
E_{AS}	15	mJ
dv/dt	4.5	A
T_J	-55 to + 175	°C
T_{STG}		
	300 (1.6mm from case)	
	10 lbf•in (1.1 N•m)	

Thermal Resistance

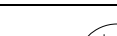
Parameter	Min.	Max.	Units
$R_{\theta JC}$	—	—	1.7
$R_{\theta CS}$	—	0.50	—
$R_{\theta JA}$	—	—	62

** When mounted on FR-4 board using minimum recommended footprint. For recommended footprint and soldering techniques refer to application note #AN-994.

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	60	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	—	0.065	—	V/°C	Reference to 25°C , $I_D = 1mA$
$R_{DS(ON)}$	—	—	0.050	Ω	$V_{GS} = 10V, I_D = 18A$ ④
$V_{GS(th)}$	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	9.4	—	—	S	$V_{DS} = 25V, I_D = 18A$
I_{DSS}	—	—	25	—	$V_{DS} = 60V, V_{GS} = 0V$
			250		$V_{DS} = 48V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	—	—	100	—	$V_{GS} = 20V$
			-100		$V_{GS} = -20V$
Q_g	—	—	46	nC	$I_D = 30A$
Q_{gs}	—	—	11		$V_{DS} = 48V$
Q_{gd}	—	—	22		$V_{GS} = 10V$, See Fig. 6 and 13 ④
$t_{d(on)}$	—	13	—	—	$V_{DD} = 30V$
t_r	—	100	—		$I_D = 30A$
$t_{d(off)}$	—	29	—		$R_G = 12\Omega$
t_f	—	52	—		$R_D = 1.0\Omega$, See Fig. 10 ④
L_D	—	4.5	—	nH	Between lead, 6 mm (0.25 in.) from package and center of die contact
L_C	—	7.5	—		
C_{iss}	—	1300	—	pF	$V_{GS} = 0V$
C_{oss}	—	640	—		$V_{DS} = 25V$
C_{rss}	—	96	—		$f = 1.0MHz$, See Fig. 5
r	1340	—	1480	—	$I_D = 30A, V_{GS} = 10V$
C_{oss}	—	9.0	—	pF	$V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz$

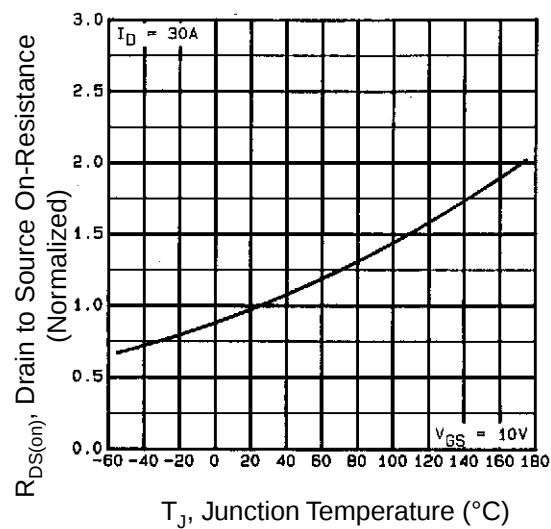
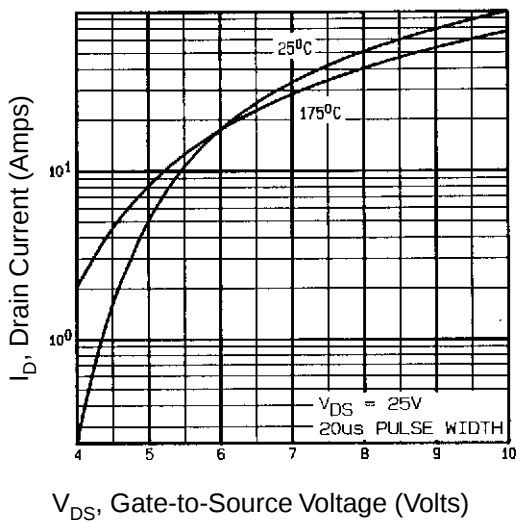
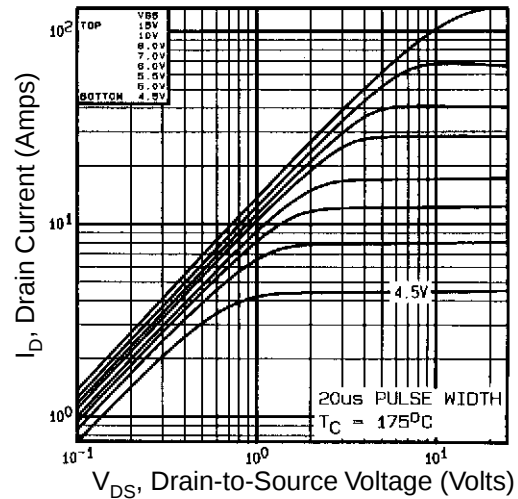
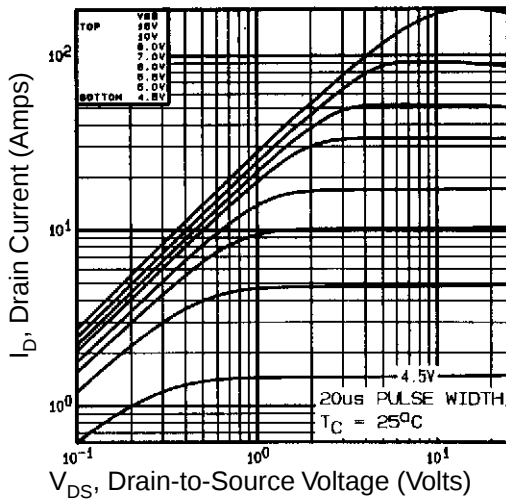
Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	30	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	120		
V _{SD}	Diode Forward Voltage	—	—	1.6	V	T _J = 25°C, I _S = 30A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	120	230	ns	T _J = 25°C, I _F = 30A
Q _{rr}	Reverse Recovery Charge	—	0.70	1.4	nC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

③ $I_{SD} \leq 30A, di/dt \leq 200A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 175^\circ\text{C}$ ② $V_{DD} = 25V$, starting $T_J = 25^\circ\text{C}$, $L = 0.019mH$
 $R_G = 25\Omega, I_{AS} = 30A$. (See Figure 12)④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.



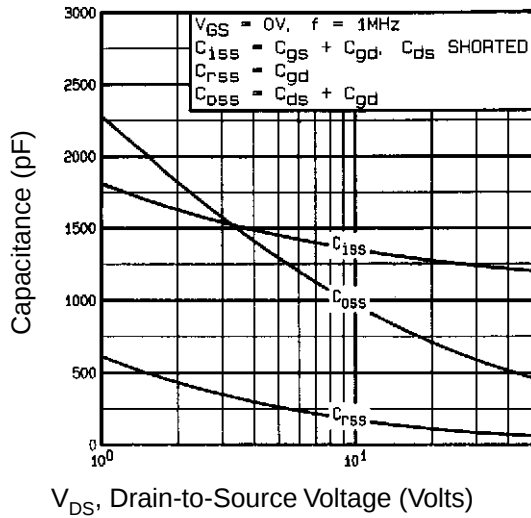


Fig. 5 Typical Capacitance vs. Drain-to-Source Voltage

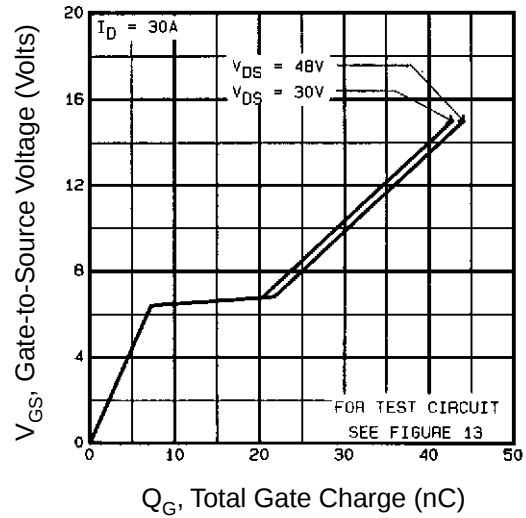


Fig. 6 Typical Gate Charge vs. Gate-to-Source Voltage

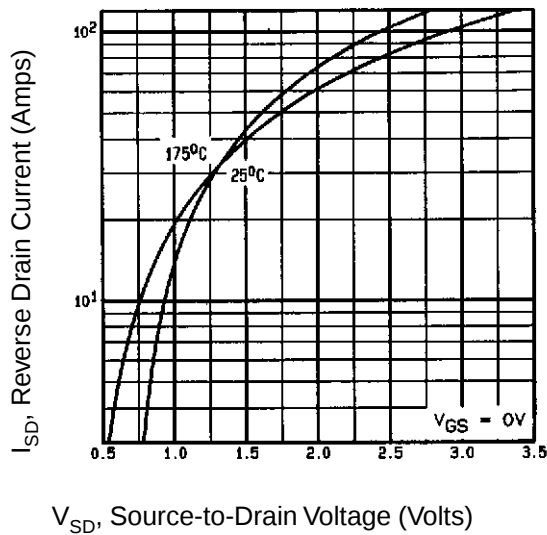


Fig. 7 Typical Source-Drain Diode Forward Voltage

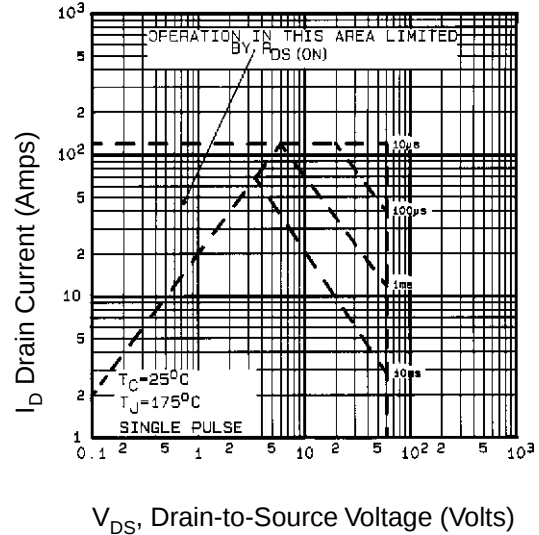


Fig. 8 Maximum Safe Operating Area

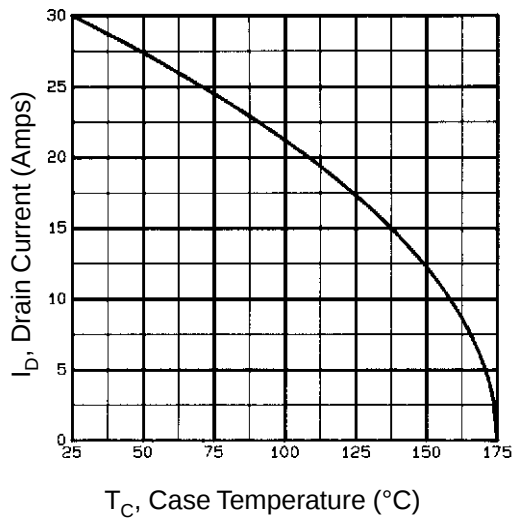


Fig. 9 Maximum Drain Current vs. Case Temperature

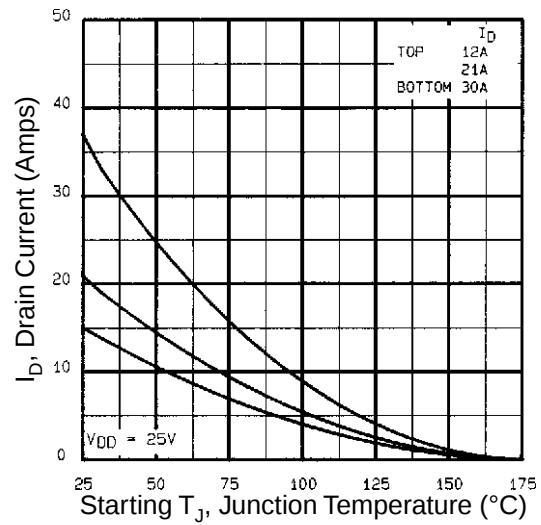


Fig. 12c Maximum Avalanche Energy vs. Drain Current

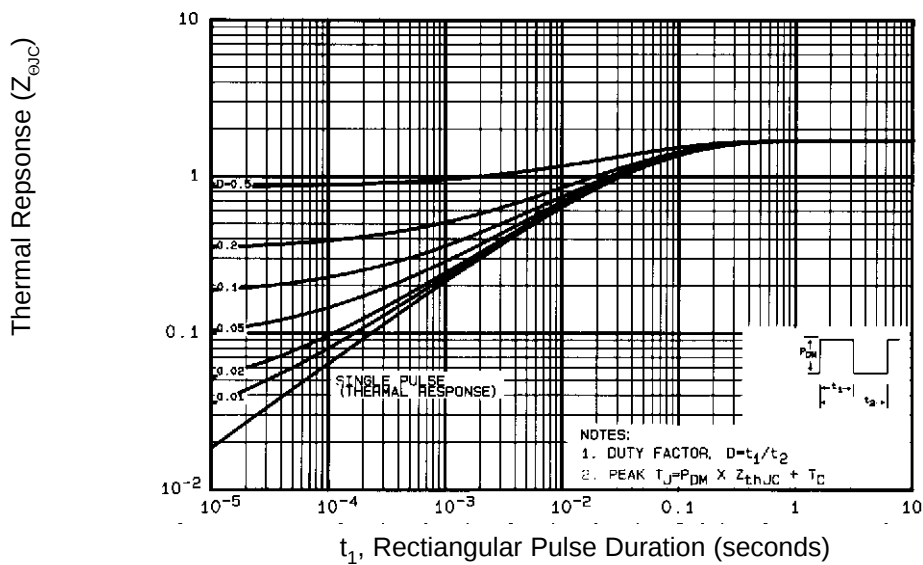


Fig. 11 Maximum Effective Transient Thermal Impedance, Junction-to-Case

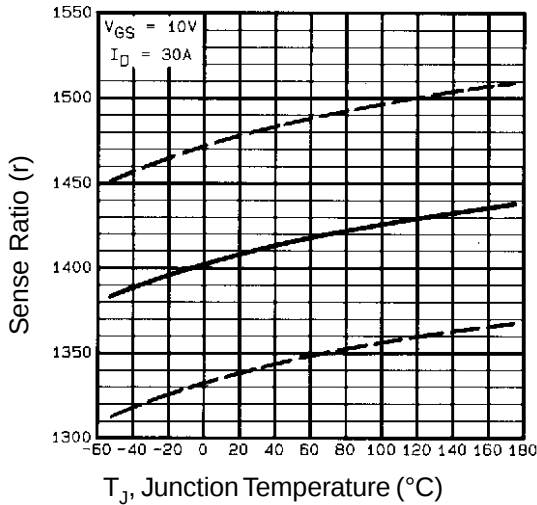


Fig. 15 Typical HEXSense Ratio vs. Junction Temperature

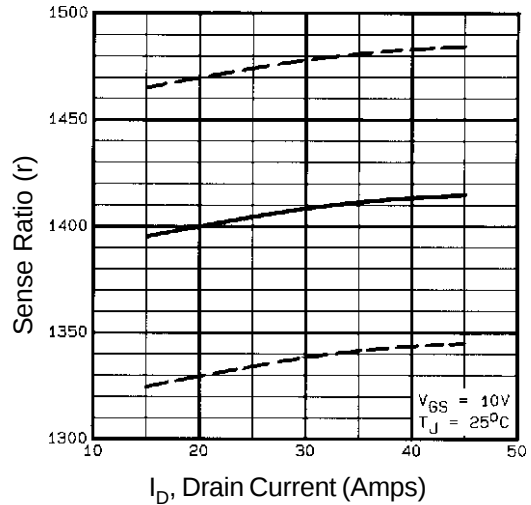


Fig. 16 Typical HEXSense Ratio vs. Drain Current

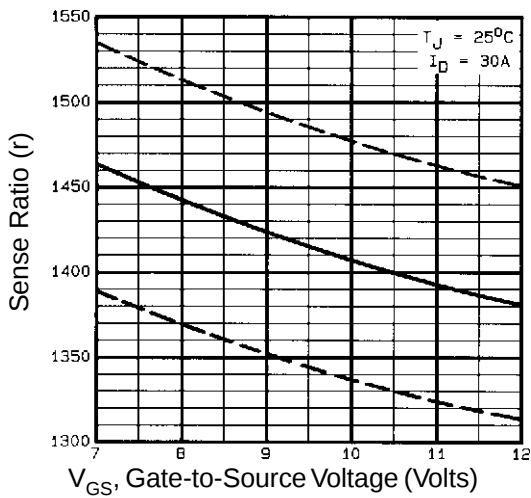


Fig. 17 Typical HEXSense Ratio vs. Gate Voltage

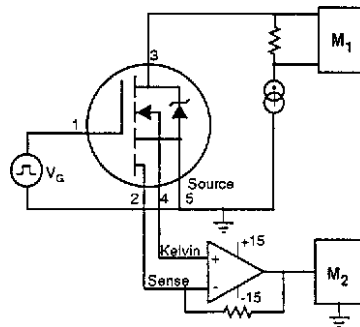


Fig. 18 HEXSense Ratio Test Circuit

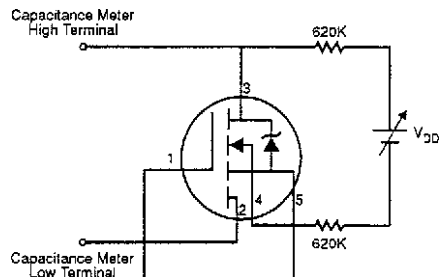


Fig. 19 HEXSense Sensing Cell Output Capacitance Test Circuit

Mechanical drawings, Appendix A
Part marking information, Appendix B
Test Circuit diagrams, Appendix C



Notice

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