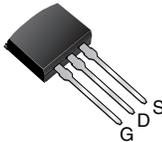
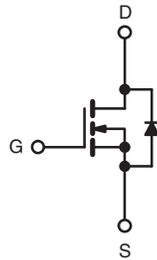
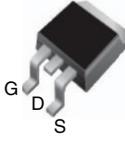


## Power MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V)	200
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$ 1.5
$Q_g$ (Max.) (nC)	8.2
$Q_{gs}$ (nC)	1.8
$Q_{gd}$ (nC)	4.5
Configuration	Single

**I<sup>2</sup>PAK (TO-262)**

**D<sup>2</sup>PAK (TO-263)**


N-Channel MOSFET

### FEATURES

- Surface mount
- Available in tape and reel
- Dynamic dV/dt rating
- Repetitive avalanche rated
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS\***  
Available  
**HALOGEN**  
**FREE**  
Available

### Note

\* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

### DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D<sup>2</sup>PAK (TO-263) is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D<sup>2</sup>PAK (TO-263) is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

ORDERING INFORMATION				
Package	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)	I <sup>2</sup> PAK (TO-262)
Lead (Pb)-free and halogen-free	SiHF610S-GE3	SiHF610STRL-GE3 <sup>a</sup>	SiHF610STRR-GE3 <sup>a</sup>	SiHF610L-GE3 <sup>a</sup>
Lead (Pb)-free	IRF610SPbF	IRF610STRLPbF <sup>a</sup>	IRF610STRRPbF <sup>a</sup>	IRF610LPbF <sup>a</sup>

### Note

a. See device orientation.

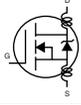
ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			$V_{DS}$	200	V
Gate-Source Voltage			$V_{GS}$	$\pm 20$	
Continuous Drain Current	$V_{GS}$ at 10 V	$T_C = 25\text{ }^\circ\text{C}$	$I_D$	3.3	A
		$T_C = 100\text{ }^\circ\text{C}$		2.1	
Pulsed Drain Current <sup>a</sup>			$I_{DM}$	10	W/ $^\circ\text{C}$
Linear Derating Factor				0.29	
Linear Derating Factor (PCB mount) <sup>e</sup>				0.025	
Single Pulse Avalanche Energy <sup>b</sup>			$E_{AS}$	64	mJ
Repetitive Avalanche Current <sup>a</sup>			$I_{AR}$	3.3	A
Repetitive Avalanche Energy <sup>a</sup>			$E_{AR}$	3.6	mJ
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$		$P_D$	36	W
Maximum Power Dissipation (PCB mount) <sup>e</sup>	$T_A = 25\text{ }^\circ\text{C}$			3.0	
Peak Diode Recovery dV/dt <sup>c</sup>			dV/dt	5.0	V/ns
Operating Junction and Storage Temperature Range			$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
Soldering Recommendations (Peak temperature) <sup>d</sup>	for 10 s			300	

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$ , starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 8.8\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 3.3\text{ A}$  (see fig. 12).
- $I_{SD} \leq 3.3\text{ A}$ ,  $dI/dt \leq 70\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).



THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB mount) <sup>c</sup>	R <sub>thJA</sub>	-	-	40	°C/W
Maximum Junction-to-Ambient	R <sub>thJA</sub>	-	-	62	
Maximum Junction-to-Case (Drain)	R <sub>thJC</sub>	-	-	3.5	

SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0, I <sub>D</sub> = 250 μA		200	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	0.30	-	V/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V		-	-	25	μA
		V <sub>DS</sub> = 160V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	250	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 2.0 A <sup>b</sup>	-	-	1.5	Ω
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 2.0 A <sup>b</sup>		0.80	-	-	S
<b>Dynamic</b>							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1.0 MHz, see fig. 5		-	140	-	pF
Output Capacitance	C <sub>oss</sub>			-	53	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	15	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 3.3 A, V <sub>DS</sub> = 160 V see fig. 6 and 13 <sup>b</sup>	-	-	8.2	nC
Gate-Source Charge	Q <sub>gs</sub>			-	-	1.8	
Gate-Drain Charge	Q <sub>gd</sub>			-	-	4.5	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 100 V, I <sub>D</sub> = 3.3 A, R <sub>g</sub> = 24 Ω, R <sub>D</sub> = 30 Ω, see fig. 10 <sup>b</sup>		-	8.2	-	ns
Rise Time	t <sub>r</sub>			-	17	-	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	14	-	
Fall Time	t <sub>f</sub>			-	8.9	-	
Internal Drain Inductance	L <sub>D</sub>	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal Source Inductance	L <sub>S</sub>			-	7.5	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	3.3	A
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>			-	-	10	
Body Diode Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 3.3 A, V <sub>GS</sub> = 0 V <sup>b</sup>		-	-	2.0	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 3.3 A, di/dt = 100 A/μs <sup>b</sup>		-	150	310	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			-	0.60	1.4	μC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.
- c. When mounted on 1" square PCB (FR-4 or G-10 material).



## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

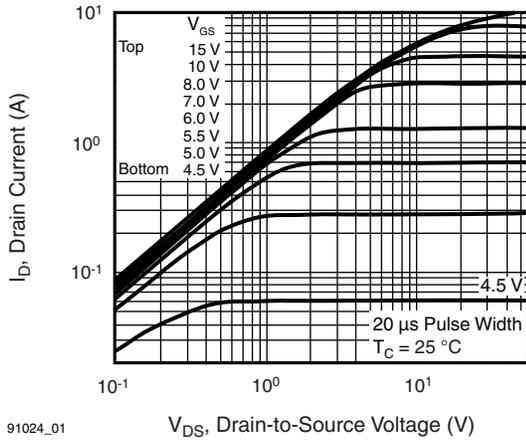


Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^\circ\text{C}$

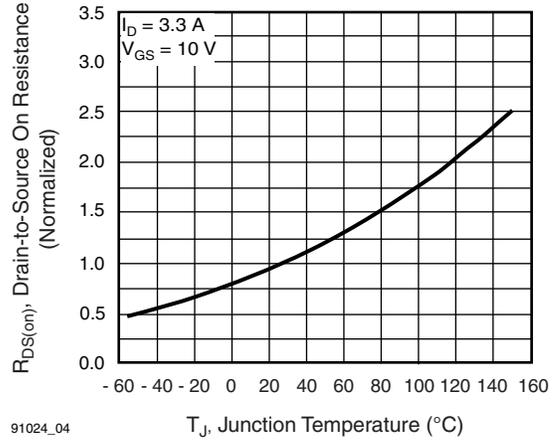


Fig. 4 - Normalized On-Resistance vs. Temperature

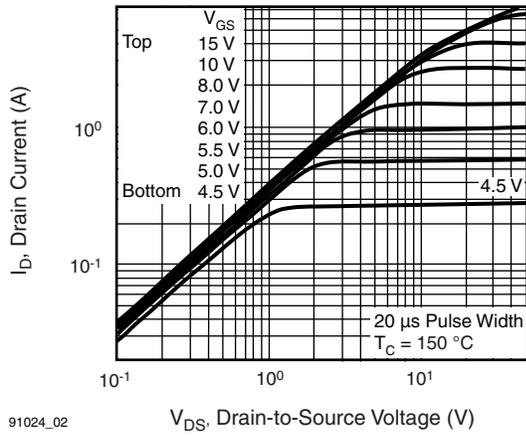


Fig. 2 - Typical Output Characteristics,  $T_C = 150\text{ }^\circ\text{C}$

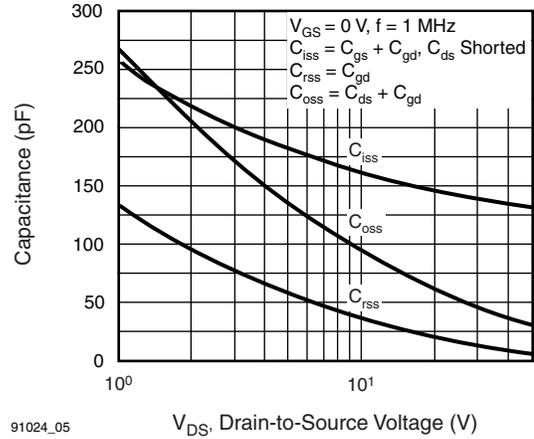


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

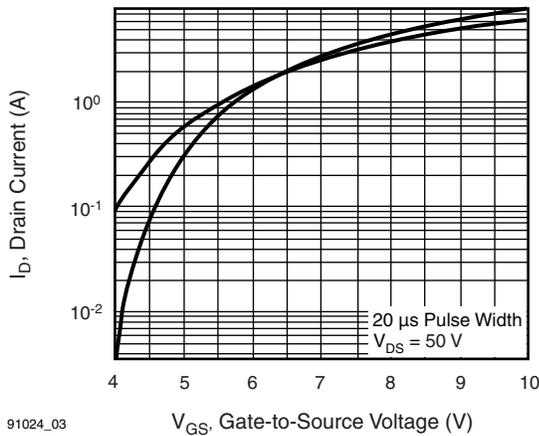


Fig. 3 - Typical Transfer Characteristics

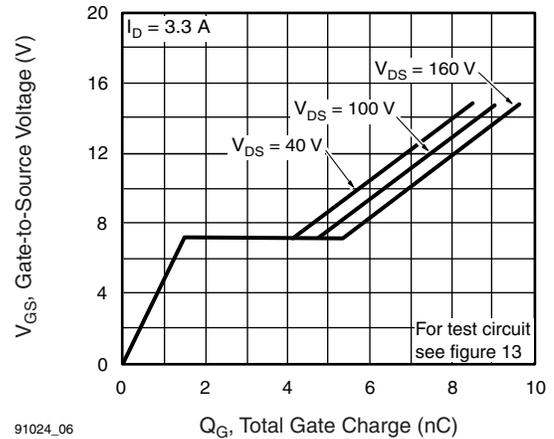
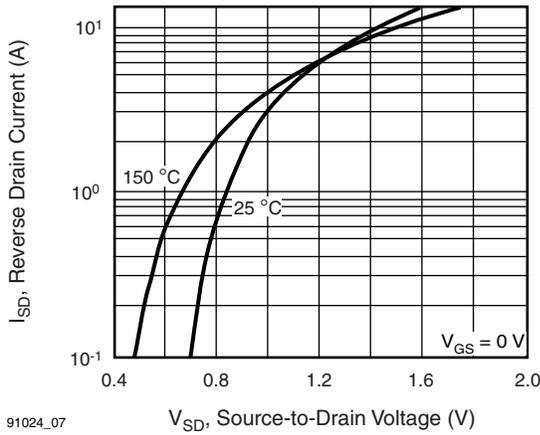
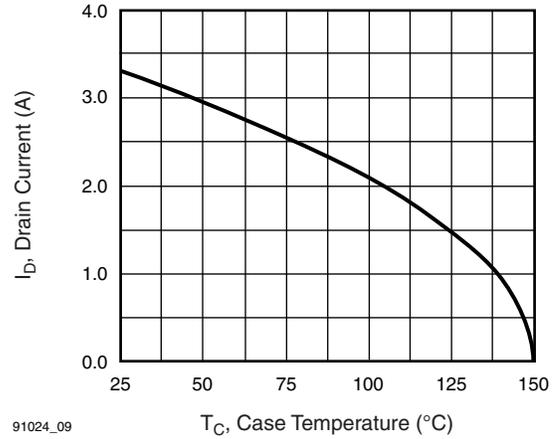


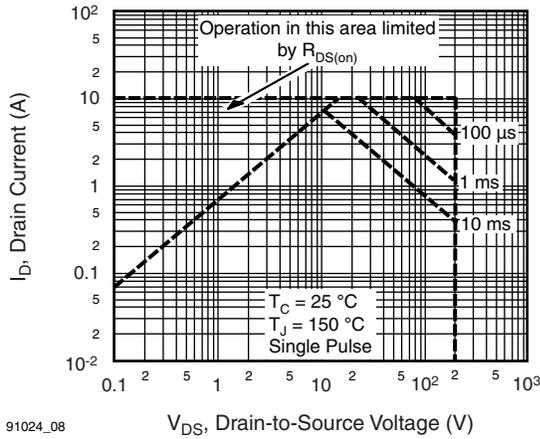
Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



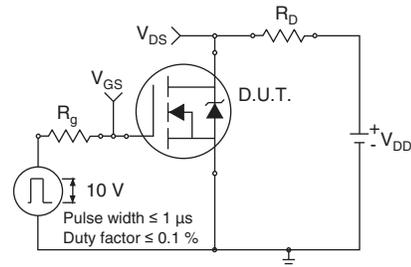
**Fig. 7 - Typical Source-Drain Diode Forward Voltage**



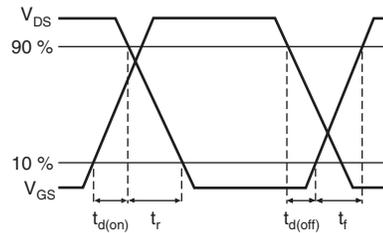
**Fig. 9 - Maximum Drain Current vs. Case Temperature**



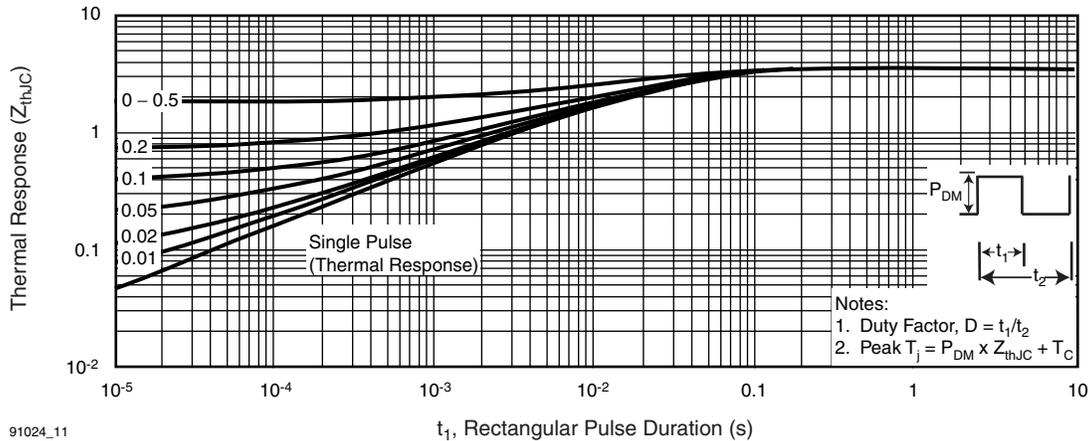
**Fig. 8 - Maximum Safe Operating Area**



**Fig. 10a - Switching Time Test Circuit**



**Fig. 10b - Switching Time Waveforms**



**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**

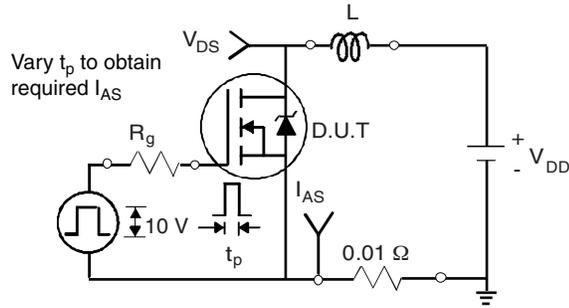


Fig. 12a - Unclamped Inductive Test Circuit

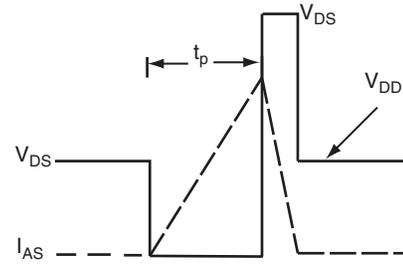
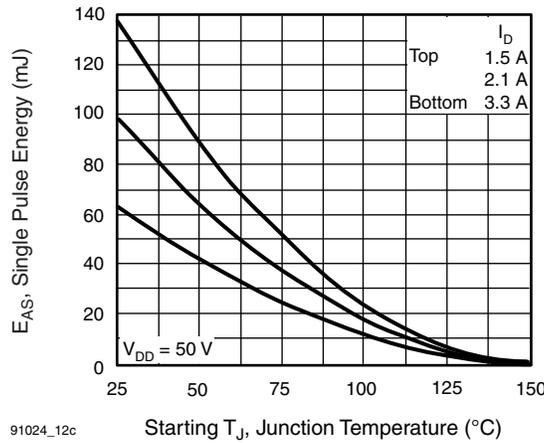


Fig. 12b - Unclamped Inductive Waveforms



91024\_12c

Fig. 12c - Maximum Avalanche Energy vs. Drain Current

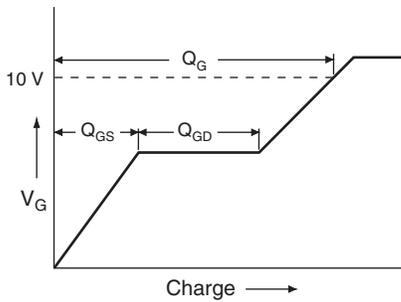


Fig. 13a - Basic Gate Charge Waveform

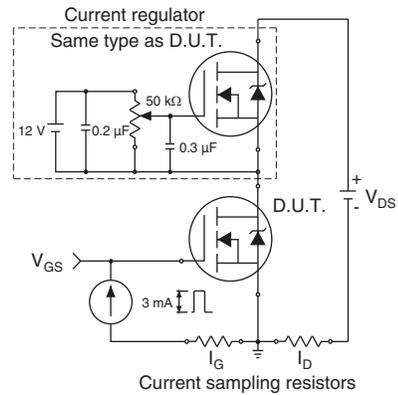
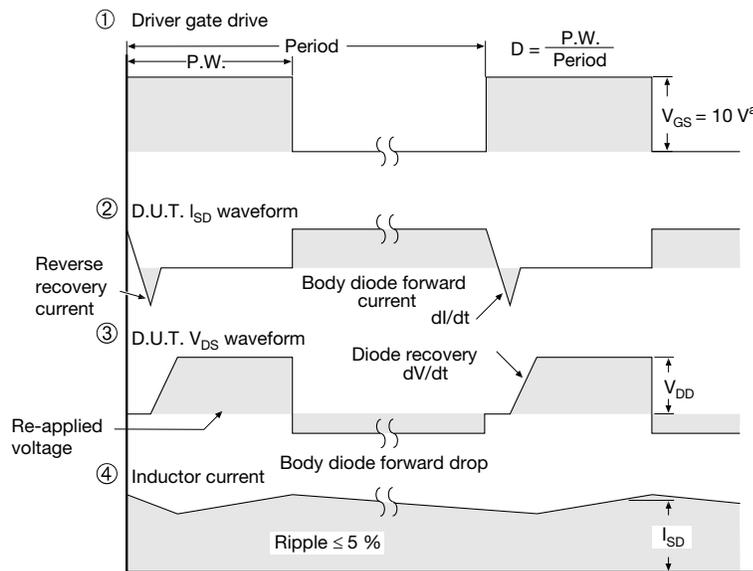
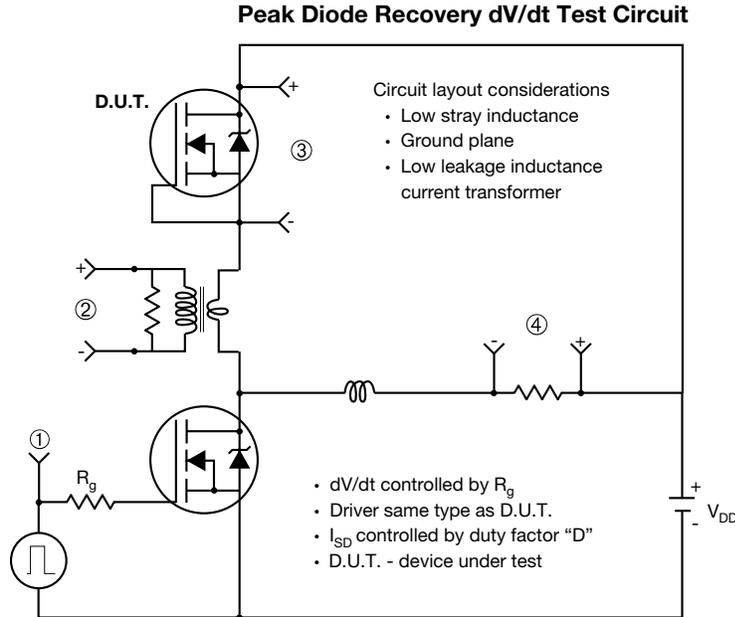


Fig. 13b - Gate Charge Test Circuit



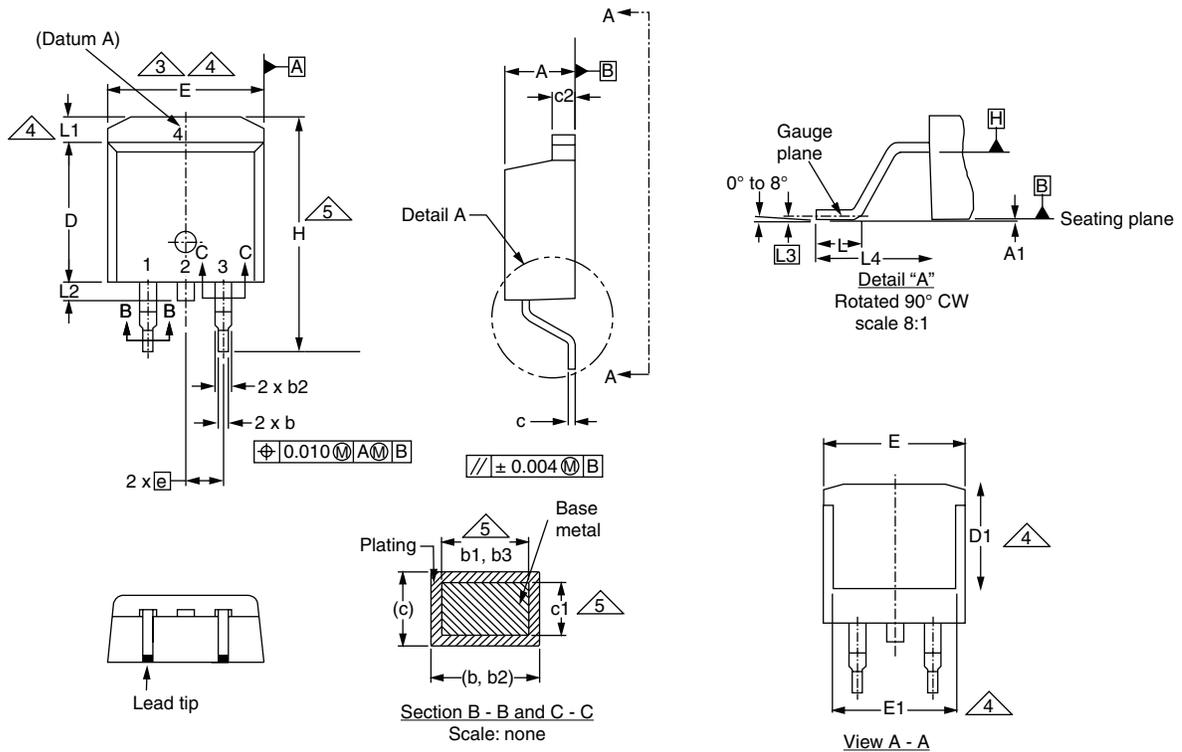
**Note**

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 14 - For N-Channel**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?91024](http://www.vishay.com/ppg?91024).

### TO-263AB (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08  
DWG: 5970

#### Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.



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