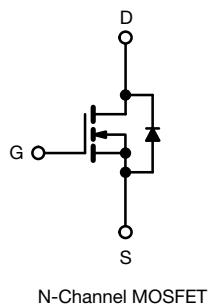
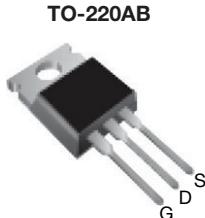


Power MOSFET

PRODUCT SUMMARY	
V _{DS} (V)	200
R _{DS(on)} (Ω)	V _{GS} = 10 V 0.18
Q _g (Max.) (nC)	70
Q _{gs} (nC)	13
Q _{gd} (nC)	39
Configuration	Single



ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free	IRF640PbF SiHF640-E3
SnPb	IRF640 SiHF640

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	200	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current	I _D	18	A
		11	
Pulsed Drain Current ^a	I _{DM}	72	
Linear Derating Factor		1.0	W/°C
Single Pulse Avalanche Energy ^b	E _{AS}	580	mJ
Repetitive Avalanche Current ^a	I _{AR}	18	A
Repetitive Avalanche Energy ^a	E _{AR}	13	mJ
Maximum Power Dissipation	P _D	125	W
Peak Diode Recovery dV/dt ^c	dV/dt	5.0	V/ns
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +150	°C
Soldering Recommendations (Peak temperature) ^d	for 10 s	300	
Mounting Torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- V_{DD} = 50 V, starting T_J = 25 °C, L = 2.7 mH, R_g = 25 Ω, I_{AS} = 18 A (see fig. 12).
- I_{SD} ≤ 18 A, dI/dt ≤ 150 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C.
- 1.6 mm from case.



FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

DESCRIPTION

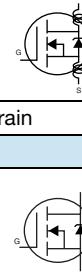
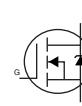
Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

THERMAL RESISTANCE RATINGS

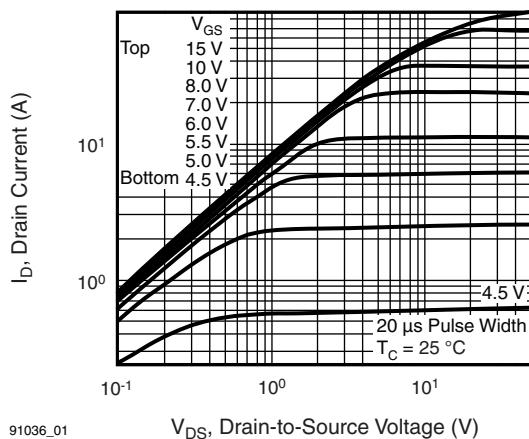
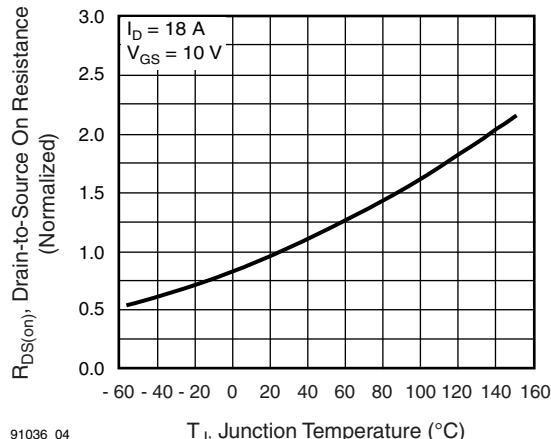
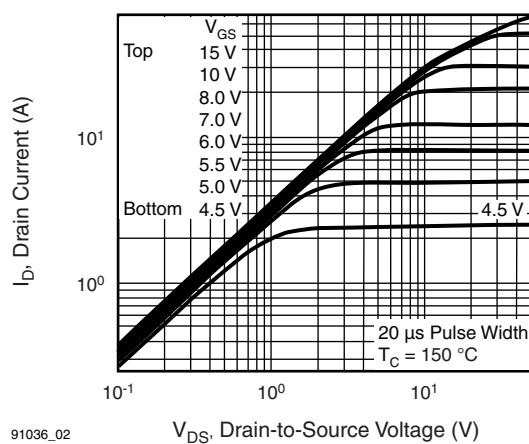
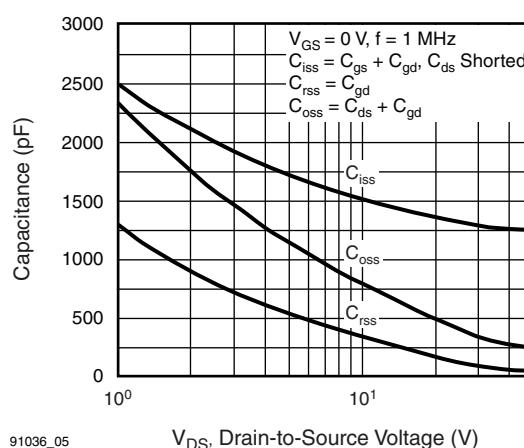
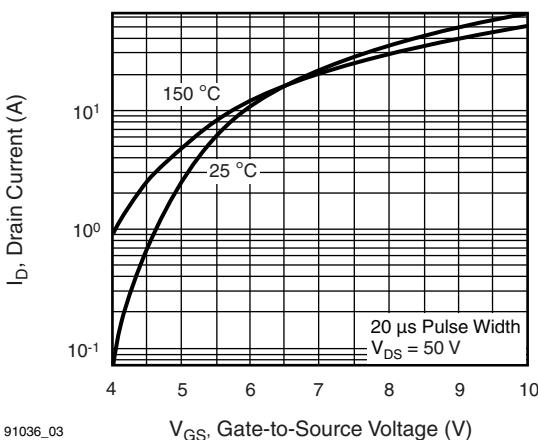
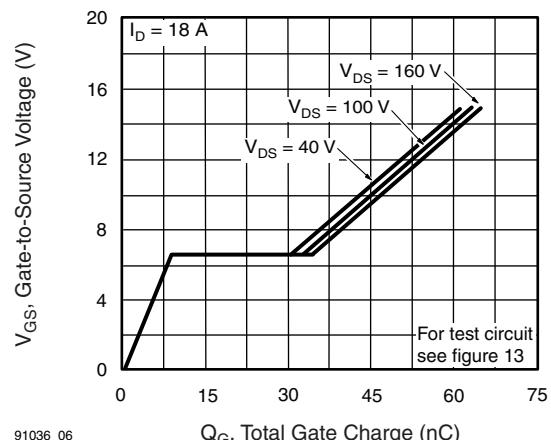
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.0	

SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$		200	-	-	V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25°C , $I_D = 1 \text{ mA}$		-	0.29	-	$\text{V}/^\circ\text{C}$	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$		2.0	-	4.0	V	
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 200 \text{ V}$, $V_{GS} = 0 \text{ V}$		-	-	25	μA	
		$V_{DS} = 160 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 125^\circ\text{C}$		-	-	250		
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$	$I_D = 11 \text{ A}^b$	-	-	0.18	Ω	
Forward Transconductance	g_{fs}	$V_{DS} = 50 \text{ V}$, $I_D = 11 \text{ A}^b$		6.7	-	-	S	
Dynamic								
Input Capacitance	C_{iss}	$V_{GS} = 0 \text{ V}$, $V_{DS} = 25 \text{ V}$, $f = 1.0 \text{ MHz}$, see fig. 5		-	1300	-	pF	
Output Capacitance	C_{oss}			-	430	-		
Reverse Transfer Capacitance	C_{rss}			-	130	-		
Total Gate Charge	Q_g	$V_{GS} = 10 \text{ V}$	$I_D = 18 \text{ A}$, $V_{DS} = 160 \text{ V}$, see fig. 6 and 13 ^b	-	-	70	nC	
Gate-Source Charge	Q_{gs}			-	-	13		
Gate-Drain Charge	Q_{gd}			-	-	39		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 100 \text{ V}$, $I_D = 18 \text{ A}$, $R_g = 9.1 \Omega$, $R_D = 5.4 \Omega$, see fig. 10 ^b		-	14	-	ns	
Rise Time	t_r		-	51	-			
Turn-Off Delay Time	$t_{d(off)}$		-	45	-			
Fall Time	t_f		-	36	-			
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH	
Internal Source Inductance	L_S			-	7.5	-		
Gate Input Resistance	R_g	$f = 1 \text{ MHz}$, open drain		0.5	-	3.6	Ω	
Drain-Source Body Diode Characteristics								
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	18	A	
Pulsed Diode Forward Current ^a	I_{SM}			-	-	72		
Body Diode Voltage	V_{SD}	$T_J = 25^\circ\text{C}$, $I_S = 18 \text{ A}$, $V_{GS} = 0 \text{ V}^b$		-	-	2.0	V	
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25^\circ\text{C}$, $I_F = 18 \text{ A}$, $dl/dt = 100 \text{ A}/\mu\text{s}^b$		-	300	610	ns	
Body Diode Reverse Recovery Charge	Q_{rr}			-	3.4	7.1	μC	
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)						

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300 \mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics, $T_C = 25 \text{ }^\circ\text{C}$

Fig. 4 - Normalized On-Resistance vs. Temperature

Fig. 2 - Typical Output Characteristics, $T_C = 150 \text{ }^\circ\text{C}$

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 3 - Typical Transfer Characteristics

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

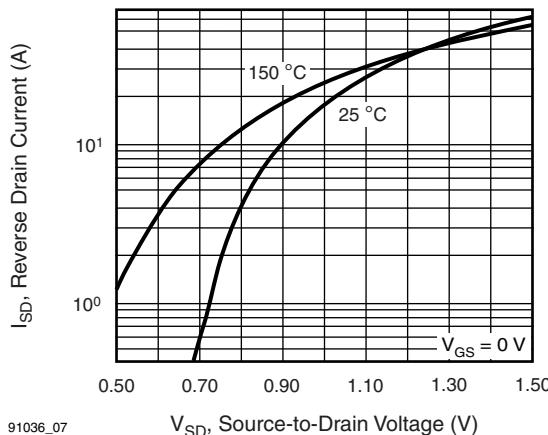


Fig. 7 - Typical Source-Drain Diode Forward Voltage

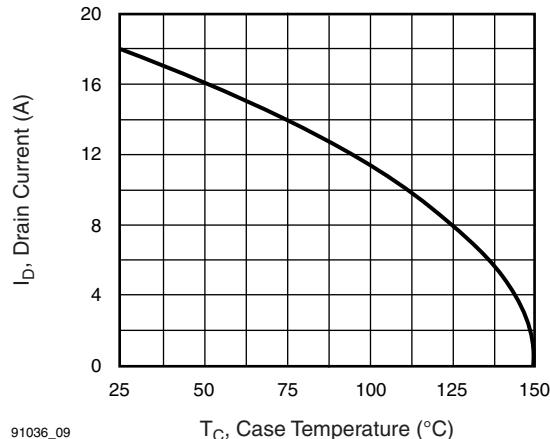


Fig. 9 - Maximum Drain Current vs. Case Temperature

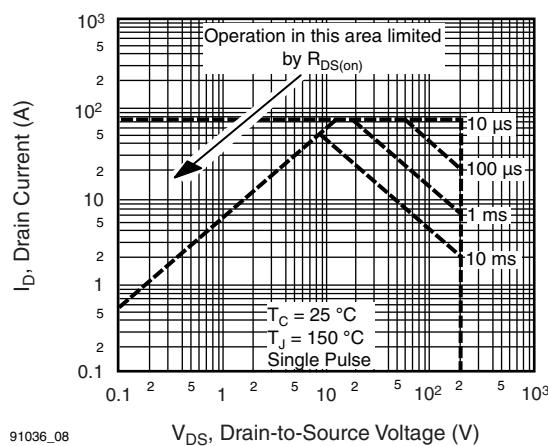


Fig. 8 - Maximum Safe Operating Area

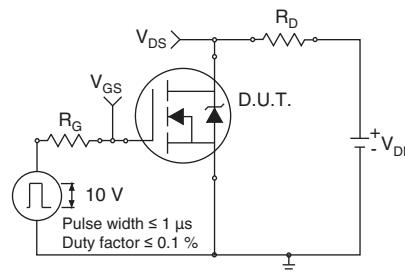


Fig. 10a - Switching Time Test Circuit

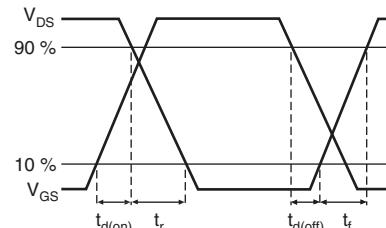


Fig. 10b - Switching Time Waveforms

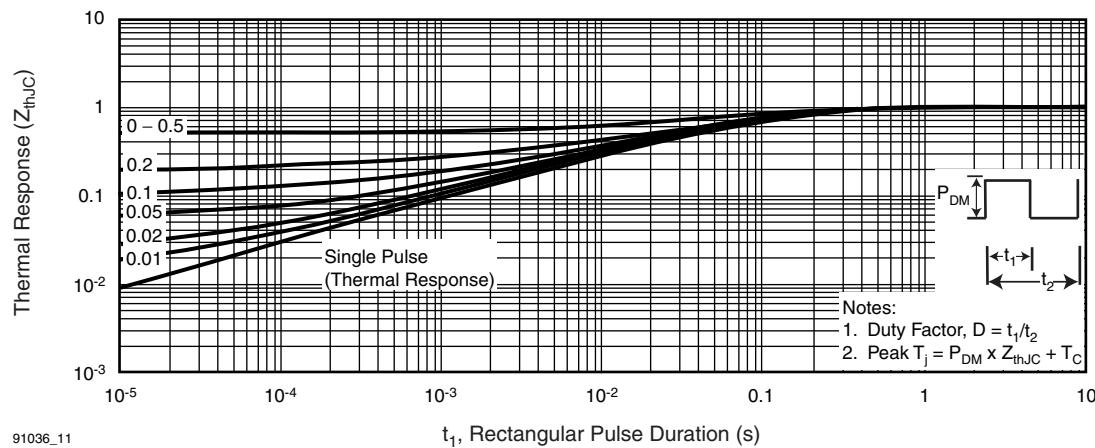
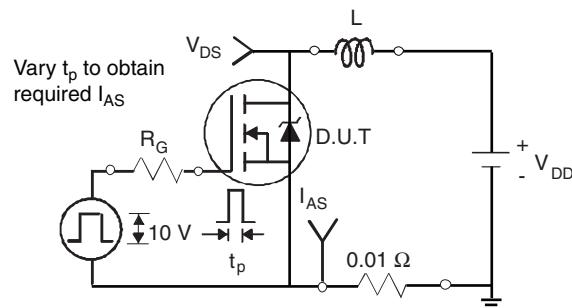
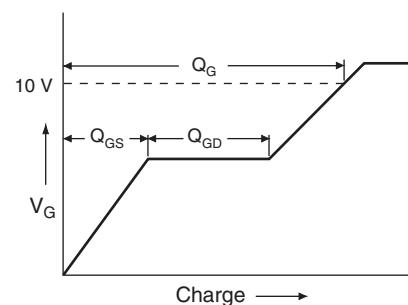
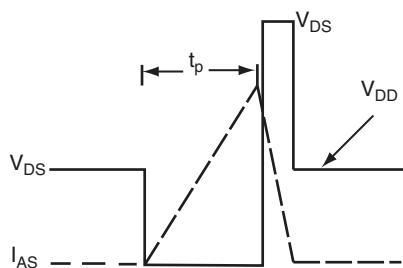
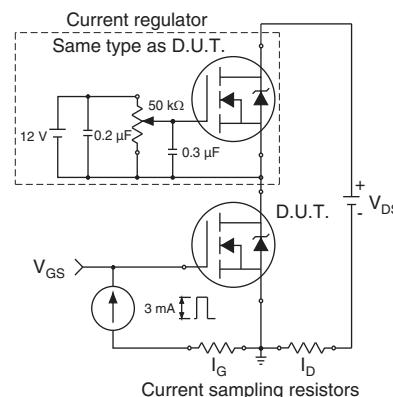
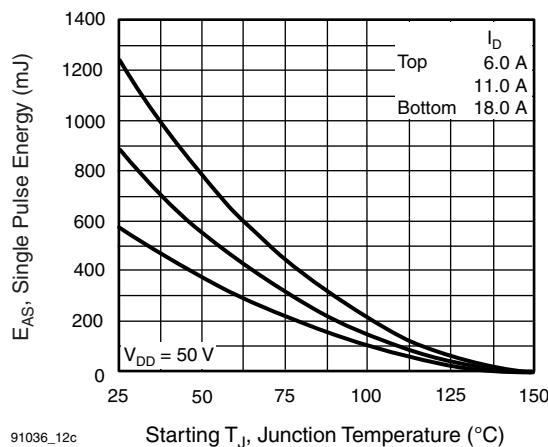
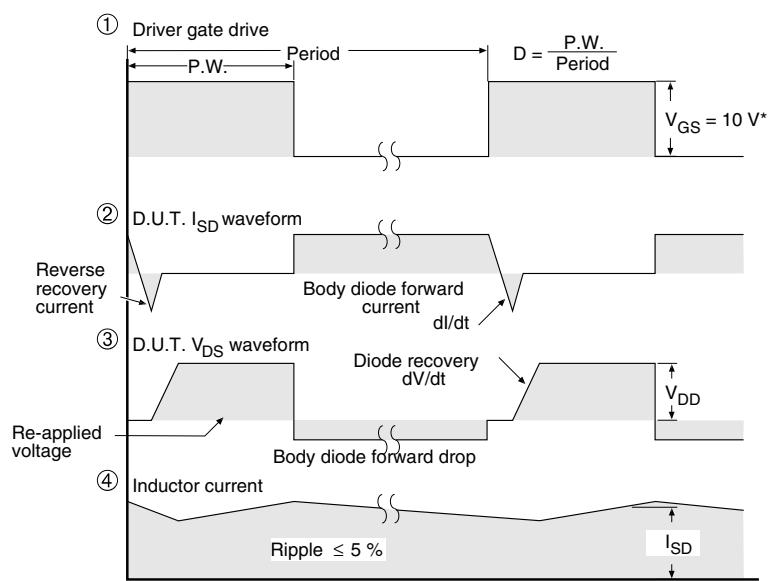
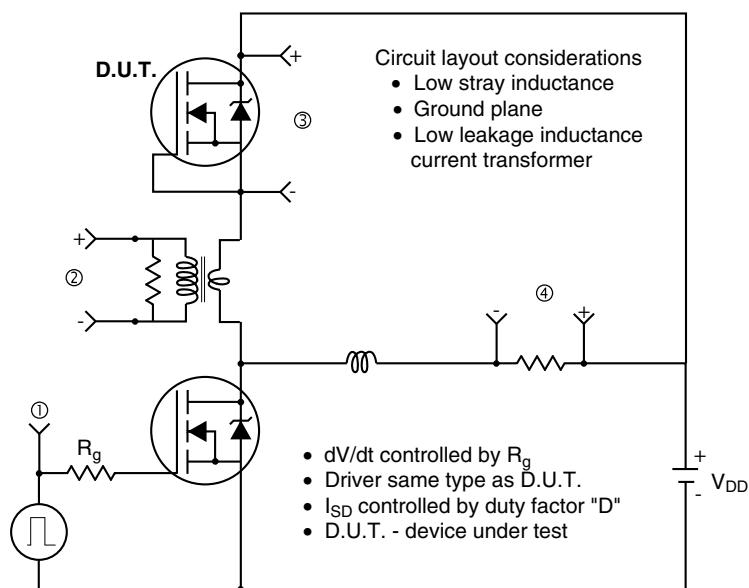


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case


Fig. 12a - Unclamped Inductive Test Circuit

Fig. 13a - Basic Gate Charge Waveform

Fig. 12b - Unclamped Inductive Waveforms

Fig. 13b - Gate Charge Test Circuit

Fig. 12c - Maximum Avalanche Energy vs. Drain Current

Peak Diode Recovery dV/dt Test Circuit

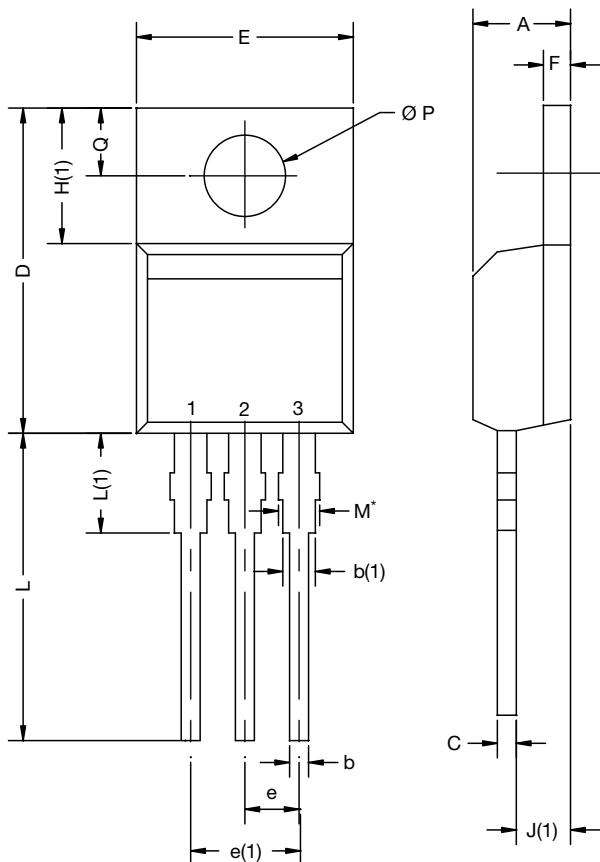


* $V_{GS} = 5 \text{ V}$ for logic level devices

Fig. 14 - For N-Channel

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TO-220-1



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.24	4.65	0.167	0.183
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.78	0.045	0.070
c	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
E	9.96	10.52	0.392	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.10	6.71	0.240	0.264
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
Ø P	3.53	3.94	0.139	0.155
Q	2.54	3.00	0.100	0.118

ECN: X15-0364-Rev. C, 14-Dec-15
DWG: 6031

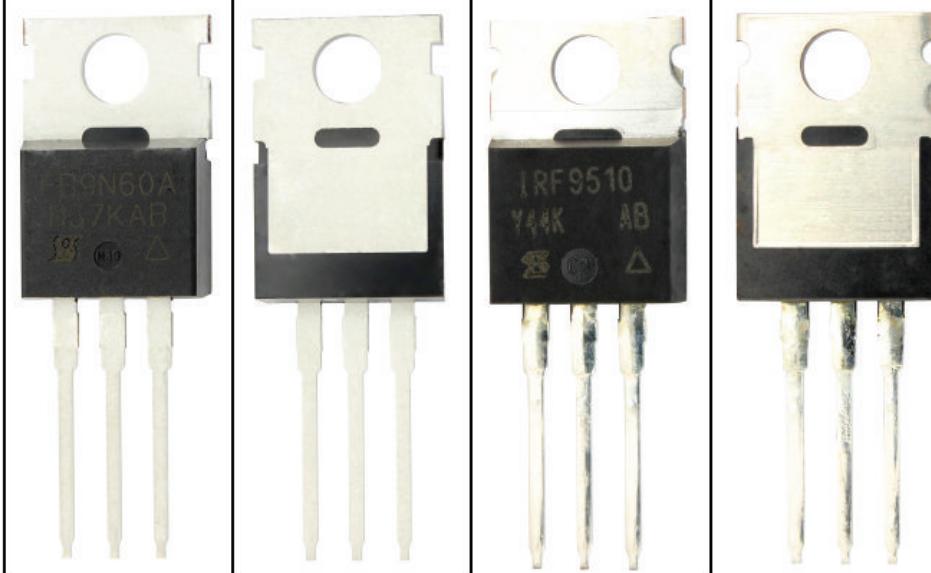
Note

- $M^* = 0.052$ inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM

Package Picture

ASE

Xi'an



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