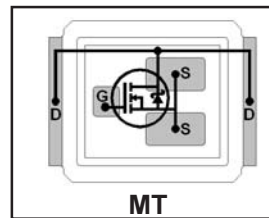


- Application Specific MOSFETs
- Ideal for CPU Core DC-DC Converters
- Low Conduction Losses
- High Cdv/dt Immunity
- Low Profile (<0.7 mm)
- Dual Sided Cooling Compatible
- Compatible with existing Surface Mount Techniques

V_{DS}	$R_{DS(on)}$ max	Q_g (typ.)
30V	3.3m Ω @ $V_{GS} = 10V$	50nC
	4.4m Ω @ $V_{GS} = 4.5V$	



Applicable DirectFET Outline and Substrate Outline (see p.9,10 for details)

SQ	SX	ST		MQ	MX	MT				
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Description

The IRF6607 combines the latest HEXFET® Power MOSFET Silicon technology with the advanced DirectFET™ packaging to achieve the lowest on-state resistance in a package that has the footprint of an SO-8 and only 0.7 mm profile. The DirectFET package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques, when application note AN-1035 is followed regarding the manufacturing methods and process. The DirectFET package allows dual sided cooling to maximize thermal transfer in power systems, IMPROVING previous best thermal resistance by 80%.

The IRF6607 balances both low resistance and low charge along with ultra low package inductance to reduce both conduction and switching losses. The reduced total losses make this product ideal for high efficiency DC-DC converters that power the latest generation of processors operating at higher frequencies. The IRF6607 has been optimized for parameters that are critical in synchronous buck converters including $R_{ds(on)}$, gate charge and Cdv/dt-induced turn on immunity. The IRF6607 offers particularly low $R_{ds(on)}$ and high Cdv/dt immunity for synchronous FET applications.

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	± 12	
I_D @ $T_C = 25^\circ C$	Continuous Drain Current, V_{GS} @ 10V ④	94	A
I_D @ $T_A = 25^\circ C$	Continuous Drain Current, V_{GS} @ 10V ④	27	
I_D @ $T_A = 70^\circ C$	Continuous Drain Current, V_{GS} @ 10V ⑦	22	
I_{DM}	Pulsed Drain Current ①	220	
P_D @ $T_A = 25^\circ C$	Power Dissipation ④	3.6	W
P_D @ $T_A = 70^\circ C$	Power Dissipation ④	2.3	
P_D @ $T_C = 25^\circ C$	Power Dissipation ⑦	42	
	Linear Derating Factor	0.029	W/°C
T_J	Operating Junction and	-40 to + 150	°C
T_{STG}	Storage Temperature Range		

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ④ ⑧	—	35	°C/W
$R_{\theta JA}$	Junction-to-Ambient ⑤ ⑧	12.5	—	
$R_{\theta JA}$	Junction-to-Ambient ⑥ ⑧	20	—	
$R_{\theta JC}$	Junction-to-Case ⑦ ⑧	—	3.0	
$R_{\theta J-PCB}$	Junction-to-PCB Mounted	—	1.0	

Notes ① through ⑧ are on page 10
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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

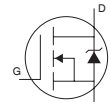
	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	29	—	mV/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	2.5	3.3	$m\Omega$	$V_{GS} = 10V, I_D = 25A$ ③
		—	3.4	4.4		$V_{GS} = 4.5V, I_D = 20A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	1.3	—	2.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-5.3	—	mV/ $^\circ\text{C}$	
I_{DSS}	Drain-to-Source Leakage Current	—	—	30	μA	$V_{DS} = 24V, V_{GS} = 0V$
		—	—	50	μA	$V_{DS} = 30V, V_{GS} = 0V$
		—	—	100		$V_{DS} = 24V, V_{GS} = 0V, T_J = 70^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 12V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -12V$
g_{fs}	Forward Transconductance	120	—	—	S	$V_{DS} = 15V, I_D = 20A$
Q_g	Total Gate Charge	—	50	75	nC	$V_{DS} = 15V$ $V_{GS} = 4.5V$ $I_D = 20A$ See Fig. 16
Q_{gs1}	Pre-V _{th} Gate-to-Source Charge	—	13	—		
Q_{gs2}	Post-V _{th} Gate-to-Source Charge	—	4.0	—		
Q_{gd}	Gate-to-Drain Charge	—	16	—		
Q_{godr}	Gate Charge Overdrive	—	18	—		
Q_{sw}	Switch Charge ($Q_{gs2} + Q_{gd}$)	—	20	—		
Q_{oss}	Output Charge	—	30	—	nC	$V_{DS} = 16V, V_{GS} = 0V$
R_G	Gate Resistance	—	0.86	1.9	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	60	—	ns	$V_{DD} = 15V, V_{GS} = 4.5V$ ③ $I_D = 20A$ Clamped Inductive Load
t_r	Rise Time	—	8.0	—		
$t_{d(off)}$	Turn-Off Delay Time	—	32	—		
t_f	Fall Time	—	13	—		
C_{iss}	Input Capacitance	—	6930	—	pF	$V_{GS} = 0V$ $V_{DS} = 15V$ $f = 1.0MHz$
C_{oss}	Output Capacitance	—	1260	—		
C_{rss}	Reverse Transfer Capacitance	—	510	—		

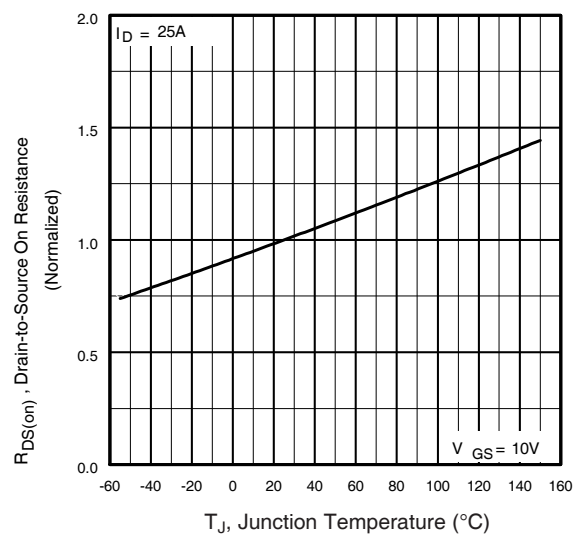
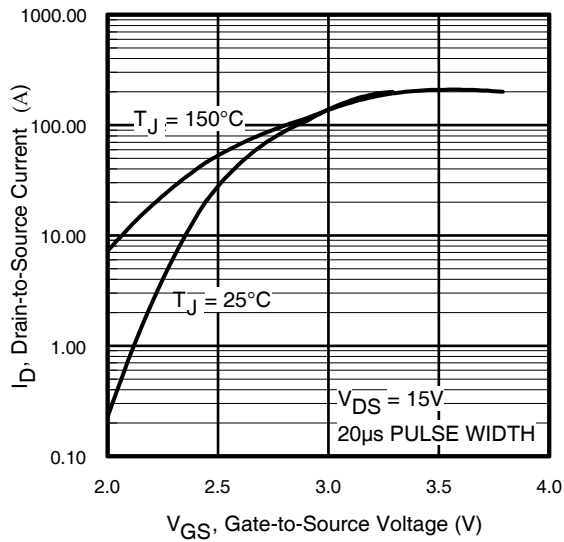
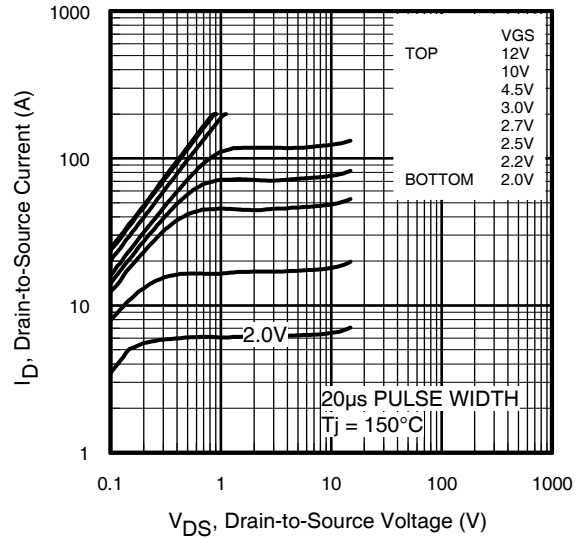
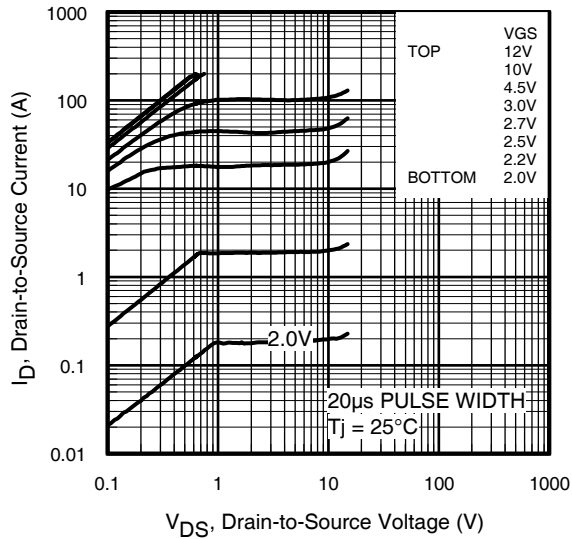
Avalanche Characteristics

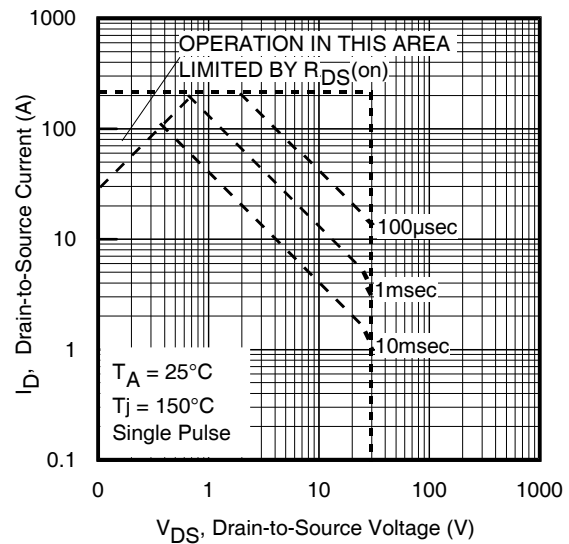
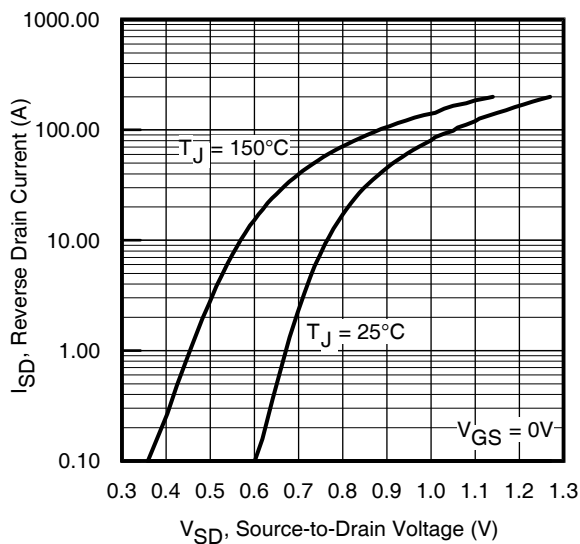
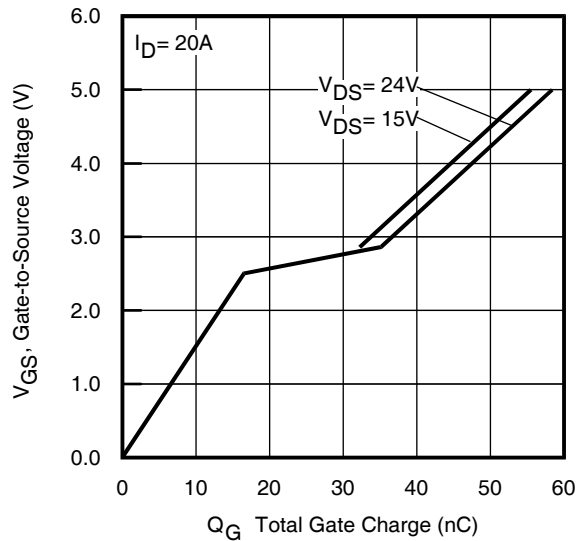
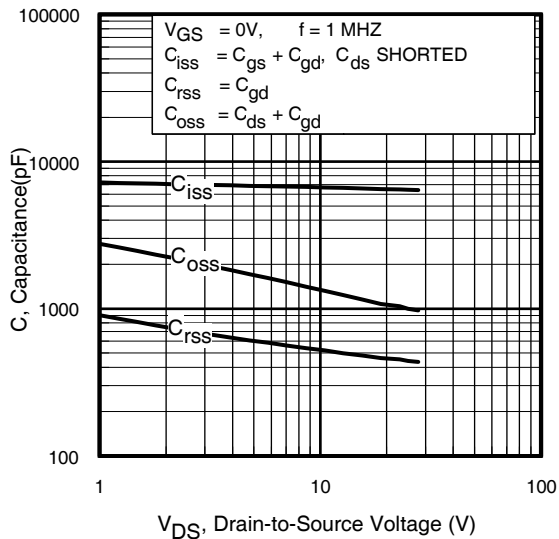
	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	51	mJ
I_{AR}	Avalanche Current ①	—	20	A
E_{AR}	Repetitive Avalanche Energy ①	—	0.36	mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	38	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	220		
V_{SD}	Diode Forward Voltage	—	1.0	1.3	V	$T_J = 25^\circ\text{C}, I_S = 20A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	46	69	ns	$T_J = 25^\circ\text{C}, I_F = 20A$
Q_{rr}	Reverse Recovery Charge	—	54	81	nC	$di/dt = 100A/\mu s$ ③







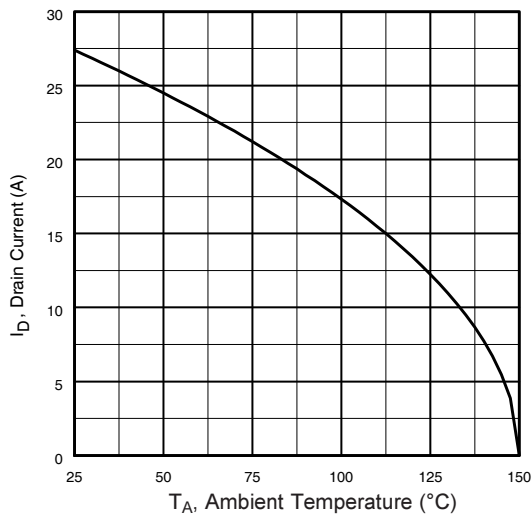


Fig 9. Maximum Drain Current Vs. Ambient Temperature

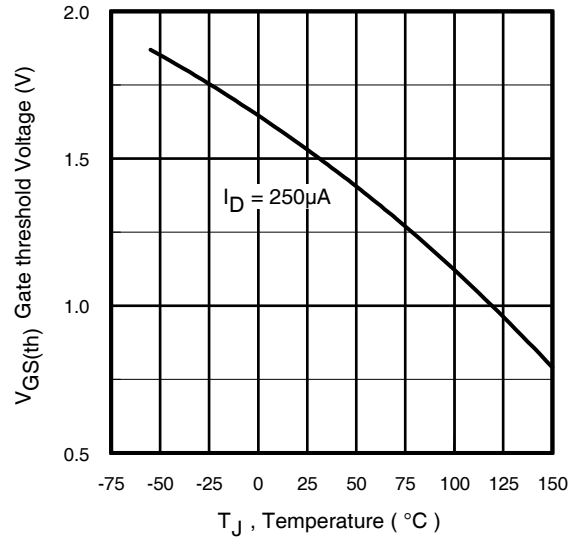


Fig 10. Threshold Voltage Vs. Temperature

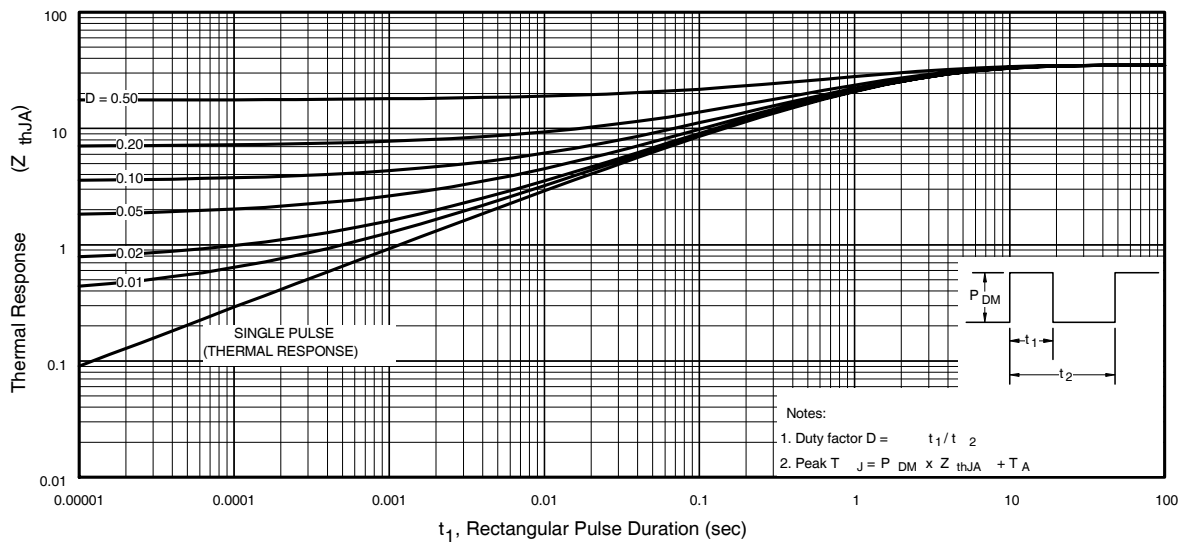


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

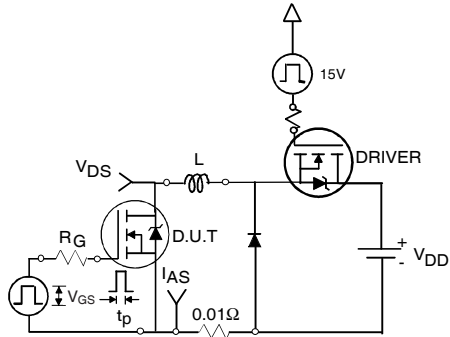


Fig 12a. Unclamped Inductive Test Circuit

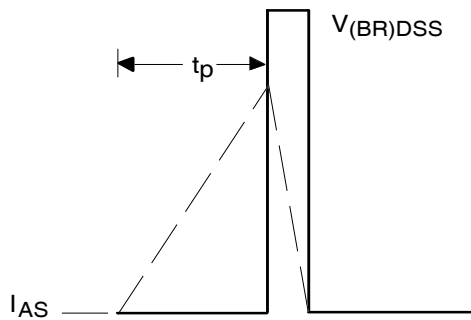


Fig 12b. Unclamped Inductive Waveforms

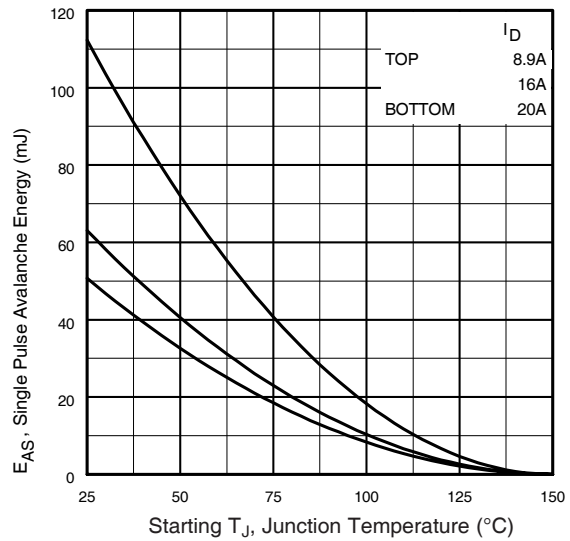


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

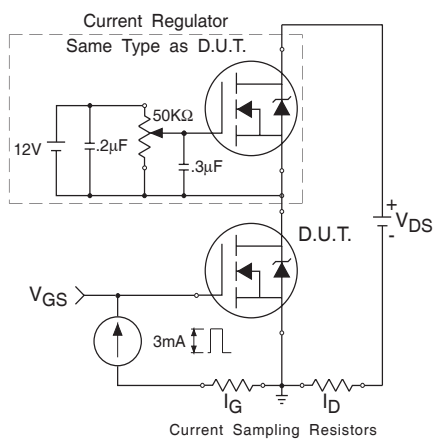


Fig 13. Gate Charge Test Circuit

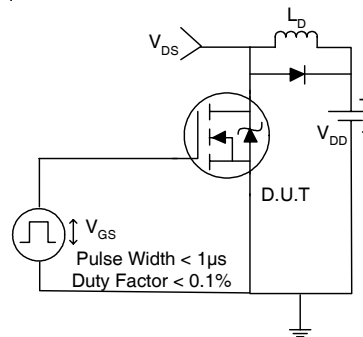


Fig 14a. Switching Time Test Circuit

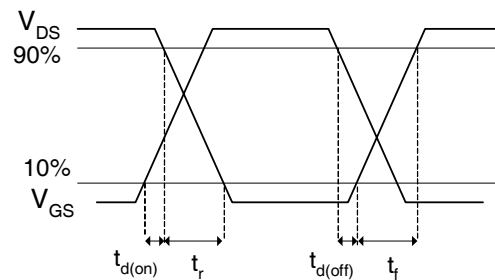


Fig 14b. Switching Time Waveforms

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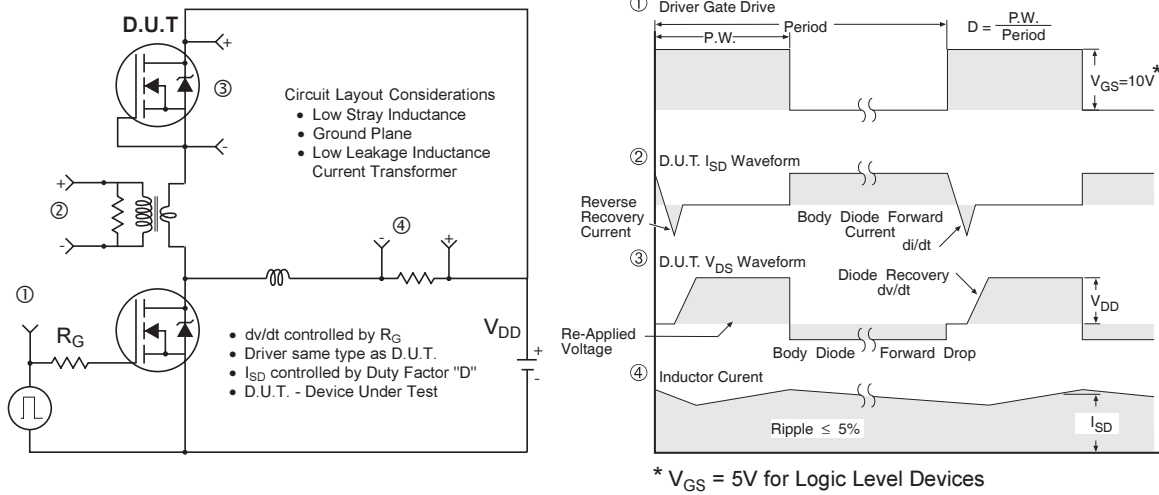


Fig 15. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

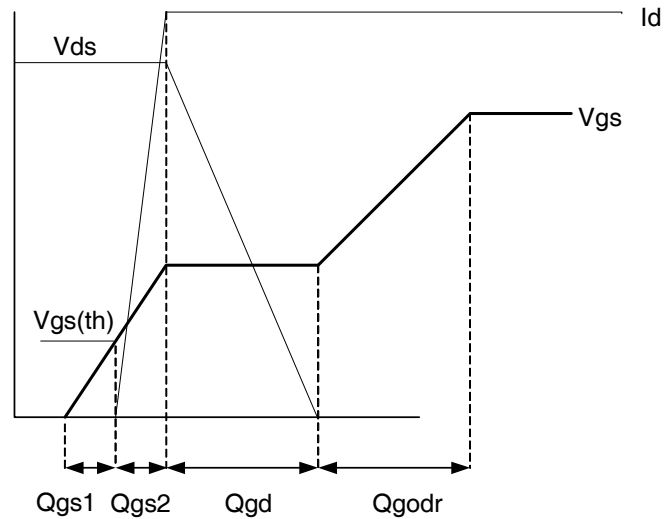


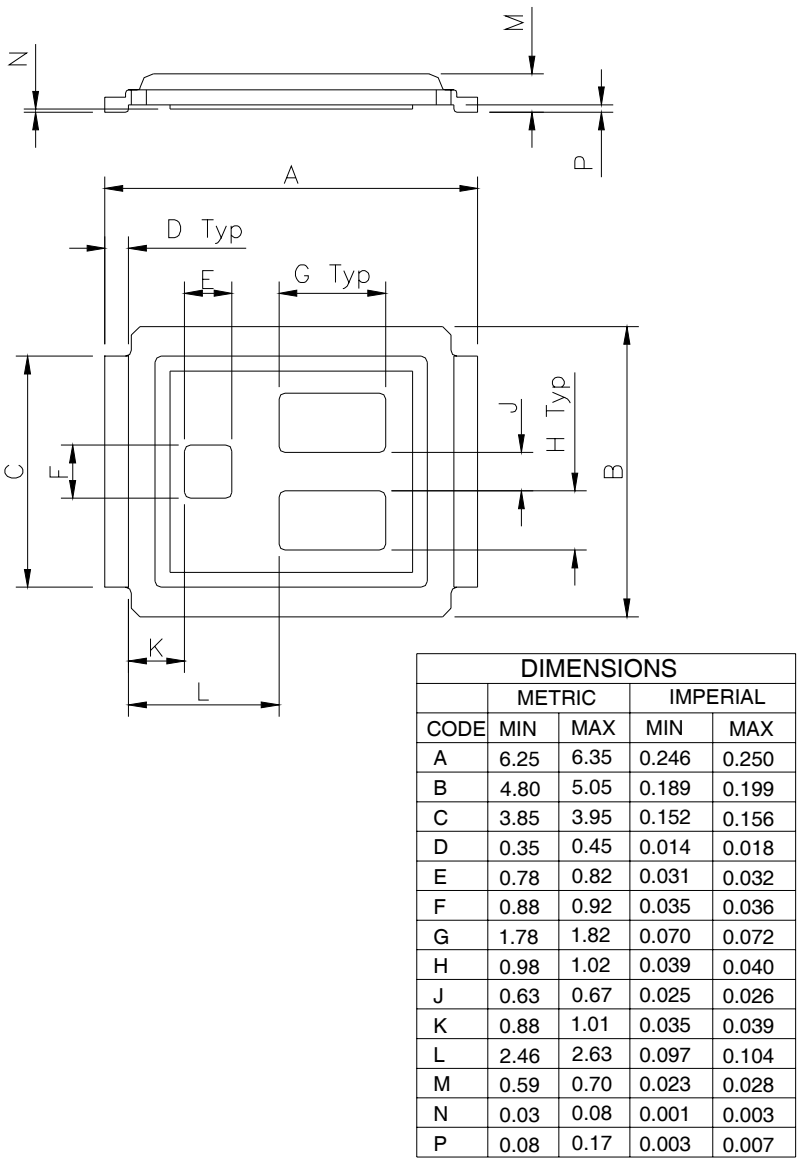
Fig 16. Gate Charge Waveform

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DirectFET™ Outline Dimension, MT Outline (Medium Size Can, T-Designation).

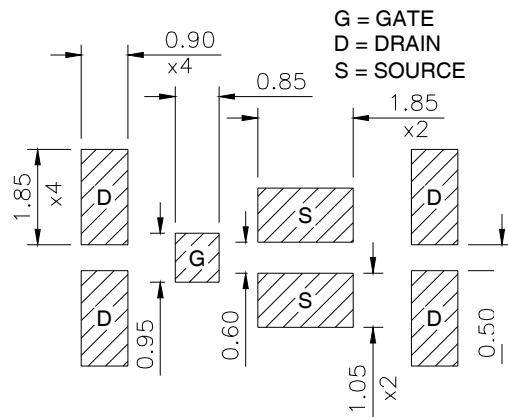
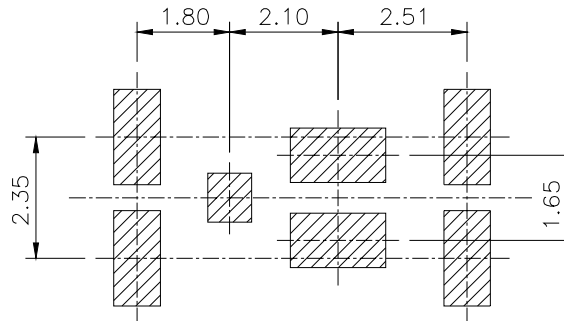
Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET. This includes all recommendations for stencil and substrate designs.



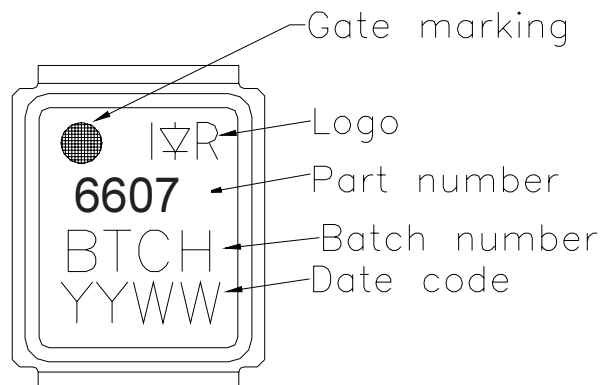
DirectFET™ Substrate and PCB Layout, MT Outline (MediumSize Can, T-Designation).

Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET.

This includes all recommendations for stencil and substrate designs.



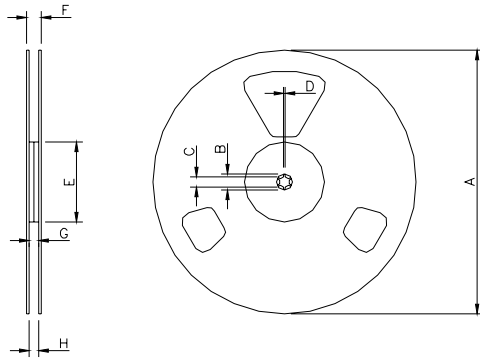
DirectFET™ Part Marking



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DirectFET™ Tape & Reel Dimension (Showing component orientation).



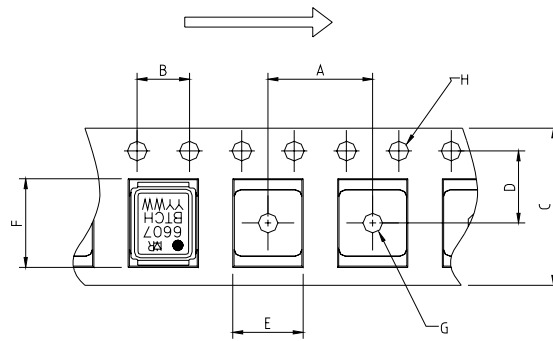
NOTE: Controlling dimensions in mm
Std reel quantity is 4800 parts. (ordered as IRF6607). For 1000 parts on 7" reel,
order IRF6607TR1

REEL DIMENSIONS							
STANDARD OPTION (QTY 4800)				TR1 OPTION (QTY 1000)			
CODE	METRIC	IMPERIAL	METRIC	IMPERIAL	CODE	METRIC	IMPERIAL
A	330.0	N.C	12.992	N.C	177.77	N.C	6.9
B	20.2	N.C	0.795	N.C	19.06	N.C	0.75
C	12.8	13.2	0.504	0.520	13.5	12.8	0.53
D	1.5	N.C	0.059	N.C	1.5	N.C	0.059
E	100.0	N.C	3.937	N.C	58.72	N.C	2.31
F	N.C	18.4	N.C	0.724	N.C	13.50	N.C
G	12.4	14.4	0.488	0.567	11.9	12.01	0.47
H	11.9	15.4	0.469	0.606	11.9	12.01	0.47

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.25\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 20\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ Surface mounted on 1 in. square Cu board.
- ⑤ Used double sided cooling, mounting pad.
- ⑥ Mounted on minimum footprint full size board with metalized back and with small clip heatsink.
- ⑦ T_C measured with thermal couple mounted to top (Drain) of part.
- ⑧ R_{θ} is measured at T_J of approximately 90°C .

Loaded Tape Feed Direction



NOTE: CONTROLLING
DIMENSIONS IN MM

DIMENSIONS				
CODE	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	7.90	8.10	0.311	0.319
B	3.90	4.10	0.154	0.161
C	11.90	12.30	0.469	0.484
D	5.45	5.55	0.215	0.219
E	5.10	5.30	0.201	0.209
F	6.50	6.70	0.256	0.264
G	1.50	N.C	0.059	N.C
H	1.50	1.60	0.059	0.063

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

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IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
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Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>