

Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	- 200	
$R_{DS(on)}$ (Ω)	$V_{GS} = -10$ V	3.0
Q_g (Max.) (nC)	11	
Q_{gs} (nC)	7.0	
Q_{gd} (nC)	4.0	
Configuration	Single	

FEATURES

- Surface Mount
- Available in Tape and Reel
- Dynamic dV/dt Rating
- P-Channel
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Lead (Pb)-free Available

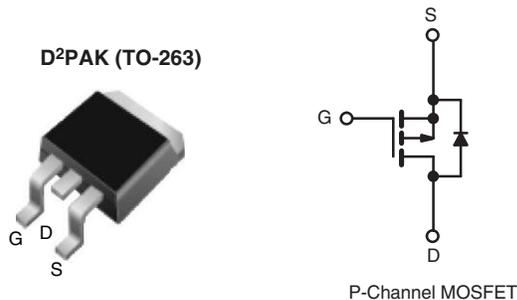


Available
RoHS*
COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D²PAK (TO-263) is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²PAK (TO-263) is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.



ORDERING INFORMATION	
Package	D ² PAK (TO-263)
Lead (Pb)-free	IRF9610SPbF
	SiHF9610S-E3
SnPb	IRF9610S
	SiHF9610S

ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	V_{DS}	- 200	V	
Gate-Source Voltage	V_{GS}	± 20		
Continuous Drain Current	V_{GS} at - 10 V	$T_C = 25$ °C	- 1.8	A
		$T_C = 100$ °C	- 1.0	
Pulsed Drain Current ^a	I_{DM}	- 7.0	W/°C	
Linear Derating Factor		0.16		
Linear Derating Factor (PCB Mount) ^d		0.025		
Maximum Power Dissipation	P_D	$T_C = 25$ °C	20	W
Maximum Power Dissipation (PCB Mount) ^d		$T_A = 25$ °C	3.0	
Peak Diode Recovery dV/dt^b	dV/dt	- 5.0	V/ns	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	°C	
Soldering Recommendations (Peak Temperature)	for 10 s	300°		

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 5).
- $I_{SD} \leq -1.8$ A, $dI/dt \leq 70$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C.
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Maximum Junction-to-Ambient (PCB Mount) ^a	R_{thJA}	-	40	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	6.4	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-200	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = -1\text{ mA}$	-	-0.23	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-2.0	-	-4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -200\text{ V}, V_{GS} = 0\text{ V}$	-	-	-100	μA
		$V_{DS} = -160\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	-500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -0.90\text{ A}^b$	-	-	3.0	Ω
Forward Transconductance	g_{fs}	$V_{DS} = -50\text{ V}, I_D = -0.90\text{ A}^b$	0.90	-	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = -25\text{ V}, f = 1.0\text{ MHz}$, see fig. 10	-	170	-	pF
Output Capacitance	C_{oss}		-	50	-	
Reverse Transfer Capacitance	C_{rss}		-	15	-	
Total Gate Charge	Q_g	$V_{GS} = -10\text{ V}, I_D = -3.5\text{ A}, V_{DS} = -160\text{ V}$, see fig. 11 and 18 ^b	-	-	11	nC
Gate-Source Charge	Q_{gs}		-	-	7.0	
Gate-Drain Charge	Q_{gd}		-	-	4.0	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -100\text{ V}, I_D = -0.90\text{ A}, R_G = 50\text{ }\Omega, R_D = 110\text{ }\Omega$, see fig. 17 ^b	-	8.0	-	ns
Rise Time	t_r		-	15	-	
Turn-Off Delay Time	$t_{d(off)}$		-	1.0	-	
Fall Time	t_f		-	8.0	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal Source Inductance	L_S		-	7.5	-	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p-n junction diode 	-	-	-1.8	A
Pulsed Diode Forward Current ^a	I_{SM}		-	-	-7.0	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = -1.8\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	-5.8	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = -1.8\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$	-	240	360	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	1.7	2.6	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 5).
- b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

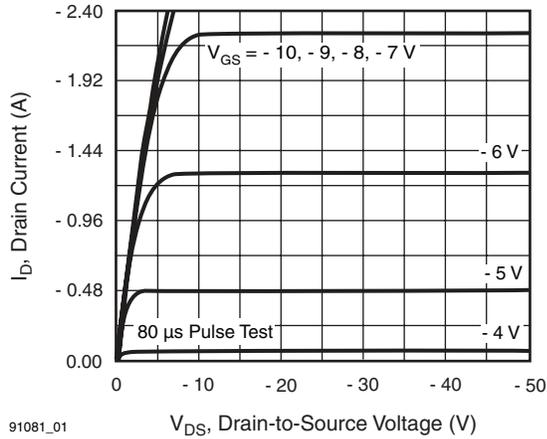


Fig. 1 - Typical Output Characteristics

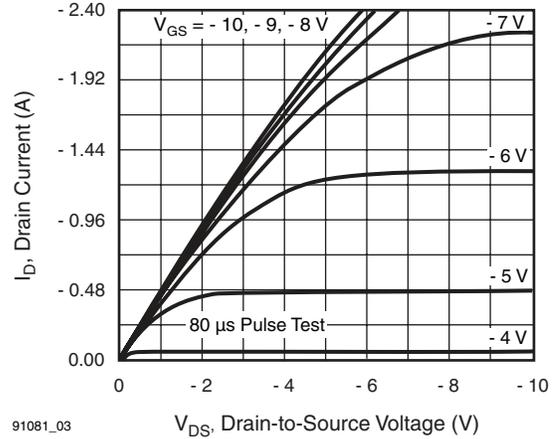


Fig. 3 - Typical Saturation Characteristics

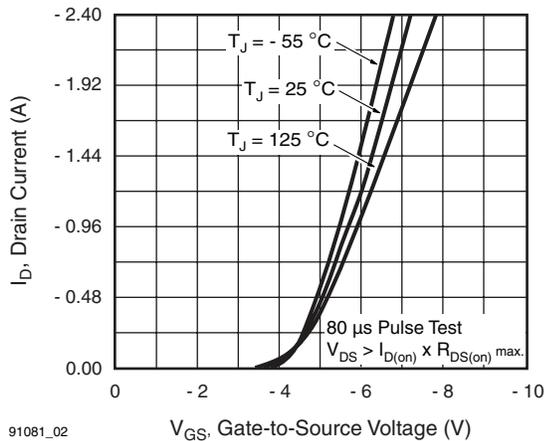


Fig. 2 - Typical Transfer Characteristics

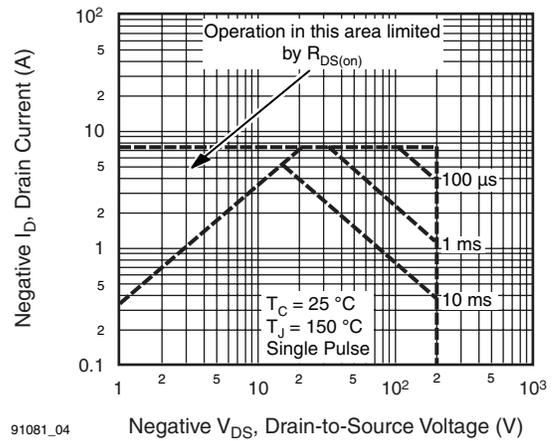


Fig. 4 - Maximum Safe Operating Area

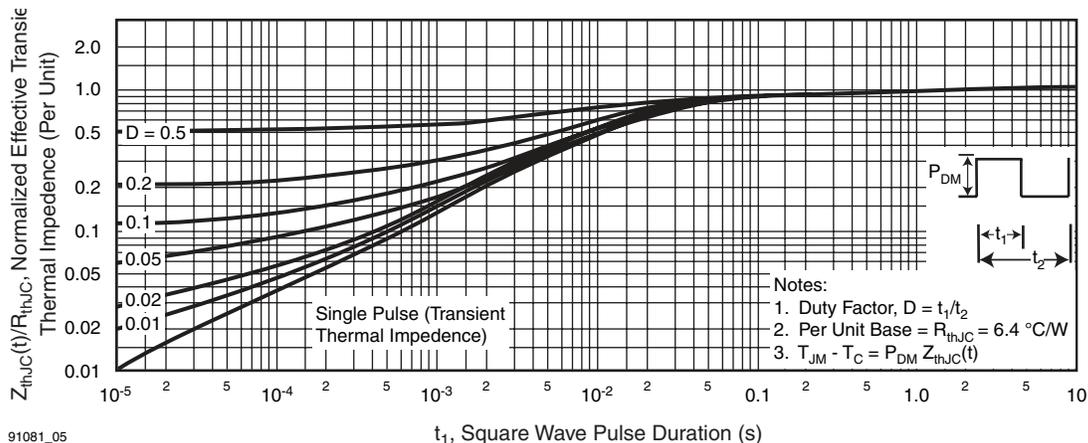
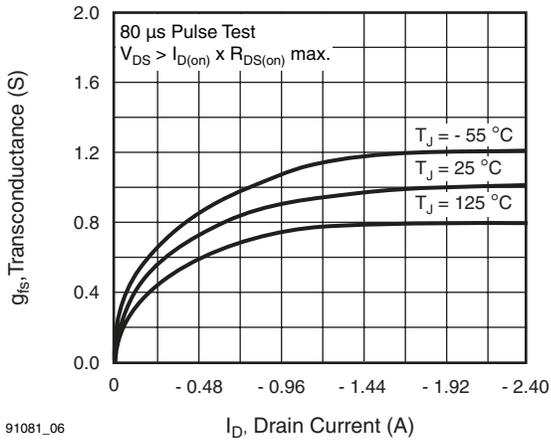
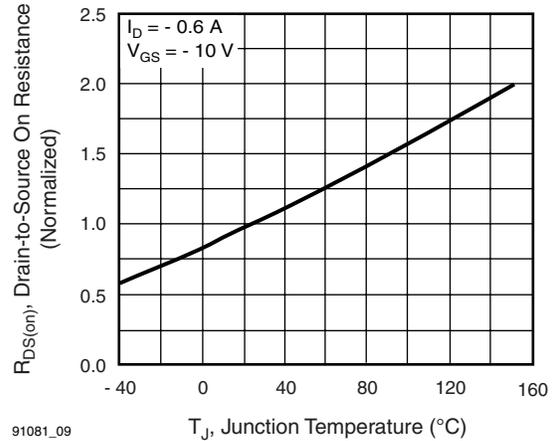


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case vs. Pulse Duration



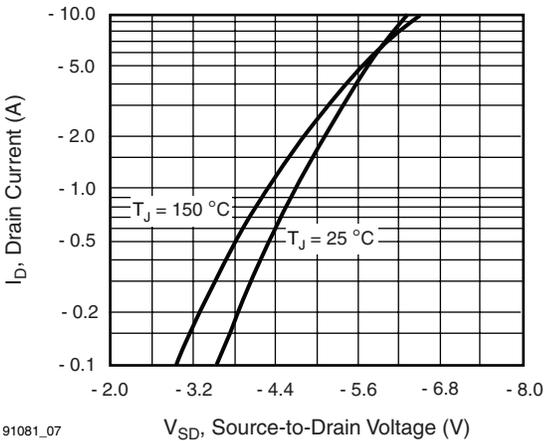
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Fig. 6 - Typical Transconductance vs. Drain Current



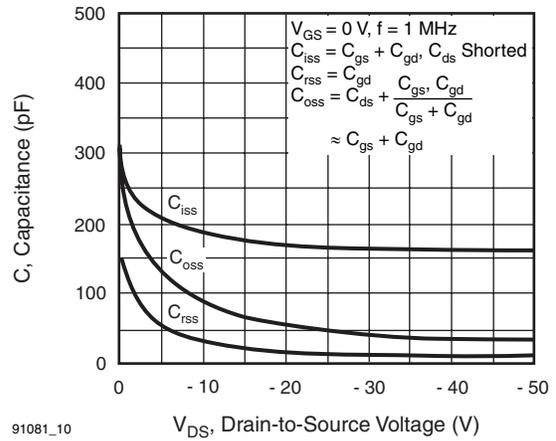
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Fig. 9 - Normalized On-Resistance vs. Temperature



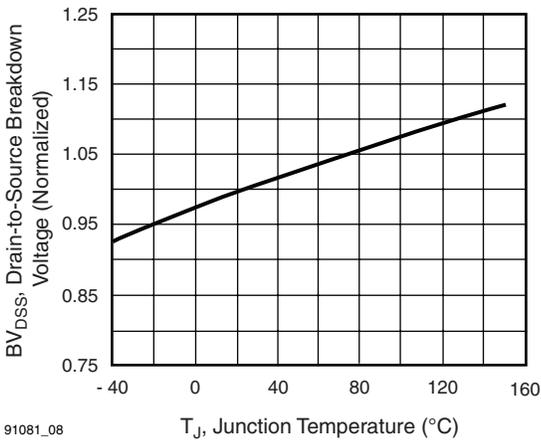
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Fig. 7 - Typical Source-Drain Diode Forward Voltage



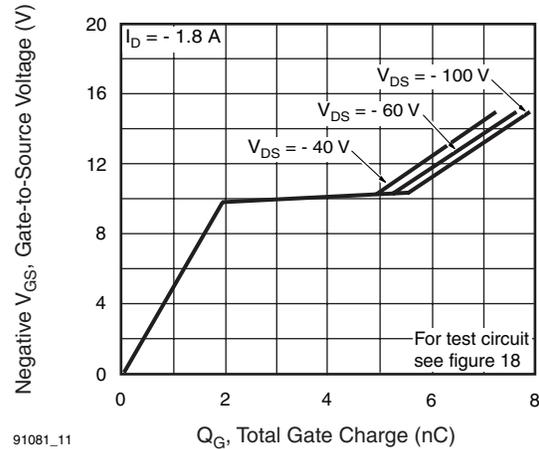
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Fig. 10 - Typical Capacitance vs. Drain-to-Source Voltage



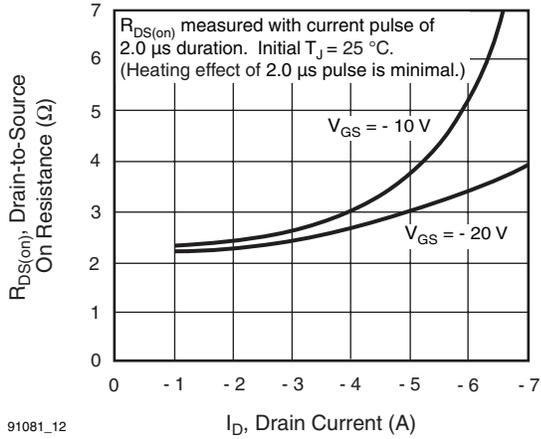
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Fig. 8 - Breakdown Voltage vs. Temperature



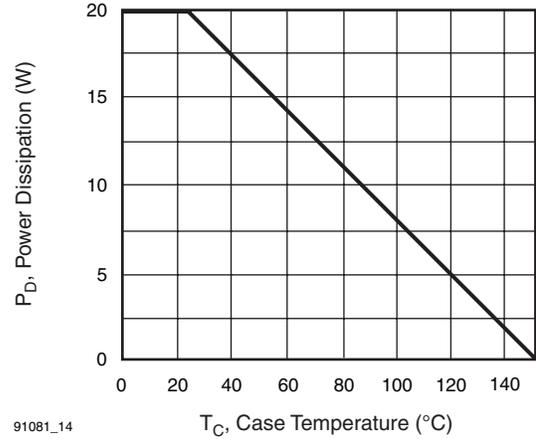
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Fig. 11 - Typical Gate Charge vs. Gate-to-Source Voltage



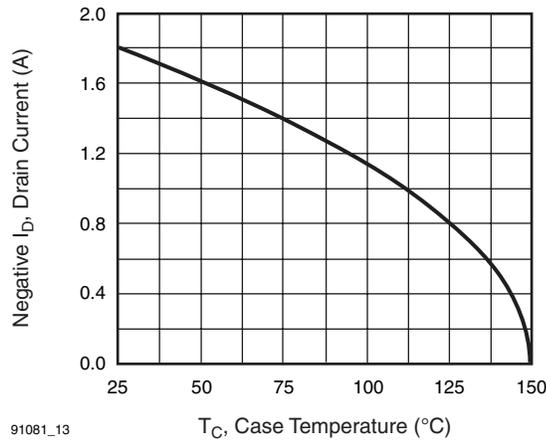
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Fig. 12 - Typical On-Resistance vs. Drain Current



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Fig. 14 - Power vs. Temperature Derating Curve



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Fig. 13 - Maximum Drain Current vs. Case Temperature

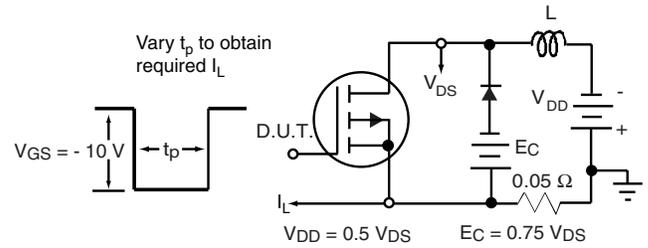


Fig. 15 - Clamped Inductive Test Circuit

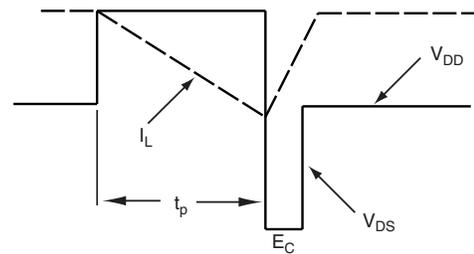


Fig. 16 - Clamped Inductive Waveforms

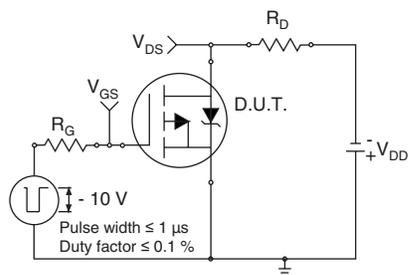


Fig. 17a - Switching Time Test Circuit

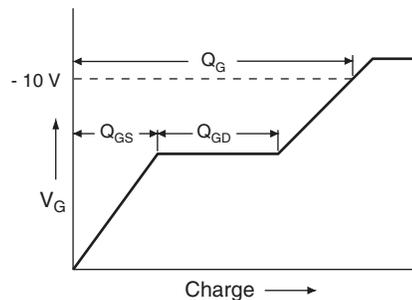


Fig. 18a - Basic Gate Charge Waveform

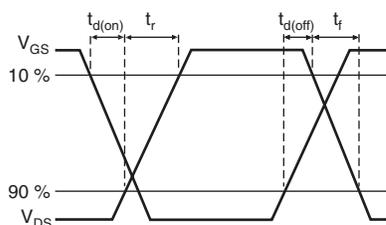


Fig. 17b - Switching Time Waveforms

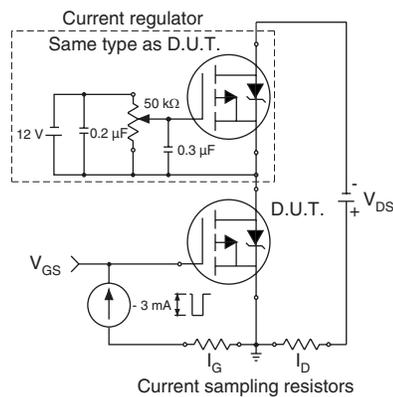
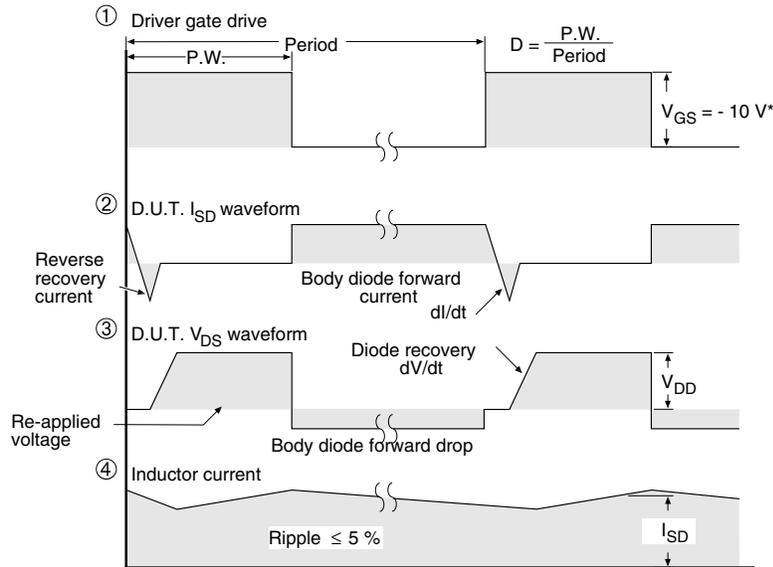
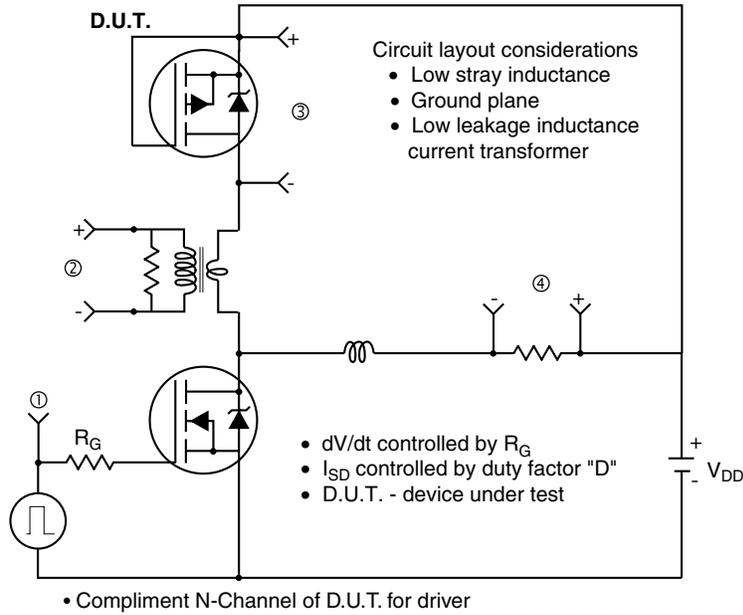


Fig. 18b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = -5\text{ V}$ for logic level and -3 V drive devices

Fig. 19 - For P-Channel

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