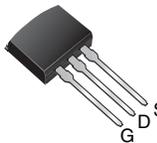


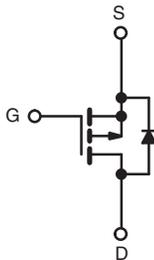
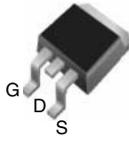
## Power MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	- 60	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = -10$ V	0.28
$Q_g$ (Max.) (nC)	19	
$Q_{gs}$ (nC)	5.4	
$Q_{gd}$ (nC)	11	
Configuration	Single	

I<sup>2</sup>PAK (TO-262)



D<sup>2</sup>PAK (TO-263)



P-Channel MOSFET

### FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Advanced Process Technology
- Surface Mount (IRF9Z24S, SiHF9Z24S)
- Low-Profile Through-Hole (IRF9Z24L, SiHF9Z24L)
- 175 °C Operating Temperature
- Fast Switching
- P-Channel
- Fully Avalanche Rated
- Compliant to RoHS Directive 2002/95/EC



RoHS\*  
COMPLIANT  
HALOGEN  
FREE  
Available

### DESCRIPTION

Third generation Power MOSFETs from Vishay utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D<sup>2</sup>PAK is a surface mount power package capable of accommodating die size up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D<sup>2</sup>PAK is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

The through-hole version (IR9Z24L, SiH9Z24L) is available for low-profile applications.

ORDERING INFORMATION				
Package	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)	I <sup>2</sup> PAK (TO-262)
Lead (Pb)-free and Halogen-free	SiHF9Z24S-GE3	SiHF9Z24STRL-GE3 <sup>a</sup>	SiHF9Z24STRR-GE3 <sup>a</sup>	-
Lead (Pb)-free	IRF9Z24SPbF	IRF9Z24STRLPbF <sup>a</sup>	IRF9Z24STRRPbF <sup>a</sup>	IRF9Z24LPbF
	SiHF9Z24S-E3	SiHF9Z24STL-E3 <sup>a</sup>	SiHF9Z24STR-E3 <sup>a</sup>	SiHF9Z24L-E3
SnPb	IRF9Z24S	IRF9Z24STRL <sup>a</sup>	IRF9Z24STRR <sup>a</sup>	IRF9Z24L
	SiHF9Z24S	SiHF9Z24STL <sup>a</sup>	SiHF9Z24STR <sup>a</sup>	SiHF9Z24L

#### Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL		LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$		- 60	V
Gate-Source Voltage	$V_{GS}$		$\pm 20$	
Continuous Drain Current <sup>e</sup>	$V_{GS}$ at - 10 V	$T_C = 25$ °C	- 11	A
		$T_C = 100$ °C	- 7.7	
Pulsed Drain Current <sup>a, e</sup>	$I_{DM}$		- 44	
Linear Derating Factor			0.40	W/°C
Single Pulse Avalanche Energy <sup>b, e</sup>	$E_{AS}$		240	mJ
Repetitive Avalanche Current <sup>a</sup>	$I_{AR}$		- 11	A
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$		6.0	mJ
Maximum Power Dissipation	$T_A = 25$ °C		3.7	W
	$T_C = 25$ °C		60	W
Peak Diode Recovery $dV/dt$ <sup>c, e</sup>	$dV/dt$		- 4.5	V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$		- 55 to + 175	°C
Soldering Recommendations (Peak Temperature)	for 10 s		300 <sup>d</sup>	

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = -25$  V, starting  $T_J = 25$  °C,  $L = 2.3$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = -11$  A (see fig. 12).
- $I_{SD} \leq -11$  A,  $dI/dt \leq 140$  A/ $\mu$ s,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 175$  °C.
- 1.6 mm from case.
- Uses IRF9Z24, SiHF9Z24 data and test conditions.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mount) <sup>a</sup>	$R_{thJA}$	-	-	40	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	-	2.5	

### Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

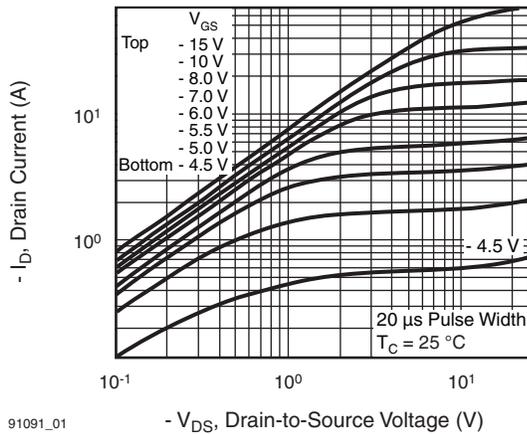
SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$		-60	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = -1\text{ mA}^c$		-	-0.056	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$		-2.0	-	-4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -60\text{ V}, V_{GS} = 0\text{ V}$		-	-	-100	$\mu\text{A}$
		$V_{DS} = -48\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$		-	-	-500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}$	$I_D = -6.6\text{ A}^b$	-	-	0.28	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = -25\text{ V}, I_D = -6.6\text{ A}^c$		1.4	-	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = -25\text{ V}, f = 1.0\text{ MHz}$ , see fig. 5 <sup>c</sup>		-	570	-	pF
Output Capacitance	$C_{oss}$			-	360	-	
Reverse Transfer Capacitance	$C_{rss}$			-	65	-	
Total Gate Charge	$Q_g$	$V_{GS} = -10\text{ V}$	$I_D = -11\text{ A}, V_{DS} = -48\text{ V}$ , see fig. 6 and 13 <sup>b, c</sup>	-	-	19	nC
Gate-Source Charge	$Q_{gs}$			-	-	5.4	
Gate-Drain Charge	$Q_{gd}$			-	-	11	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -30\text{ V}, I_D = -11\text{ A}, R_g = 18\text{ }\Omega, R_D = 2.5\text{ }\Omega$ , see fig. 10 <sup>b</sup>		-	13	-	ns
Rise Time	$t_r$			-	68	-	
Turn-Off Delay Time	$t_{d(off)}$			-	15	-	
Fall Time	$t_f$			-	29	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	-11	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	-44	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = -11\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	-6.3	V
<b>Drain-Source Body Diode Characteristics</b>							
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = -11\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b, c$		-	100	200	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	320	640	nC
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

### Notes

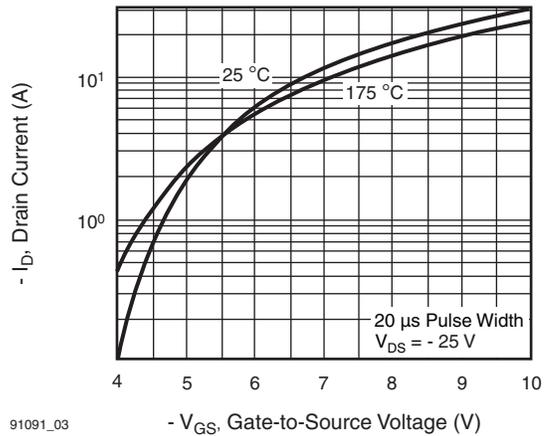
- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- Uses IRF9Z24, SiHF9Z24 data and test conditions.



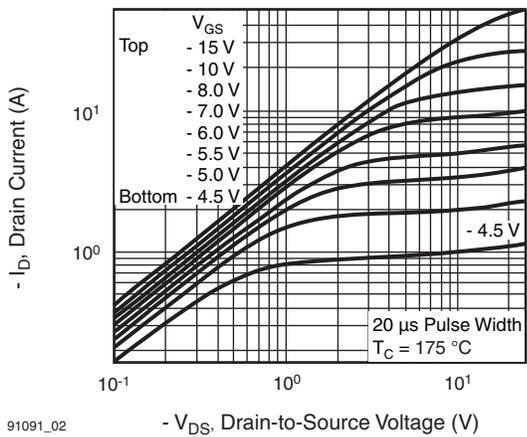
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



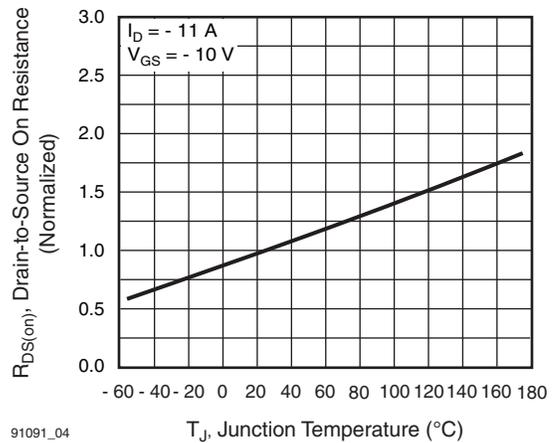
**Fig. 1 - Typical Output Characteristics**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 2 - Typical Output Characteristics**



**Fig. 4 - Normalized On-Resistance vs. Temperature**

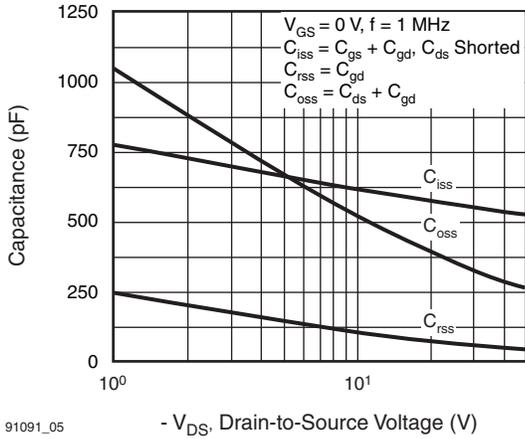


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

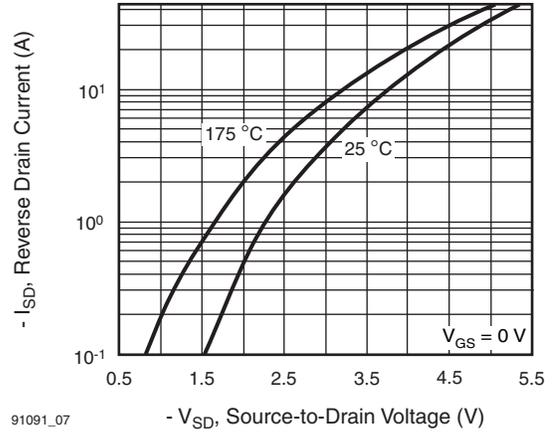


Fig. 7 - Typical Source-Drain Diode Forward Voltage

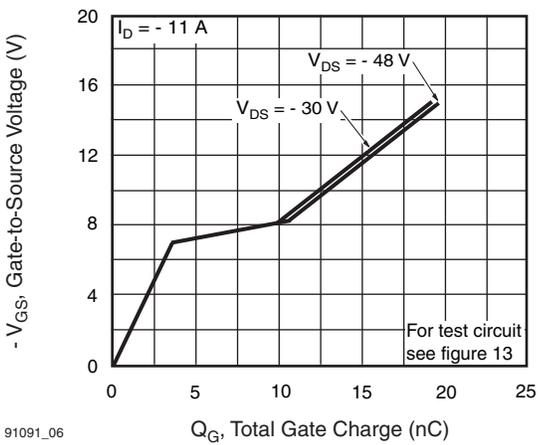


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

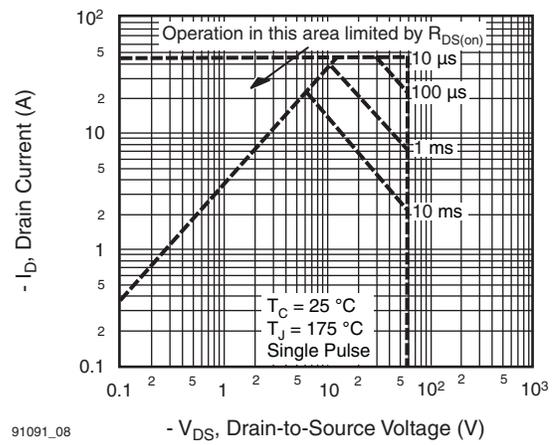
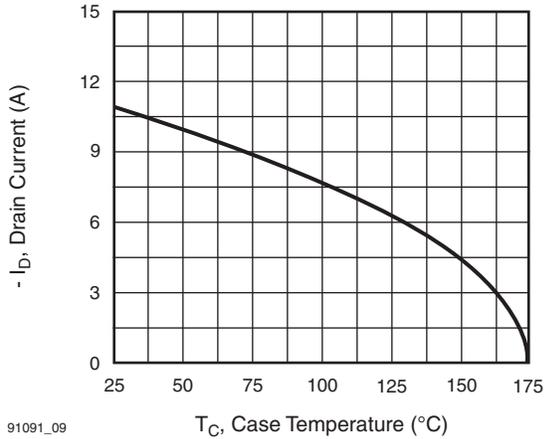
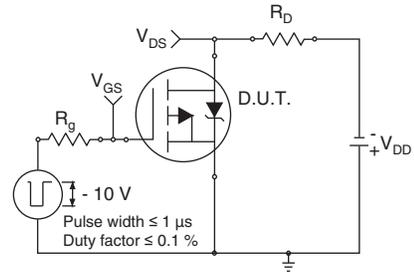


Fig. 8 - Maximum Safe Operating Area

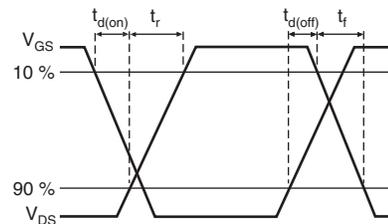


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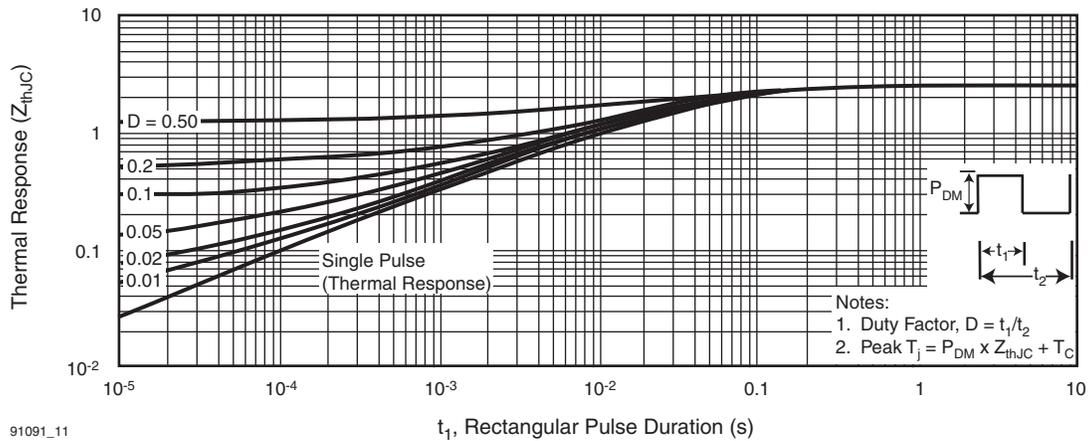
**Fig. 9 - Maximum Drain Current vs. Case Temperature**



**Fig. 10a - Switching Time Test Circuit**

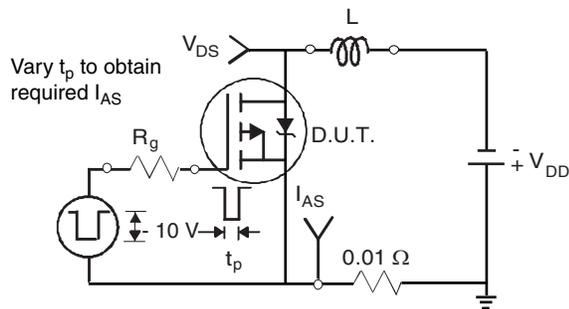


**Fig. 10b - Switching Time Waveforms**

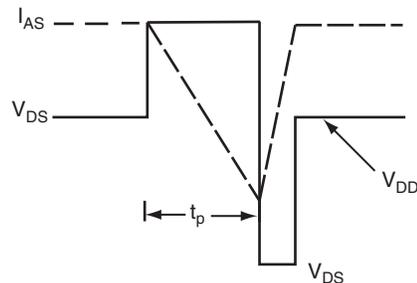


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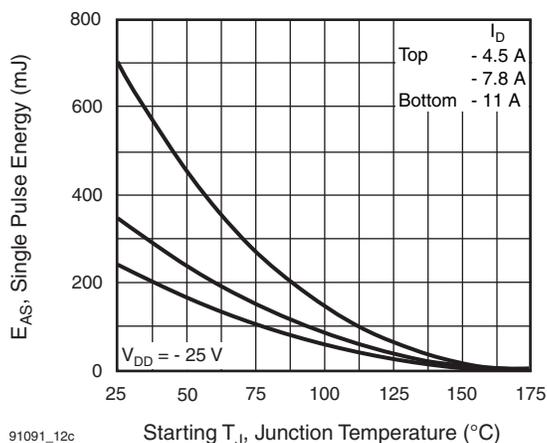
**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**



**Fig. 12a - Unclamped Inductive Test Circuit**

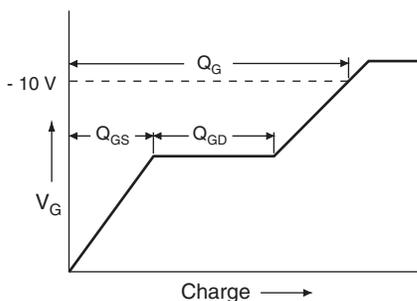


**Fig. 12b - Unclamped Inductive Waveforms**

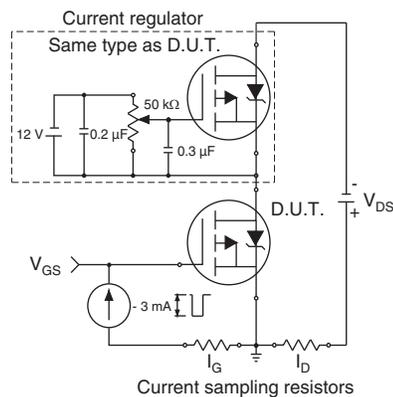


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**Fig. 12c - Maximum Avalanche Energy vs. Drain Current**

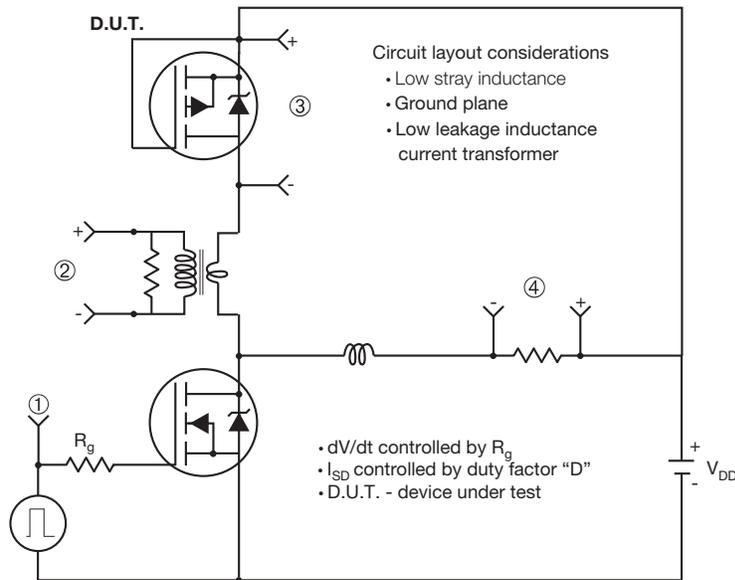


**Fig. 13a - Basic Gate Charge Waveform**

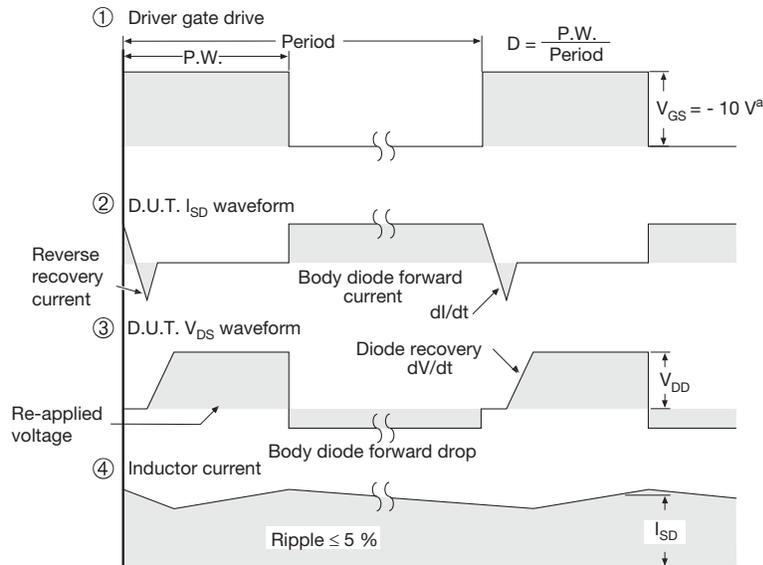


**Fig. 13b - Gate Charge Test Circuit**

### Peak Diode Recovery dV/dt Test Circuit



**Note**  
• Compliment N-Channel of D.U.T. for driver



**Note**  
a.  $V_{GS} = -5\text{ V}$  for logic level and  $-3\text{ V}$  drive devices

**Fig. 14 - For P-Channel**

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