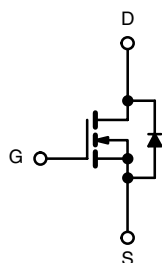
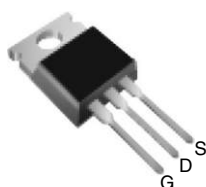


Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	500	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	0.21
Q_g (Max.) (nC)	110	
Q_{gs} (nC)	33	
Q_{gd} (nC)	54	
Configuration	Single	

TO-220



N-Channel MOSFET

FEATURES

- Low Gate Charge Q_g Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Low $R_{DS(on)}$
- Compliant to RoHS Directive 2002/95/EC



RoHS*
COMPLIANT

APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

ORDERING INFORMATION

Package	TO-220
Lead (Pb)-free	IRFB20N50KPbF
	SiHFB20N50K-E3
SnPb	IRFB20N50K
	SiHFB20N50K

ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V _{DS}	500	V
Gate-Source Voltage			V _{GS}	± 30	
Continuous Drain Current	V _{GS} at 10 V	T _C = 25 °C	I _D	20	A
		T _C = 100 °C		12	
Pulsed Drain Current ^a			I _{DM}	80	
Linear Derating Factor				2.2	W/°C
Single Pulse Avalanche Energy ^b			E _{AS}	330	mJ
Repetitive Avalanche Current ^a			I _{AR}	20	A
Repetitive Avalanche Energy ^a			E _{AR}	28	mJ
Maximum Power Dissipation	T _C = 25 °C		P _D	280	W
Peak Diode Recovery dV/dt ^c			dV/dt	10	V/ns
Operating Junction and Storage Temperature Range			T _J , T _{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300 ^d	
Mounting Torque	6-32 or M3 screw			10	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 1.6\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 20\text{ A}$.
- $I_{SD} \leq 20\text{ A}$, $dI/dt \leq 350\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	58	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.45	

SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		500	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.61	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		3.0	-	5.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 30 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 500 V, V _{GS} = 0 V		-	-	50	μA
		V _{DS} = 400 V, V _{GS} = 0 V, T _J = 125 °C		-	-	250	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 12 A ^b	-	0.21	0.25	Ω
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 12 A		11	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	2870	-	pF
Output Capacitance	C _{OSS}			-	320	-	
Reverse Transfer Capacitance	C _{rss}			-	34	-	
Output Capacitance	C _{OSS}	V _{GS} = 0 V	V _{DS} = 1.0 V, f = 1.0 MHz	-	3480	-	
Effective Output Capacitance	C _{OSS eff.}		V _{DS} = 400 V, f = 1.0 MHz	-	85	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 20 A, V _{DS} = 400 V see fig. 6 and 13 ^b	-	-	110	nC
Gate-Source Charge	Q _{gs}			-	-	33	
Gate-Drain Charge	Q _{gd}			-	-	54	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 250 V, I _D = 20 A R _g = 7.5 Ω, V _{GS} = 10 V, see fig. 10 ^b		-	22	-	ns
Rise Time	t _r			-	74	-	
Turn-Off Delay Time	t _{d(off)}			-	45	-	
Fall Time	t _f			-	33	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	20	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	80	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 20 A, V _{GS} = 0 V ^b		-	-	1.5	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 20 A, dI/dt = 100 A/μs ^b		-	520	780	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	5.3	8.0	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature.
b. Pulse width $\leq 400\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

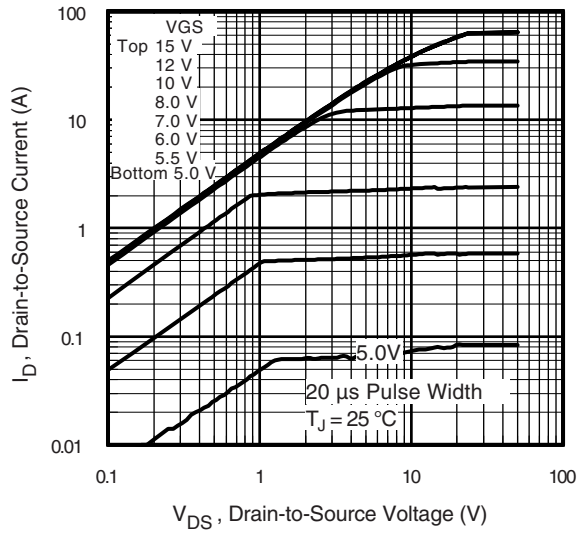


Fig. 1 - Typical Output Characteristics

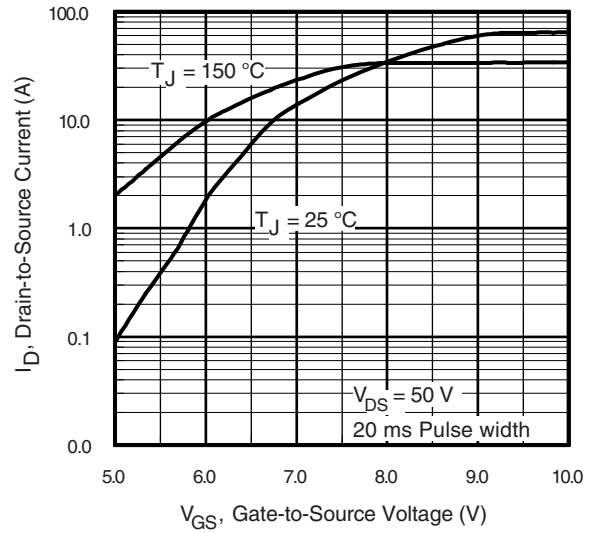


Fig. 3 - Typical Transfer Characteristics

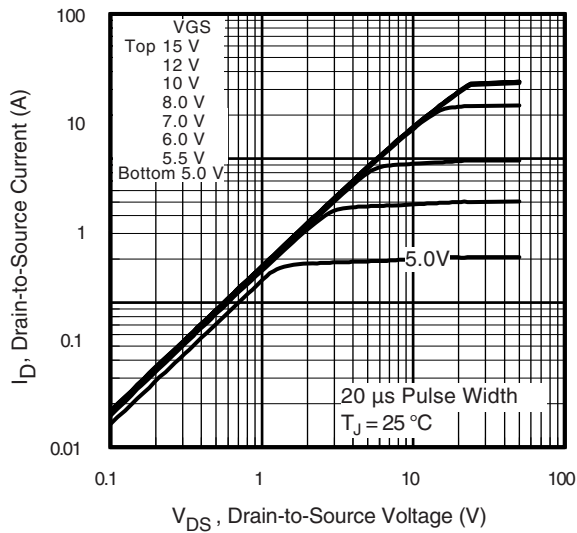


Fig. 2 - Typical Output Characteristics

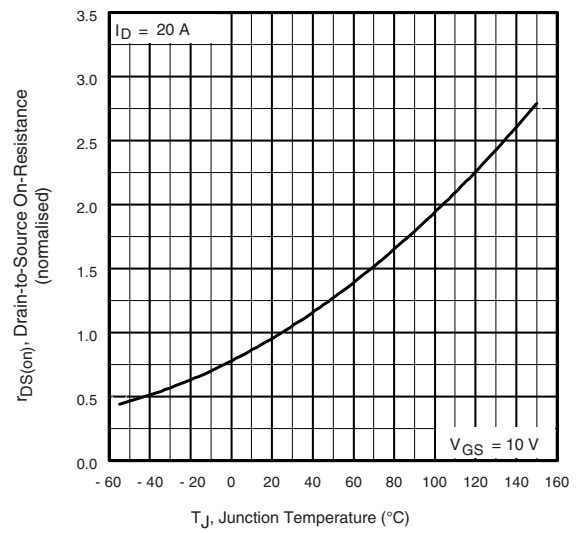


Fig. 4 - Normalized On-Resistance vs. Temperature

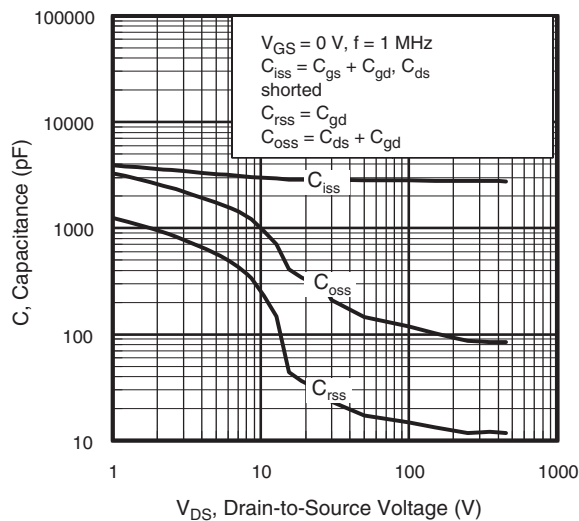


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

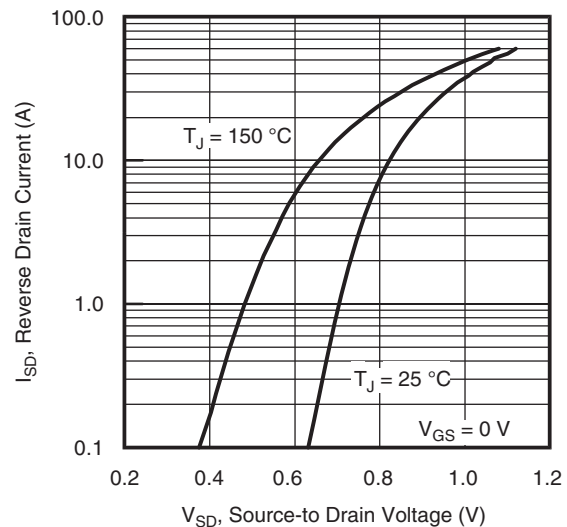


Fig. 7 - Typical Source-Drain Diode Forward Voltage

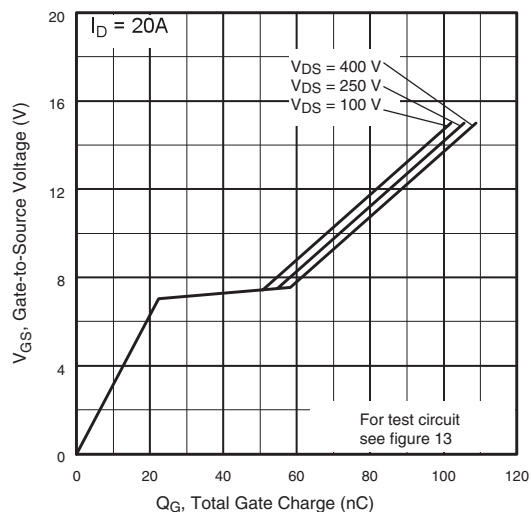


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

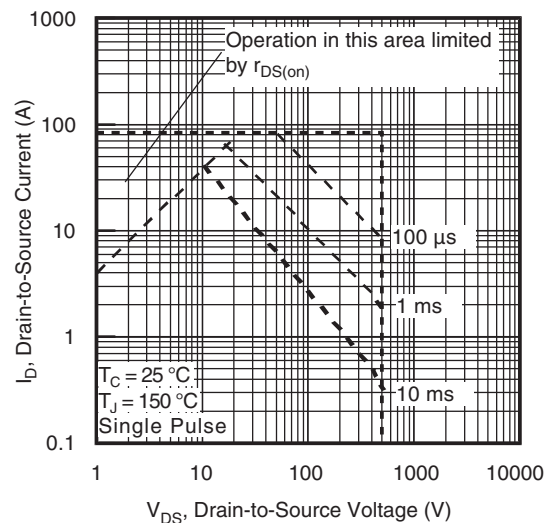


Fig. 8 - Maximum Safe Operating Area

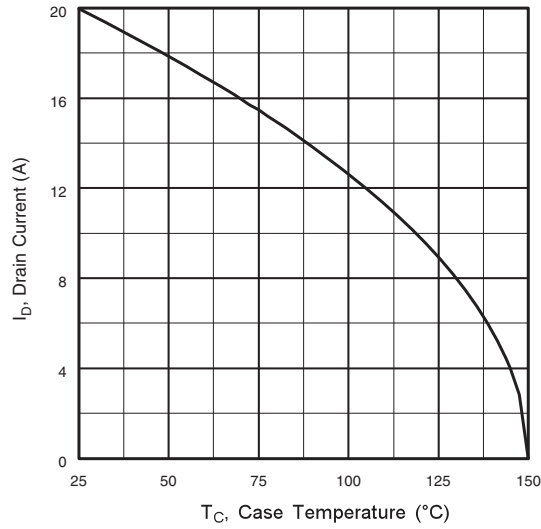


Fig. 9 - Maximum Drain Current vs. Case Temperature

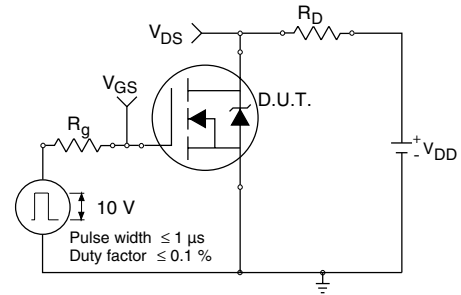


Fig. 10a - Switching Time Test Circuit

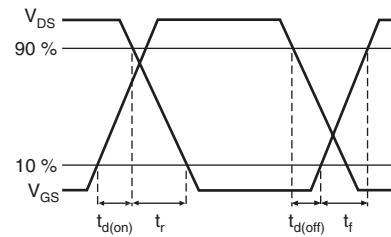


Fig. 10b - Switching Time Waveforms

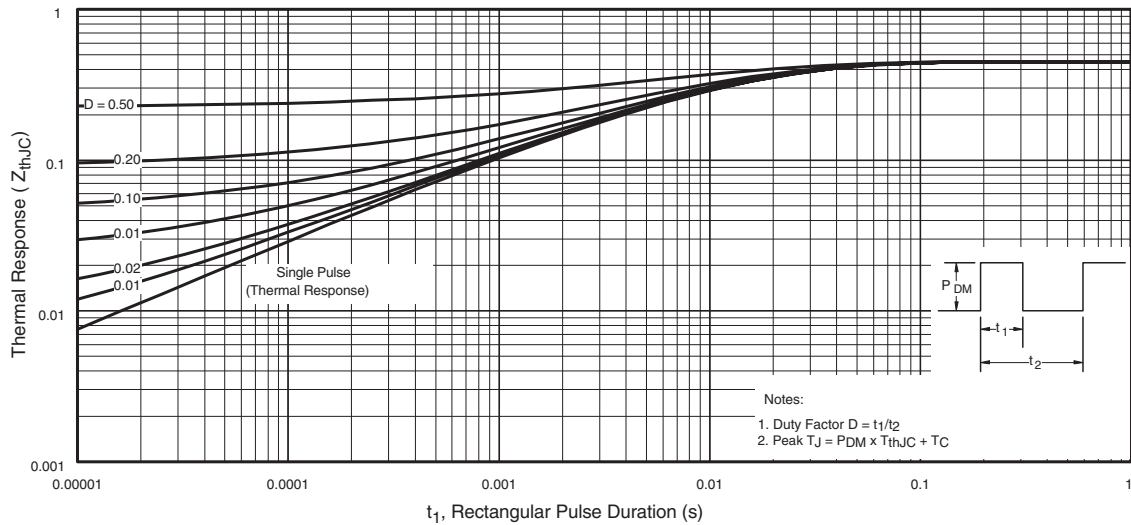


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

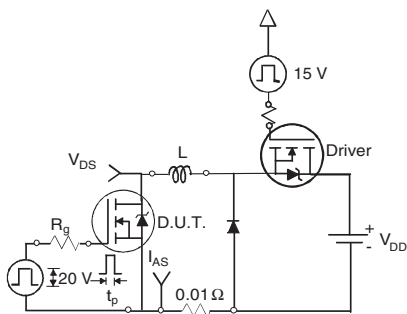


Fig. 12a - Unclamped Inductive Test Circuit

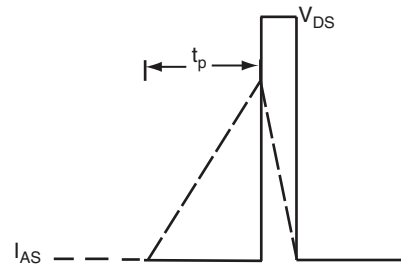


Fig. 12b - Unclamped Inductive Waveforms

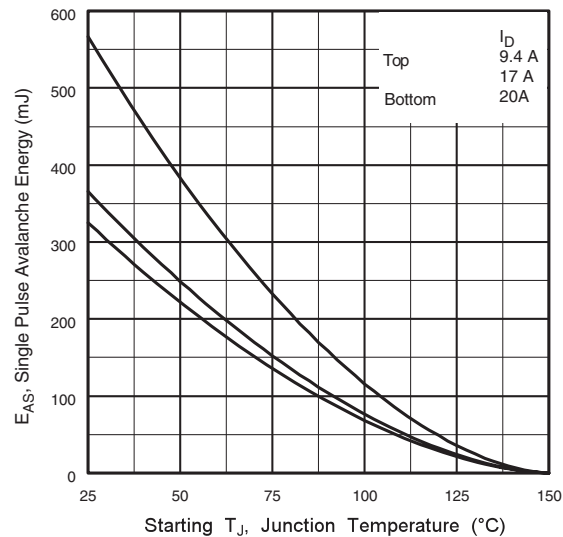


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

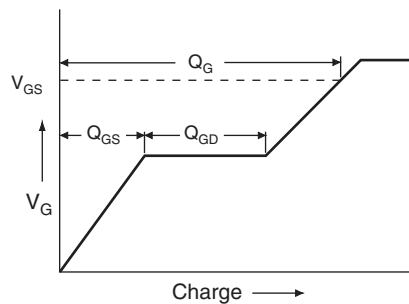


Fig. 13a - Basic Gate Charge Waveform

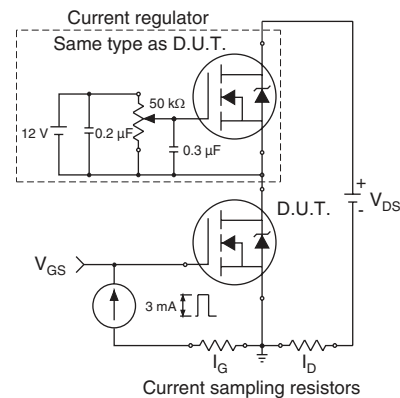
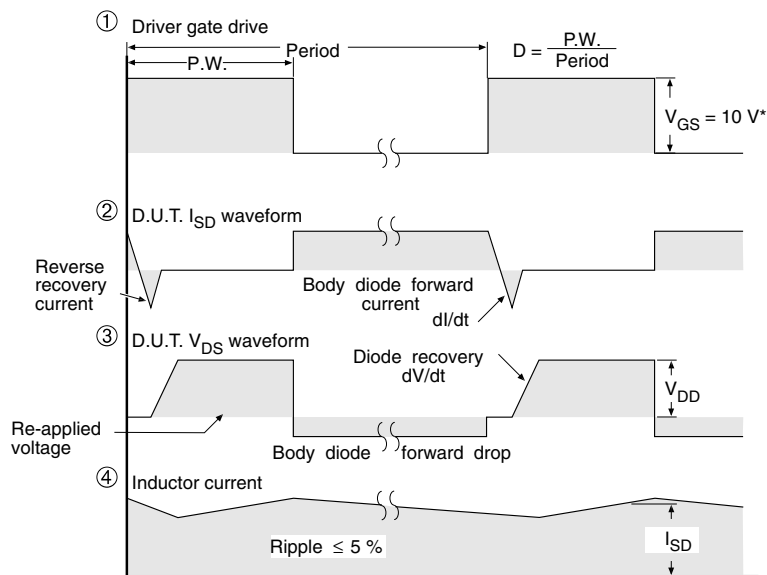
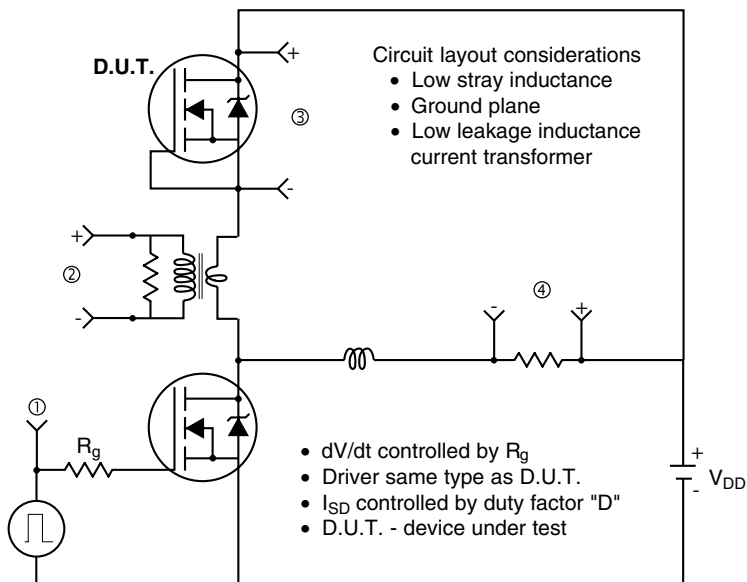


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

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