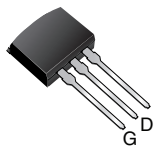
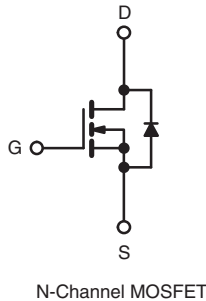


Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	600	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10$ V	2.2
Q_g (Max.) (nC)	31	
Q_{gs} (nC)	4.6	
Q_{gd} (nC)	17	
Configuration	Single	

I²PAK (TO-262)

D²PAK (TO-263)


FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Surface Mount (IRFBC30S, SiHFBC30S)
- Low-Profile Through-Hole (IRFBC30L, SiHFBC30L)
- Available in Tape and Reel (IRFBC30S, SiHFBC30S)
- Dynamic dV/dt Rating
- 150 °C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Compliant to RoHS Directive 2002/95/EC



RoHS*
COMPLIANT
HALOGEN
FREE
Available

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D²PAK is a surface mount power package capable of the accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²PAK is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application. The through-hole version (IRFBC30L, SiHFBC30L) is available for low-profile applications.

ORDERING INFORMATION

Package	D ² PAK (TO-263)	D ² PAK (TO-263)	I ² PAK (TO-262)
Lead (Pb)-free and Halogen-free	SiHFBC30S-GE3	SiHFBC30STRL-GE3 ^a	SiHFBC30L-GE3
Lead (Pb)-free	IRFBC30SPbF	IRFBC30STRLPbF ^a	IRFBC30LPbF
	SiHFBC30S-E3	SiHFBC30STL-E3 ^a	SiHFBC30L-E3

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	600	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ^e	I_D	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed Drain Current ^{a, e}	I_{DM}	14	
Linear Derating Factor		0.59	W/°C
Single Pulse Avalanche Energy ^{b, e}	E_{AS}	290	mJ
Avalanche Current ^a	I_{AR}	3.6	A
Repetitive Avalanche Energy ^a	E_{AR}	7.4	mJ
Maximum Power Dissipation	P_D	$T_A = 25$ °C	W
		$T_C = 25$ °C	
Peak Diode Recovery dV/dt ^{c, e}	dV/dt	3.0	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. $V_{DD} = 50$ V, starting $T_J = 25$ °C, $L = 41$ mH, $R_g = 25$ Ω , $I_{AS} = 3.6$ A (see fig. 12).

c. $I_{SD} \leq 3.6$ A, $dI/dt \leq 60$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C.

d. 1.6 mm from case.

e. Uses IRFBC30, SiHFBC30 data and test conditions.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mounted, steady-state) ^a	R_{thJA}	-	40	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.7	

Note

- a. When mounted on 1" square PCB (FR-4 or G-10 material).
For recommended footprint and soldering techniques refer to application note #AN-994.

SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

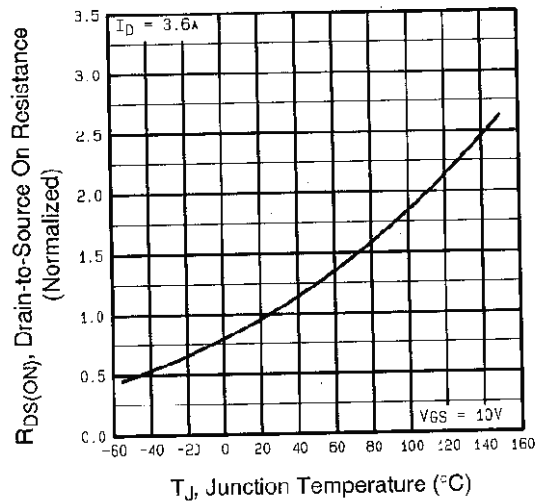
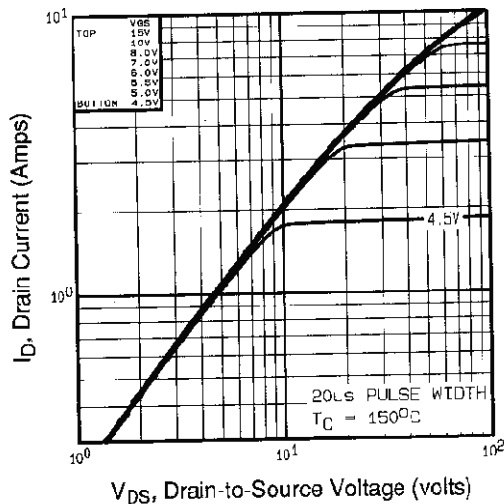
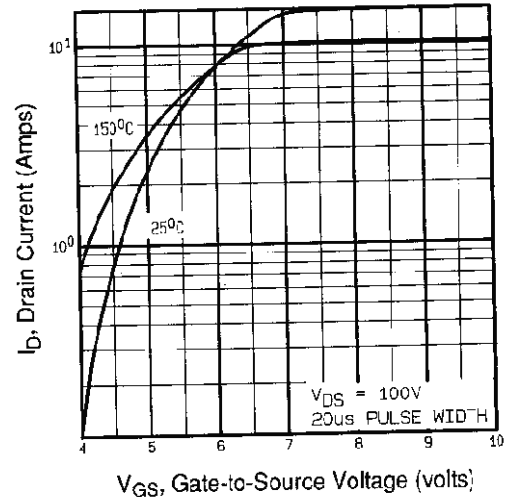
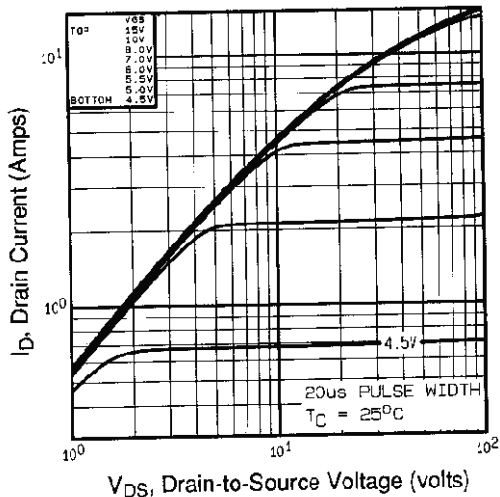
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0$, $I_D = 250\text{ }\mu\text{A}$	600	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^{\circ}\text{C}$, $I_D = 1\text{ mA}^c$	-	0.62	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 600\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	100	μA
		$V_{DS} = 480\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^{\circ}\text{C}$	-	-	500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 2.2\text{ A}^b$	-	-	2.2	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}$, $I_D = 2.2\text{ A}^c$	2.5	-	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1.0\text{ MHz}$, see fig. 5 ^c	-	660	-	pF
Output Capacitance	C_{oss}		-	86	-	
Reverse Transfer Capacitance	C_{rss}		-	19	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$, $I_D = 3.6\text{ A}$, $V_{DS} = 360\text{ V}$, see fig. 6 and 13 ^{b, c}	-	-	31	nC
Gate-Source Charge	Q_{gs}		-	-	4.6	
Gate-Drain Charge	Q_{gd}		-	-	17	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 300\text{ V}$, $I_D = 3.6\text{ A}$, $R_g = 12\text{ }\Omega$, $R_D = 82\text{ }\Omega$, see fig. 10 ^{b, c}	-	11	-	ns
Rise Time	t_r		-	13	-	
Turn-Off Delay Time	$t_{d(off)}$		-	35	-	
Fall Time	t_f		-	14	-	
Internal Source Inductance	L_S	Between lead, and center of die contact	-	7.5	-	nH
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	3.6	A
Pulsed Diode Forward Current ^a	I_{SM}		-	-	14	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_S = 3.6\text{ A}$, $V_{GS} = 0\text{ V}^b$	-	-	1.6	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_F = 3.6\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}^b, c$	-	370	810	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	2.0	4.2	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
c. Uses IRFBC30, SiHFBC30 data and test conditions.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



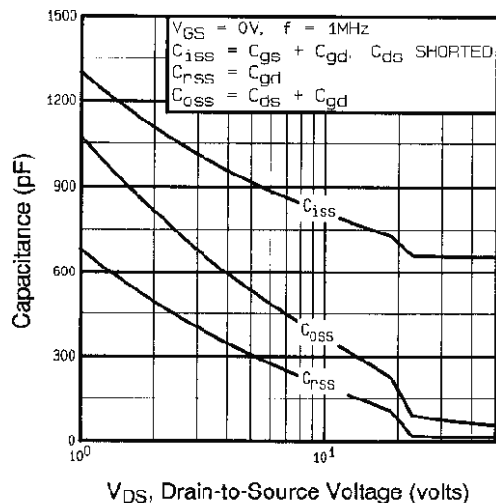


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

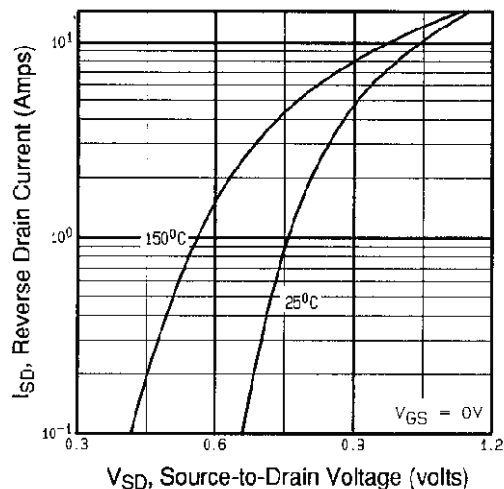


Fig. 7 - Typical Source-Drain Diode Forward Voltage

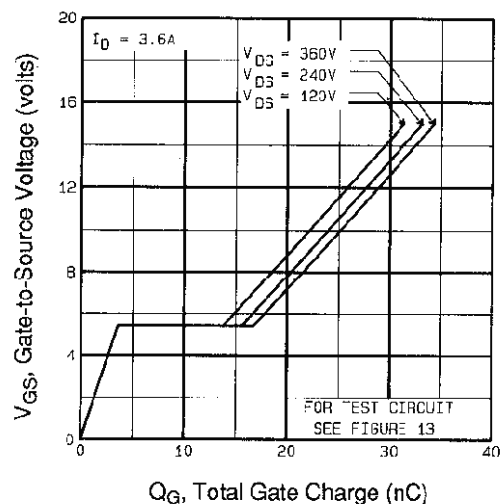


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

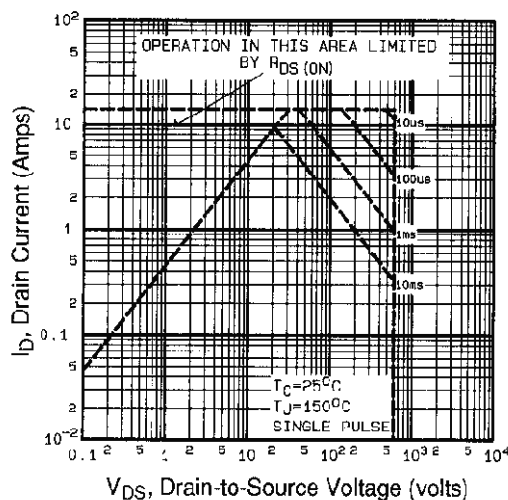


Fig. 8 - Maximum Safe Operating Area

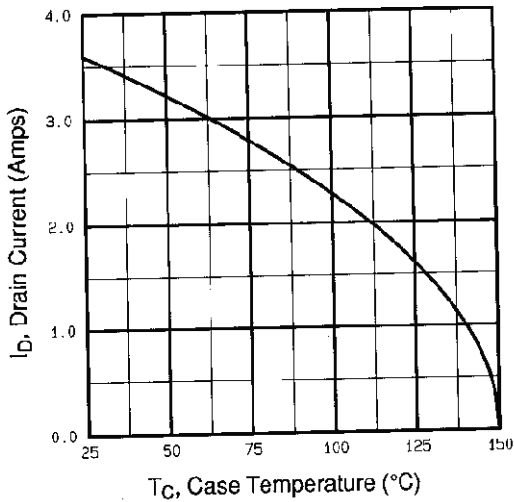


Fig. 9 - Maximum Drain Current vs. Case Temperature

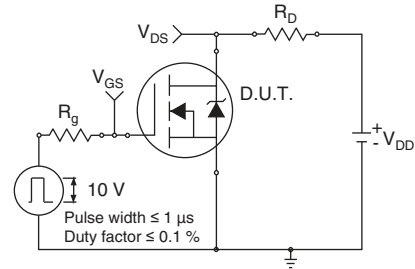


Fig. 10a - Switching Time Test Circuit

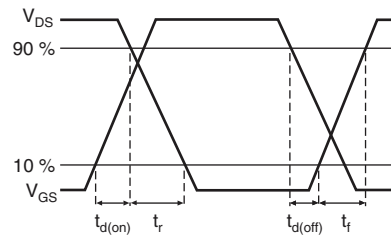


Fig. 10b - Switching Time Waveforms

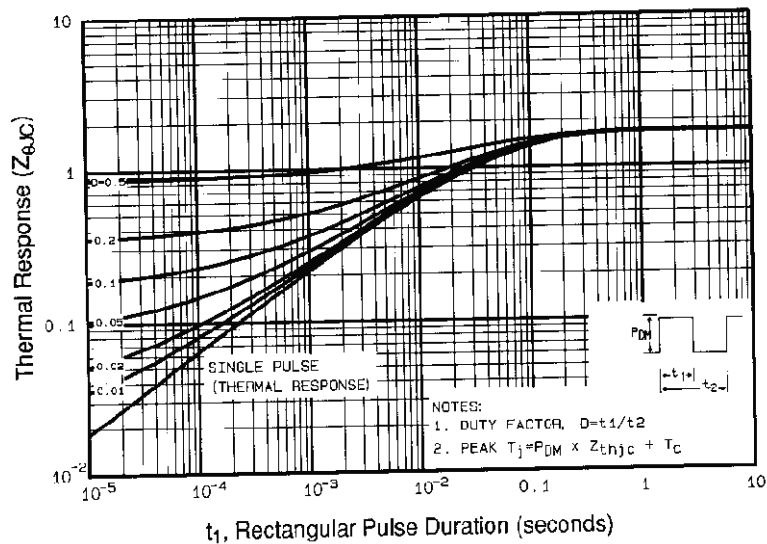


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

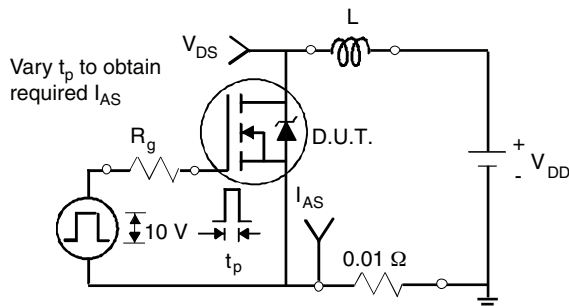


Fig. 12a - Unclamped Inductive Test Circuit

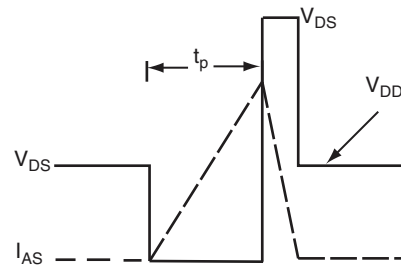


Fig. 12b - Unclamped Inductive Waveforms

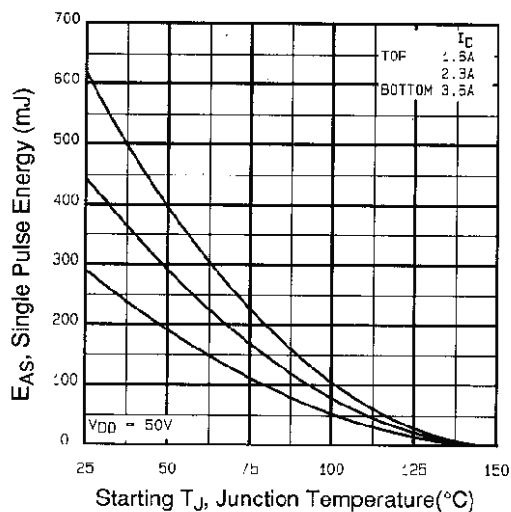


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

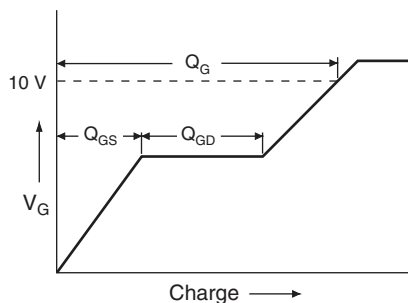


Fig. 13a - Maximum Avalanche Energy vs. Drain Current

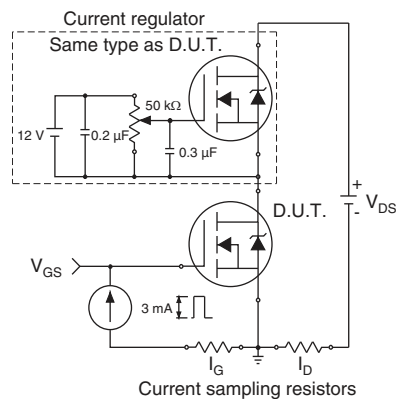
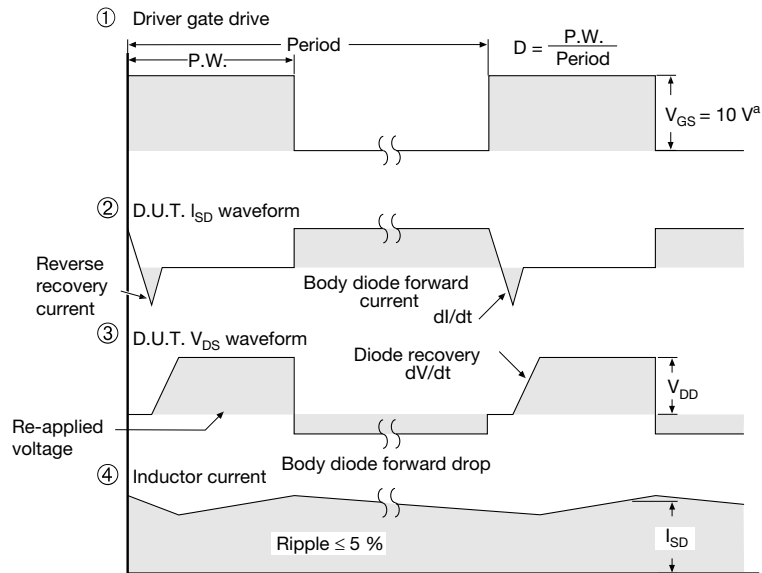
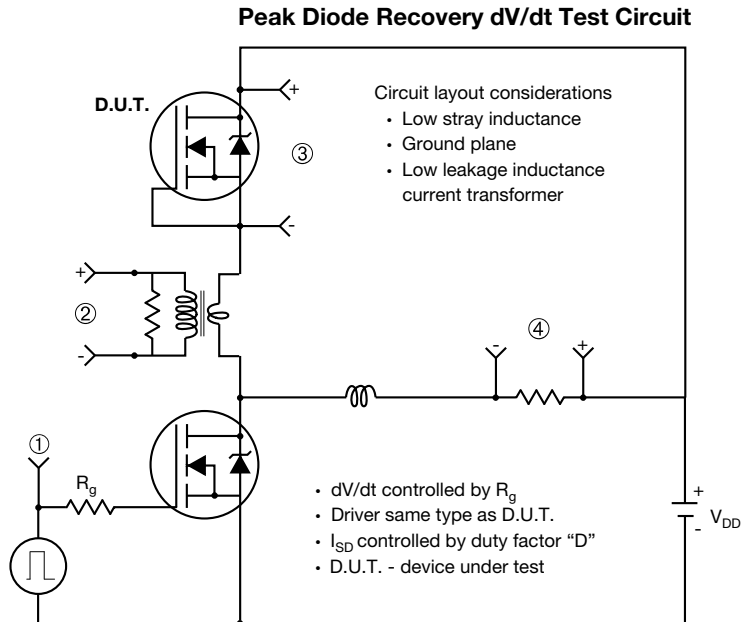


Fig. 13b - Gate Charge Test Circuit



Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

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	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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