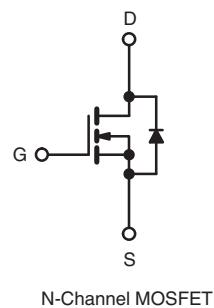
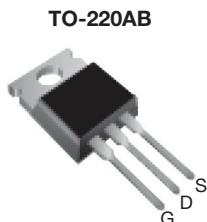


Power MOSFET

PRODUCT SUMMARY	
V _{DS} (V)	600
R _{DS(on)} (Ω)	V _{GS} = 10 V 1.2
Q _g (Max.) (nC)	60
Q _{gs} (nC)	8.3
Q _{gd} (nC)	30
Configuration	Single



FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC



RoHS*
COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free	IRFBC40PbF SiHFBC40-E3
SnPb	IRFBC40 SiHFBC40

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	600	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current	I _D	6.2	A
		3.9	
Pulsed Drain Current ^a	I _{DM}	25	
Linear Derating Factor		1.0	W/°C
Single Pulse Avalanche Energy ^b	E _{AS}	570	μJ
Repetitive Avalanche Current ^a	I _{AR}	6.2	A
Repetitive Avalanche Energy ^a	E _{AR}	13	μJ
Maximum Power Dissipation	P _D	125	W
Peak Diode Recovery dV/dt ^c	dV/dt	3.0	V/ns
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	
Mounting Torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. V_{DD} = 50 V, starting T_J = 25 °C, L = 27 mH, R_g = 25 Ω, I_{AS} = 6.2 A (see fig. 12).

c. I_{SD} ≤ 6.2 A, dI/dt ≤ 80 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C.

d. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.0	

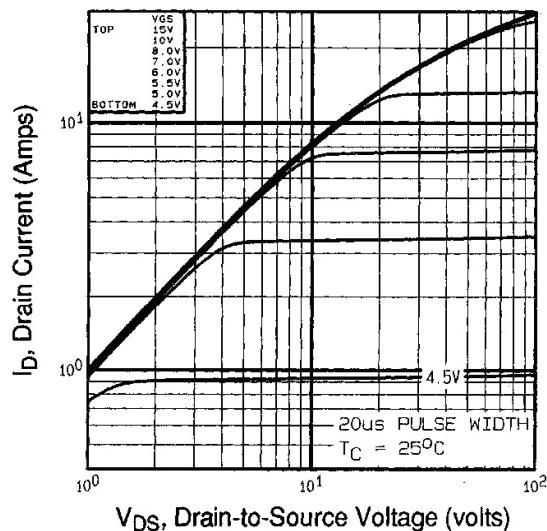
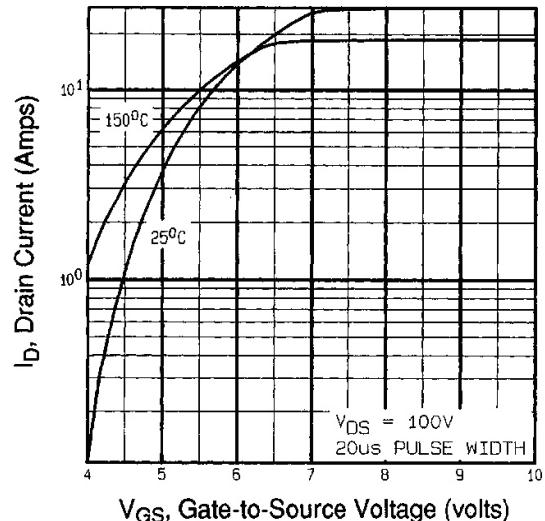
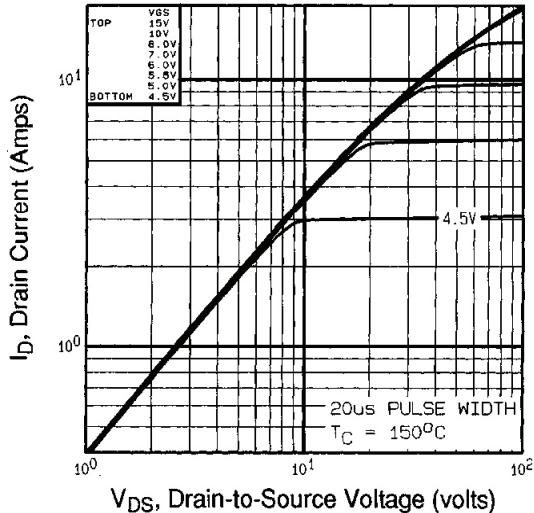
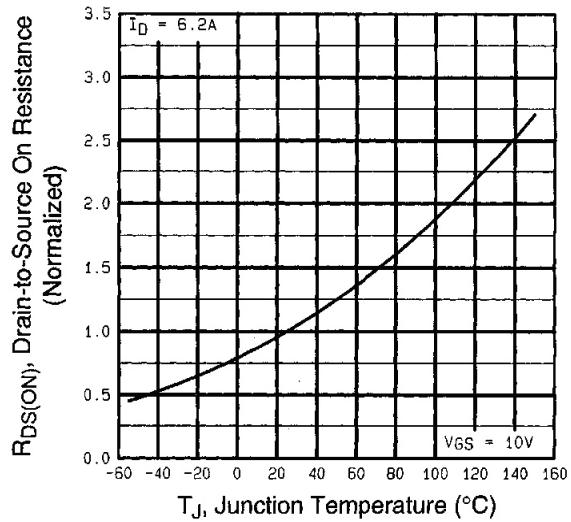
SPECIFICATIONS ($T_J = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0$ V, $I_D = 250$ μ A	600	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, $I_D = 1$ mA	-	0.7	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250$ μ A	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20$ V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 600$ V, $V_{GS} = 0$ V	-	-	100	μ A
		$V_{DS} = 480$ V, $V_{GS} = 0$ V, $T_J = 125$ °C	-	-	500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10$ V	$I_D = 3.7$ A ^b	-	-	1.2
Forward Transconductance	g_{fs}	$V_{DS} = 100$ V, $I_D = 3.7$ A ^b	4.7	-	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0$ V, $V_{DS} = 25$ V, $f = 1.0$ MHz, see fig. 5	-	1300	-	pF
Output Capacitance	C_{oss}		-	160	-	
Reverse Transfer Capacitance	C_{rss}		-	30	-	
Total Gate Charge	Q_g	$V_{GS} = 10$ V	$I_D = 6.2$ A, $V_{DS} = 360$ V, see fig. 6 and 13 ^b	-	-	60
Gate-Source Charge	Q_{gs}			-	-	8.3
Gate-Drain Charge	Q_{gd}			-	-	30
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 300$ V, $I_D = 6.2$ A, $R_g = 9.1$ Ω , $R_D = 47$ Ω , see fig. 10 ^b	-	13	-	ns
Rise Time	t_r		-	18	-	
Turn-Off Delay Time	$t_{d(off)}$		-	55	-	
Fall Time	t_f		-	20	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-
Internal Source Inductance	L_S			-	7.5	-
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	6.2
Pulsed Diode Forward Current ^a	I_{SM}			-	-	25
Body Diode Voltage	V_{SD}	$T_J = 25$ °C, $I_S = 6.2$ A, $V_{GS} = 0$ V ^b	-	-	1.5	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25$ °C, $I_F = 6.2$ A, $dl/dt = 100$ A/ μ s ^b	-	450	940	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	3.8	7.9	μ C
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width ≤ 300 μ s; duty cycle ≤ 2 %.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^{\circ}\text{C}$

Fig. 3 - Typical Transfer Characteristics

Fig. 2 - Typical Output Characteristics, $T_C = 150\text{ }^{\circ}\text{C}$

Fig. 4 - Normalized On-Resistance vs. Temperature

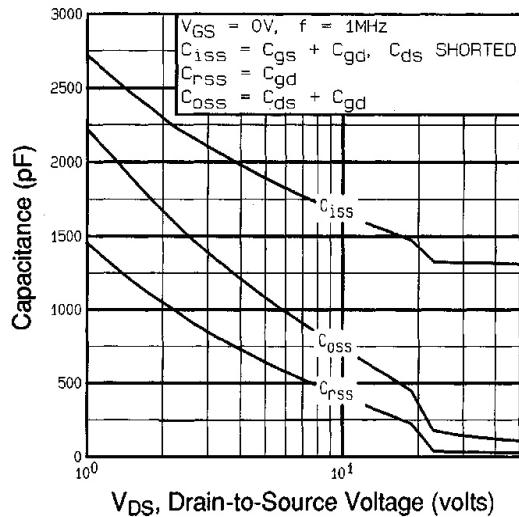


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

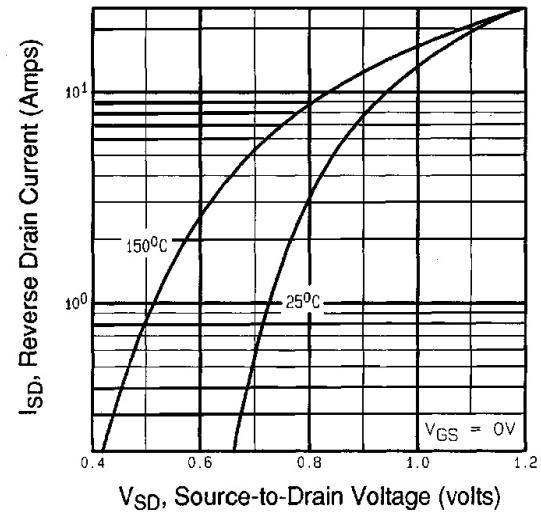


Fig. 7 - Typical Source-Drain Diode Forward Voltage

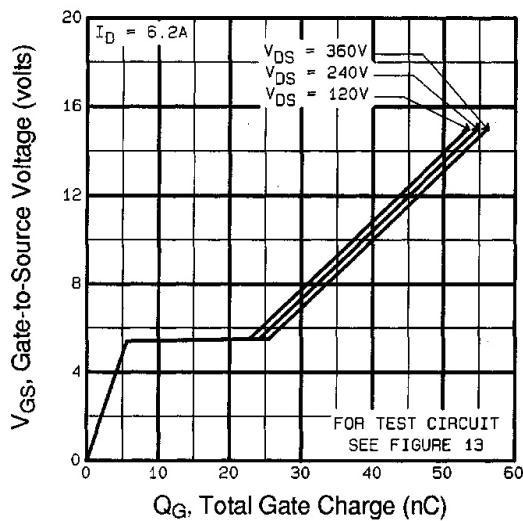


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

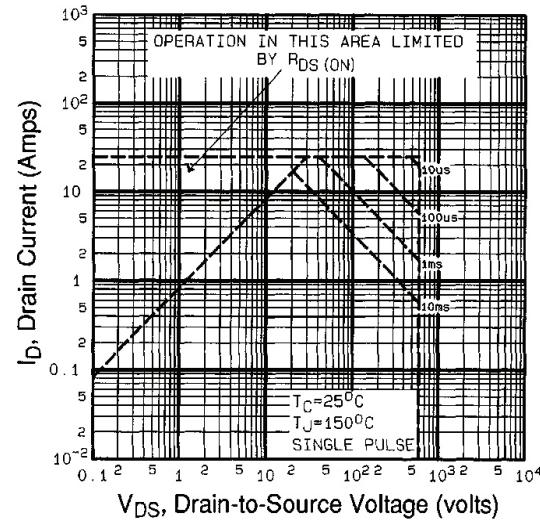
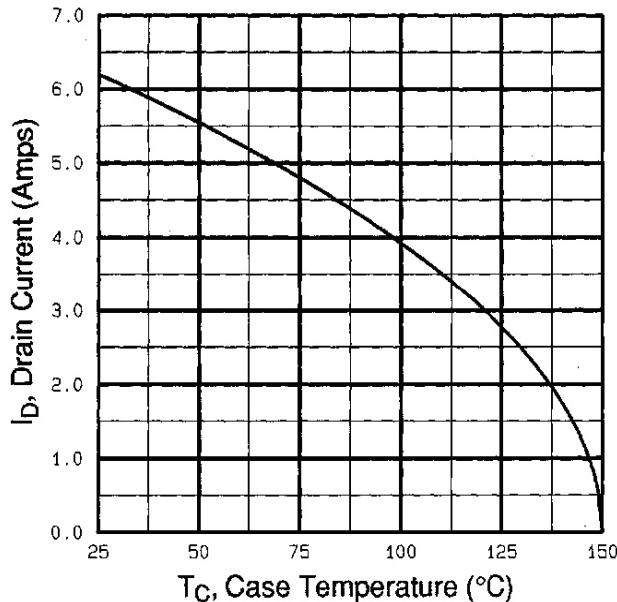
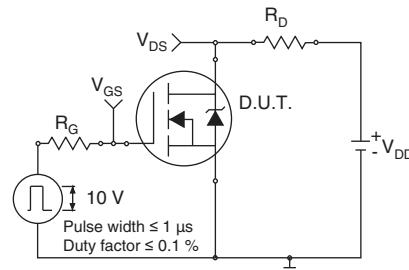
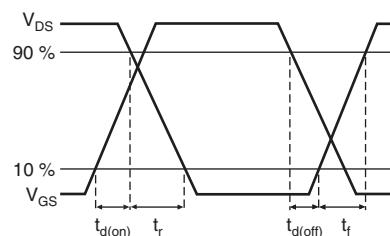
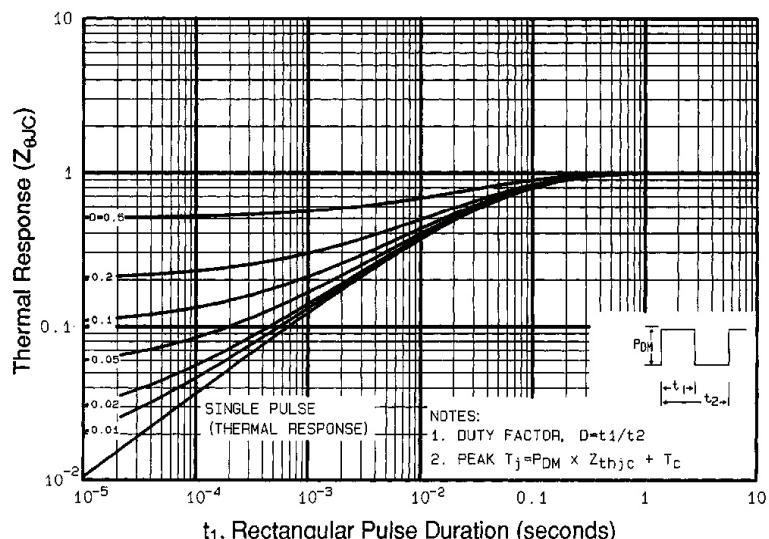


Fig. 8 - Maximum Safe Operating Area


Fig. 9 - Maximum Drain Current vs. Case Temperature

Fig. 10a - Switching Time Test Circuit

Fig. 10b - Switching Time Waveforms

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

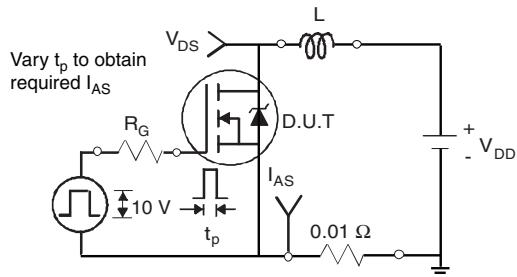


Fig. 12a - Unclamped Inductive Test Circuit

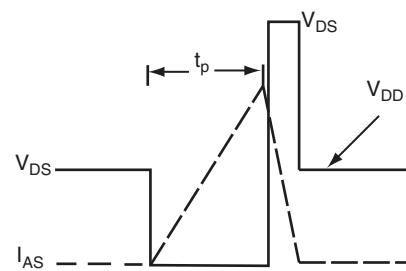


Fig. 12b - Unclamped Inductive Waveforms

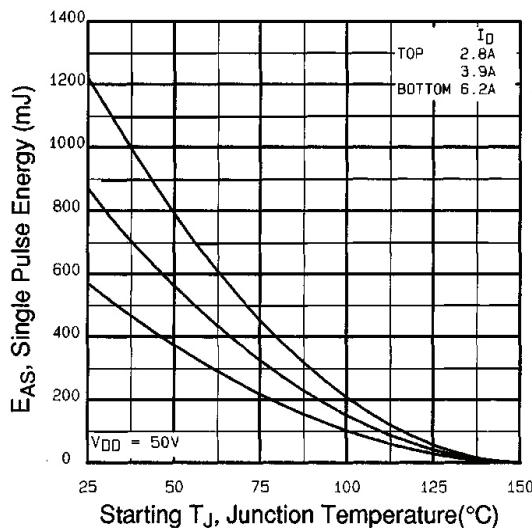


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

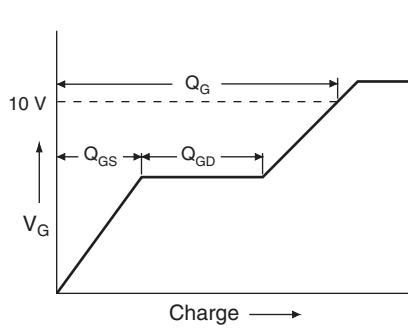


Fig. 13a - Basic Gate Charge Waveform

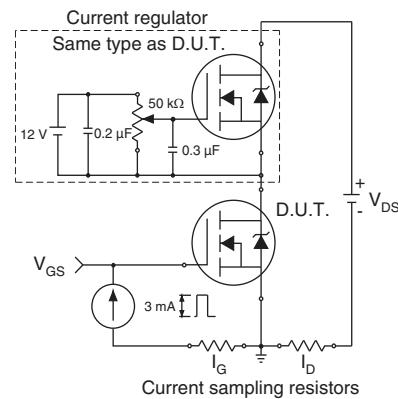
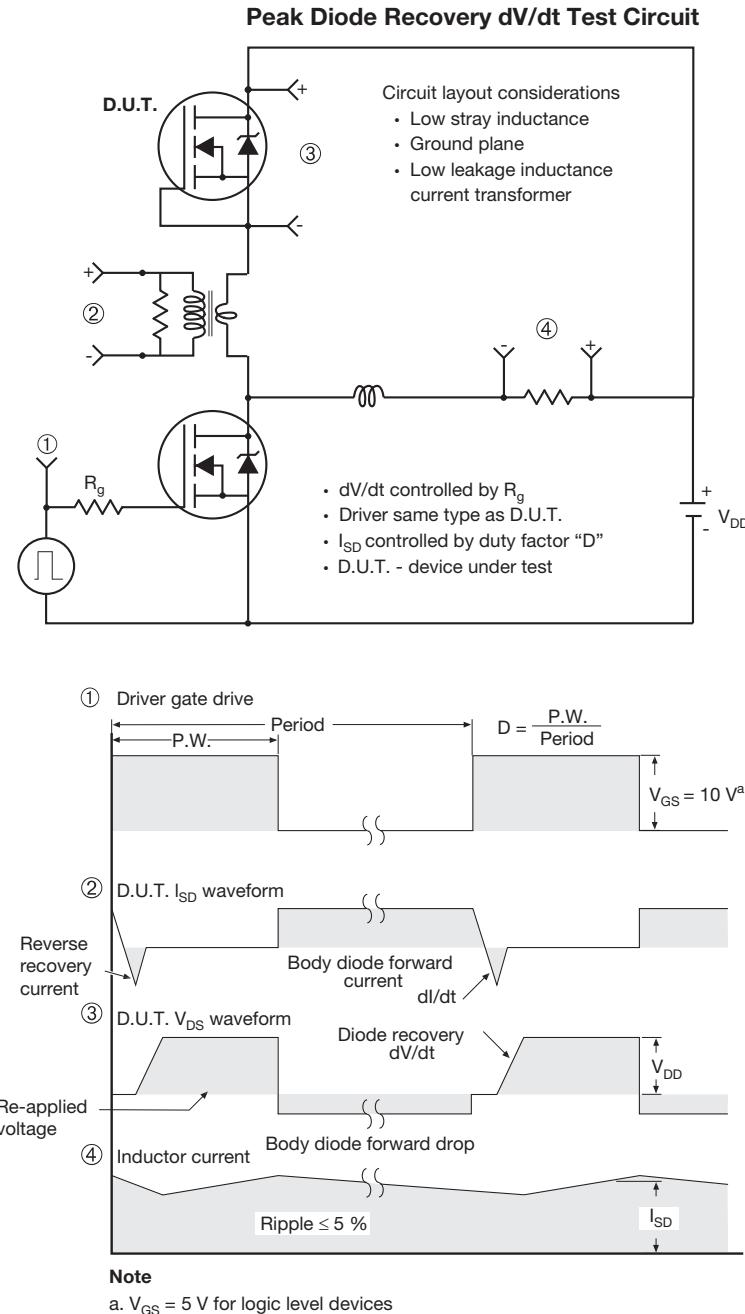
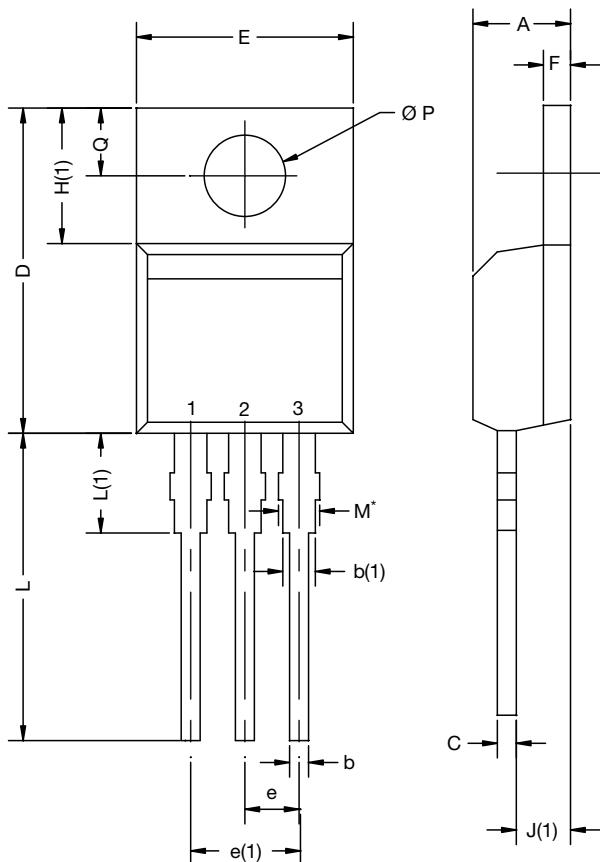


Fig. 13b - Gate Charge Test Circuit


Fig. 14 - For N-Channel

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TO-220-1



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.24	4.65	0.167	0.183
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.78	0.045	0.070
c	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
E	9.96	10.52	0.392	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.10	6.71	0.240	0.264
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
Ø P	3.53	3.94	0.139	0.155
Q	2.54	3.00	0.100	0.118

ECN: X15-0364-Rev. C, 14-Dec-15
DWG: 6031

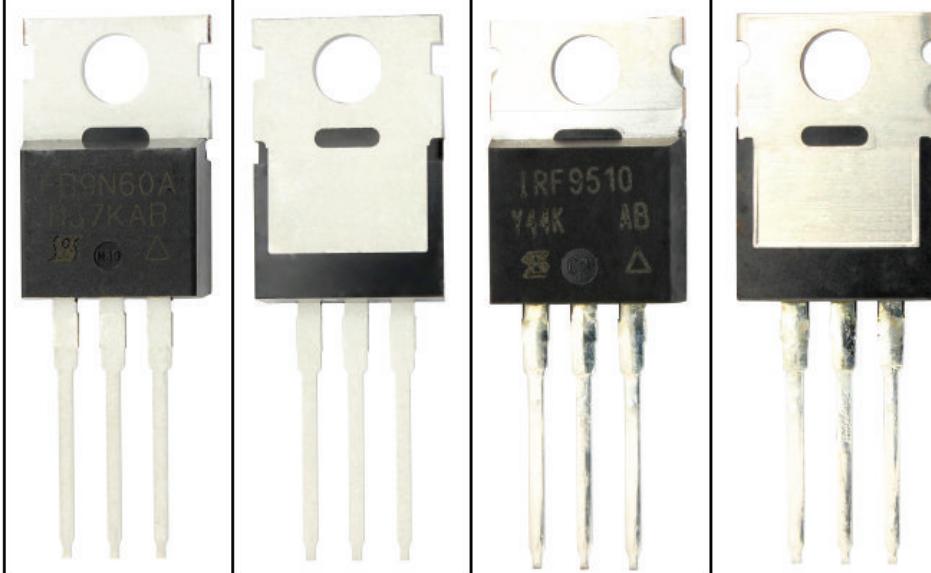
Note

- $M^* = 0.052$ inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM

Package Picture

ASE

Xi'an



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