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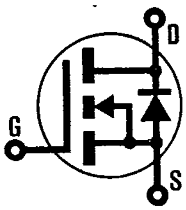
INTERNATIONAL RECTIFIER
T-37-25
Data Sheet No. PD-9.464A

INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS IRFD010 IRFD012

N-CHANNEL HEXDIP™

1-WATT RATED POWER MOSFETs
IN A 4-PIN, DUAL-IN-LINE PACKAGE



4-PIN DIP

50 Volt, 0.20 Ohm, 1-Watt HEXDIP

HEXFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. Efficient geometry and unique processing of the HEXFET design achieve a very low on-state resistance combined with high transconductance and great device ruggedness. HEXFETs feature all of the established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

The HEXDIP 4-pin, Dual-In-Line Package brings the advantages of HEXFETs to high volume applications where automatic PC Board insertion is desirable, such as circuit boards for computers, printers, telecommunications equipment and consumer products. Their compatibility with automatic insertion equipment, low-profile and end-stackable features represent the state-of-the-art in power device packaging

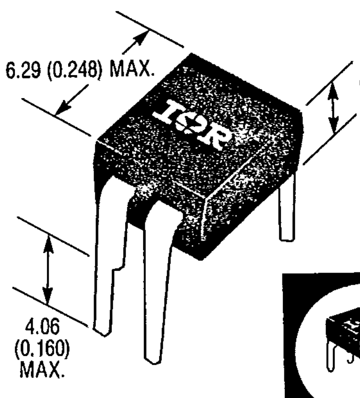
Features

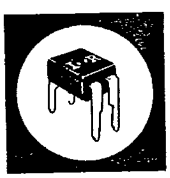
- For Automatic Insertion
- Compact, End Stackable
- Fast Switching
- Low Drive Current
- Easily Paralleled
- Excellent Temperature Stability

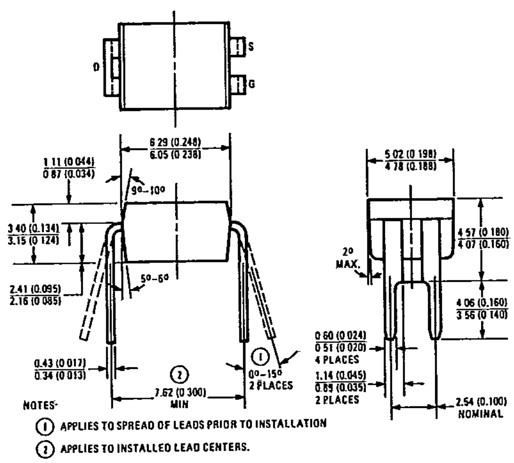
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFD010	50V	0.20Ω	1.7A
IRFD012	50V	0.30Ω	1.4A

CASE STYLE AND DIMENSIONS







Case Style HD-1 (Similar to JEDEC Outline MO-001AN)
Dimensions in Millimeters and (Inches)

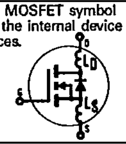
IRFD010, IRFD012 Devices

T-37-25

Absolute Maximum Ratings

	Parameter	IRFD010	IRFD012	Units
V_{DS}	Drain - Source Voltage ①	50	50	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	50	50	V
I_D @ T_C = 25°C	Continuous Drain Current	1.7	1.4	A
I_D @ T_C = 100°C	Continuous Drain Current	1.1	0.86	A
I_{DM}	Pulsed Drain Current ②	14	11	A
V_{GS}	Gate - Source Voltage	±20		V
P_D @ T_C = 25°C	Max. Power Dissipation	1		W
	Linear Derating Factor	0.0082		W/K⑤
I_{LM}	Inductive Current, Clamped	14 (See Fig. 14) L = 100μH	11	A
I_L	Unclamped Inductive Current (Avalanche Current) ③	(See Fig. 15) 1.5		A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150		°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)		°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFD010	50	–	–	V	V_{GS} = 0V
		IRFD012	50	–	–	V	I_D = 250 μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250 μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	−500	nA	V_{GS} = −20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating × 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ④	IRFD010	1.7	–	–	A	V_{DS} > $I_{D(on)}$ × $R_{DS(on)max.}$, V_{GS} = 10V
		IRFD012	1.4	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ④	IRFD010	–	0.16	0.20	Ω	V_{GS} = 10V, I_D = 0.86A
		IRFD012	–	0.20	0.30	Ω	
g_{fs}	Forward Transconductance ④	ALL	2.1	3.2	–	S(℧)	V_{DS} = 2 × V_{GS}, I_{DS} = 3.6A
C_{iss}	Input Capacitance	ALL	–	250	–	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	ALL	–	150	–	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	ALL	–	29	–	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	11	17	ns	V_{DD} = 25V, I_D ≈ 7.2A, R_G = 25Ω, R_D = 3.3Ω
t_r	Rise Time	ALL	–	33	50	ns	See Fig. 16
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	12	18	ns	(MOSFET switching times are essentially independent of
t_f	Fall Time	ALL	–	23	35	ns	operating temperature.)
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	8.8	13	nC	V_{GS} = 10V, I_D = 7.2A, V_{DS} = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially
Q_{gs}	Gate-Source Charge	ALL	–	2.2	3.3	nC	independent of operating temperature.)
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	2.6	3.9	nC	
L_D	Internal Drain Inductance	ALL	–	4.0	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die. Modified MOSFET symbol showing the internal device inductances. 
L_S	Internal Source Inductance	ALL	–	6.0	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Thermal Resistance

R_{thJA}	Junction-to-Ambient	ALL	–	–	120	K/W ⑤	Typical socket mount

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFD010	—	—	1.7	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRFD012	—	—	1.4	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFD010	—	—	14	A	
		IRFD012	—	—	11	A	
V_{SD}	Diode Forward Voltage ②	ALL	—	—	1.6	V	T_C = 25°C, I_S = 1.7A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	41	86	190	ns	T_J = 25°C, I_F = 7.2A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	0.15	0.33	0.78	μC	T_J = 25°C, I_F = 7.2A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C ② Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5). ③ @ V_{dd} = 25V, T_j = 25°C, L = 100 μH, R_G = 25Ω ④ Pulse Test: Pulse width ≤ 300 μs, Duty Cycle ≤ 2%
⑤ K/W = °C/W, W/K = W/°C

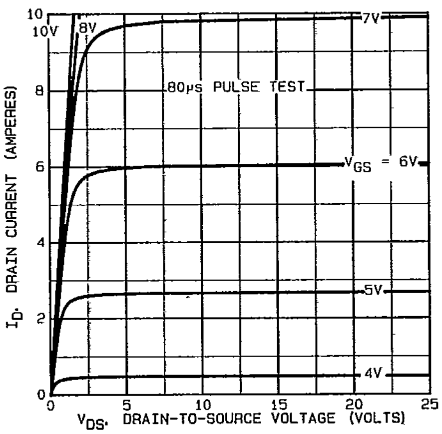


Fig. 1 — Typical Output Characteristics

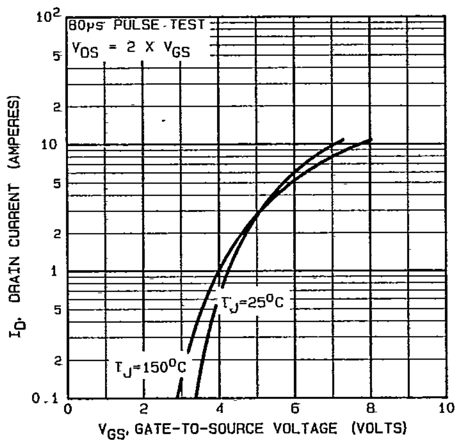


Fig. 2 — Typical Transfer Characteristics

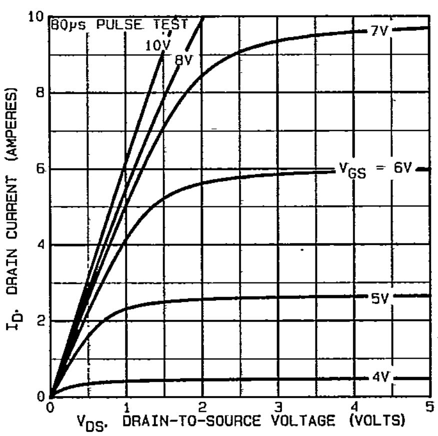


Fig. 3 — Typical Saturation Characteristics

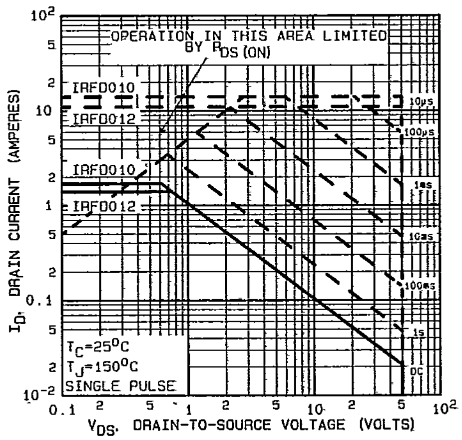


Fig. 4 — Maximum Safe Operating Area

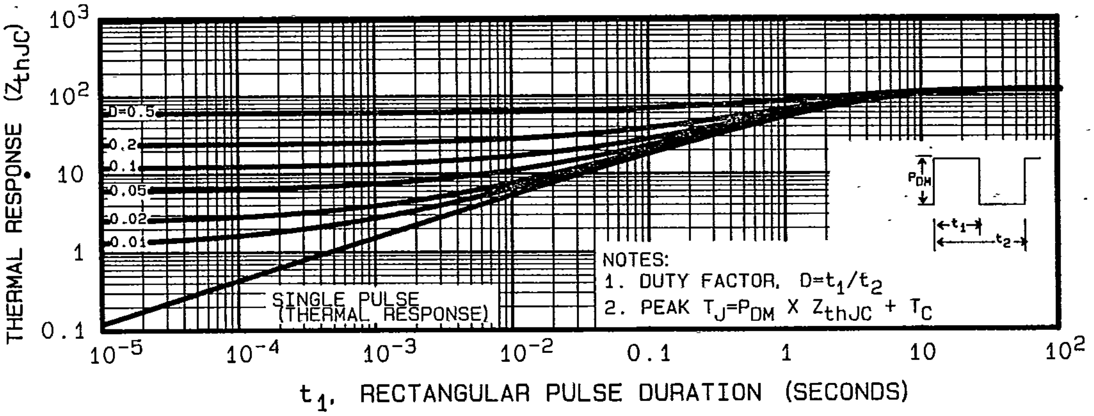


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

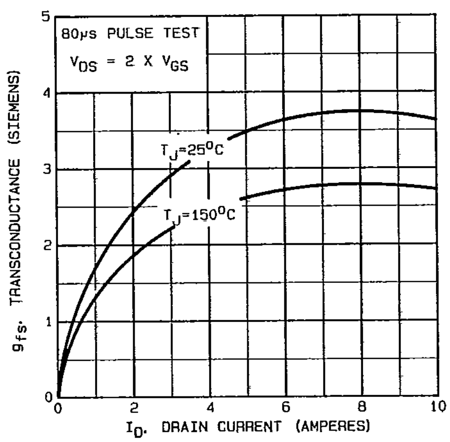


Fig. 6 — Typical Transconductance Vs. Drain Current

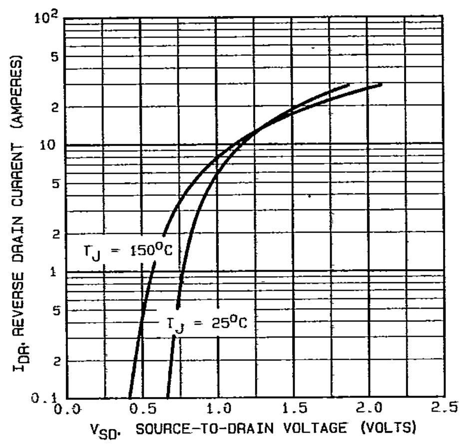


Fig. 7 — Typical Source-Drain Diode Forward Voltage

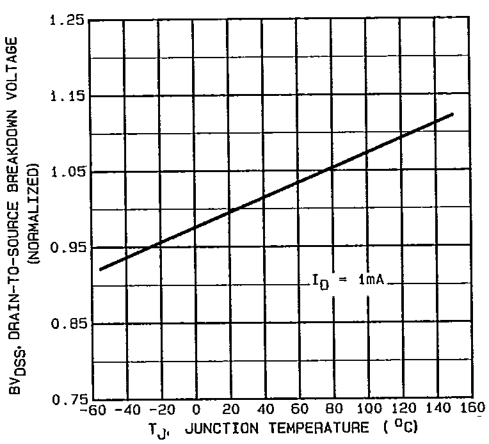


Fig. 8 — Breakdown Voltage Vs. Temperature

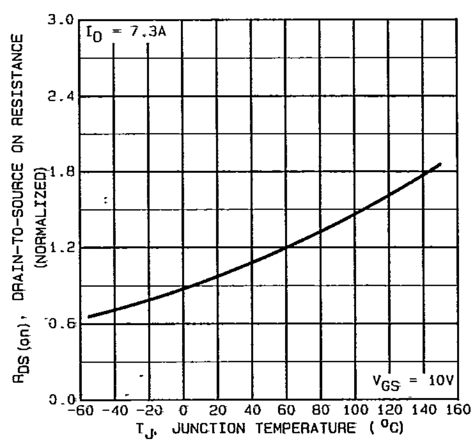


Fig. 9 — Normalized On-Resistance Vs. Temperature

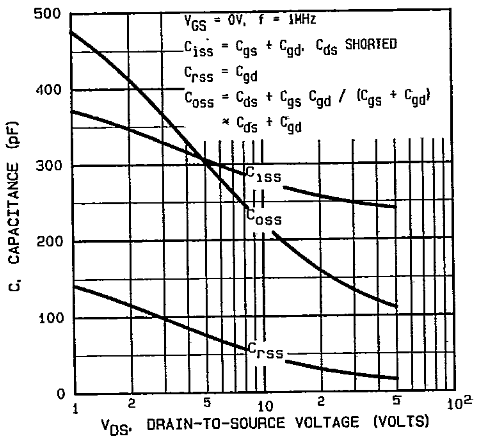


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

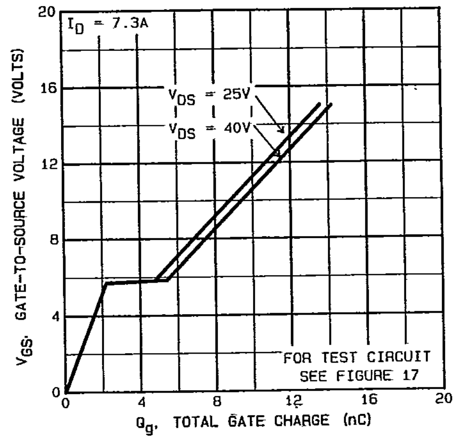


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

4-PIN DIP

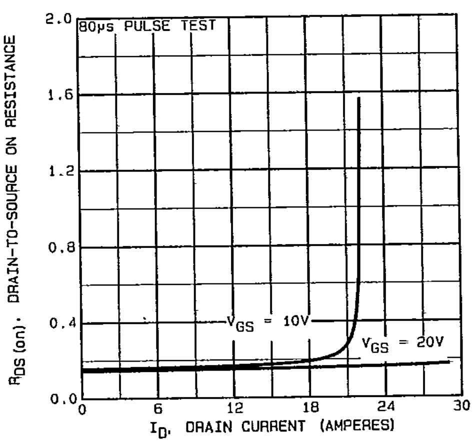


Fig. 12 — Typical On-Resistance Vs. Drain Current

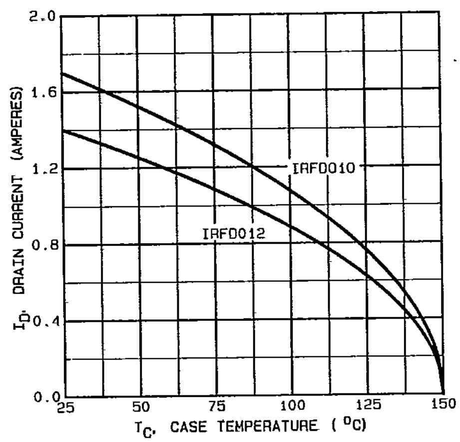


Fig. 13 — Maximum Drain Current Vs. Case Temperature

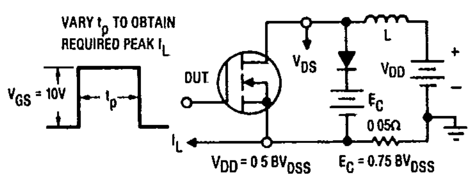


Fig. 14a — Clamped Inductive Test Circuit

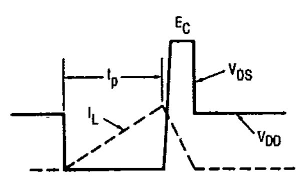


Fig. 14b — Clamped Inductive Waveforms

IRFD010, IRFD012 Devices

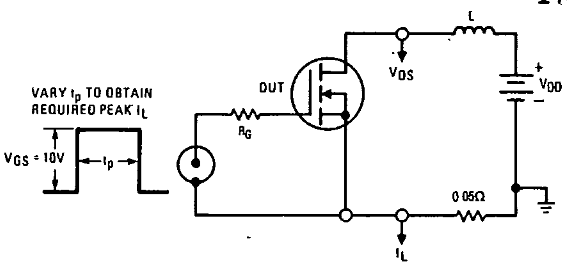


Fig. 15a — Unclamped Inductive Test Circuit

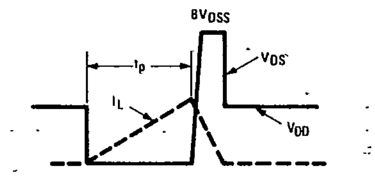


Fig 15b. — Unclamped Inductive Load Test Waveforms

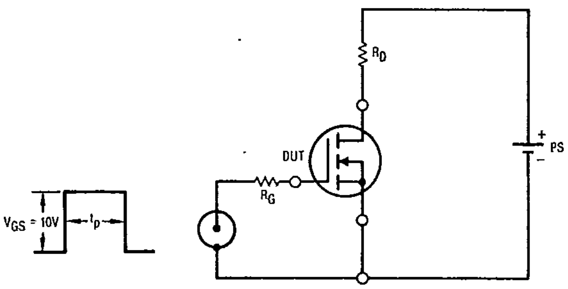


Fig. 16 — Switching Time Test Circuit

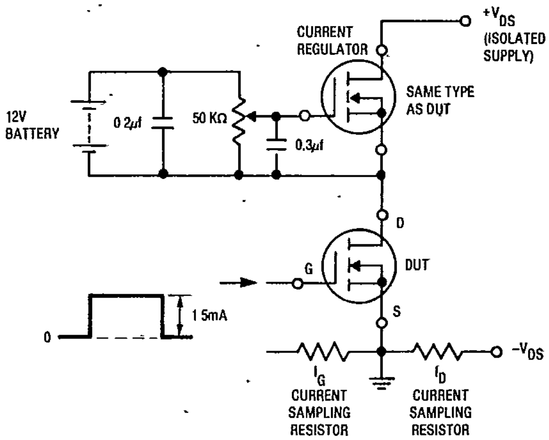


Fig. 17 — Gate Charge Test Circuit

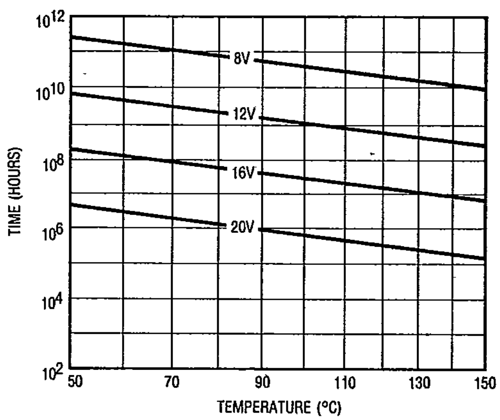


***Fig. 18 — Typical Time to Accumulated 1% Gate Failure**

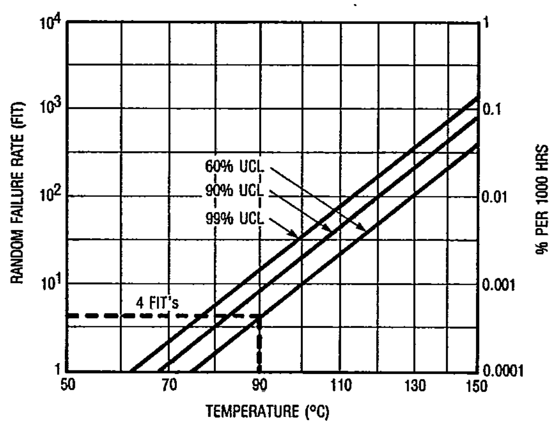


***Fig. 19 — Typical High Temperature Reverse Bias (HTRB) Failure Rate**

*The data shown is correct as of April 15, 1987. This information is updated on a quarterly basis; for the latest reliability data, please contact your local IR field office.