

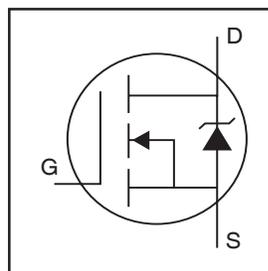
**PDP SWITCH**

**IRFI4228PbF**

**Features**

- Advanced Process Technology
- Key Parameters Optimized for PDP Sustain, Energy Recovery and Pass Switch Applications
- Low  $E_{PULSE}$  Rating to Reduce Power Dissipation in PDP Sustain, Energy Recovery and Pass Switch Applications
- Low  $Q_G$  for Fast Response
- High Repetitive Peak Current Capability for Reliable Operation
- Short Fall & Rise Times for Fast Switching
- 150°C Operating Junction Temperature for Improved Ruggedness
- Repetitive Avalanche Capability for Robustness and Reliability

Key Parameters		
$V_{DS\ max}$	150	V
$V_{DS\ (Avalanche)\ typ.}$	180	V
$R_{DS(ON)\ typ.\ @\ 10V}$	12.2	mΩ
$I_{RP\ max\ @\ T_C = 100^\circ C}$	61	A
$T_J\ max$	150	°C



G	D	S
Gate	Drain	Source

**Description**

This HEXFET® Power MOSFET is specifically designed for Sustain; Energy Recovery & Pass switch applications in Plasma Display Panels. This MOSFET utilizes the latest processing techniques to achieve low on-resistance per silicon area and low  $E_{PULSE}$  rating. Additional features of this MOSFET are 150°C operating junction temperature and high repetitive peak current capability. These features combine to make this MOSFET a highly efficient, robust and reliable device for PDP driving applications.

**Absolute Maximum Ratings**

	Parameter	Max.	Units
$V_{GS}$	Gate-to-Source Voltage	±30	V
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	34	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	21	
$I_{DM}$	Pulsed Drain Current ①	130	
$I_{RP} @ T_C = 100^\circ C$	Repetitive Peak Current ②	61	
$P_D @ T_C = 25^\circ C$	Power Dissipation	46	W
$P_D @ T_C = 100^\circ C$	Power Dissipation	18	
	Linear Derating Factor	0.37	W/°C
$T_J$	Operating Junction and Storage Temperature Range	-40 to +150	°C
$T_{STG}$			
	Soldering Temperature for 10 seconds	300	
	Mounting Torque, 6-32 or M3 Screw	10lb·in (1.1N·m)	N

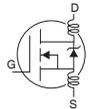
**Thermal Resistance**

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ④	—	2.73	°C/W
$R_{\theta JA}$	Junction-to-Ambient ④	—	65	

Notes ① through ⑤ are on page 8

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	150	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	190	—	mV/°C	Reference to $25^\circ\text{C}, I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	12.2	16	mΩ	$V_{GS} = 10V, I_D = 20A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-12	—	mV/°C	
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 150V, V_{GS} = 0V$
		—	—	1.0	mA	$V_{DS} = 150V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100	nA	$V_{GS} = -20V$
$g_{fs}$	Forward Transconductance	64	—	—	S	$V_{DS} = 25V, I_D = 20A$
$Q_g$	Total Gate Charge	—	73	110	nC	$V_{DD} = 75V, I_D = 20A, V_{GS} = 10V$ ③
$Q_{gd}$	Gate-to-Drain Charge	—	20	—	nC	
$t_{st}$	Shoot Through Blocking Time	100	—	—	ns	$V_{DD} = 120V, V_{GS} = 15V, R_G = 5.1\Omega$
$E_{PULSE}$	Energy per Pulse	—	62	—	μJ	$L = 220nH, C = 0.3\mu F, V_{GS} = 15V$ $V_{DS} = 120V, R_G = 5.1\Omega, T_J = 25^\circ\text{C}$
		—	110	—	μJ	$L = 220nH, C = 0.3\mu F, V_{GS} = 15V$ $V_{DS} = 120V, R_G = 5.1\Omega, T_J = 100^\circ\text{C}$
$C_{iss}$	Input Capacitance	—	4560	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	560	—		$V_{DS} = 25V$
$C_{riss}$	Reverse Transfer Capacitance	—	110	—		$f = 1.0MHz$
$C_{oss\ eff.}$	Effective Output Capacitance	—	460	—		$V_{GS} = 0V, V_{DS} = 0V\ to\ 120V$
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	7.5	—		

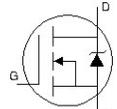


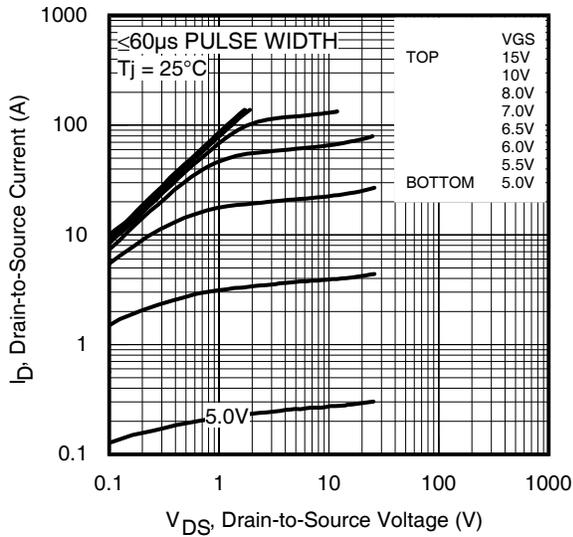
## Avalanche Characteristics

	Parameter	Typ.	Max.	Units
$E_{AS}$	Single Pulse Avalanche Energy ②	—	170	mJ
$E_{AR}$	Repetitive Avalanche Energy ①	—	4.6	mJ
$V_{DS(Avalanche)}$	Repetitive Avalanche Voltage ①	180	—	V
$I_{AS}$	Avalanche Current ②	—	20	A

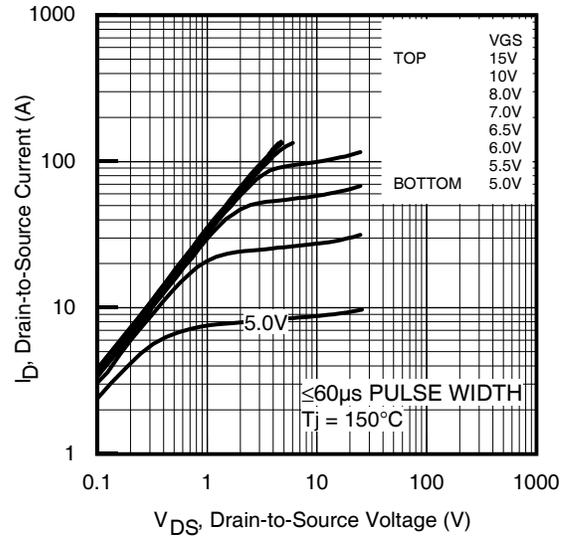
## Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S @ T_C = 25^\circ\text{C}$	Continuous Source Current (Body Diode)	—	—	34	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	130		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 20A, V_{GS} = 0V$ ③
$t_{rr}$	Reverse Recovery Time	—	74	110	ns	$T_J = 25^\circ\text{C}, I_F = 20A, V_{DD} = 50V$
$Q_{rr}$	Reverse Recovery Charge	—	230	350	nC	$di/dt = 100A/\mu s$ ③

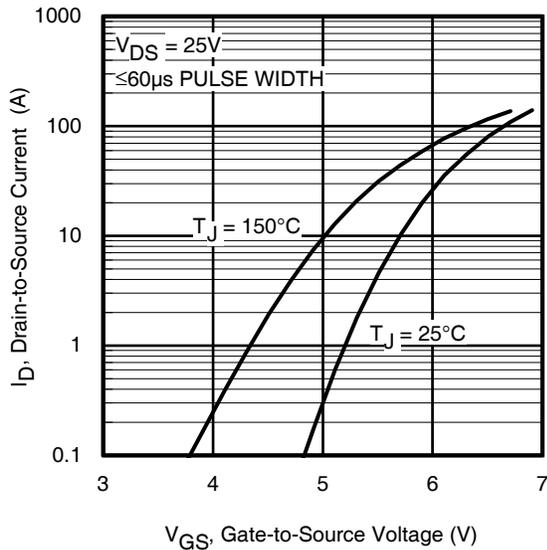




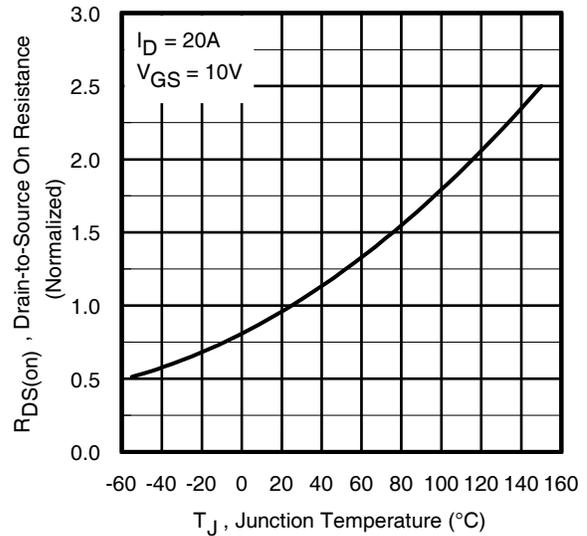
**Fig 1.** Typical Output Characteristics



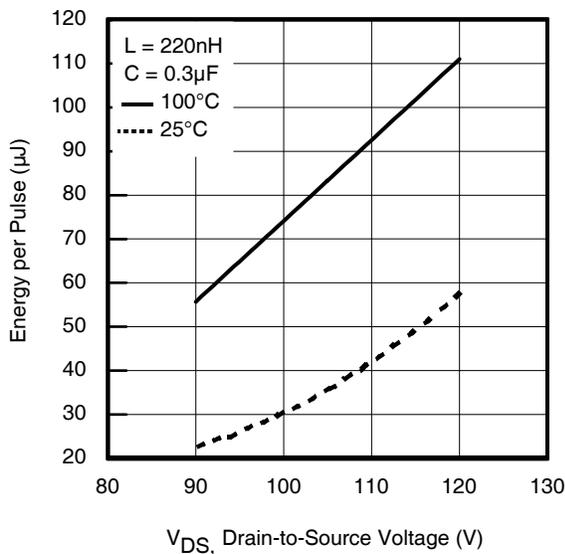
**Fig 2.** Typical Output Characteristics



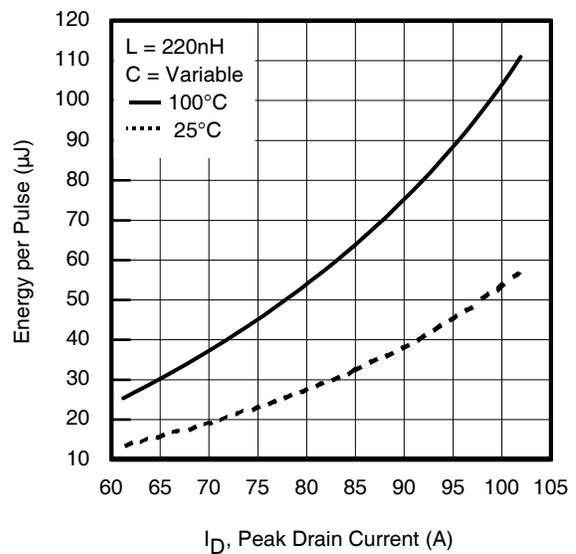
**Fig 3.** Typical Transfer Characteristics



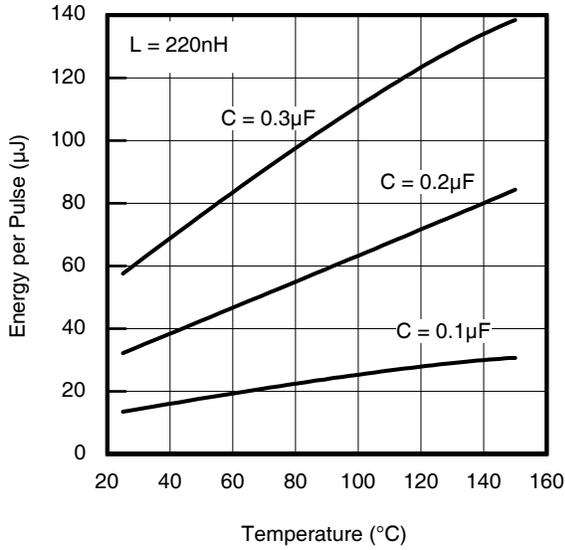
**Fig 4.** Normalized On-Resistance vs. Temperature



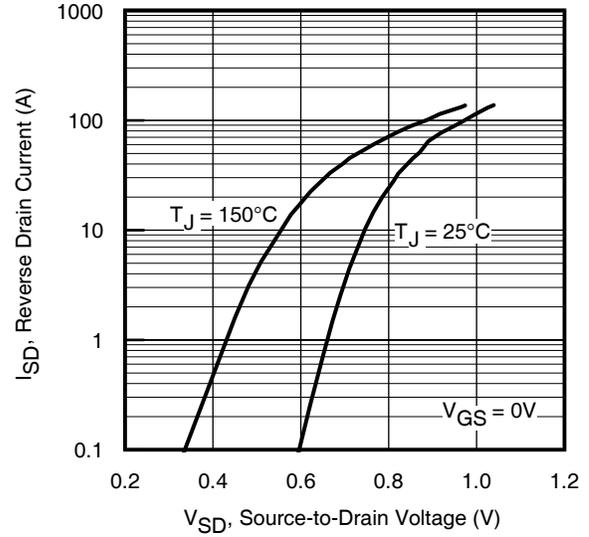
**Fig 5.** Typical  $E_{PULSE}$  vs. Drain-to-Source Voltage



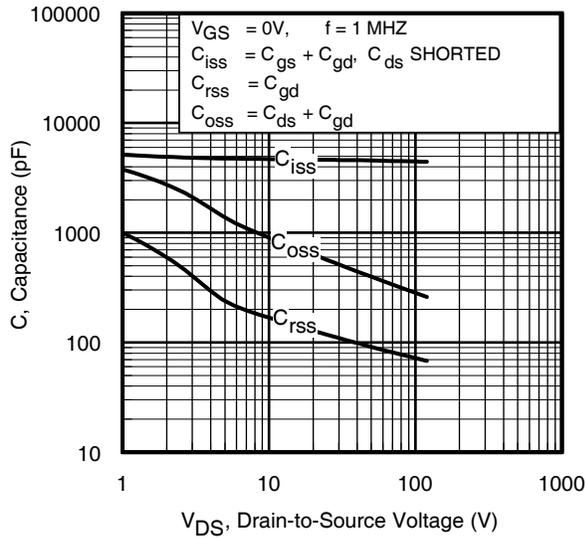
**Fig 6.** Typical  $E_{PULSE}$  vs. Drain Current



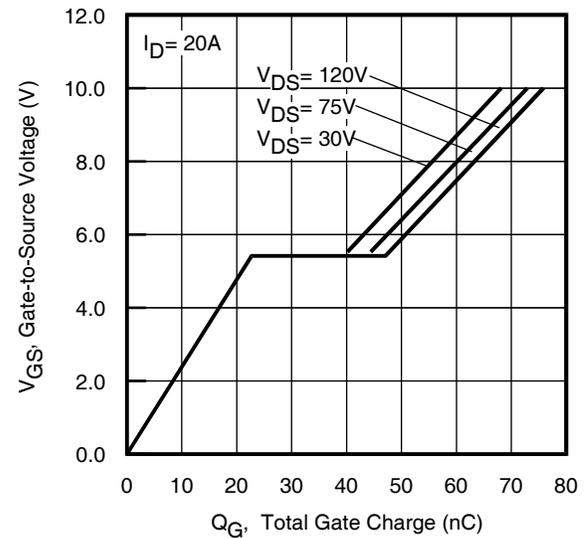
**Fig 7.** Typical  $E_{PULSE}$  vs. Temperature



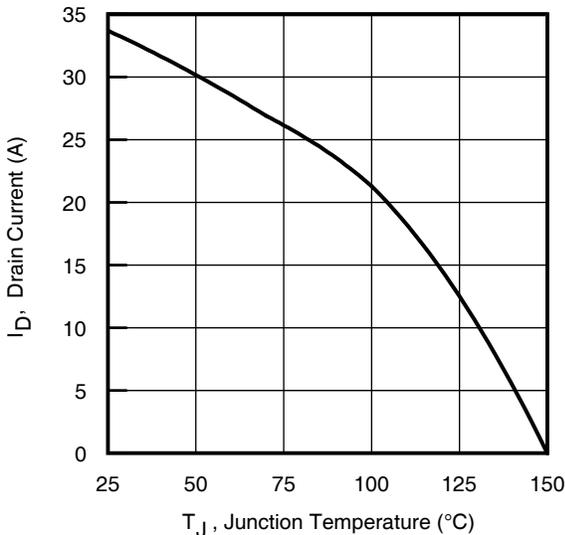
**Fig 8.** Typical Source-Drain Diode Forward Voltage



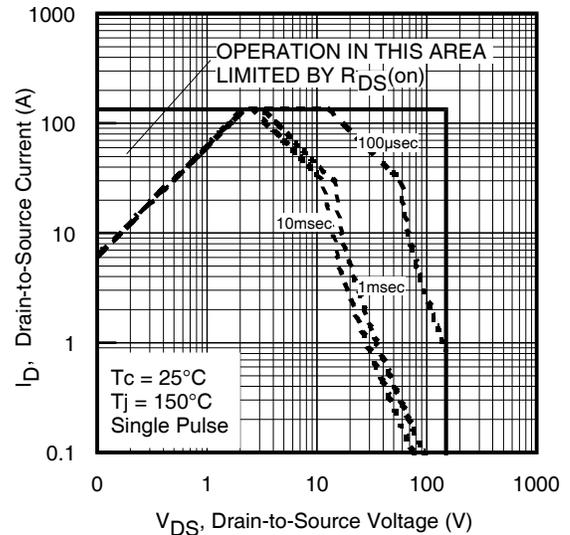
**Fig 9.** Typical Capacitance vs. Drain-to-Source Voltage



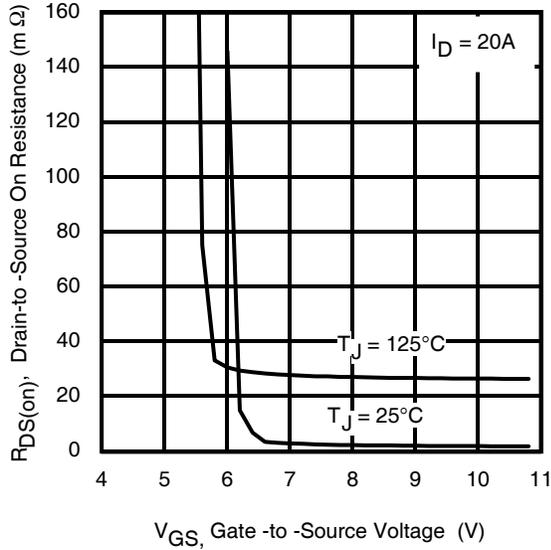
**Fig 10.** Typical Gate Charge vs. Gate-to-Source Voltage



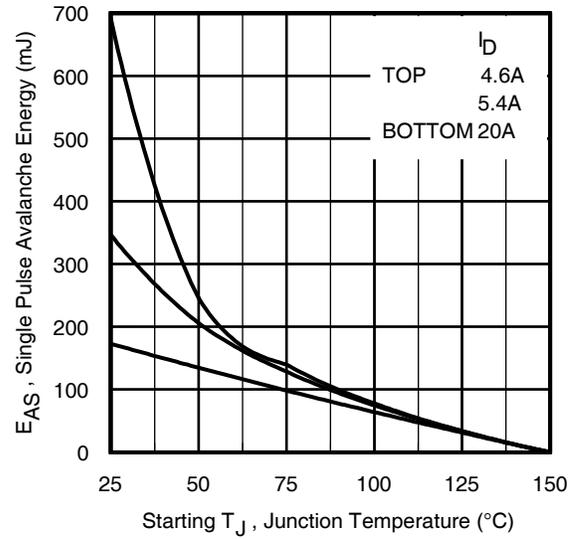
**Fig 11.** Maximum Drain Current vs. Case Temperature



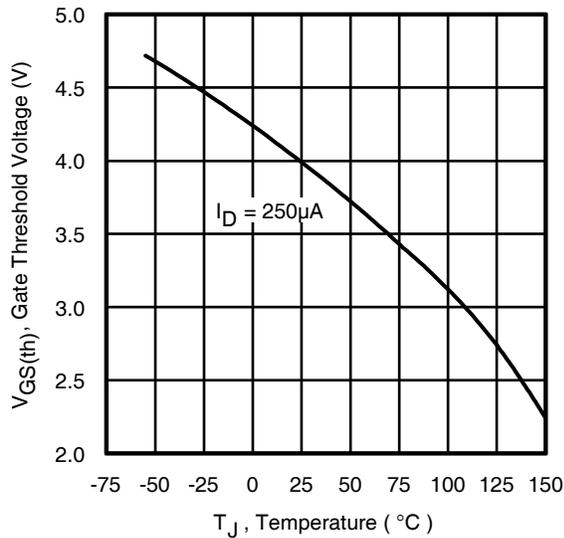
**Fig 12.** Maximum Safe Operating Area



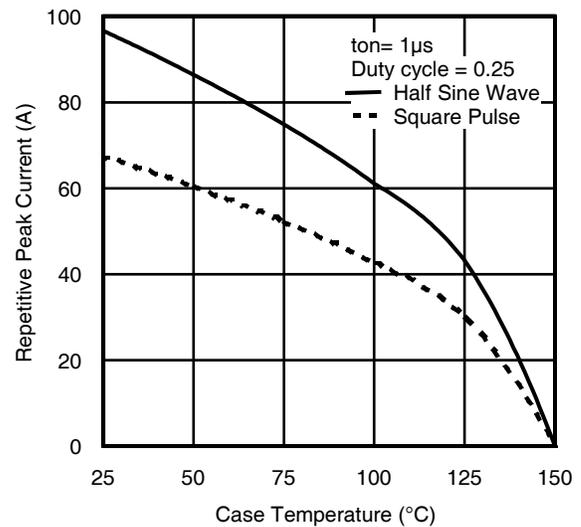
**Fig 13.** On-Resistance vs. Gate Voltage



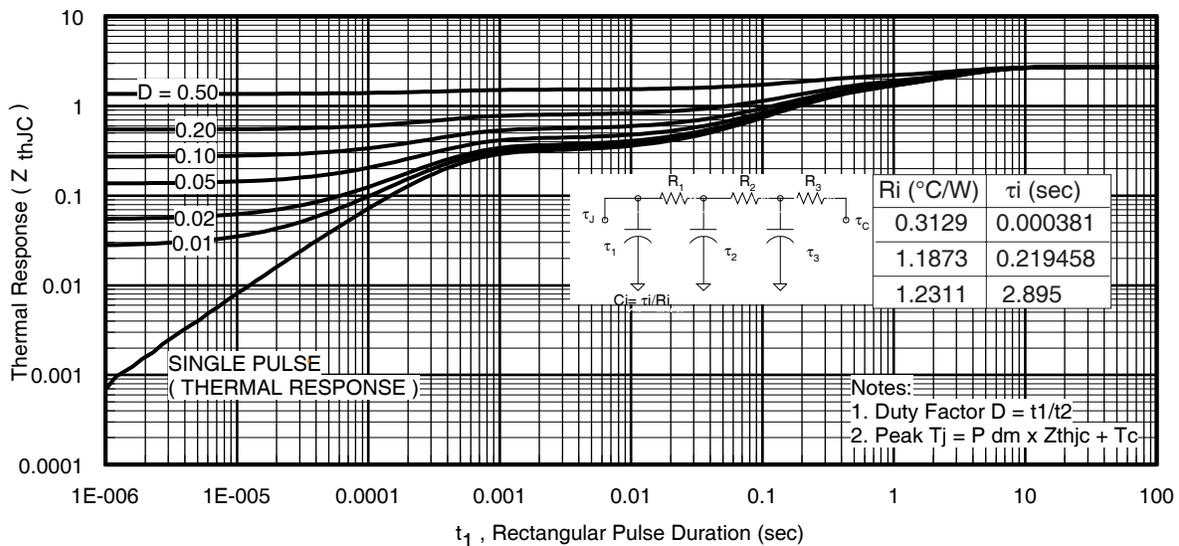
**Fig 14.** Maximum Avalanche Energy vs. Temperature



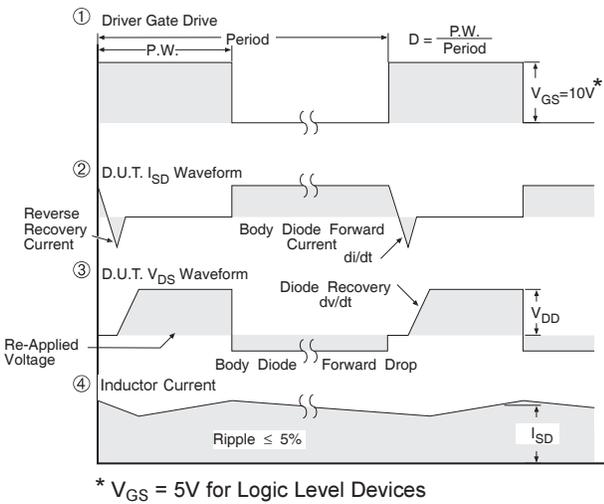
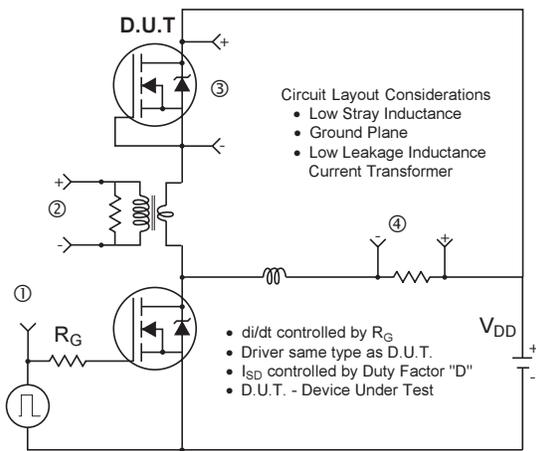
**Fig 15.** Threshold Voltage vs. Temperature



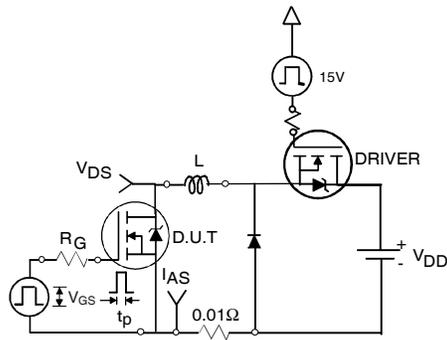
**Fig 16.** Typical Repetitive peak Current vs. Case temperature



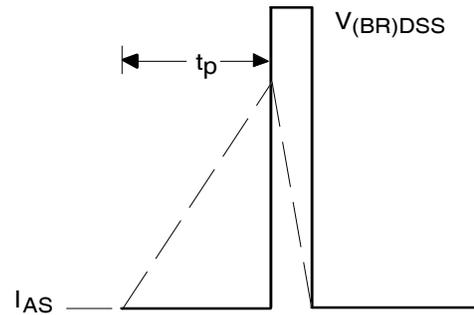
**Fig 17.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



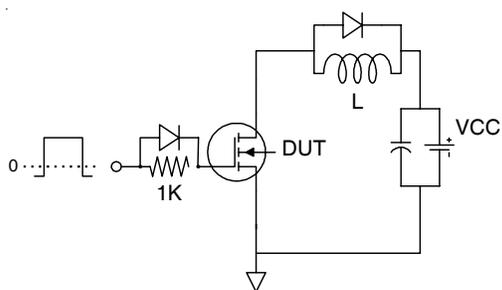
**Fig 18.** Diode Reverse Recovery Test Circuit for N-Channel HEXFET<sup>®</sup> Power MOSFETs



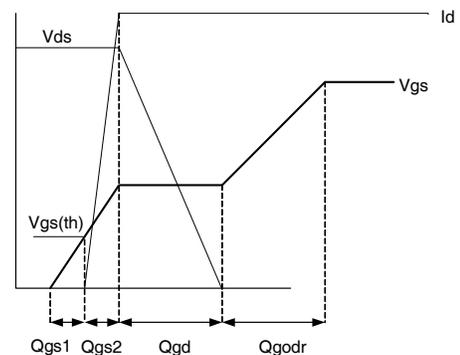
**Fig 19a.** Unclamped Inductive Test Circuit



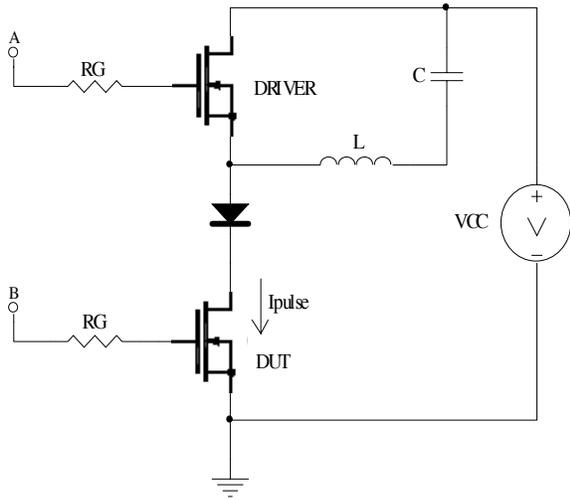
**Fig 19b.** Unclamped Inductive Waveforms



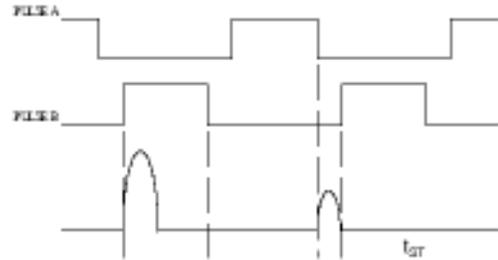
**Fig 20a.** Gate Charge Test Circuit



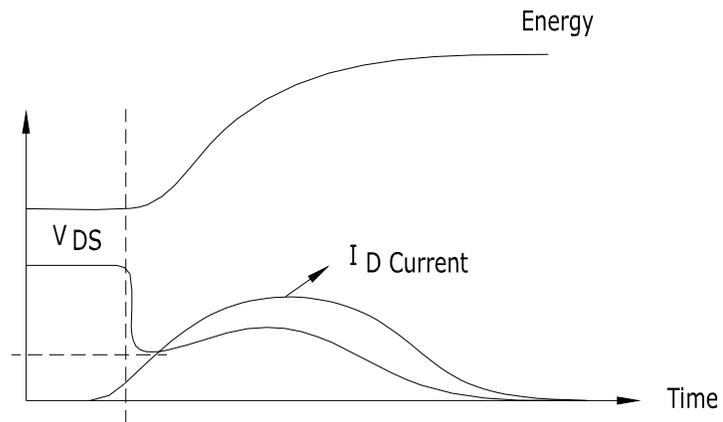
**Fig 20b.** Gate Charge Waveform



**Fig 21a.**  $t_{st}$  and  $E_{PULSE}$  Test Circuit



**Fig 21b.**  $t_{st}$  Test Waveforms



**Fig 21c.**  $E_{PULSE}$  Test Waveforms



Note: For the most current drawings please refer to the IR website at:  
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