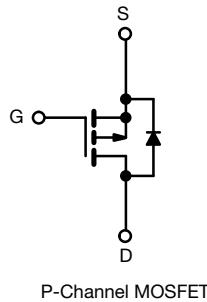
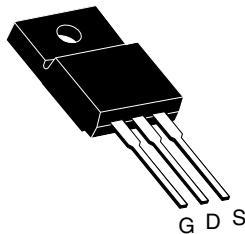


Power MOSFET

PRODUCT SUMMARY		
V _{DS} (V)	-60	
R _{DS(on)} (Ω)	V _{GS} = -10 V	0.14
Q _g max. (nC)	34	
Q _{gs} (nC)	9.9	
Q _{gd} (nC)	16	
Configuration	Single	

TO-220 FULLPAK


FEATURES

- Isolated package
- High voltage isolation = 2.5 kV_{RMS} (t = 60 s; f = 60 Hz)
- Sink to lead creepage distance = 4.8 mm
- P-channel
- 175 °C operating temperature
- Dynamic dV/dt rating
- Low thermal resistance
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 FULLPAK eliminates the need for additional insulating hardware in commercial-industrial applications. The molding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The FULLPAK is mounted to a heatsink using a single clip or by a single screw fixing.

ORDERING INFORMATION

Package	TO-220 FULLPAK
Lead (Pb)-free	IRFI9Z34GPbF SiHFI9Z34G-E3
SnPb	IRFI9Z34G SiHFI9Z34G

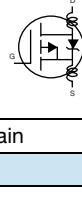
ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	-60	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current	V _{GS} at -10 V	T _C = 25 °C	A
		T _C = 100 °C	
Pulsed Drain Current ^a	I _{DM}	-48	
Linear Derating Factor		0.28	W/°C
Single Pulse Avalanche Energy ^b	E _{AS}	370	mJ
Repetitive Avalanche Current ^a	I _{AR}	-12	A
Repetitive Avalanche Energy ^a	E _{AR}	4.2	mJ
Maximum Power Dissipation	P _D	42	W
Peak Diode Recovery dV/dt ^c	dV/dt	-4.5	V/ns
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +175	°C
Soldering Recommendations (Peak temperature) ^d	for 10 s	300	
Mounting Torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

Notes

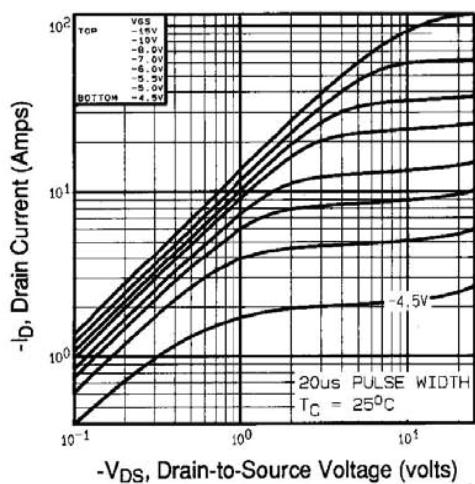
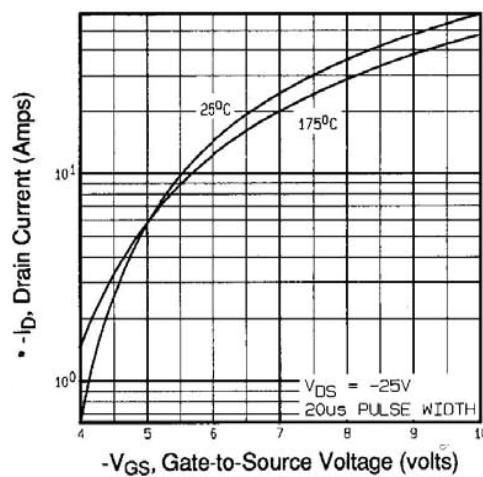
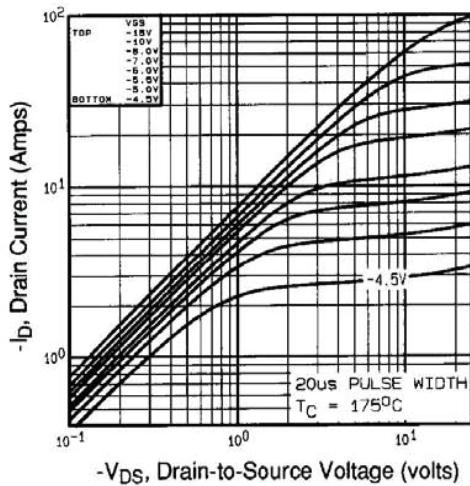
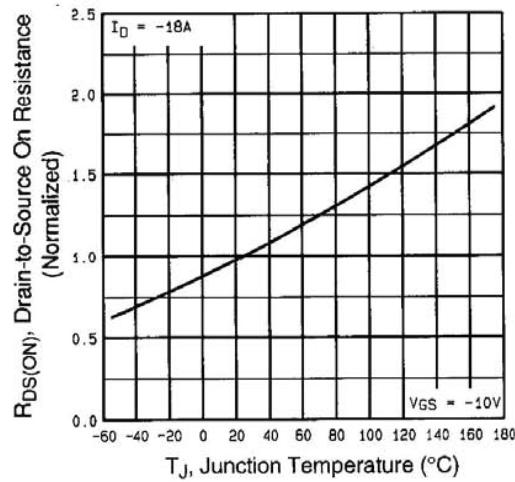
- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- V_{DD} = -25 V, starting T_J = 25 °C, L = 3.0 mH, R_G = 25 Ω, I_{AS} = -12 A (see fig. 12).
- I_{SD} ≤ -12 A, dI/dt ≤ 170 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 175 °C.
- 1.6 mm from case.

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	65	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	3.6	°C/W

SPECIFICATIONS ($T_J = 25$ °C, unless otherwise noted)								
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0$ V, $I_D = 250$ μ A		-60	-	-	V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, $I_D = -1$ mA		-	-0.060	-	V/°C	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250$ μ A		-2.0	-	-4.0	V	
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20$ V		-	-	± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -60$ V, $V_{GS} = 0$ V		-	-	-100		
		$V_{DS} = -48$ V, $V_{GS} = 0$ V, $T_J = 150$ °C		-	-	-500	μ A	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -10$ V	$I_D = -7.2$ A ^b	-	-	0.14	Ω	
Forward Transconductance	g_{fs}	$V_{DS} = -25$ V, $I_D = -7.2$ A ^b		5.4	-	-	S	
Dynamic								
Input Capacitance	C_{iss}	$V_{GS} = 0$ V, $V_{DS} = -25$ V, $f = 1.0$ MHz, see fig. 5		-	1100	-	pF	
Output Capacitance	C_{oss}			-	620	-		
Reverse Transfer Capacitance	C_{rss}			-	100	-		
Drain to Sink Capacitance	C	$f = 1.0$ MHz		-	12	-		
Total Gate Charge	Q_g	$V_{GS} = -10$ V	$I_D = -18$ A, $V_{DS} = -48$ V, see fig. 6 and 13 ^b	-	-	34	nC	
Gate-Source Charge	Q_{gs}			-	-	9.9		
Gate-Drain Charge	Q_{gd}			-	-	16		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -30$ V, $I_D = -18$ A, $R_G = 12$ Ω , $R_D = 1.5$ Ω , see fig. 10 ^b		-	18	-	ns	
Rise Time	t_r		-	120	-			
Turn-Off Delay Time	$t_{d(off)}$		-	20	-			
Fall Time	t_f		-	58	-			
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH	
Internal Source Inductance	L_S			-	7.5	-		
Gate Input Resistance	R_g	$f = 1$ MHz, open drain		0.7	-	3.9	Ω	
Drain-Source Body Diode Characteristics								
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p-n junction diode		-	-	-12	A	
Pulsed Diode Forward Current ^a	I_{SM}			-	-	-48		
Body Diode Voltage	V_{SD}	$T_J = 25$ °C, $I_S = -12$ A, $V_{GS} = 0$ V ^b		-	-	-6.3	V	
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25$ °C, $I_F = -18$ A, $dI/dt = 100$ A/ μ s ^b		-	100	200	ns	
Body Diode Reverse Recovery Charge	Q_{rr}			-	0.28	0.52	μ C	
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)						

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width ≤ 300 μ s; duty cycle ≤ 2 %.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics, $T_c = 25\text{ }^{\circ}\text{C}$

Fig. 3 - Typical Transfer Characteristics

Fig. 2 - Typical Output Characteristics, $T_c = 175\text{ }^{\circ}\text{C}$

Fig. 4 - Normalized On-Resistance vs. Temperature

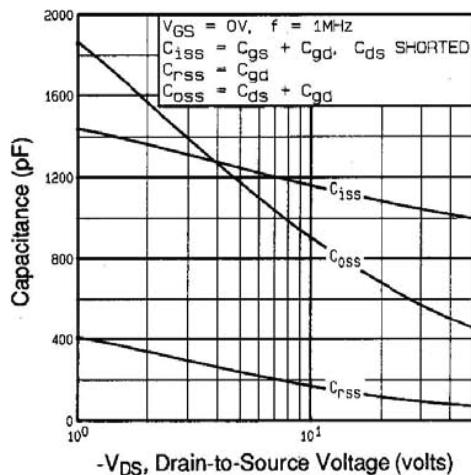


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

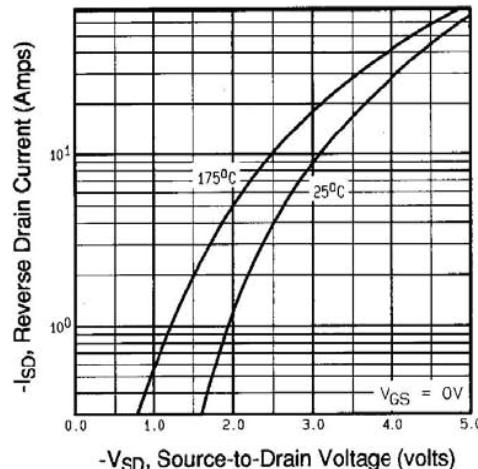


Fig. 7 - Typical Source-Drain Diode Forward Voltage

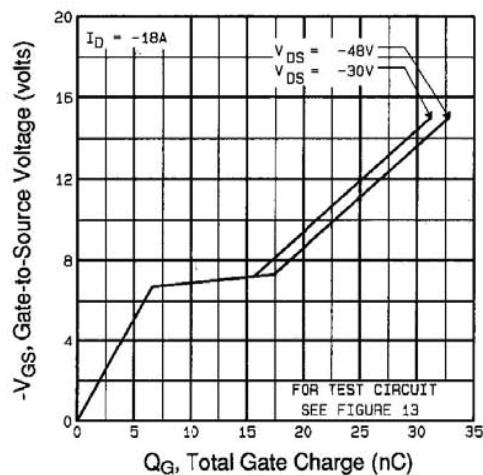


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

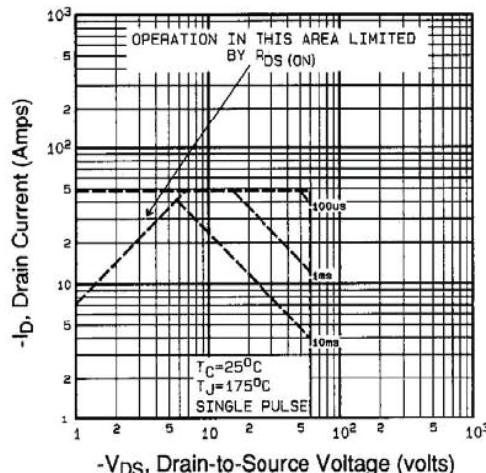


Fig. 8 - Maximum Safe Operating Area

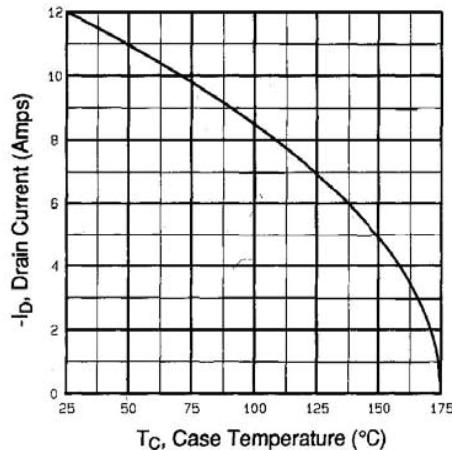


Fig. 9 - Maximum Drain Current vs. Case Temperature

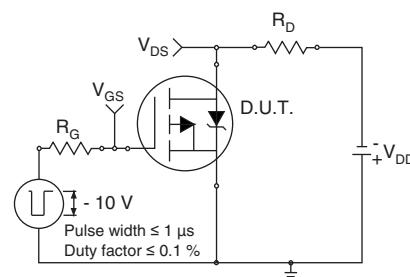


Fig. 10a - Switching Time Test Circuit

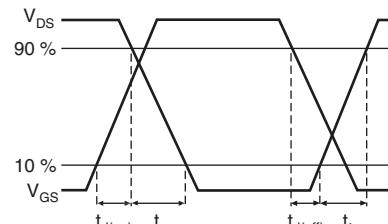


Fig. 10b - Switching Time Waveforms

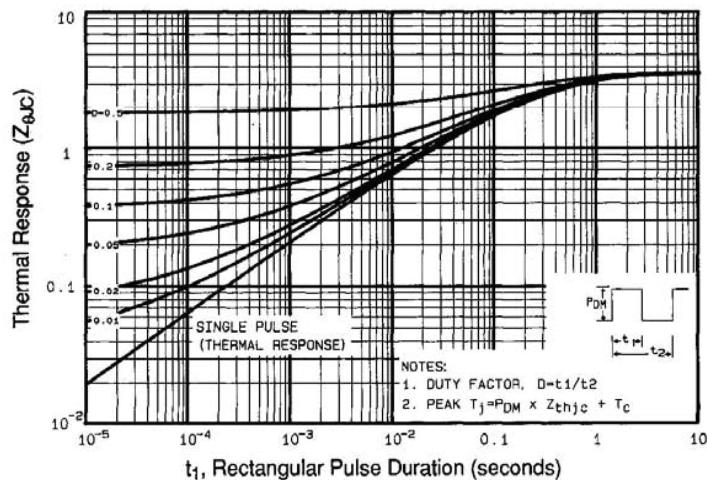


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

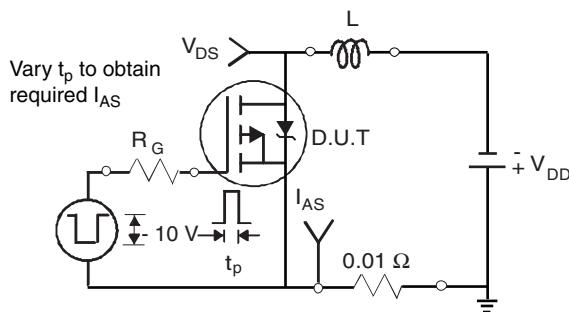


Fig. 12a - Unclamped Inductive Test Circuit

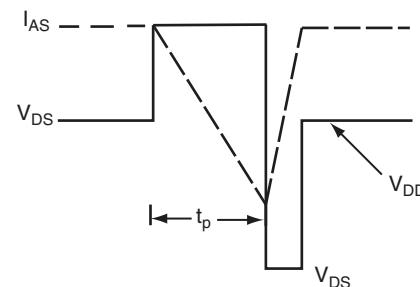
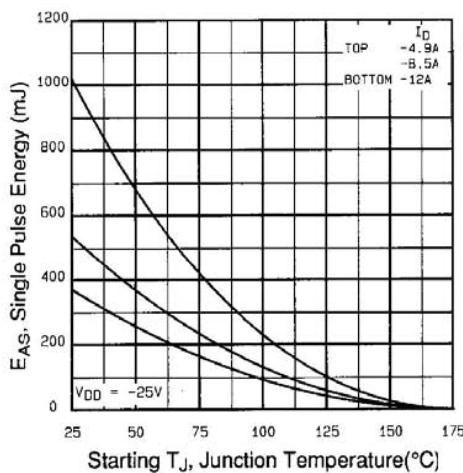
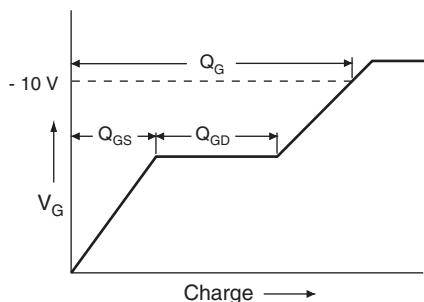
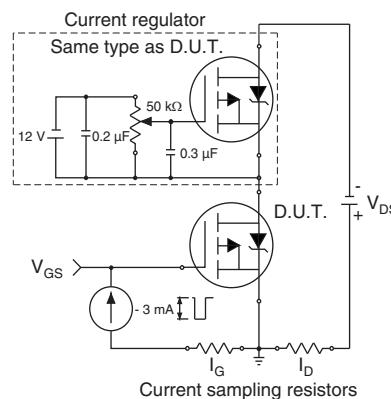
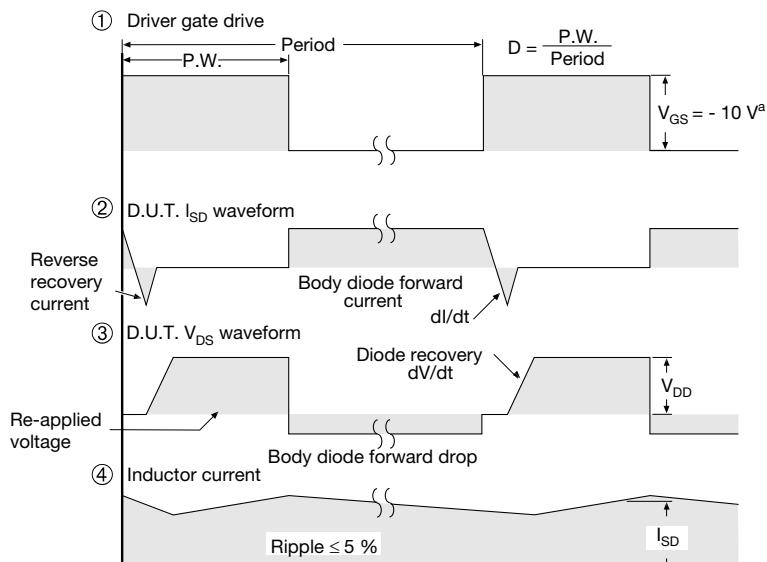
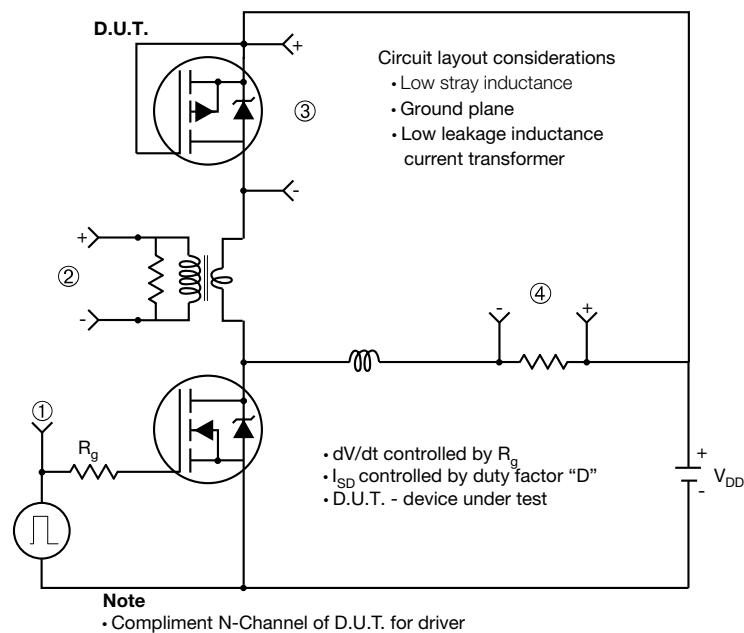


Fig. 12b - Unclamped Inductive Waveforms


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

Fig. 13a - Basic Gate Charge Waveform

Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

Fig. 14 - For P-Channel

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