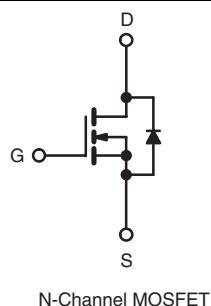
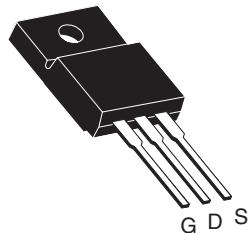


## Power MOSFET

PRODUCT SUMMARY	
V <sub>DS</sub> (V)	600
R <sub>DS(on)</sub> (Ω)	V <sub>GS</sub> = 10 V 1.2
Q <sub>g</sub> (Max.) (nC)	39
Q <sub>gs</sub> (nC)	10
Q <sub>gd</sub> (nC)	19
Configuration	Single

TO-220 FULLPAK



### ORDERING INFORMATION

Package	TO-220 FULLPAK
Lead (Pb)-free	IRFIBC40GLCPbF SiHFIBC40GLC-E3
SnPb	IRFIBC40GLC SiHFIBC40GLC

### ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ , unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V <sub>DS</sub>	600	V
Gate-Source Voltage	V <sub>GS</sub>	± 20	
Continuous Drain Current	I <sub>D</sub>	3.5	A
		2.2	
Pulsed Drain Current <sup>a</sup>	I <sub>DM</sub>	14	
Linear Derating Factor		0.32	W/°C
Single Pulse Avalanche Energy <sup>b</sup>	E <sub>AS</sub>	320	mJ
Repetitive Avalanche Current <sup>a</sup>	I <sub>AR</sub>	3.5	A
Repetitive Avalanche Energy <sup>a</sup>	E <sub>AR</sub>	4.0	mJ
Maximum Power Dissipation	P <sub>D</sub>	40	W
Peak Diode Recovery dV/dt <sup>c</sup>	dV/dt	3.0	V/ns
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s	300 <sup>d</sup>	
Mounting Torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

#### Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. V<sub>DD</sub> = 50 V, starting T<sub>J</sub> = 25 °C, L = 12 µH, R<sub>G</sub> = 25 Ω, I<sub>AS</sub> = 3.5 A (see fig. 12).
- c. I<sub>SD</sub> ≤ 6.2 A, dI/dt ≤ 80 A/µs, V<sub>DD</sub> ≤ V<sub>DS</sub>, T<sub>J</sub> ≤ 150 °C.
- d. 1.6 mm from case.

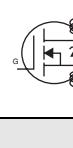
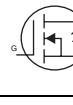
\* Pb containing terminations are not RoHS compliant, exemptions may apply



**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	65	$^{\circ}\text{C}/\text{W}$
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	3.1	

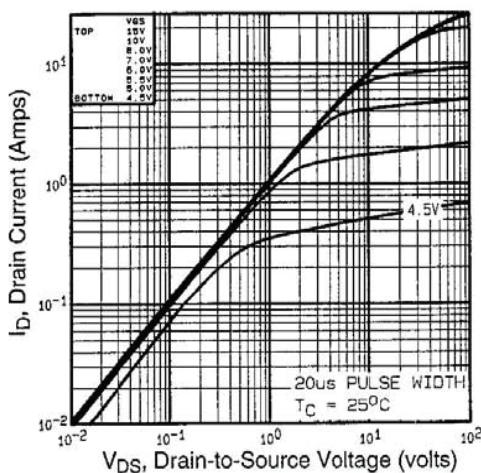
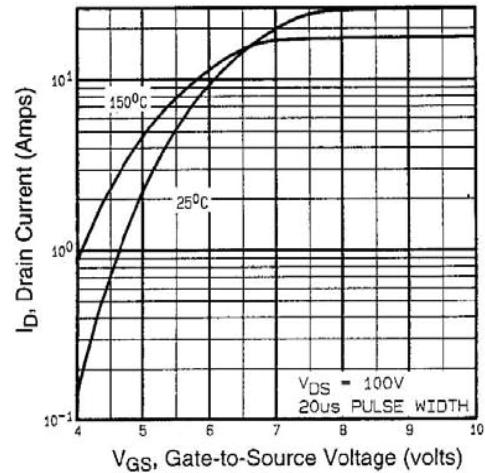
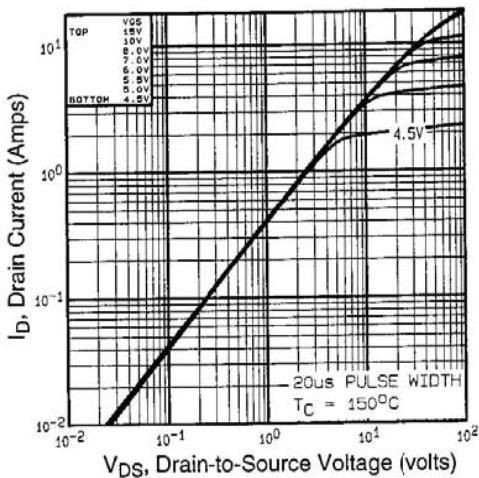
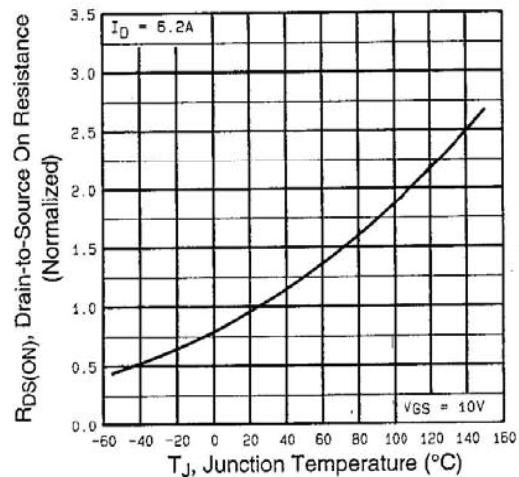
 **SPECIFICATIONS  $T_J = 25^{\circ}\text{C}$ , unless otherwise noted**

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}$ , $I_D = 250 \mu\text{A}$		600	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25^{\circ}\text{C}$ , $I_D = 1 \text{ mA}$		-	0.70	-	$^{\circ}\text{C}/\text{C}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250 \mu\text{A}$		2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20 \text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 600 \text{ V}$ , $V_{GS} = 0 \text{ V}$		-	-	25	$\mu\text{A}$
		$V_{DS} = 480 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $T_J = 125^{\circ}\text{C}$		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$	$I_D = 2.1 \text{ A}^b$	-	-	1.2	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 100 \text{ V}$	$I_D = 3.7 \text{ A}^b$	3.7	-	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0 \text{ V}$ , $V_{DS} = 25 \text{ V}$ , $f = 1.0 \text{ MHz}$ , see fig. 5		-	1100	-	pF
Output Capacitance	$C_{oss}$			-	140	-	
Reverse Transfer Capacitance	$C_{rss}$			-	15	-	
Drain to Sink Capacitance	C	$f = 1.0 \text{ MHz}$		-	12	-	nC
Total Gate Charge	$Q_g$	$V_{GS} = 10 \text{ V}$	$I_D = 6.2 \text{ A}$ , $V_{DS} = 360 \text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	39	
Gate-Source Charge	$Q_{gs}$			-	-	10	
Gate-Drain Charge	$Q_{gd}$			-	-	19	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 300 \text{ V}$ , $I_D = 6.2 \text{ A}$ , $R_G = 9.1 \Omega$ , $R_D = 47 \Omega$ , see fig. 10 <sup>b</sup>		-	12	-	ns
Rise Time	$t_r$			-	20	-	
Turn-Off Delay Time	$t_{d(off)}$			-	27	-	
Fall Time	$t_f$			-	17	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal Source Inductance	$L_S$			-	7.5	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode		-	-	3.5	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	14	
Body Diode Voltage	$V_{SD}$	$T_J = 25^{\circ}\text{C}$ , $I_S = 3.5 \text{ A}$ , $V_{GS} = 0 \text{ V}^b$		-	-	1.5	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25^{\circ}\text{C}$ , $I_F = 6.2 \text{ A}$ , $dI/dt = 100 \text{ A}/\mu\text{s}^b$		-	440	660	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	2.1	3.2	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width  $\leq 300 \mu\text{s}$ ; duty cycle  $\leq 2\%$ .

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

**Fig. 1 - Typical Output Characteristics,  $T_C = 25^\circ\text{C}$** 

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 2 - Typical Output Characteristics,  $T_C = 150^\circ\text{C}$** 

**Fig. 4 - Normalized On-Resistance vs. Temperature**

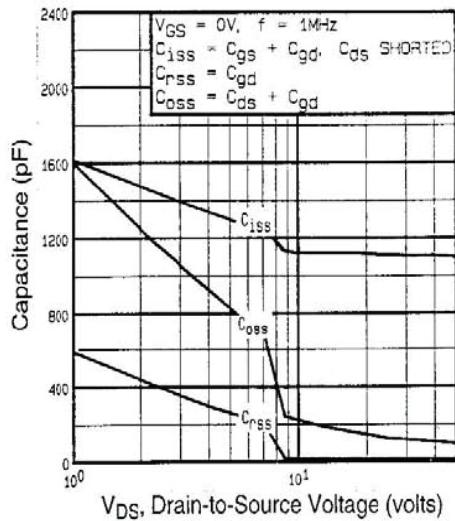


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

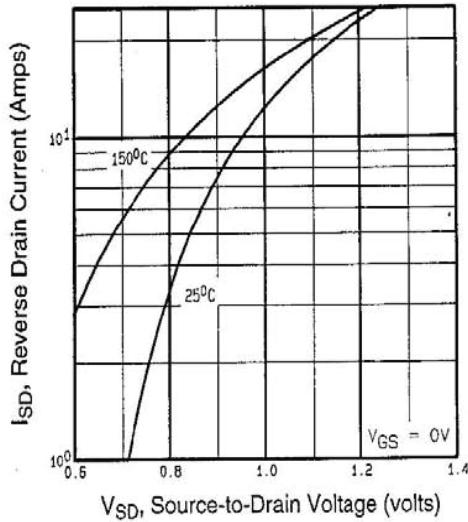


Fig. 7 - Typical Source-Drain Diode Forward Voltage

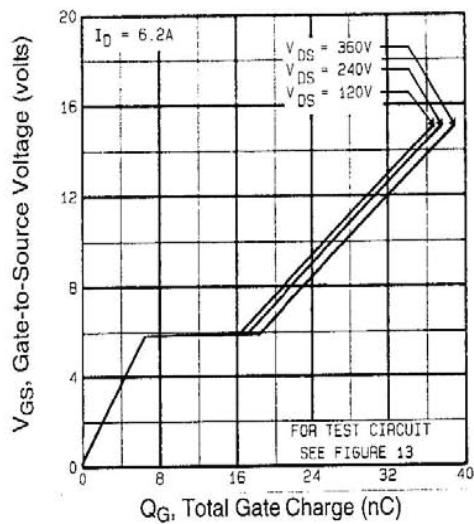


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

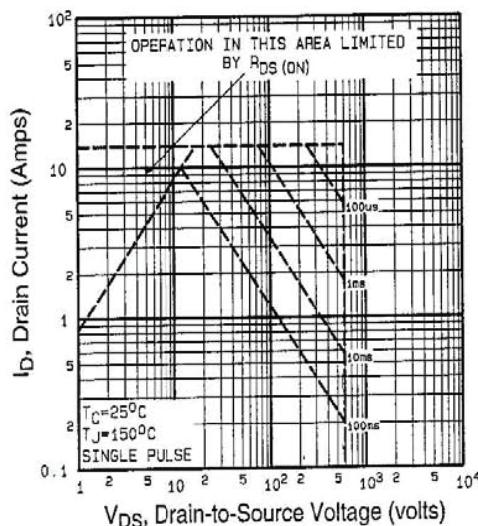


Fig. 8 - Maximum Safe Operating Area

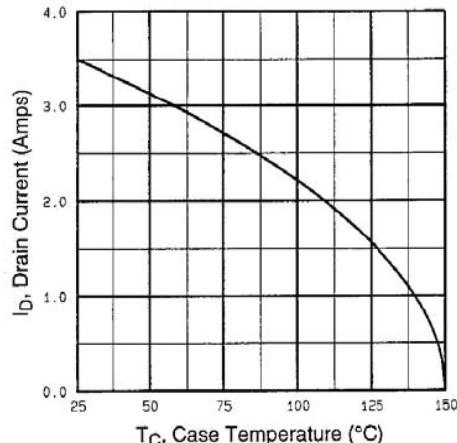


Fig. 9 - Maximum Drain Current vs. Case Temperature

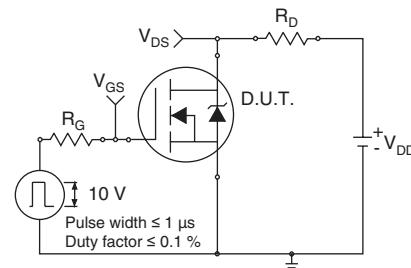


Fig. 10a - Switching Time Test Circuit

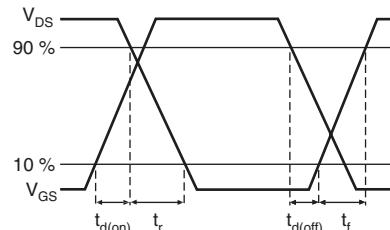


Fig. 10b - Switching Time Waveforms

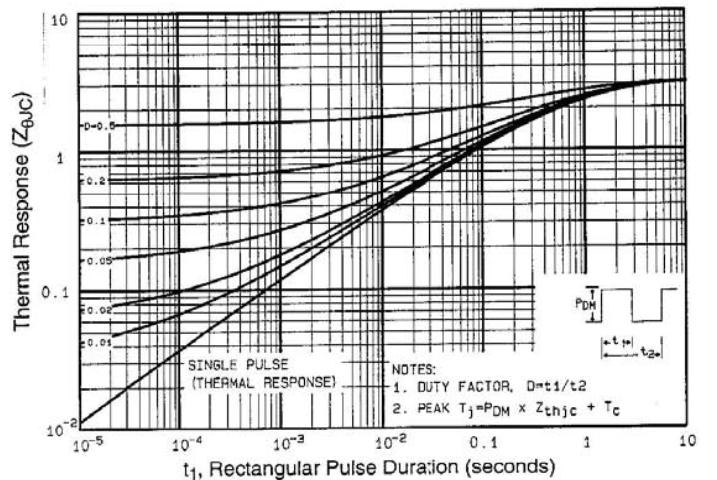


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

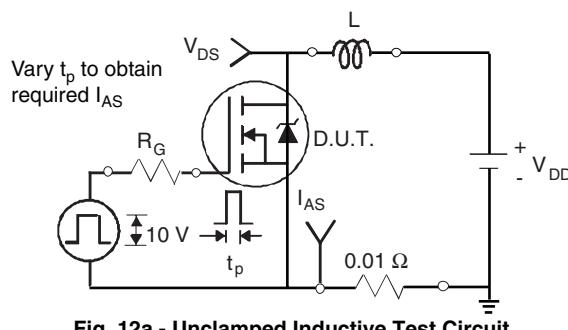


Fig. 12a - Unclamped Inductive Test Circuit

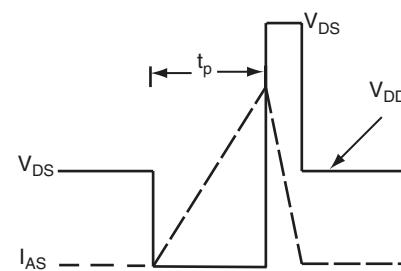


Fig. 12b - Unclamped Inductive Waveforms

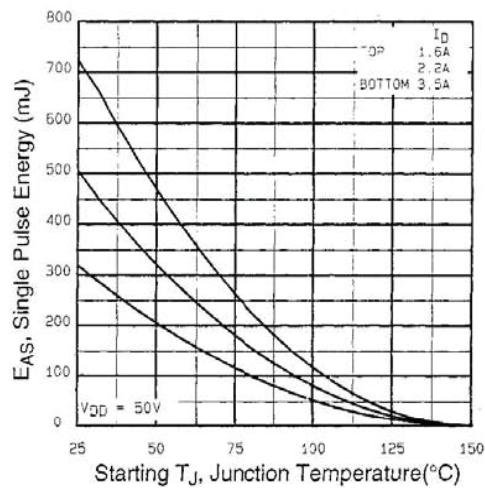


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

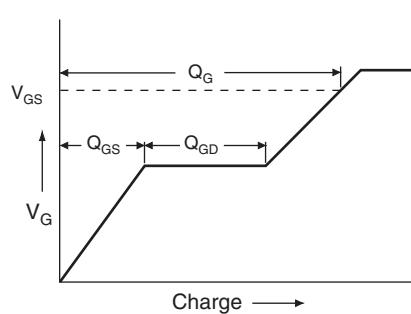


Fig. 13a - Basic Gate Charge Waveform

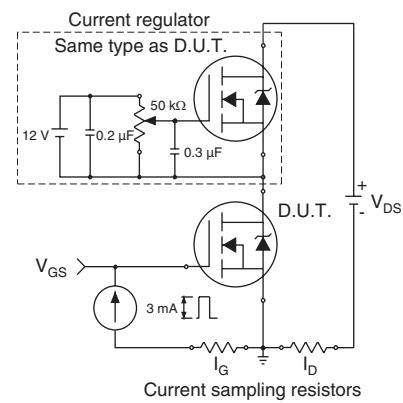
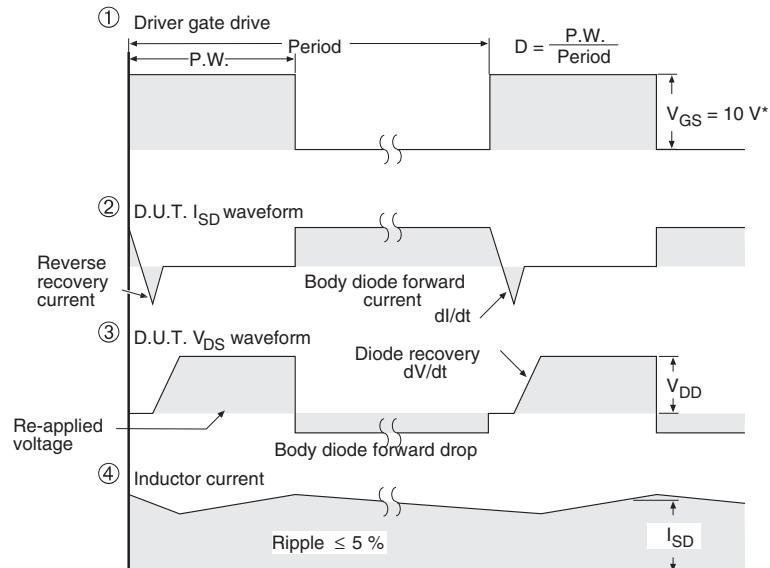
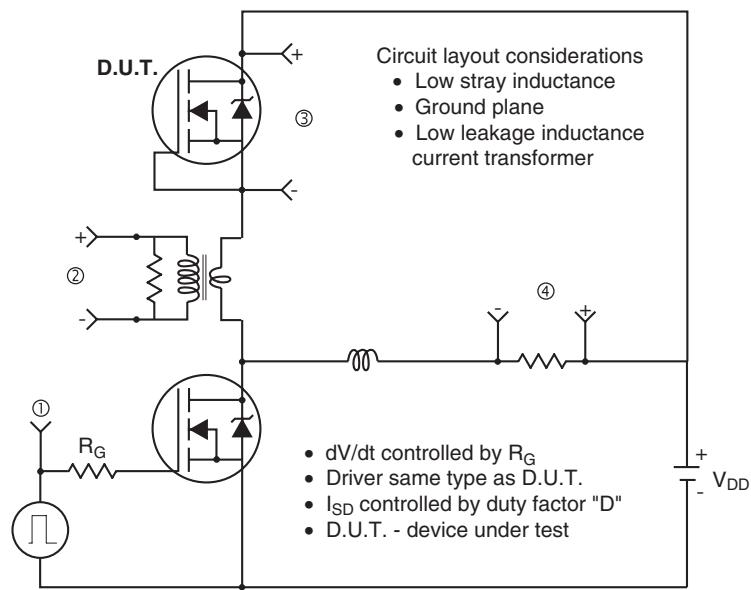


Fig. 13b - Gate Charge Test Circuit

### Peak Diode Recovery $dV/dt$ Test Circuit

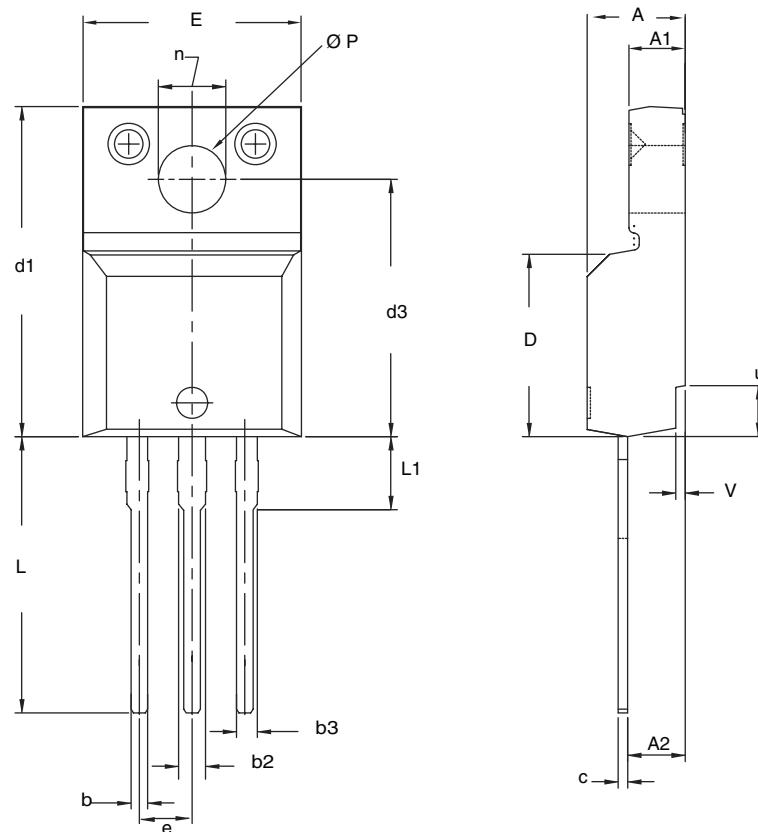


\*  $V_{GS} = 5 V$  for logic level devices

**Fig. 14 - For N-Channel**

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### TO-220 FULLPAK (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
ØP	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
v	0.400	0.500	0.016	0.020

ECN: X09-0126-Rev. B, 26-Oct-09  
DWG: 5972

#### Notes

1. To be used only for process drawing.
2. These dimensions apply to all TO-220, FULLPAK leadframe versions 3 leads.
3. All critical dimensions should C meet  $C_{pk} > 1.33$ .
4. All dimensions include burrs and plating thickness.
5. No chipping or package damage.

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