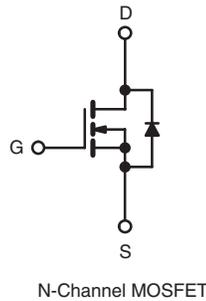
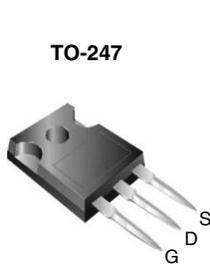


Power MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	600
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$ 0.385
Q_g (Max.) (nC)	100
Q_{gs} (nC)	30
Q_{gd} (nC)	46
Configuration	Single



FEATURES

- Superfast Body Diode Eliminates the Need for External Diodes in ZVS Applications
- Lower Gate Charge Results in Simple Drive Requirements
- Enhanced dV/dt Capabilities Offer Improved Ruggedness
- Higher Gate Voltage Threshold Offers Improved Noise Immunity
- Lead (Pb)-free Available



RoHS*
COMPLIANT

APPLICATIONS

- Zero Voltage Switching SMPS
- Telecom and Server Power Supplies
- Uninterruptible Power Supplies
- Motor Control Applications

ORDERING INFORMATION	
Package	TO-247
Lead (Pb)-free	IRFP15N60LPbF
	SiHFP15N60L-E3
SnPb	IRFP15N60L
	SiHFP15N60L

ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	600	V
Gate-Source Voltage	V_{GS}	± 30	
Continuous Drain Current	V_{GS} at 10 V	$T_C = 25\text{ }^\circ\text{C}$	15
		$T_C = 100\text{ }^\circ\text{C}$	9.7
Pulsed Drain Current ^a	I_{DM}	60	A
Linear Derating Factor		2.3	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy ^b	E_{AS}	320	mJ
Repetitive Avalanche Current ^a	I_{AR}	15	A
Repetitive Avalanche Energy ^a	E_{AR}	28	mJ
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	280
Peak Diode Recovery dV/dt^c	dV/dt	10	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	
Mounting Torque	6-32 or M3 screw	10	
		1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 2.9\text{ mH}$, $R_G = 25\text{ }\Omega$, $I_{AS} = 15\text{ A}$, $dV/dt = 10\text{ V/ns}$ (see fig. 12a).
- $I_{SD} \leq 15\text{ A}$, $dI/dt \leq 340\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.24	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.44	

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	600	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$	-	0.39	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3.0	-	5.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 30\text{ V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	-	-	50	μA
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	2.0	mA
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 9.0\text{ A}^b$	-	0.385	0.460	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}, I_D = 9.0\text{ A}$	8.3	-	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$, see fig. 5	-	2720	-	pF
Output Capacitance	C_{oss}		-	260	-	
Reverse Transfer Capacitance	C_{rss}		-	20	-	
Effective Output Capacitance	$C_{oss\text{ eff.}}$	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ V to } 480\text{ V}^c$	-	120	-	pF
Effective Output Capacitance (Energy Related)	$C_{oss\text{ eff. (ER)}}$		-	100	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}, I_D = 15\text{ A}, V_{DS} = 480\text{ V}$, see fig. 7 and 15 ^b	-	-	100	nC
Gate-Source Charge	Q_{gs}		-	-	30	
Gate-Drain Charge	Q_{gd}		-	-	46	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 300\text{ V}, I_D = 15\text{ A}, R_G = 1.8\text{ }\Omega, V_{GS} = 10\text{ V}$, see fig. 11a and 11b ^b	-	20	-	ns
Rise Time	t_r		-	44	-	
Turn-Off Delay Time	$t_{d(off)}$		-	28	-	
Fall Time	t_f		-	5.5	-	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	15	A
Pulsed Diode Forward Current ^a	I_{SM}		-	-	60	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 15\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	1.5	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 15\text{ A}$	-	130	200	ns
		$T_J = 125\text{ }^\circ\text{C}, di/dt = 100\text{ A}/\mu\text{s}^b$	-	240	360	
Body Diode Reverse Recovery Charge	Q_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 15\text{ A}, V_{GS} = 0\text{ V}^b$	-	450	670	nC
		$T_J = 125\text{ }^\circ\text{C}, di/dt = 100\text{ A}/\mu\text{s}^b$	-	1080	1620	
Reverse Recovery Time	I_{RRM}	$T_J = 25\text{ }^\circ\text{C}$	-	5.8	8.7	A
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DS} . $C_{oss\text{ eff. (ER)}}$ is a fixed capacitance that stores the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DS} .

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

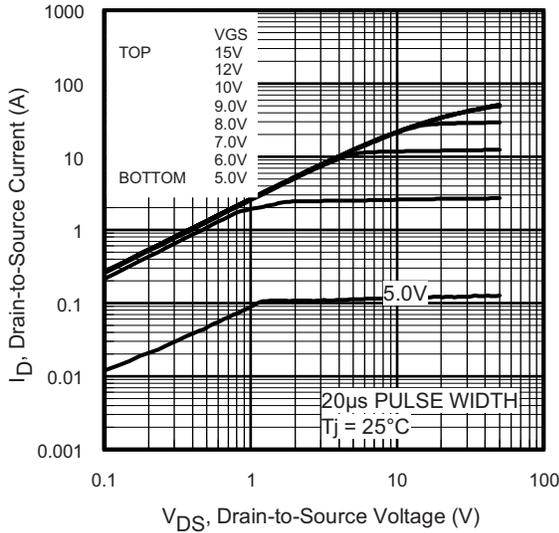


Fig. 1 - Typical Output Characteristics

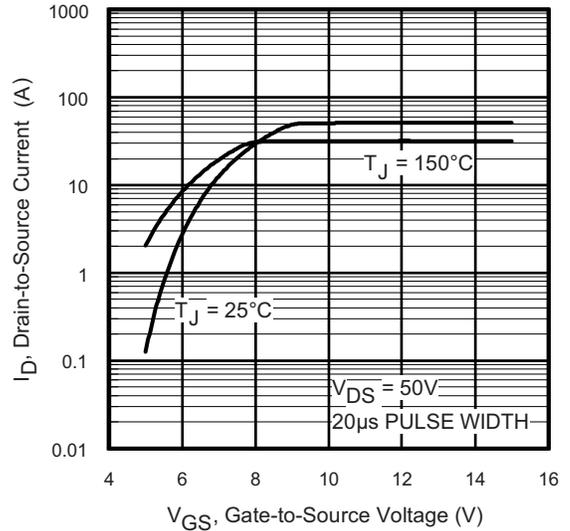


Fig. 3 - Typical Transfer Characteristics

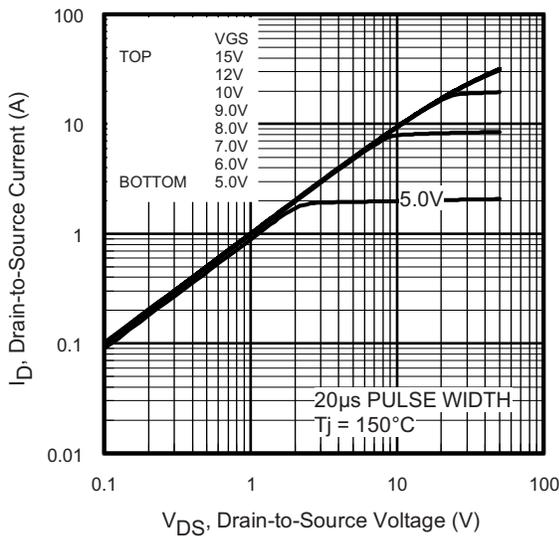


Fig. 2 - Typical Output Characteristics

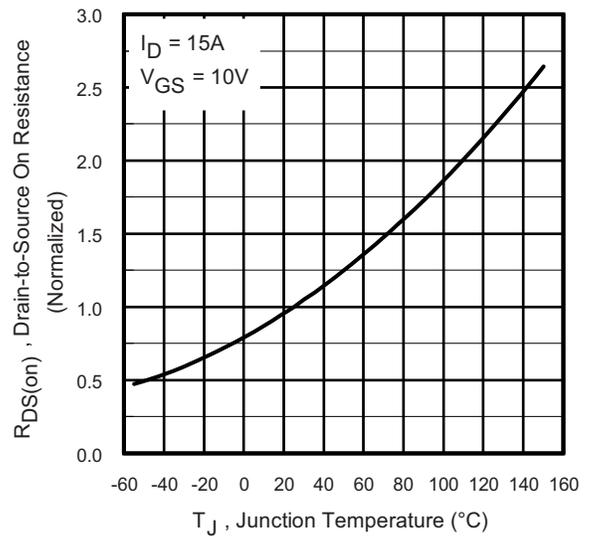


Fig. 4 - Normalized On-Resistance vs. Temperature

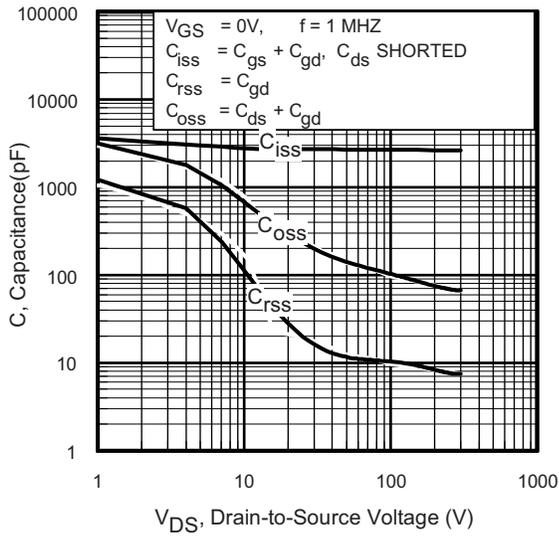


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

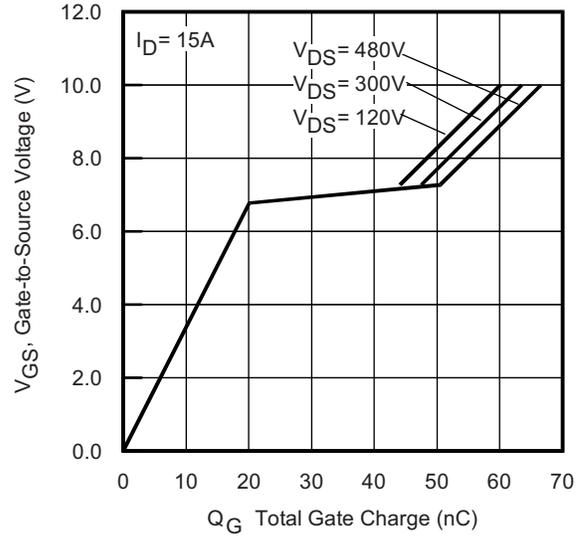


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

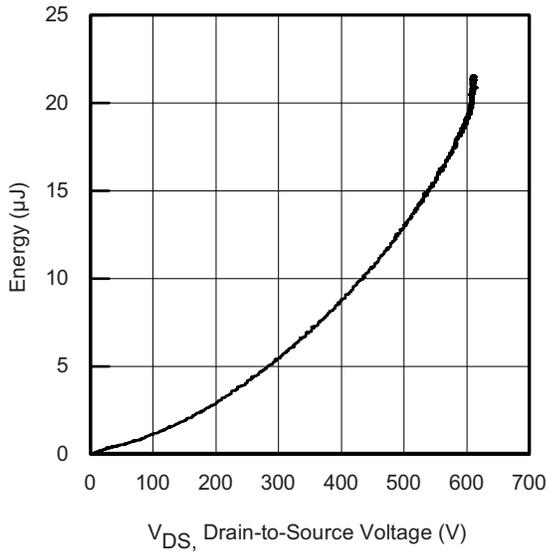


Fig. 6 - Typical Output Capacitance Stored Energy vs. V_{DS}

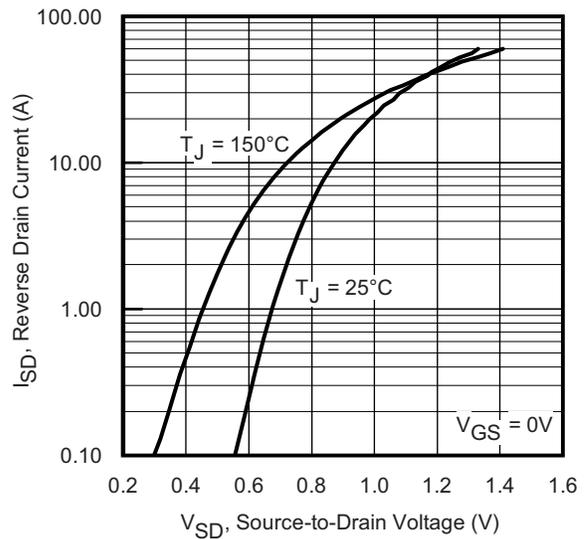


Fig. 8 - Typical Source-Drain Diode Forward Voltage

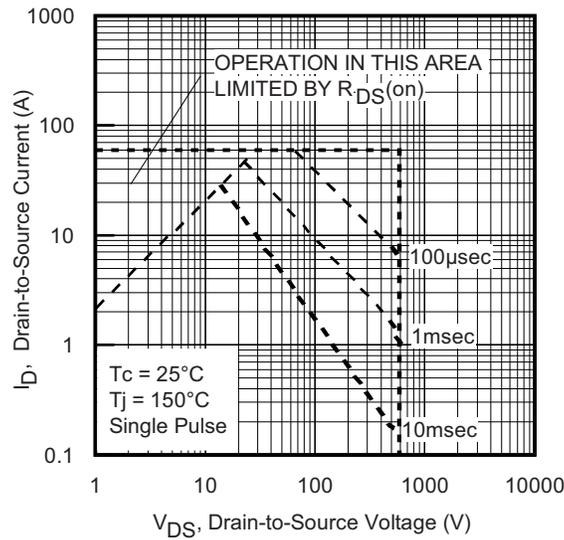


Fig. 9 - Maximum Safe Operating Area

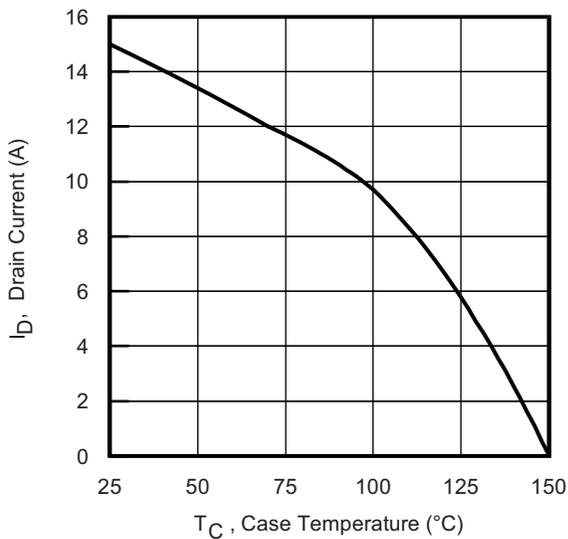


Fig. 10 - Maximum Drain Current vs. Case Temperature

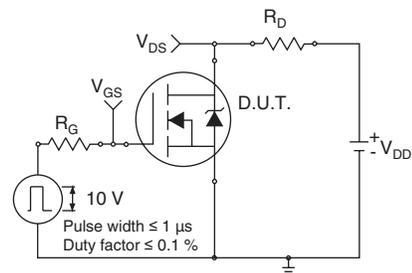


Fig. 11a - Switching Time Test Circuit

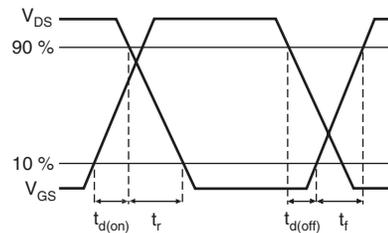


Fig. 11b - Switching Time Waveforms

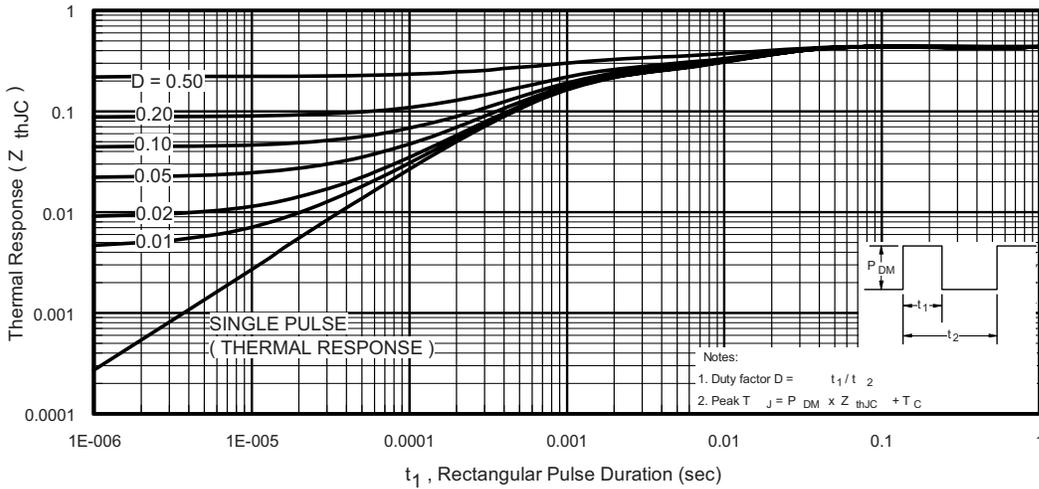


Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

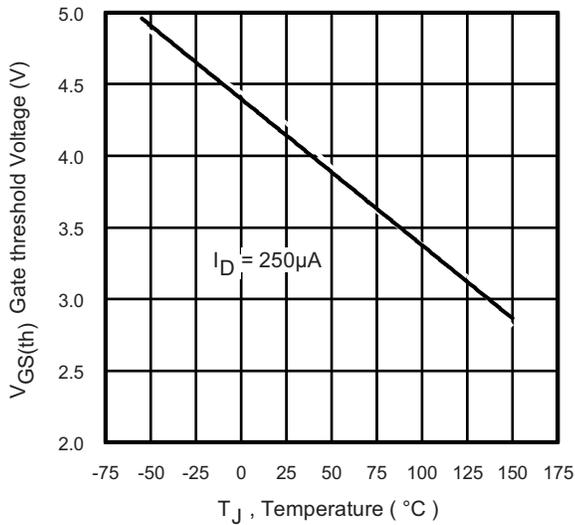


Fig. 13 - Threshold Voltage vs. Temperature

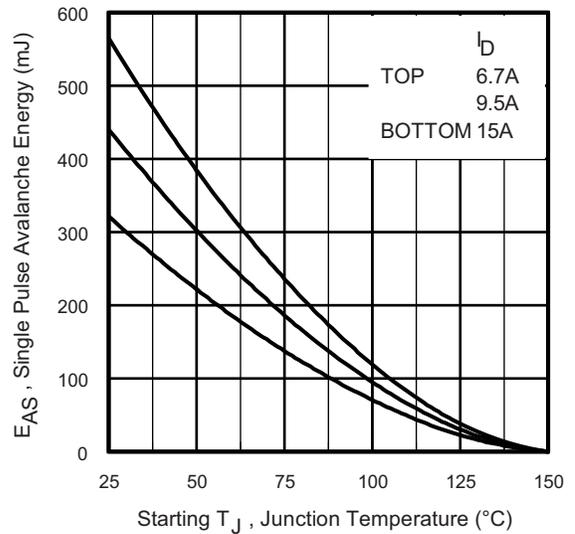


Fig. 14a - Maximum Avalanche Energy vs. Drain Current

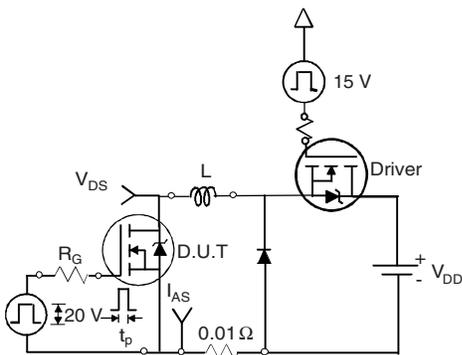


Fig. 14b - Unclamped Inductive Test Circuit

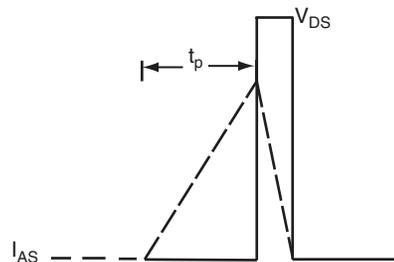


Fig. 14c - Unclamped Inductive Waveforms

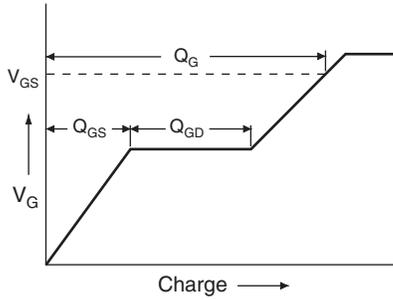


Fig. 15a - Basic Gate Charge Waveform

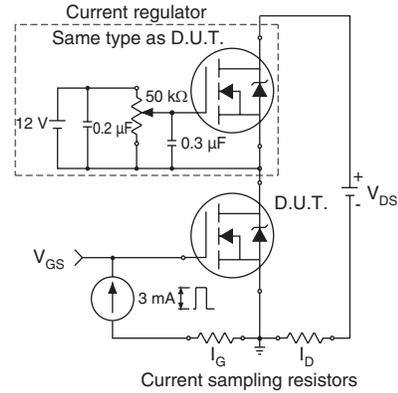


Fig. 15b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

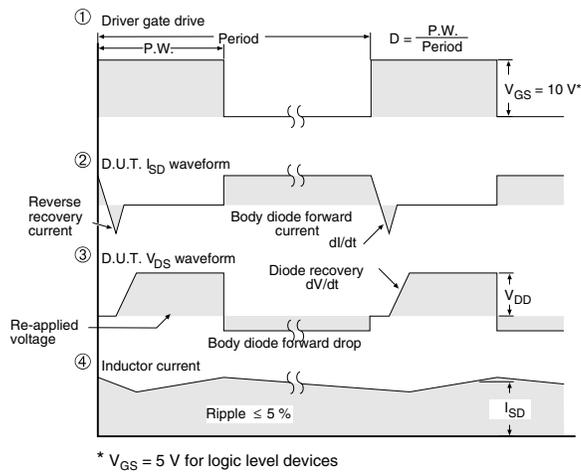
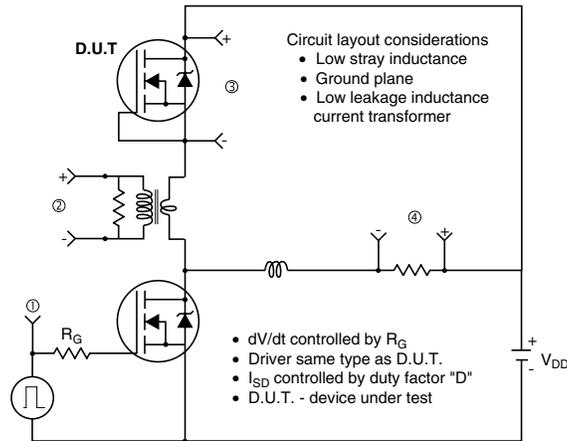


Fig. 16 - For N-Channel

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