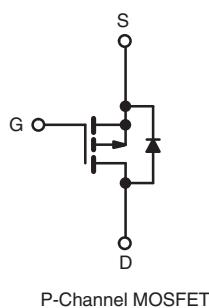


## Power MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	- 100	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = - 10$ V	0.20
$Q_g$ (Max.) (nC)	61	
$Q_{gs}$ (nC)	14	
$Q_{gd}$ (nC)	29	
Configuration	Single	

TO-247AC



P-Channel MOSFET

### FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- P-Channel
- Isolated Central Mounting Hole
- 175 °C Operating Temperature
- Fast Switching
- Ease of Parallelizing
- Compliant to RoHS Directive 2002/95/EC


**RoHS\***  
COMPLIANT

### DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-247AC package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220AB devices. The TO-247AC is similar but superior to the earlier TO-218 package because of its isolated mounting hole. It also provides greater creepage distance between pins to meet the requirements of most safety specifications.

### ORDERING INFORMATION

Package	TO-247AC
Lead (Pb)-free	IRFP9140PbF SiHFP9140-E3
SnPb	IRFP9140 SiHFP9140

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	- 100	
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$I_D$	- 21	A
		- 15	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	- 84	
Linear Derating Factor		1.2	W/°C
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	960	mJ
Repetitive Avalanche Current <sup>a</sup>	$I_{AR}$	- 21	A
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	18	mJ
Maximum Power Dissipation	$P_D$	180	W
Peak Diode Recovery dV/dt <sup>c</sup>	dV/dt	- 5.5	V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature)	for 10 s	300 <sup>d</sup>	
Mounting Torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = - 25$  V, starting  $T_J = 25$  °C,  $L = 3.3$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = - 21$  A (see fig. 12).
- $I_{SD} \leq - 21$  A,  $dI/dt \leq 200$  A/ $\mu$ s,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 175$  °C.
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.24	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.83	

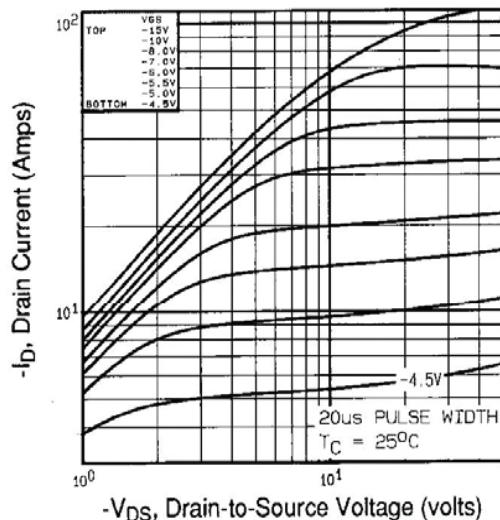
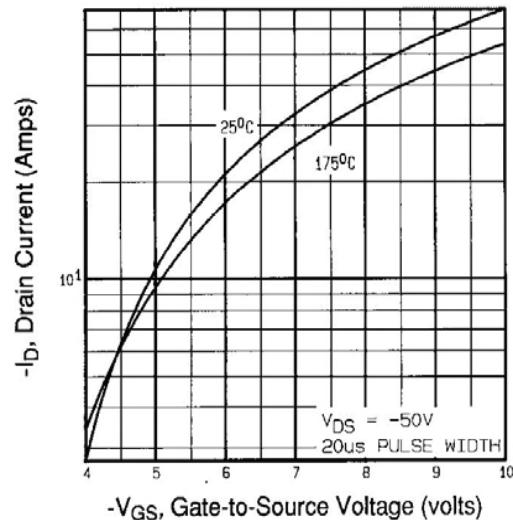
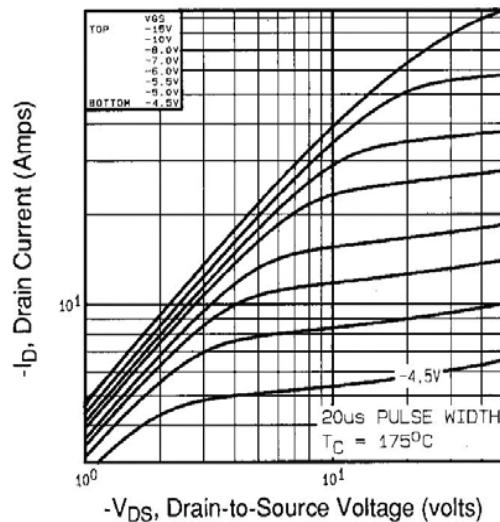
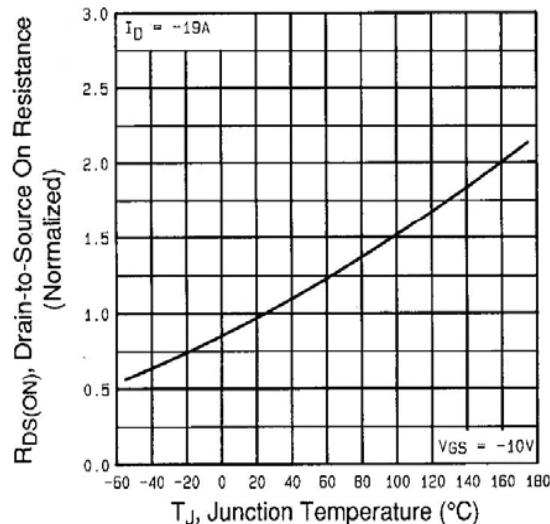
**SPECIFICATIONS** ( $T_J = 25^\circ\text{C}$ , unless otherwise noted)

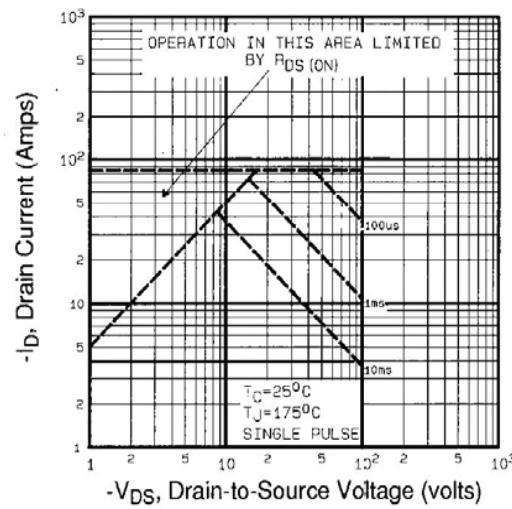
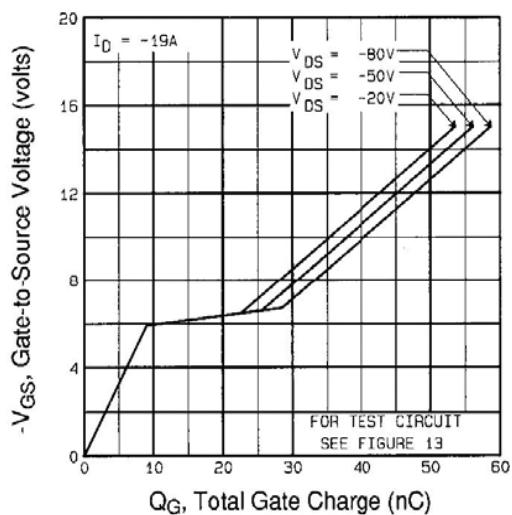
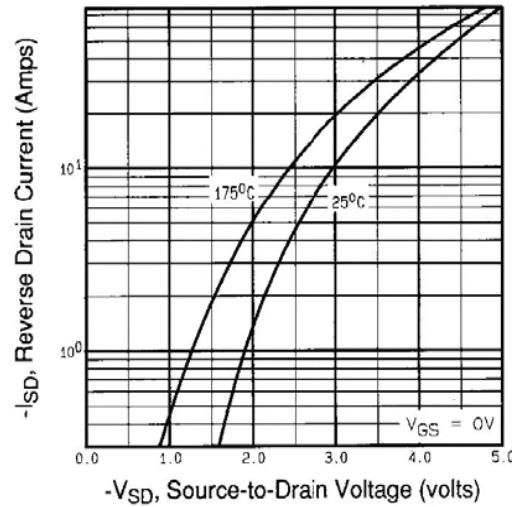
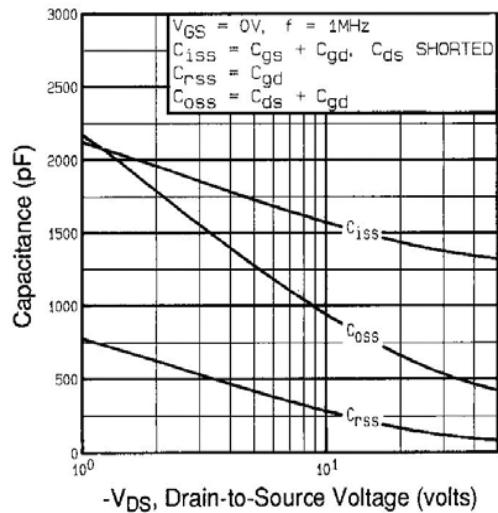
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
<b>Static</b>								
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = -250\text{ }\mu\text{A}$		-100	-	-	V	
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25^\circ\text{C}$ , $I_D = -1\text{ mA}$		-	-0.087	-	$\text{V}/^\circ\text{C}$	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = -250\text{ }\mu\text{A}$		-2.0	-	-4.0	V	
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -100\text{ V}$ , $V_{GS} = 0\text{ V}$		-	-	-100	$\mu\text{A}$	
		$V_{DS} = -80\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 150^\circ\text{C}$		-	-	-500		
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}$	$I_D = -13\text{ A}^b$	-	-	0.20	$\Omega$	
Forward Transconductance	$g_{fs}$	$V_{DS} = -50\text{ V}$ , $I_D = -13\text{ A}^b$		6.2	-	-	S	
<b>Dynamic</b>								
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = -25\text{ V}$ , $f = 1.0\text{ MHz}$ , see fig. 5		-	1400	-	pF	
Output Capacitance	$C_{oss}$			-	590	-		
Reverse Transfer Capacitance	$C_{rss}$			-	140	-		
Total Gate Charge	$Q_g$	$V_{GS} = -10\text{ V}$	$I_D = -19\text{ A}$ , $V_{DS} = -80\text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	61	nC	
Gate-Source Charge	$Q_{gs}$			-	-	14		
Gate-Drain Charge	$Q_{gd}$			-	-	29		
Turn-On Delay Time	$t_{d(on)}$			-	16	-		
Rise Time	$t_r$	$V_{DD} = -50\text{ V}$ , $I_D = -19\text{ A}$ , $R_g = 9.1\text{ }\Omega$ , $R_D = 2.4\text{ }\Omega$ , see fig. 10 <sup>b</sup>		-	73	-	ns	
Turn-Off Delay Time	$t_{d(off)}$			-	34	-		
Fall Time	$t_f$			-	57	-		
Internal Drain Inductance	$L_D$			-	5.0	-		
Internal Source Inductance	$L_S$	Between lead, 6 mm (0.25") from package and center of die contact		-	13	-	nH	
<b>Drain-Source Body Diode Characteristics</b>								
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode		-	-	-21	A	
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	-84		
Body Diode Voltage	$V_{SD}$	$T_J = 25^\circ\text{C}$ , $I_S = -21\text{ A}$ , $V_{GS} = 0\text{ V}^b$		-	-	-5.0	V	
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25^\circ\text{C}$ , $I_F = -19\text{ A}$ , $dI/dt = 100\text{ A}/\mu\text{s}^b$		-	130	260	ns	
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	0.35	0.70	$\mu\text{C}$	
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )						

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Fig. 1 - Typical Output Characteristics,  $T_c = 25^\circ\text{C}$** 

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 2 - Typical Output Characteristics,  $T_c = 175^\circ\text{C}$** 

**Fig. 4 - Normalized On-Resistance vs. Temperature**



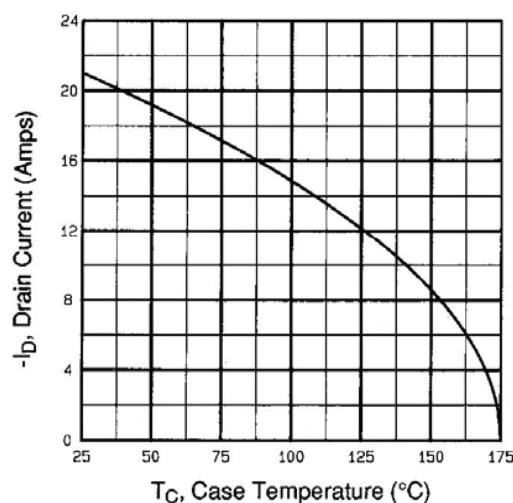


Fig. 9 - Maximum Drain Current vs. Case Temperature

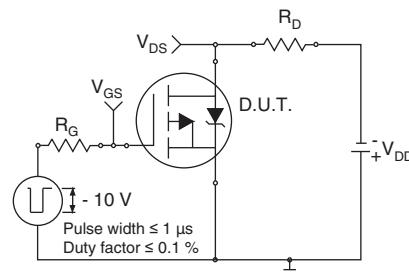


Fig. 10a - Switching Time Test Circuit

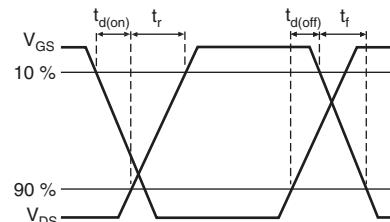


Fig. 10b - Switching Time Waveforms

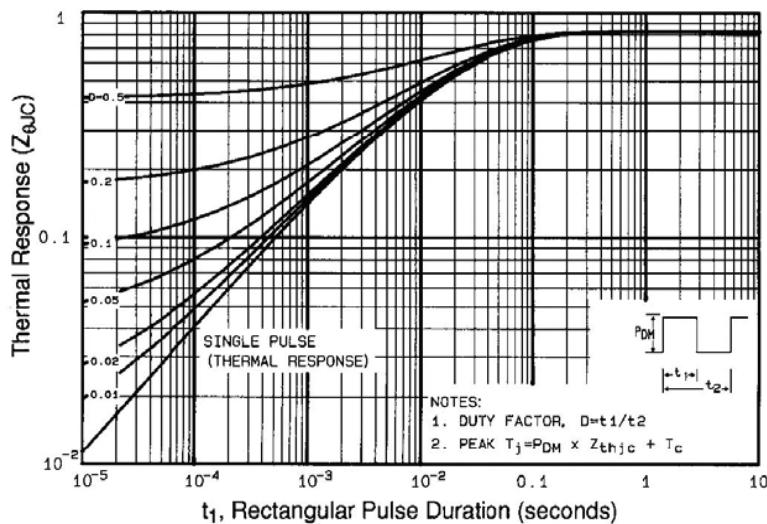


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

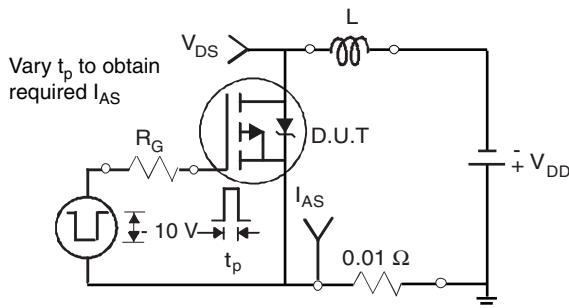


Fig. 12a - Unclamped Inductive Test Circuit

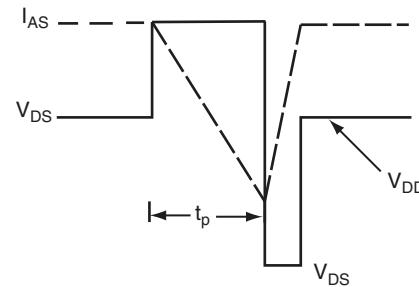


Fig. 12b - Unclamped Inductive Waveforms

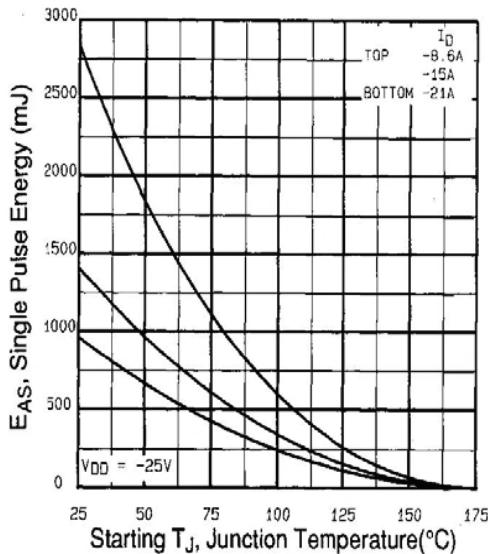


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

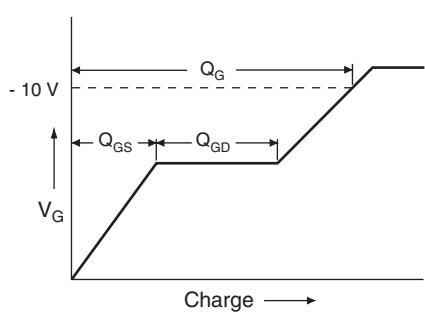


Fig. 13a - Basic Gate Charge Waveform

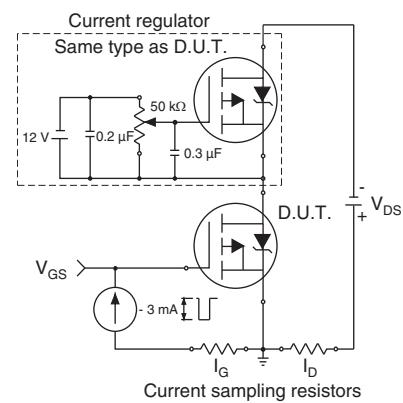
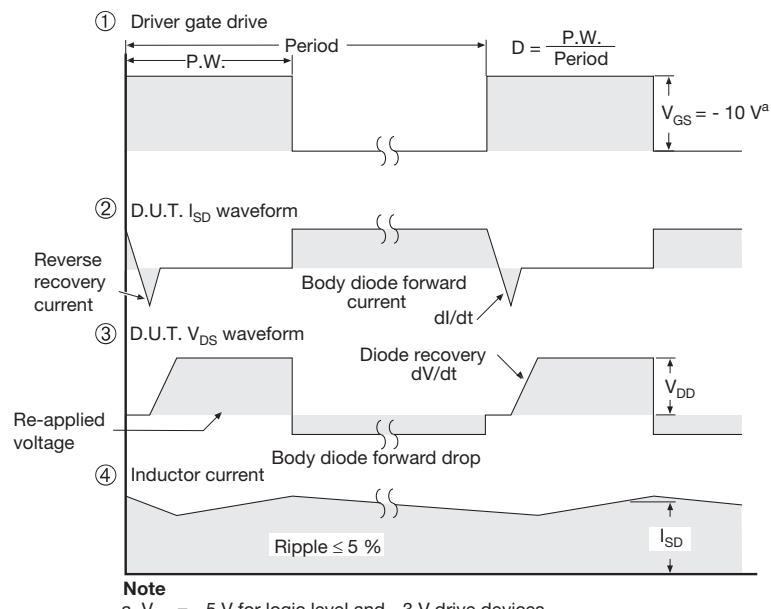
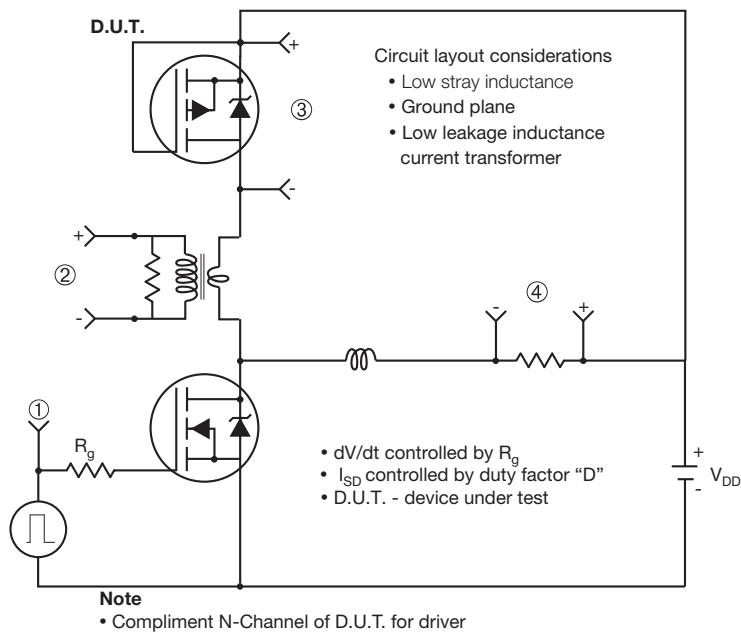
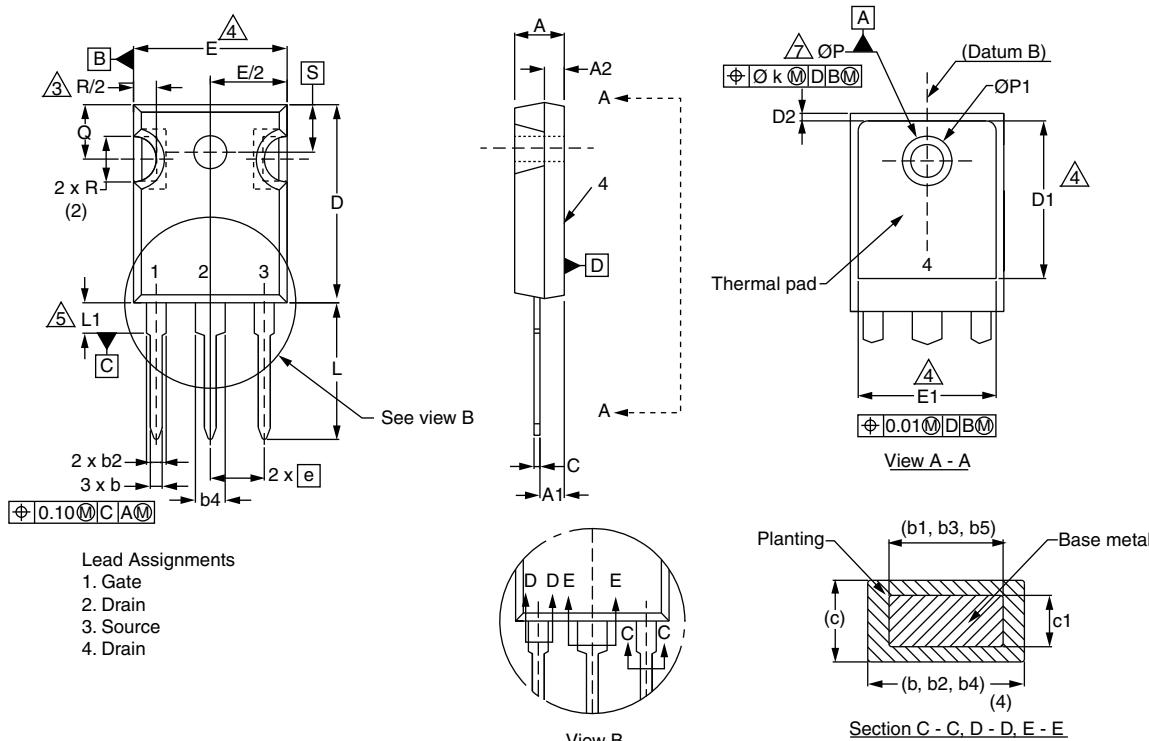


Fig. 13b - Gate Charge Test Circuit

**Peak Diode Recovery dV/dt Test Circuit**

**Fig. 14 - For P-Channel**

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### TO-247AC (High Voltage)



Lead Assignments  
 1. Gate  
 2. Drain  
 3. Source  
 4. Drain

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.58	5.31	0.180	0.209
A1	2.21	2.59	0.087	0.102
A2	1.17	2.49	0.046	0.098
b	0.99	1.40	0.039	0.055
b1	0.99	1.35	0.039	0.053
b2	1.53	2.39	0.060	0.094
b3	1.65	2.37	0.065	0.093
b4	2.42	3.43	0.095	0.135
b5	2.59	3.38	0.102	0.133
c	0.38	0.86	0.015	0.034
c1	0.38	0.76	0.015	0.030
D	19.71	20.82	0.776	0.820
D1	13.08	-	0.515	-

ECN: X13-0103-Rev. D, 01-Jul-13  
 DWG: 5971

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D2	0.51	1.30	0.020	0.051
E	15.29	15.87	0.602	0.625
E1	13.72	-	0.540	-
e	5.46 BSC		0.215 BSC	
Ø k	0.254		0.010	
L	14.20	16.25	0.559	0.640
L1	3.71	4.29	0.146	0.169
N	7.62 BSC		0.300 BSC	
Ø P	3.51	3.66	0.138	0.144
Ø P1	-	7.39	-	0.291
Q	5.31	5.69	0.209	0.224
R	4.52	5.49	0.178	0.216
S	5.51 BSC		0.217 BSC	

#### Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Contour of slot optional.
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
4. Thermal pad contour optional with dimensions D1 and E1.
5. Lead finish uncontrolled in L1.
6. Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154").
7. Outline conforms to JEDEC outline TO-247 with exception of dimension c.
8. Xian and Mingxin actually photo.



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