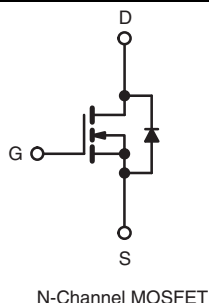
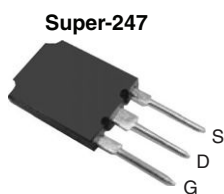


Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	600	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	0.110
Q_g (Max.) (nC)	330	
Q_{gs} (nC)	84	
Q_{gd} (nC)	150	
Configuration	Single	



FEATURES

- Low Gate Charge Q_g Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Enhanced Body Diode dV/dt Capability
- Compliant to RoHS Directive 2002/95/EC



RoHS*
COMPLIANT

APPLICATIONS

- Hard Switching Primary or PFC Switch
- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- Motor Drive

ORDERING INFORMATION

Package	Super-247
Lead (Pb)-free	IRFPS40N60KPbF
	SiHFPS40N60K-E3
SnPb	IRFPS40N60K
	SiHFPS40N60K

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	600	V
Gate-Source Voltage	V_{GS}	± 30	
Continuous Drain Current	I_D	$T_C = 25\text{ }^\circ\text{C}$	A
		$T_C = 100\text{ }^\circ\text{C}$	
Pulsed Drain Current ^a	I_{DM}	160	
Linear Derating Factor		4.5	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy ^b	E_{AS}	600	mJ
Repetitive Avalanche Current ^a	I_{AR}	40	A
Repetitive Avalanche Energy ^a	E_{AR}	57	mJ
Maximum Power Dissipation	P_D	570	W
Peak Diode Recovery dV/dt ^c	dV/dt	7.5	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 0.84\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 38\text{ A}$, $dV/dt = 5.5\text{ V/ns}$ (see fig. 12a).
- $I_{SD} \leq 38\text{ A}$, $dI/dt \leq 150\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.24	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.22	

SPECIFICATIONS ($T_J = 25\text{ °C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		600	-	-	V	
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.63	-	V/°C	
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		3.0	-	5.0	V	
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 30 V		-	-	± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 600 V, V _{GS} = 0 V		-	-	50	μA	
		V _{DS} = 480 V, V _{GS} = 0 V, T _J = 125 °C		-	-	250		
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 24 A ^b	-	0.110	0.130	Ω	
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 24 A ^b		21	-	-	S	
Dynamic								
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	7970	-	pF	
Output Capacitance	C _{oss}			-	750	-		
Reverse Transfer Capacitance	C _{rss}			-	75	-		
Output Capacitance	C _{oss}	V _{GS} = 0 V	V _{DS} = 1.0 V , f = 1.0 MHz	-	9440	-	pF	
			V _{DS} = 480 V , f = 1.0 MHz	-	200	-		
Effective Output Capacitance	C _{oss eff.}		V _{DS} = 0 V to 480 V ^c	-	260	-		
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 38 A, V _{DS} = 480 V, see fig. 6 and 13 ^b	-	-	330	nC	
Gate-Source Charge	Q _{gs}			-	-	84		
Gate-Drain Charge	Q _{gd}			-	-	150		
Turn-On Delay Time	t _{d(on)}		V _{GS} = 10 V	V _{DD} = 300 V, I _D = 38 A, R _G = 4.3 Ω, see fig. 10 ^b	-	47	-	ns
Rise Time	t _r				-	110	-	
Turn-Off Delay Time	t _{d(off)}	-			97	-		
Fall Time	t _f	-			60	-		
Drain-Source Body Diode Characteristics								
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	40	A	
Pulsed Diode Forward Current ^a	I _{SM}			-	-	160		
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 38 A, V _{GS} = 0 V ^b		-	-	1.5	V	
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C	I _F = 38 A, dI/dt = 100 A/μs	-	630	950	ns	
		T _J = 125 °C		-	730	1090		
Body Diode Reverse Recovery Charge	Q _{rr}	T _J = 25 °C		-	14	20	μC	
		T _J = 125 °C		-	17	25		
Body Diode Recovery Current	I _{RRM}	T _J = 25 °C		-	39	58	A	
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)						

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

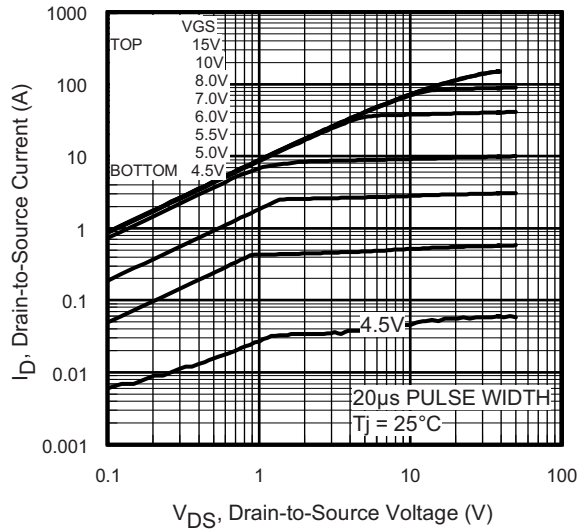


Fig. 1 - Typical Output Characteristics

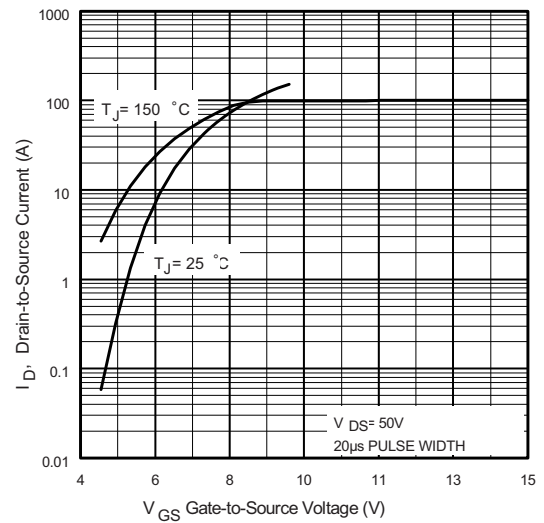


Fig. 3 - Typical Transfer Characteristics

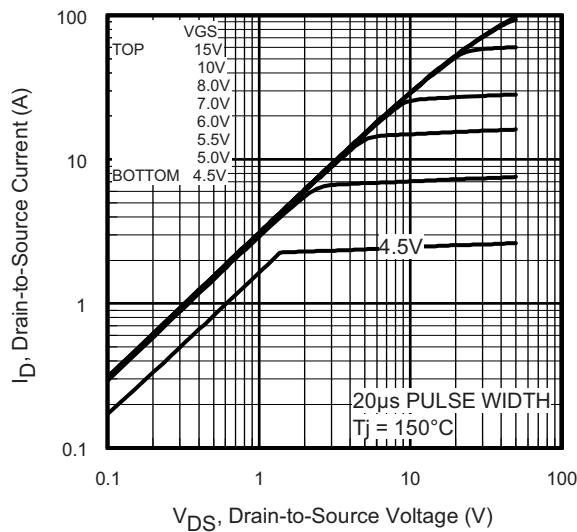


Fig. 2 - Typical Output Characteristics

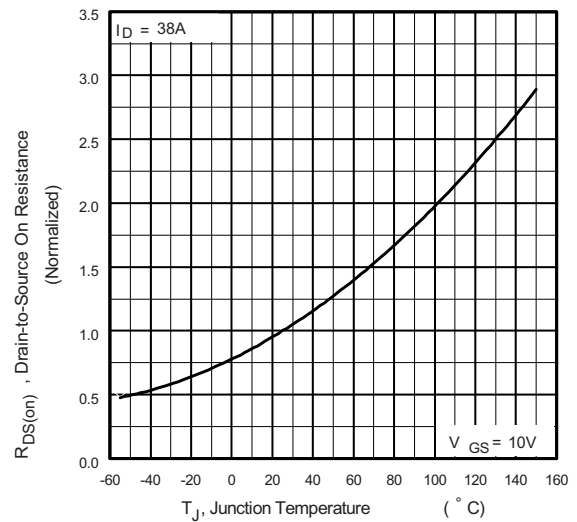


Fig. 4 - Normalized On-Resistance vs. Temperature

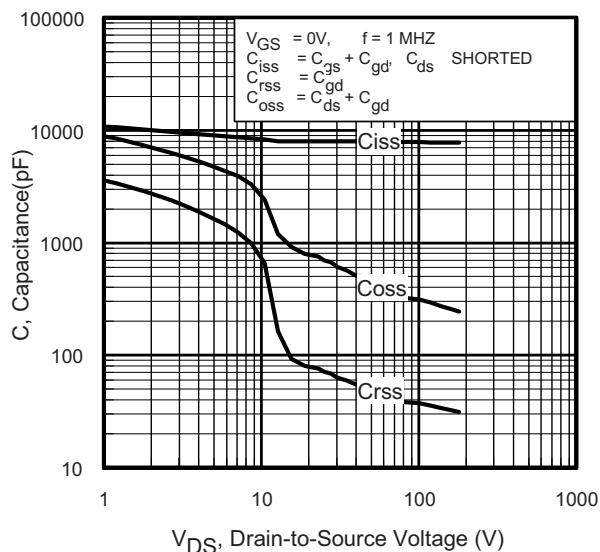


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

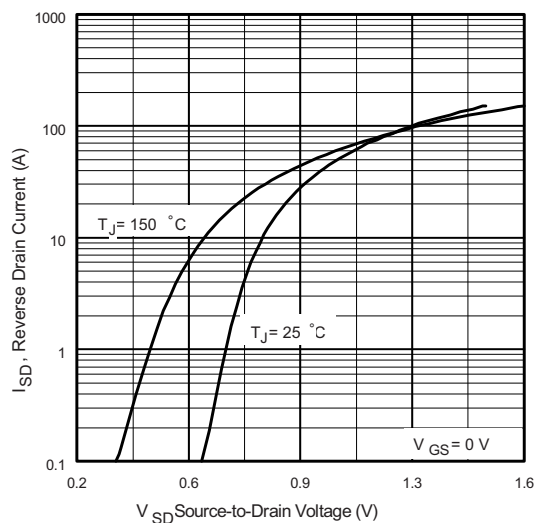


Fig. 7 - Typical Source-Drain Diode Forward Voltage

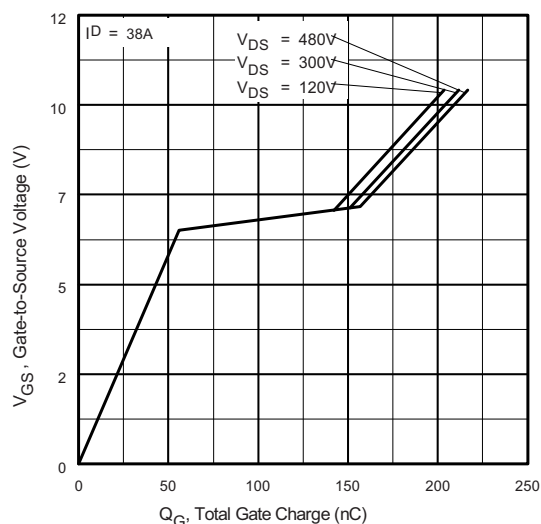


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

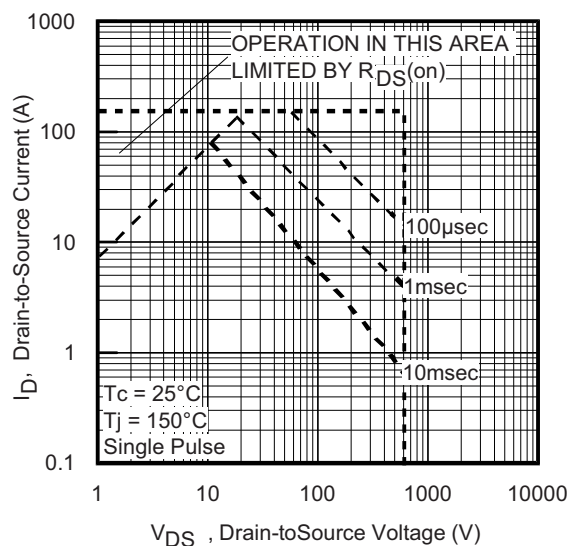


Fig. 8 - Maximum Safe Operating Area

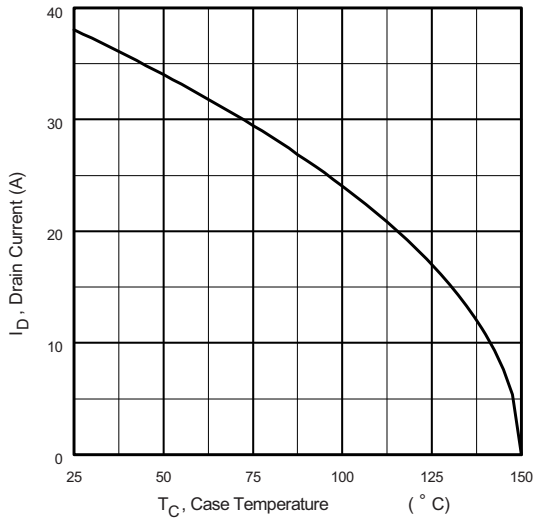


Fig. 9 - Maximum Drain Current vs. Case Temperature

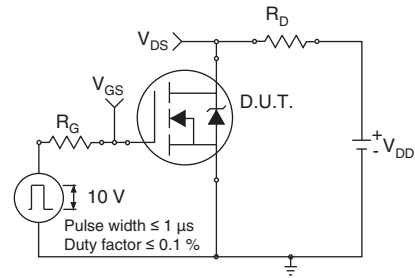


Fig. 10a - Switching Time Test Circuit

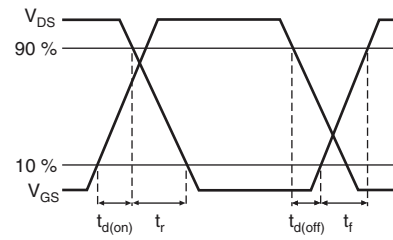


Fig. 10b - Switching Time Waveforms

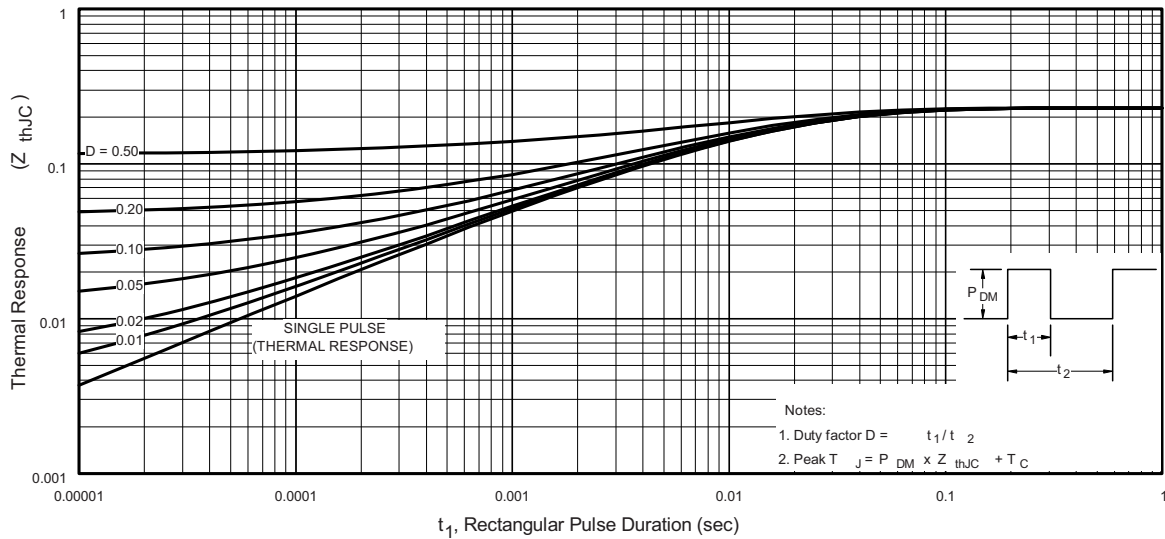


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

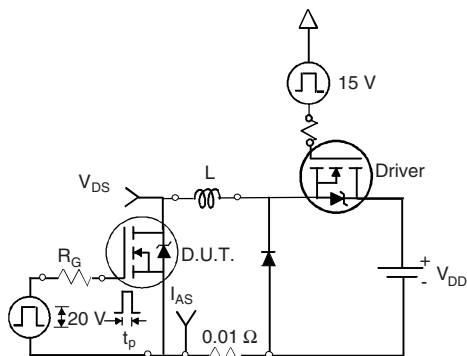


Fig. 12a - Unclamped Inductive Test Circuit

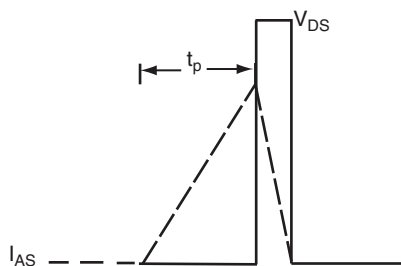


Fig. 12b - Unclamped Inductive Waveforms

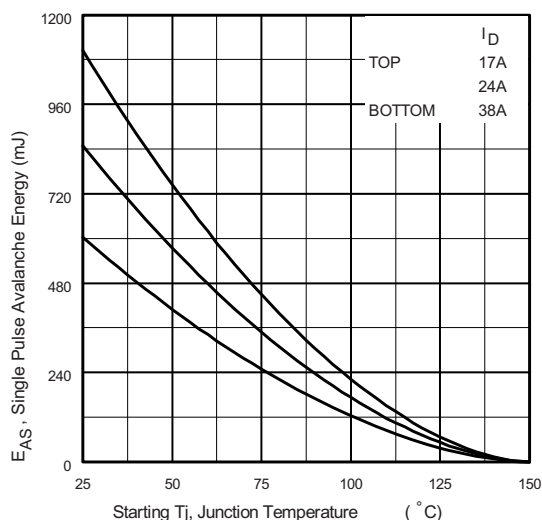


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

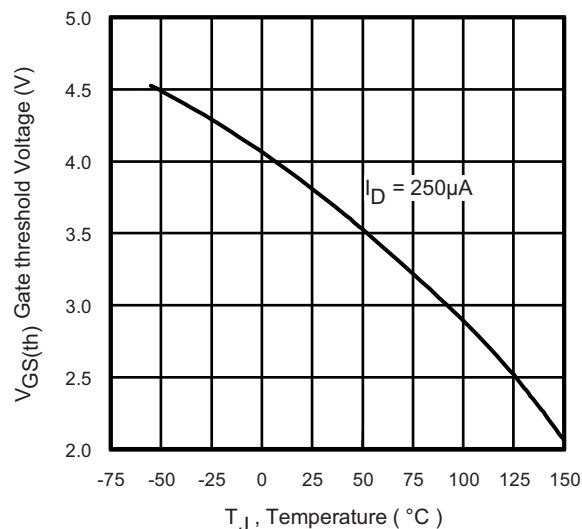


Fig. 12d - Threshold Voltage vs. Temperature

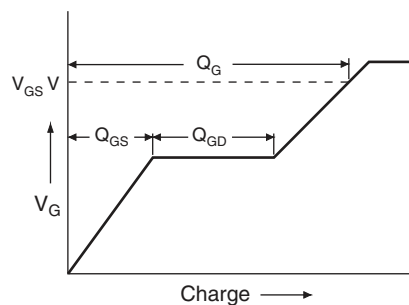


Fig. 13a - Basic Gate Charge Waveform

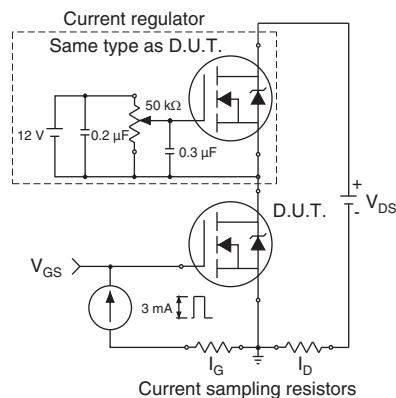
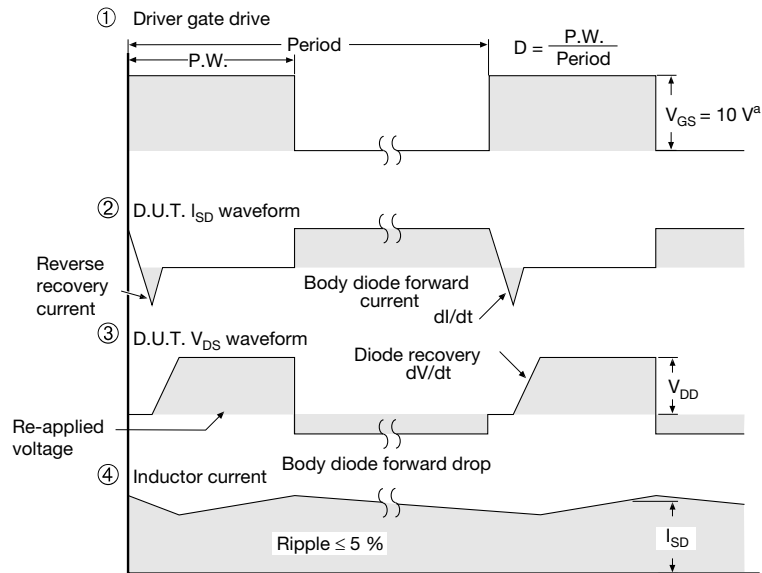
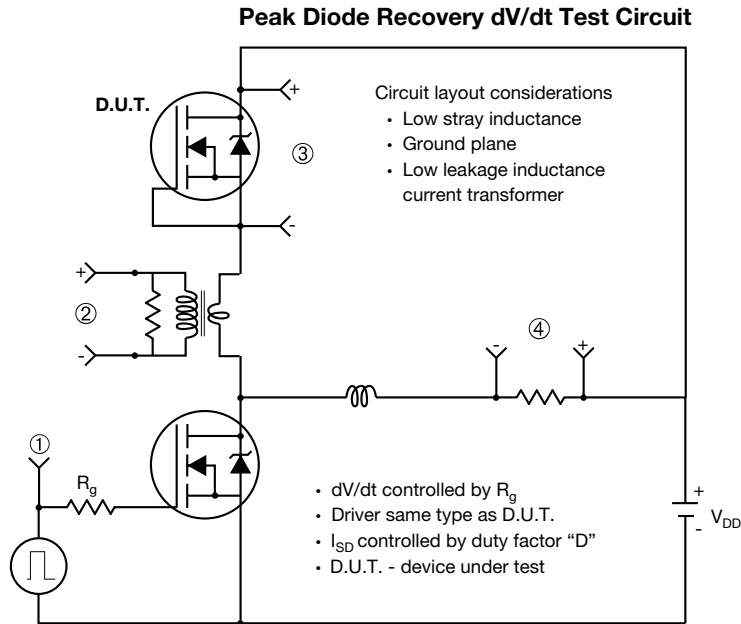


Fig. 13b - Gate Charge Test Circuit



Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

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