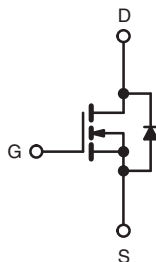
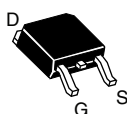


Power MOSFET

PRODUCT SUMMARY

V _{DS} (V)	100	
R _{DS(on)} (Ω)	V _{GS} = 10 V	0.54
Q _g (Max.) (nC)	8.3	
Q _{gs} (nC)	2.3	
Q _{gd} (nC)	3.8	
Configuration	Single	

**DPAK
(TO-252)**



N-Channel MOSFET

FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Surface Mount (IRFR110, SiHFR110)
- Available in Tape and Reel
- Fast Switching
- Ease of Paralleling
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE
Available

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The DPAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. Power dissipation levels up to 1.5 W are possible in typical surface mount applications.

ORDERING INFORMATION

Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)
Lead (Pb)-free and Halogen-free	SiHFR110-GE3	SiHFR110TRL-GE3	SiHFR110TR-GE3	SiHFR110TRR-GE3
Lead (Pb)-free	IRFR110PbF	IRFR110TRLPbF ^a	IRFR110TRPbF ^a	IRFR110TRRPbF ^a
	SiHFR110-E3	SiHFR110TL-E3 ^a	SiHFR110T-E3 ^a	SiHFR110TR-E3 ^a

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	100	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current	V _{GS} at 10 V	T _C = 25 °C	A
		T _C = 100 °C	
Pulsed Drain Current ^a	I _{DM}	17	W/°C
Linear Derating Factor		0.20	
Linear Derating Factor (PCB Mount) ^e		0.020	mJ
Single Pulse Avalanche Energy ^b	E _{AS}	75	
Repetitive Avalanche Current ^a	I _{AR}	4.3	A
Repetitive Avalanche Energy ^a	E _{AR}	2.5	mJ
Maximum Power Dissipation	P _D	T _C = 25 °C	W
Maximum Power Dissipation (PCB Mount) ^e		T _A = 25 °C	
Peak Diode Recovery dV/dt ^c	dV/dt	5.5	V/ns
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature) ^d	for 10 s	260	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- V_{DD} = 25 V, starting T_J = 25 °C, L = 8.1 mH, R_g = 25 Ω, I_{AS} = 4.3 A (see fig. 12).
- I_{SD} ≤ 5.6 A, dI/dt ≤ 75 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C.
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	110	°C/W
Maximum Junction-to-Ambient (PCB Mount) ^a	R_{thJA}	-	50	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	5.0	

Note

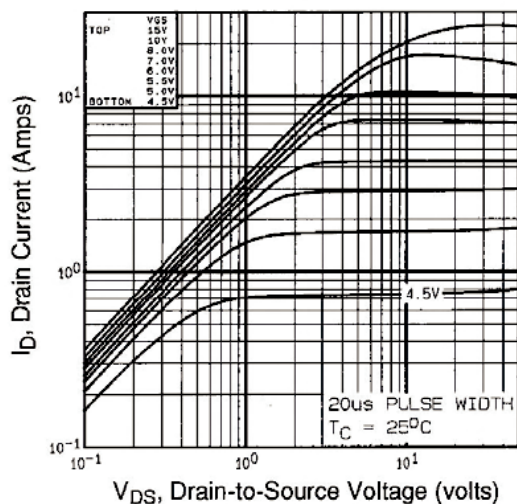
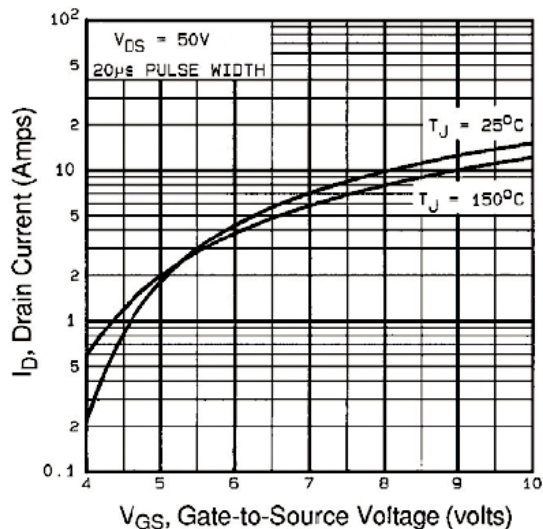
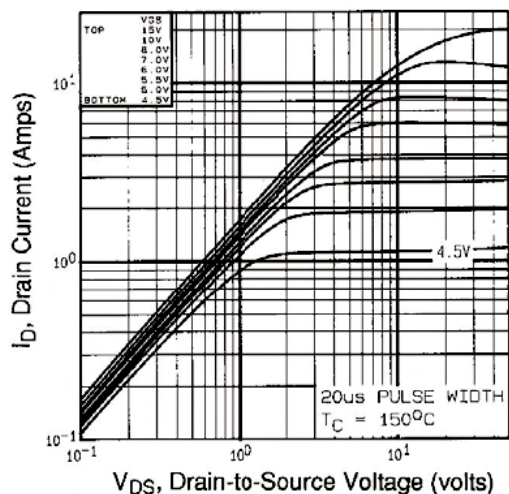
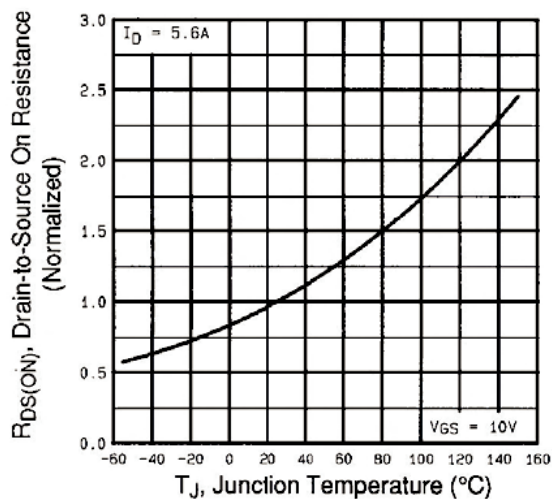
a. When mounted on 1" square PCB (FR-4 or G-10 material).

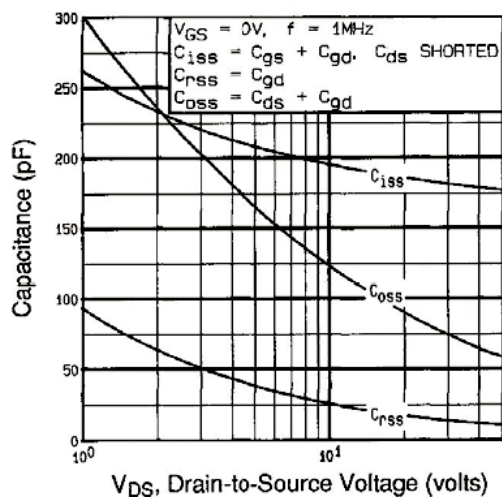
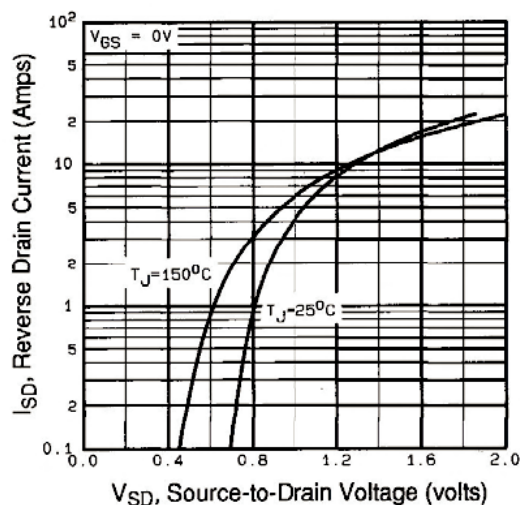
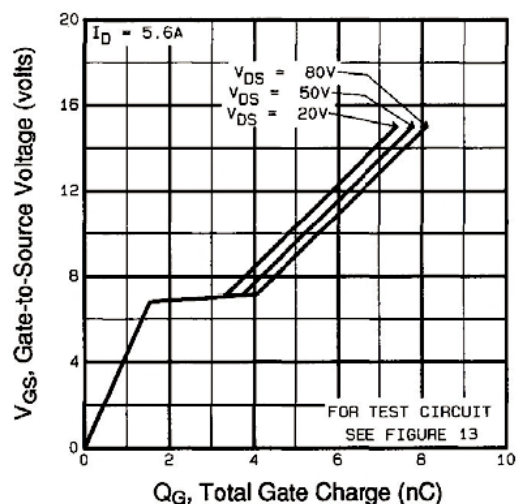
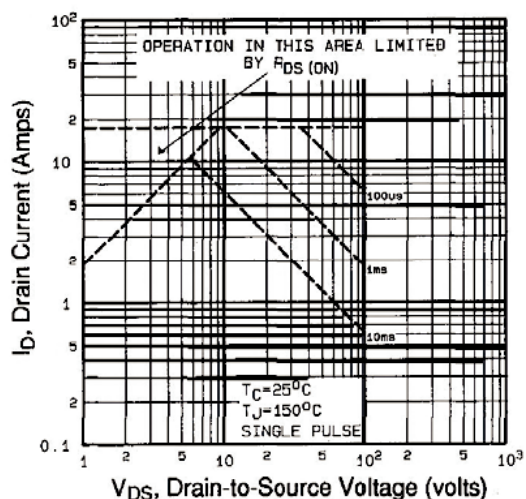
SPECIFICATIONS ($T_J = 25\text{ °C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		100	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.13	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V		-	-	25	μA
		V _{DS} = 80 V, V _{GS} = 0 V, T _J = 125 °C		-	-	250	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 2.6 A ^b	-	-	0.54	Ω
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 2.6 A		1.6	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	180	-	pF
Output Capacitance	C _{oss}			-	80	-	
Reverse Transfer Capacitance	C _{rss}			-	15	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 5.6 A, V _{DS} = 80 V, see fig. 6 and 13 ^b	-	-	8.3	nC
Gate-Source Charge	Q _{gs}			-	-	2.3	
Gate-Drain Charge	Q _{gd}			-	-	3.8	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 50 V, I _D = 5.6 A, R _g = 24 Ω, R _D = 8.4 Ω, see fig. 10 ^b		-	6.9	-	ns
Rise Time	t _r			-	16	-	
Turn-Off Delay Time	t _{d(off)}			-	15	-	
Fall Time	t _f			-	9.4	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal Source Inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	4.3	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	17	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 4.3 A, V _{GS} = 0 V ^b		-	-	2.5	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 5.6 A, dI/dt = 100 A/μs ^b		-	100	200	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	0.44	0.88	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics, $T_C = 25^\circ\text{C}$

Fig. 3 - Typical Transfer Characteristics

Fig. 2 - Typical Output Characteristics, $T_C = 150^\circ\text{C}$

Fig. 4 - Normalized On-Resistance vs. Temperature


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 7 - Typical Source-Drain Diode Forward Voltage

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 8 - Maximum Safe Operating Area

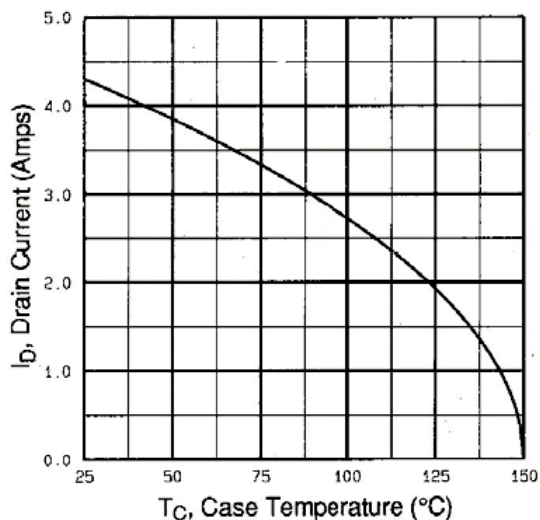
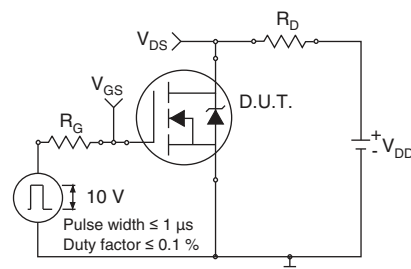
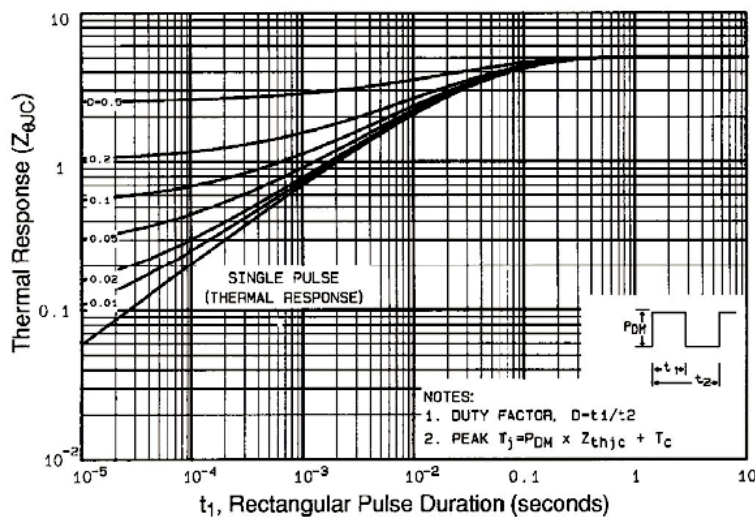
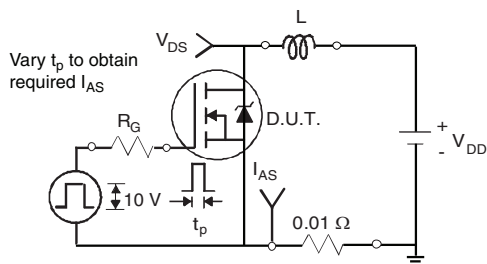
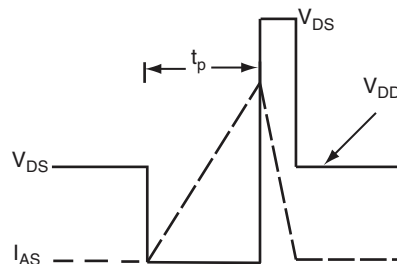
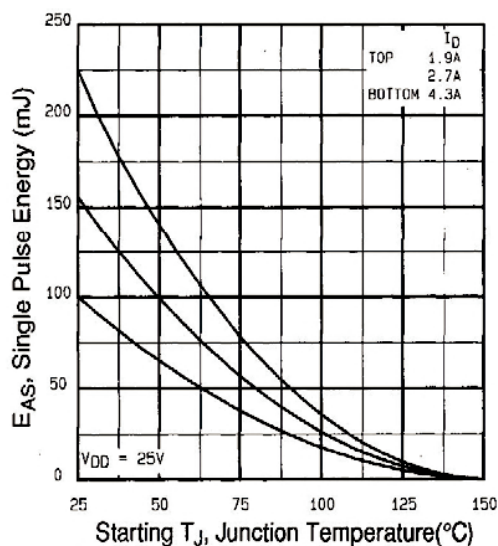
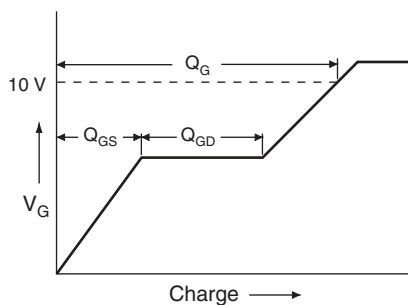
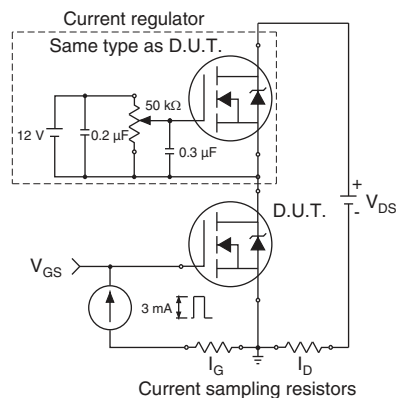
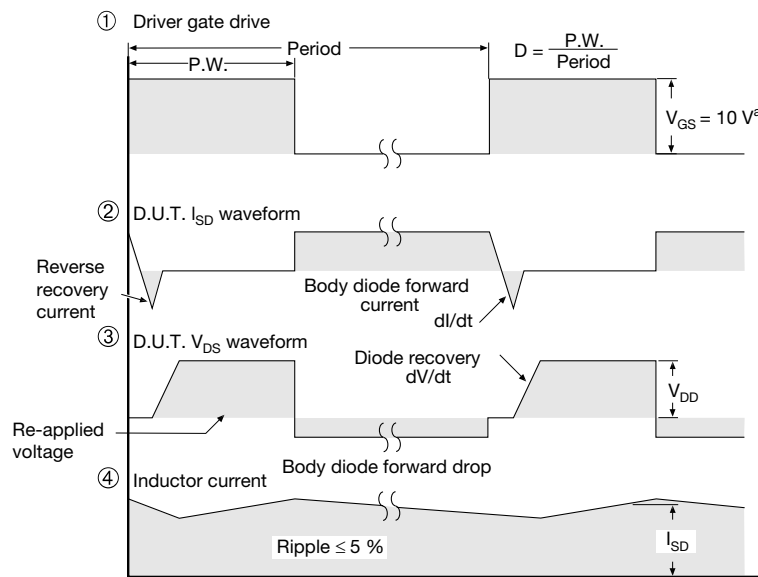
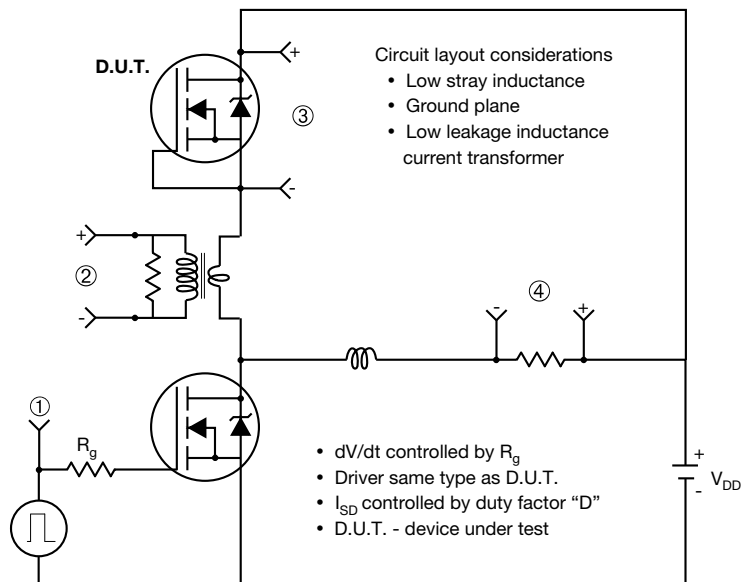

Fig. 9 - Maximum Drain Current vs. Case Temperature

Fig. 10a - Switching Time Test Circuit

Fig. 10b - Switching Time Waveforms

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig. 12a - Unclamped Inductive Test Circuit

Fig. 12b - Unclamped Inductive Waveforms


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

Fig. 13a - Basic Gate Charge Waveform

Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91265.



TO-252AA Case Outline



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060
ECN: T16-0236-Rev. P, 16-May-16 DWG: 5347				

Notes

- Dimension L3 is for reference only.

TO-251AA (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.39	0.086	0.094
A1	0.89	1.14	0.035	0.045
b	0.64	0.89	0.025	0.035
b1	0.65	0.79	0.026	0.031
b2	0.76	1.14	0.030	0.045
b3	0.76	1.04	0.030	0.041
b4	4.95	5.46	0.195	0.215
c	0.46	0.61	0.018	0.024
c1	0.41	0.56	0.016	0.022
c2	0.46	0.86	0.018	0.034
D	5.97	6.22	0.235	0.245

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
e	2.29 BSC		2.29 BSC	
L	8.89	9.65	0.350	0.380
L1	1.91	2.29	0.075	0.090
L2	0.89	1.27	0.035	0.050
L3	1.14	1.52	0.045	0.060
θ1	0°	15°	0°	15°
θ2	25°	35°	25°	35°

ECN: S-82111-Rev. A, 15-Sep-08
DWG: 5968

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension are shown in inches and millimeters.
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.13 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
4. Thermal pad contour optional with dimensions b4, L2, E1 and D1.
5. Lead dimension uncontrolled in L3.
6. Dimension b1, b3 and c1 apply to base metal only.
7. Outline conforms to JEDEC outline TO-251AA.

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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