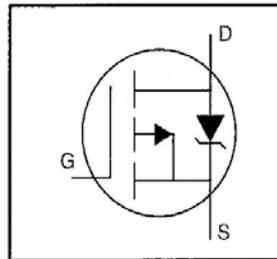


- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Surface Mount (IRFR9110)
- Straight Lead (IRFU9110)
- Available in Tape & Reel
- P-Channel
- Fast Switching
- Lead-Free



$$V_{DSS} = -100V$$

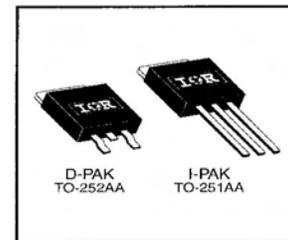
$$R_{DS(on)} = 1.2\Omega$$

$$I_D = -3.1A$$

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D-Pak is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.



Absolute Maximum Ratings

| | Parameter | Max. | Units |
|---------------------------|--|-----------------------|-------|
| $I_D @ T_C = 25^\circ C$ | Continuous Drain Current, $V_{GS} @ -10 V$ | -3.1 | A |
| $I_D @ T_C = 100^\circ C$ | Continuous Drain Current, $V_{GS} @ -10 V$ | -2.0 | |
| I_{DM} | Pulsed Drain Current ① | -12 | |
| $P_D @ T_C = 25^\circ C$ | Power Dissipation | 25 | W |
| $P_D @ T_A = 25^\circ C$ | Power Dissipation (PCB Mount)** | 2.5 | |
| | Linear Derating Factor | 0.20 | W/°C |
| | Linear Derating Factor (PCB Mount)** | 0.020 | |
| V_{GS} | Gate-to-Source Voltage | ± 20 | V |
| E_{AS} | Single Pulse Avalanche Energy ② | 140 | mJ |
| I_{AR} | Avalanche Current ① | -3.1 | A |
| E_{AR} | Repetitive Avalanche Energy ① | 2.5 | mJ |
| dv/dt | Peak Diode Recovery dv/dt ③ | -5.5 | V/ns |
| T_J, T_{STG} | Junction and Storage Temperature Range | -55 to +150 | °C |
| | Soldering Temperature, for 10 seconds | 260 (1.6mm from case) | |

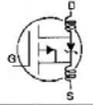
Thermal Resistance

| | Parameter | Min. | Typ. | Max. | Units |
|-----------------|-----------------------------------|------|------|------|-------|
| $R_{\theta JC}$ | Junction-to-Case | --- | --- | 5.0 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient (PCB mount)** | --- | --- | 50 | |
| $R_{\theta JA}$ | Junction-to-Ambient | --- | --- | 110 | |

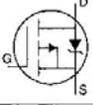
** When mounted on 1" square PCB (FR-4 or G-10 Material).

For recommended footprint and soldering techniques refer to application note #AN-994.

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

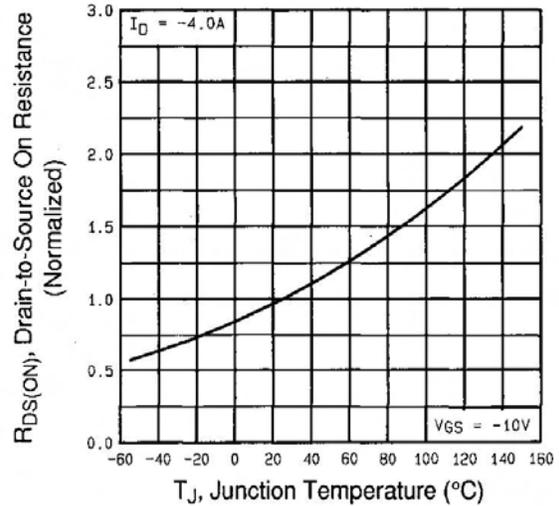
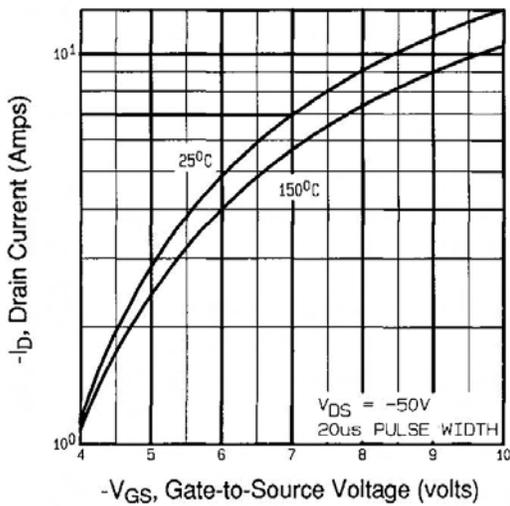
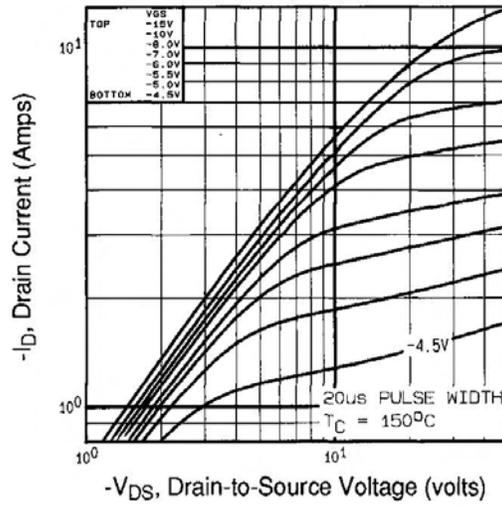
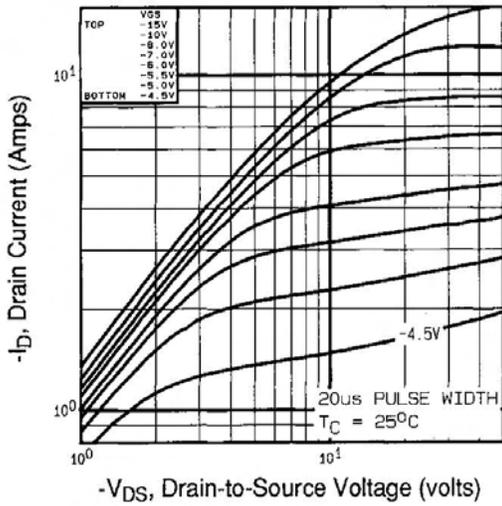
| | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
|--|--------------------------------------|------|--------|------|-------|--|
| V _{(BR)DSS} | Drain-to-Source Breakdown Voltage | -100 | — | — | V | V _{GS} =0V, I _D =-250μA |
| ΔV _{(BR)DSS} /ΔT _J | Breakdown Voltage Temp. Coefficient | — | -0.093 | — | V/°C | Reference to 25°C, I _D =-1mA |
| R _{DS(on)} | Static Drain-to-Source On-Resistance | — | — | 1.2 | Ω | V _{GS} =-10V, I _D =-1.9A ④ |
| V _{GS(th)} | Gate Threshold Voltage | -2.0 | — | -4.0 | V | V _{DS} =V _{GS} , I _D =-250μA |
| g _{fs} | Forward Transconductance | 0.97 | — | — | S | V _{DS} =-50V, I _D =-1.9A ④ |
| I _{DSS} | Drain-to-Source Leakage Current | — | — | -100 | μA | V _{DS} =-100V, V _{GS} =0V |
| | | — | — | -500 | μA | V _{DS} =-80V, V _{GS} =0V, T _J =125°C |
| I _{GSS} | Gate-to-Source Forward Leakage | — | — | -100 | nA | V _{GS} =-20V |
| | Gate-to-Source Reverse Leakage | — | — | 100 | nA | V _{GS} =20V |
| Q _g | Total Gate Charge | — | — | 8.7 | nC | I _D =-4.0A |
| Q _{gs} | Gate-to-Source Charge | — | — | 2.2 | nC | V _{DS} =-80V |
| Q _{gd} | Gate-to-Drain ("Miller") Charge | — | — | 4.1 | nC | V _{GS} =-10V See Fig. 6 and 13 ④ |
| t _{d(on)} | Turn-On Delay Time | — | 10 | — | ns | V _{DD} =-50V |
| t _r | Rise Time | — | 27 | — | | I _D =-4.0A |
| t _{d(off)} | Turn-Off Delay Time | — | 15 | — | | R _G =24Ω |
| t _f | Fall Time | — | 17 | — | | R _D =11Ω See Figure 10 ④ |
| L _D | Internal Drain Inductance | — | 4.5 | — | nH | Between lead, 6 mm (0.25in.) from package and center of die contact |
| L _S | Internal Source Inductance | — | 7.5 | — | |  |
| C _{iss} | Input Capacitance | — | 200 | — | pF | V _{GS} =0V |
| C _{oss} | Output Capacitance | — | 94 | — | | V _{DS} =-25V |
| C _{rss} | Reverse Transfer Capacitance | — | 18 | — | | f=1.0MHz See Figure 5 |

Source-Drain Ratings and Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
|-----------------|--|--|------|------|-------|--|
| I _S | Continuous Source Current (Body Diode) | — | — | -3.1 | A | MOSFET symbol showing the integral reverse p-n junction diode.  |
| I _{SM} | Pulsed Source Current (Body Diode) ① | — | — | -12 | | |
| V _{SD} | Diode Forward Voltage | — | — | -5.5 | V | T _J =25°C, I _S =-3.1A, V _{GS} =0V ④ |
| t _{rr} | Reverse Recovery Time | — | 80 | 160 | ns | T _J =25°C, I _F =-4.0A |
| Q _{rr} | Reverse Recovery Charge | — | 0.17 | 0.30 | μC | di/dt=100A/μs ④ |
| t _{on} | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D) | | | | |

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ② V_{DD}=-25V, starting T_J=25°C, L=21mH R_G=25Ω, I_{AS}=-3.1A (See Figure 12)
- ③ I_{SD}≤-4.0A, di/dt≤75A/μs, V_{DD}≤V_{(BR)DSS}, T_J≤150°C
- ④ Pulse width ≤ 300 μs; duty cycle ≤2%.



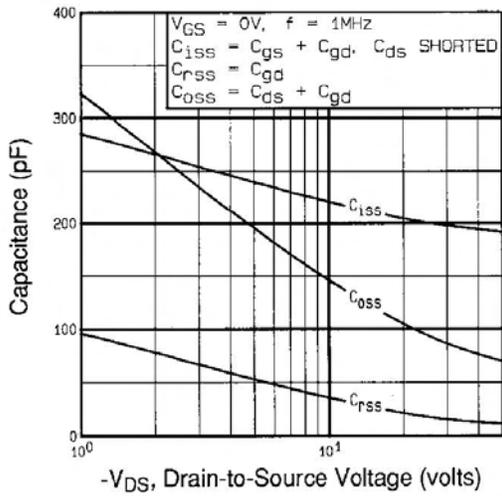


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

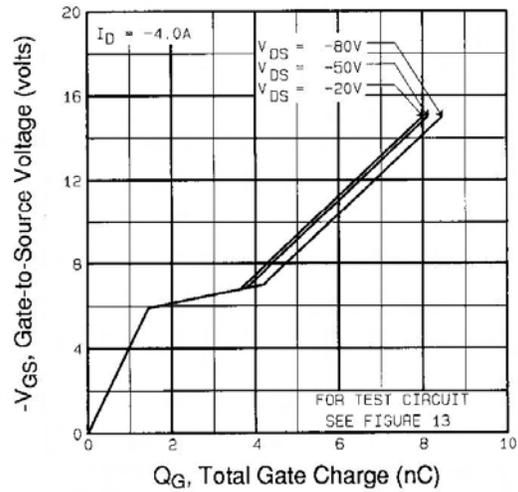


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

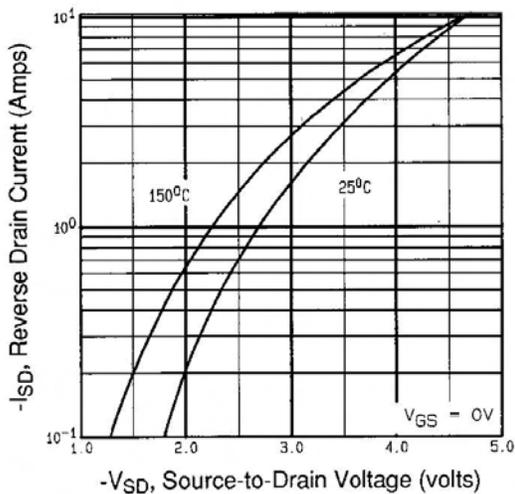


Fig 7. Typical Source-Drain Diode Forward Voltage

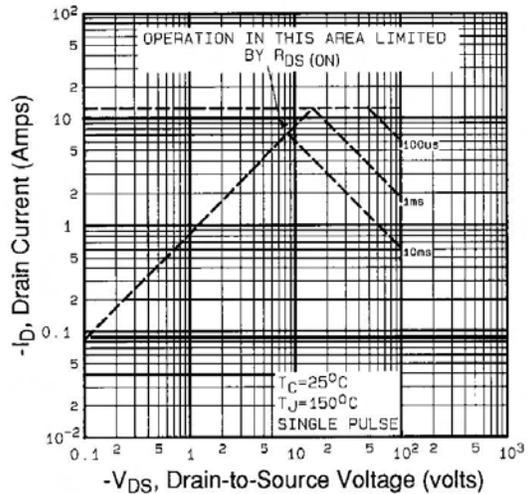


Fig 8. Maximum Safe Operating Area

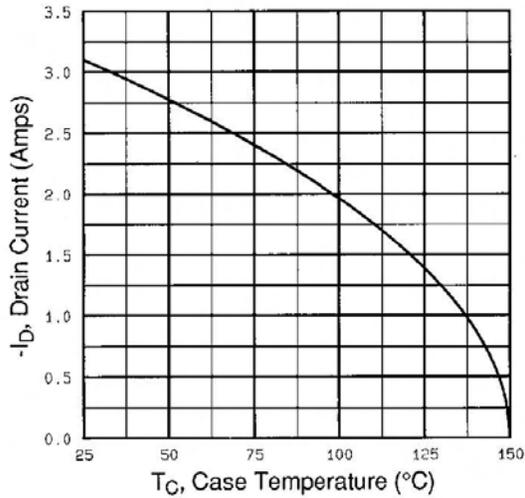


Fig 9. Maximum Drain Current Vs. Case Temperature

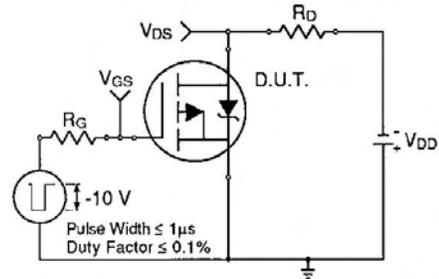


Fig 10a. Switching Time Test Circuit

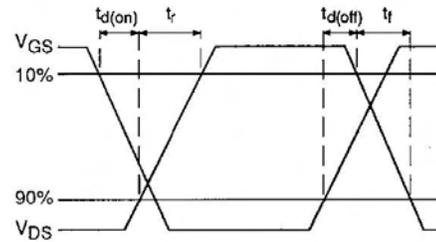


Fig 10b. Switching Time Waveforms

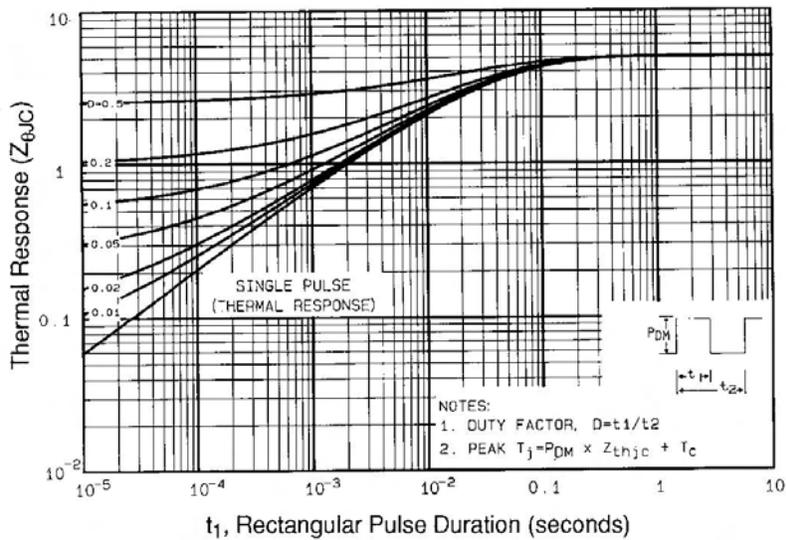


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

IRFR/U9110PbF

International
IR Rectifier

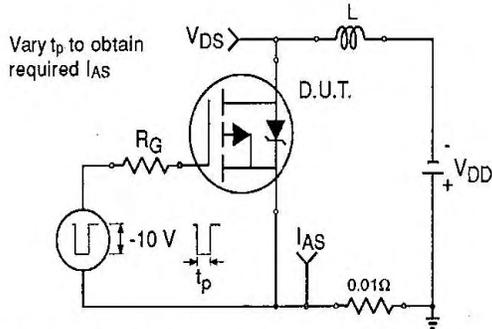


Fig 12a. Unclamped Inductive Test Circuit

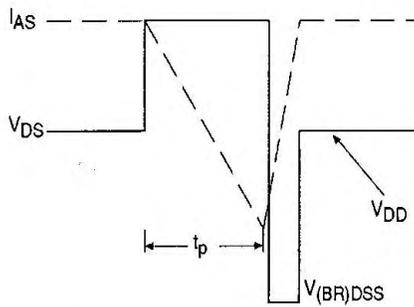


Fig 12b. Unclamped Inductive Waveforms

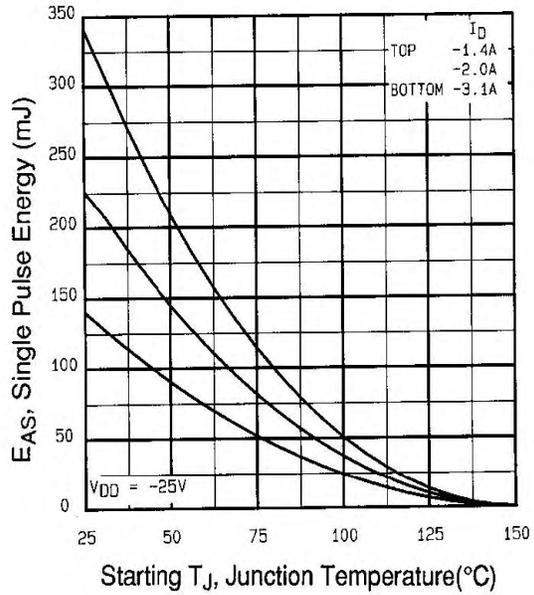


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

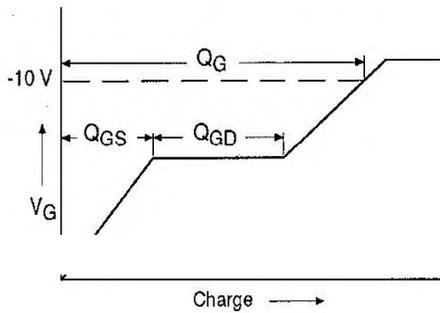


Fig 13a. Basic Gate Charge Waveform

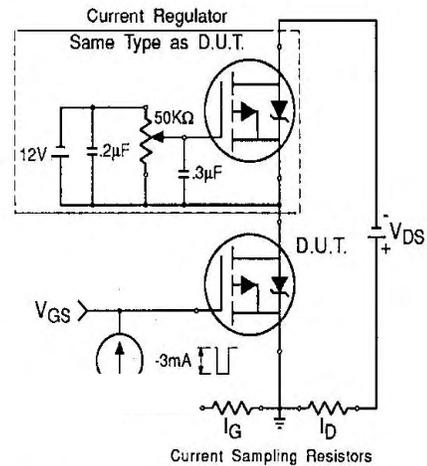
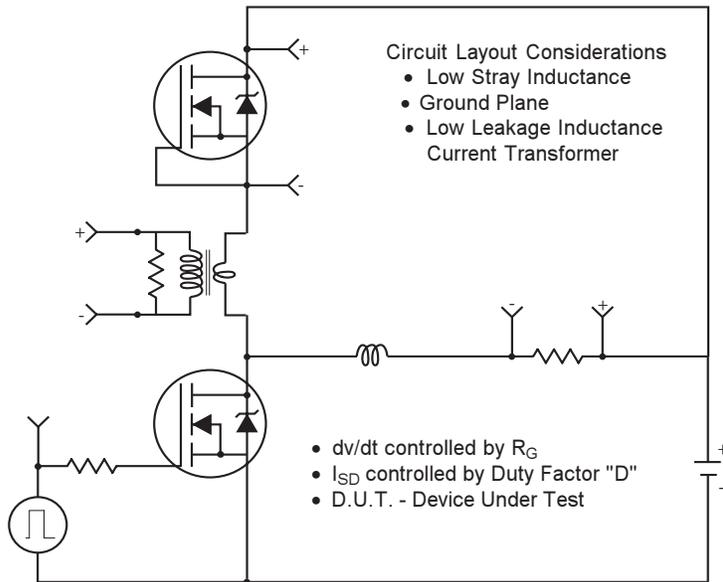


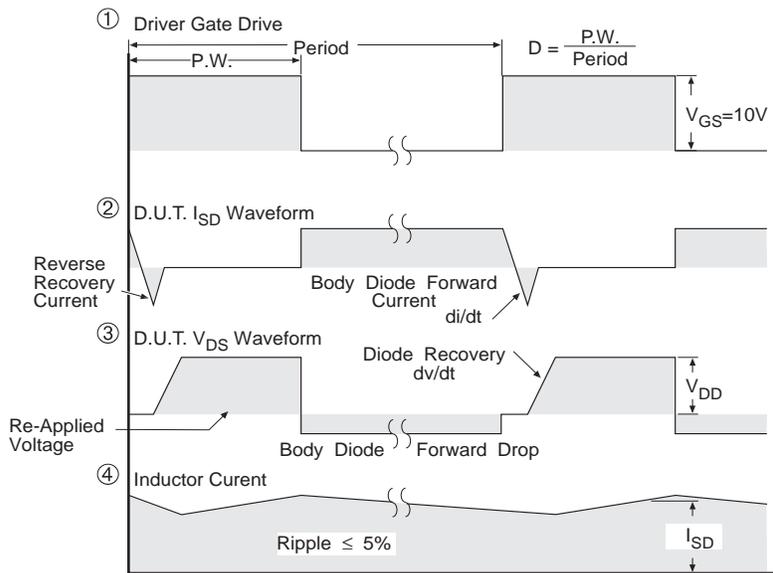
Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity for P-Channel

** Use P-Channel Driver for P-Channel Measurements



*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

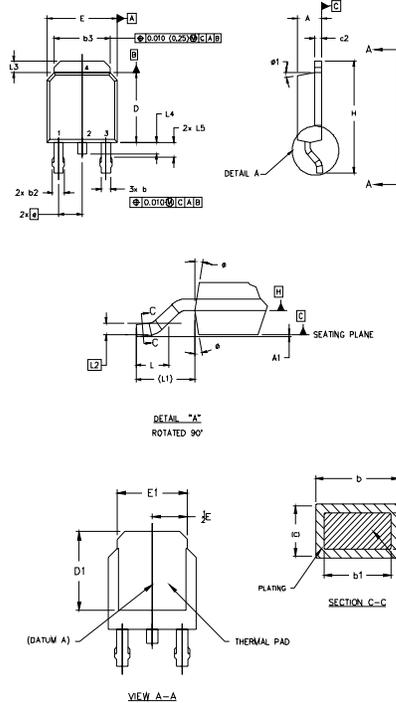
Fig 14 For P Channel HEXFETS

IRFR/U9110PbF

International
IR Rectifier

D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

- 1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
- 2.0 DIMENSIONS ARE SHOWN IN INCHES (MILLIMETERS).
- 3.0 LEAD DIMENSION UNCONTROLLED IN L5
- 4.0 DIMENSION D1 AND E1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.0 SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 (0.127) AND .010 [0.2540 FROM THE LEAD TIP.
- 6.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 7.0 OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

| SYMBOL | DIMENSIONS | | | | NOTES |
|--------|-------------|-------|-----------|-------|-------|
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | 2.18 | 2.30 | .086 | .094 | |
| A1 | | 0.13 | | .005 | |
| b | 0.64 | 0.89 | .025 | .035 | 5 |
| b1 | 0.64 | 0.79 | .025 | 0.031 | 5 |
| b2 | 0.76 | 1.14 | .030 | .045 | |
| b3 | 4.95 | 5.46 | .195 | .215 | |
| c | 0.46 | 0.61 | .018 | .024 | 5 |
| c1 | 0.41 | 0.56 | .016 | .022 | 5 |
| c2 | .046 | 0.89 | .018 | .035 | 5 |
| D | 5.97 | 6.22 | .235 | .245 | 6 |
| D1 | 5.21 | - | .205 | - | 4 |
| E | 6.35 | 6.73 | .250 | .265 | 6 |
| E1 | 4.32 | - | .170 | - | 4 |
| e | 2.29 | | .090 BSC | | |
| H | 9.40 | 10.41 | .370 | .410 | |
| L | 1.40 | 1.78 | .055 | .070 | |
| L1 | 2.74 REF. | | .108 REF. | | |
| L2 | 0.051 BSC | | .020 BSC | | |
| L3 | 0.89 | 1.27 | .035 | .050 | |
| L4 | 1.14 | 1.52 | .045 | .060 | |
| L5 | | | | | 3 |
| ø | Ø | 10' | Ø | 10' | |
| ø1 | Ø | 15' | Ø | 15' | |

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

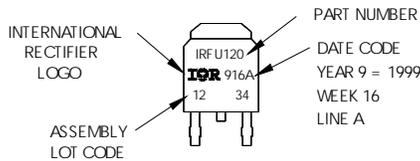
IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

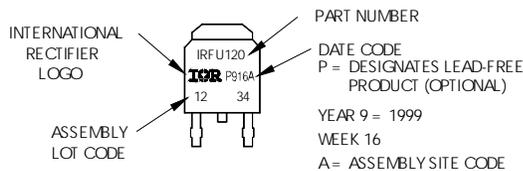
D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW 16, 1999
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position
indicates "Lead-Free"



OR



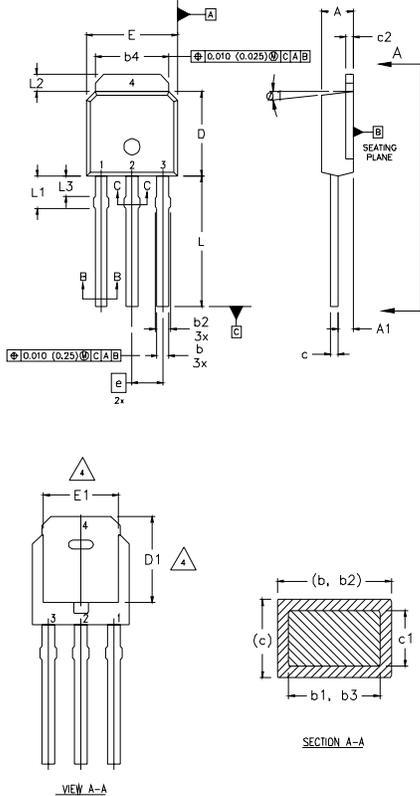
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I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

- 1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
- 2 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 3 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 4 THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
- 5 LEAD DIMENSION UNCONTROLLED IN L3.
- 6 DIMENSION b1, b3 APPLY TO BASE METAL ONLY.
- 7 OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA.
- 8 CONTROLLING DIMENSION : INCHES.

LEAD ASSIGNMENTS

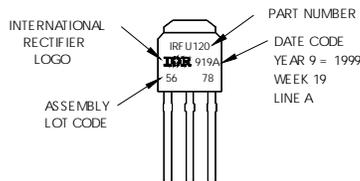
HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

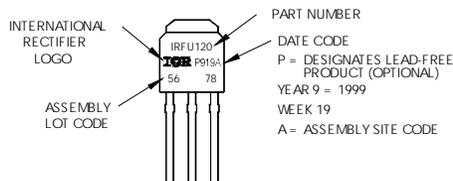
| SYMBOL | DIMENSIONS | | | | NOTES |
|--------|-------------|------|-----------|-------|-------|
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | 2.18 | 2.39 | 0.086 | .094 | |
| A1 | 0.89 | 1.14 | 0.035 | 0.045 | |
| b | 0.64 | 0.89 | 0.025 | 0.035 | |
| b1 | 0.64 | 0.79 | 0.025 | 0.031 | 4 |
| b2 | 0.76 | 1.14 | 0.030 | 0.045 | |
| b3 | 0.76 | 1.04 | 0.030 | 0.041 | |
| b4 | 5.00 | 5.46 | 0.195 | 0.215 | 4 |
| c | 0.46 | 0.61 | 0.018 | 0.024 | |
| c1 | 0.41 | 0.56 | 0.016 | 0.022 | |
| c2 | .046 | 0.86 | 0.018 | 0.035 | |
| D | 5.97 | 6.22 | 0.235 | 0.245 | 3, 4 |
| D1 | 5.21 | - | 0.205 | - | 4 |
| E | 6.35 | 6.73 | 0.250 | 0.265 | 3, 4 |
| E1 | 4.32 | - | 0.170 | - | 4 |
| e | 2.29 | | 0.090 BSC | | |
| L | 8.89 | 9.60 | 0.350 | 0.380 | |
| L1 | 1.91 | 2.29 | 0.075 | 0.090 | |
| L2 | 0.89 | 1.27 | 0.035 | 0.050 | 4 |
| L3 | 1.14 | 1.52 | 0.045 | 0.060 | 5 |
| ø1 | Ø | 15' | Ø | 15' | |

I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120 WITH ASSEMBLY LOT CODE 5678 ASSEMBLED ON VW 19, 1999 IN THE ASSEMBLY LINE "A"
Note: "P" in ass embly line position indicates "Lead-Free"



OR

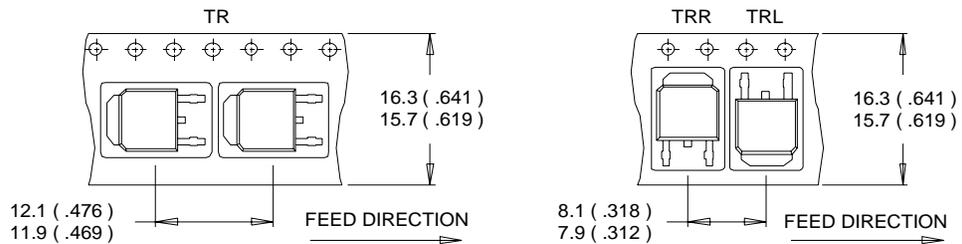


IRFR/U9110PbF

International
IR Rectifier

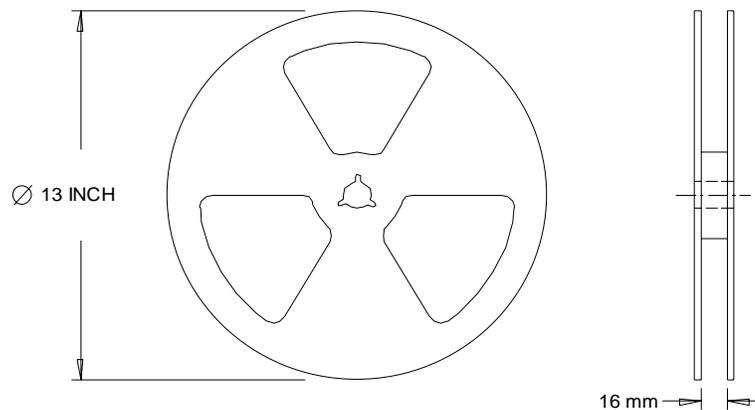
D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Data and specifications subject to change without notice.

International
IR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105

TAC Fax: (310) 252-7903

12/04

Document Number: 91279

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Specifications of the products displayed herein are subject to change without notice. Vishay Intertechnology, Inc., or anyone on its behalf, assumes no responsibility or liability for any errors or inaccuracies.

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The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Vishay for any damages resulting from such improper use or sale.

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