International **IGR** Rectifier

SMPS MOSFET

IRFS9N60A

HEXFET® Power MOSFET

Applications
- Switch Mode Power Supply (SMPS)
- Uninterruptable Power Supply
- High Speed Power Switching

V_{DSS}	R_{DS}(on) max	I_D
600V	0.75Ω	9.2A

Benefits
- Low Gate Charge Qg results in Simple Drive Requirement
- Improved Gate, Avalanche and dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current

G D S

D²Pak
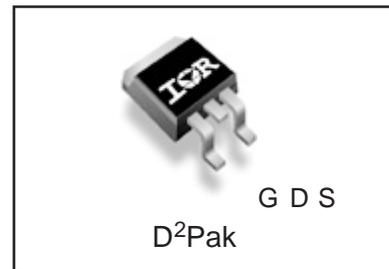
Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	9.2	
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	5.8	A
I_{DM}	Pulsed Drain Current ①	37	
P_D @T_C = 25°C	Power Dissipation	170	W
	Linear Derating Factor	1.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J	Operating Junction and	-55 to + 150	
T_{STG}	Storage Temperature Range		°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Applicable Off Line SMPS Topologies:

- Active Clamped Forward
- Main Switch

Notes ① through ⑤ are on page 9

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Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	600	——	——	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.66	——	V/°C	Reference to 25°C, I_D = 1mA⑥
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	——	0.75	Ω	V_{GS} = 10V, I_D = 5.5.A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
I_{DSS}	Drain-to-Source Leakage Current	——	——	25	µA	V_{DS} = 600V, V_{GS} = 0V
		——	——	250		V_{DS} = 480V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 30V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -30V

Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	5.5	——	——	S	V_{DS} = 25V, I_D = 3.1A
Q_g	Total Gate Charge	——	——	49	nC	I_D = 9.2A
Q_{gs}	Gate-to-Source Charge	——	——	13		V_{DS} = 400V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	——	20		V_{GS} = 10V, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	——	13	——	ns	V_{DD} = 300V
t_r	Rise Time	——	25	——		I_D = 9.2A
$t_{d(off)}$	Turn-Off Delay Time	——	30	——		R_G = 9.1Ω
t_f	Fall Time	——	22	——		R_D = 35.5Ω,See Fig. 10 ④
C_{iss}	Input Capacitance	——	1400	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	180	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	7.1	——		f = 1.0MHz, See Fig. 5
C_{oss}	Output Capacitance	——	1957	——		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	——	49	——		V_{GS} = 0V, V_{DS} = 480V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	——	96	——		V_{GS} = 0V, V_{DS} = 0V to 480V ⑤

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	——	290	mJ
I_{AR}	Avalanche Current①	——	9.2	A
E_{AR}	Repetitive Avalanche Energy①	——	17	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	0.75	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted,steady-state)	——	40	°C/W

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	9.2	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	37		
V_{SD}	Diode Forward Voltage	——	——	1.5	V	T_J = 25°C, I_S = 9.2A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	530	800	ns	T_J = 25°C, I_F = 9.2A
Q_{rr}	Reverse RecoveryCharge	——	3.0	4.4	µC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				
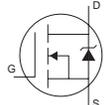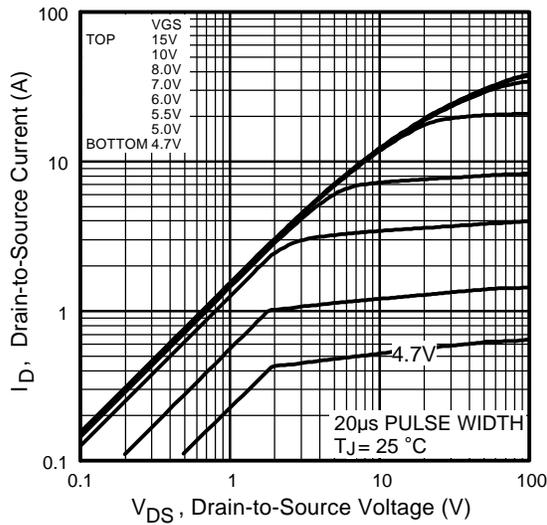
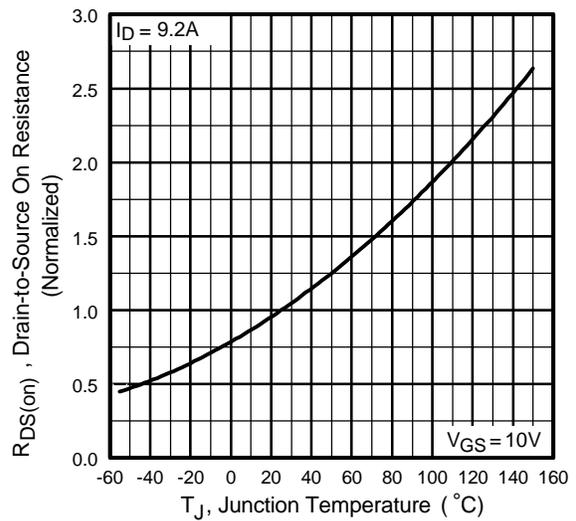2   www.irf.com
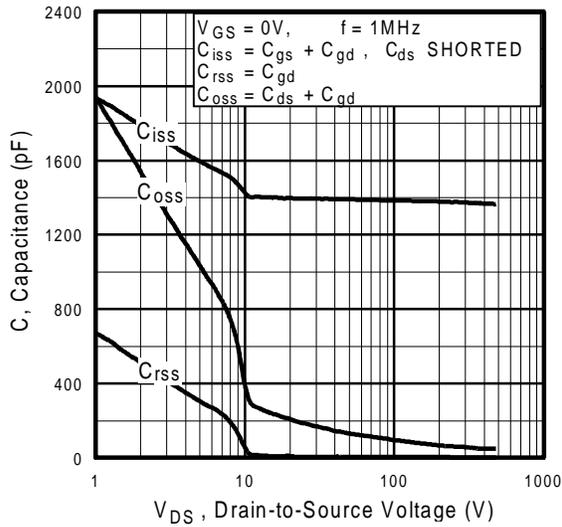
Fig 1. Typical Output Characteristics

VGS
TOP   15V
      10V
      8.0V
      7.0V
      6.0V
      5.5V
      5.0V
BOTTOM 4.7V

4.7V

20μs PULSE WIDTH
T_J = 25 °C

I_D, Drain-to-Source Current (A)

V_{DS}, Drain-to-Source Voltage (V)

Fig 2. Typical Output Characteristics

VGS
TOP   15V
      10V
      8.0V
      7.0V
      6.0V
      5.5V
      5.0V
BOTTOM 4.7V

4.7V

20μs PULSE WIDTH
T_J = 150 °C

I_D, Drain-to-Source Current (A)
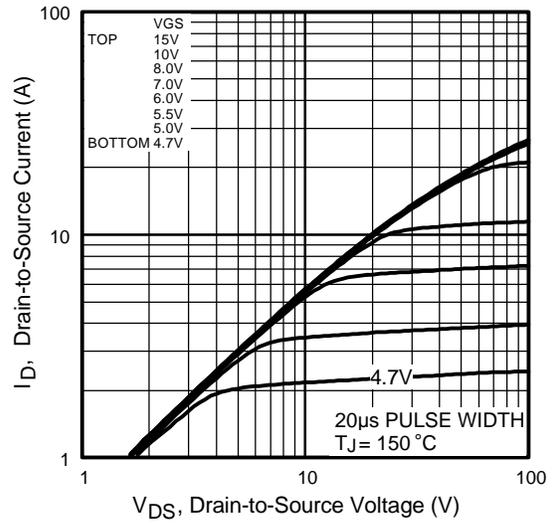
V_{DS}, Drain-to-Source Voltage (V)
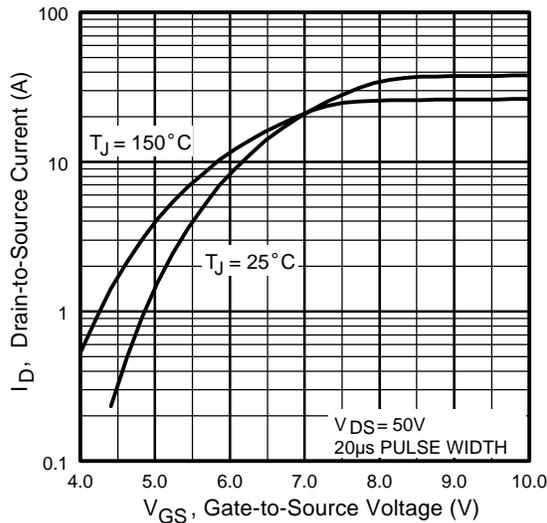
Fig 3. Typical Transfer Characteristics

T_J = 150 °C

T_J = 25 °C

V_{DS} = 50V
20μs PULSE WIDTH

I_D, Drain-to-Source Current (A)

V_{GS}, Gate-to-Source Voltage (V)

Fig 4. Normalized On-Resistance
Vs. Temperature

I_D = 9.2A

V_{GS} = 10V

$R_{DS(on)}$, Drain-to-Source On Resistance (Normalized)

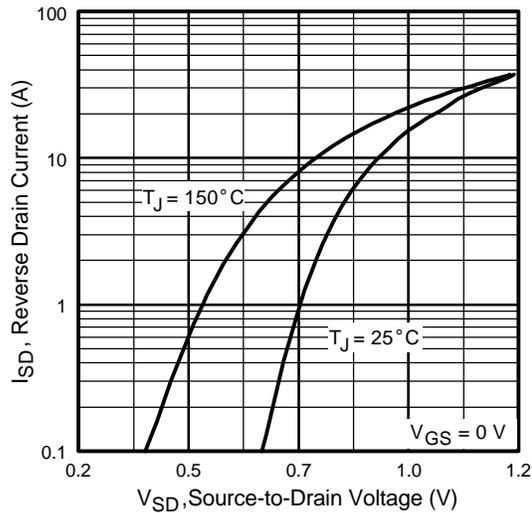T_J, Junction Temperature (°C)
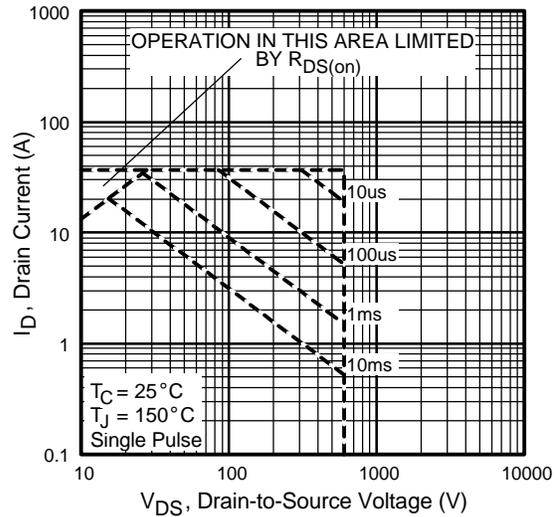
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Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage
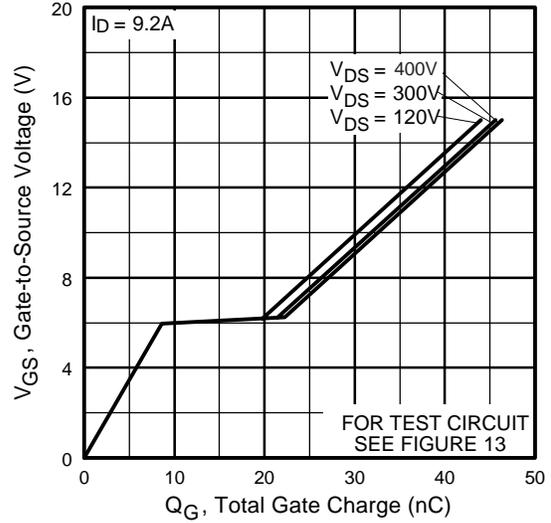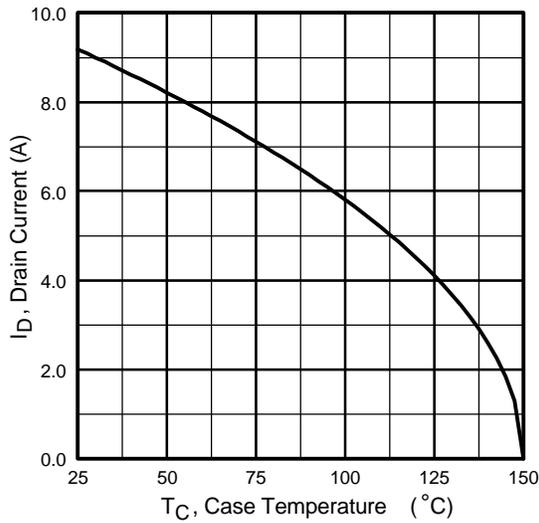

Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

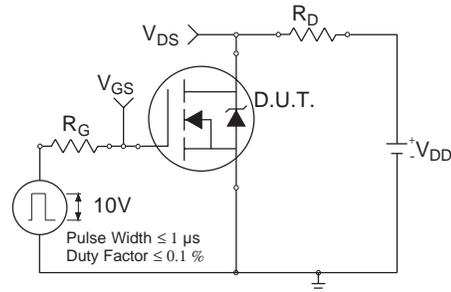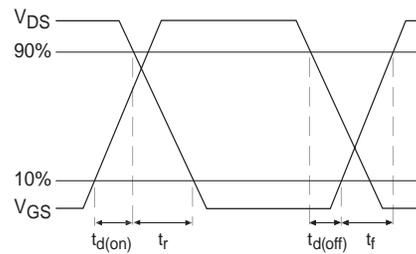**Fig 7.** Typical Source-Drain Diode Forward Voltage

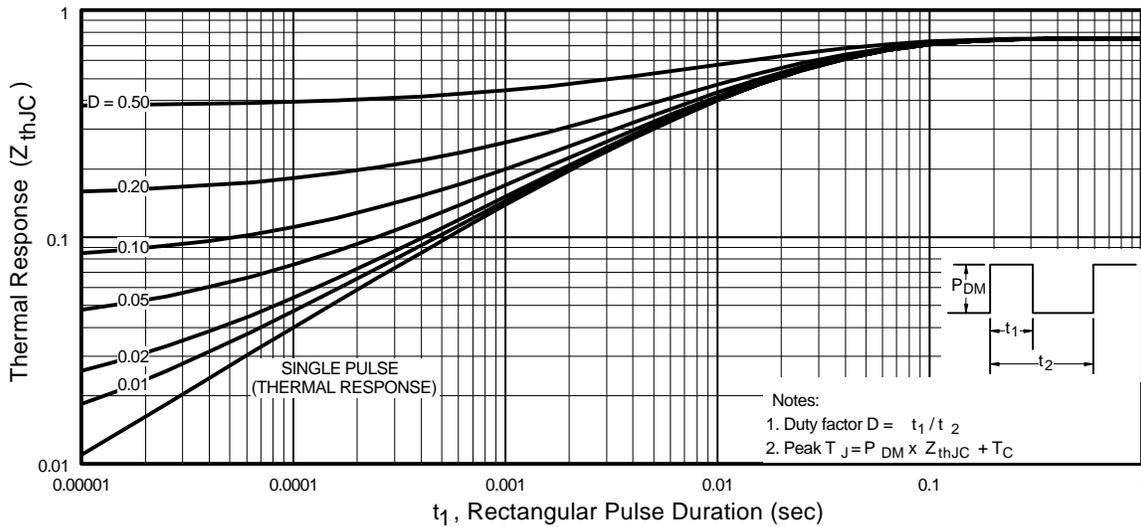**Fig 8.** Maximum Safe Operating Area

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Fig 9. Maximum Drain Current Vs. Case Temperature

Fig 10a. Switching Time Test Circuit

Fig 10b. Switching Time Waveforms

Notes:
1. Duty factor $D = t_1 / t_2$
2. Peak $T_J = P_{DM} \times Z_{thJC} + T_C$

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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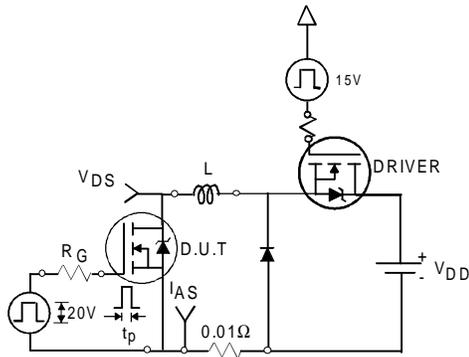
Fig 12a. Unclamped Inductive Test Circuit
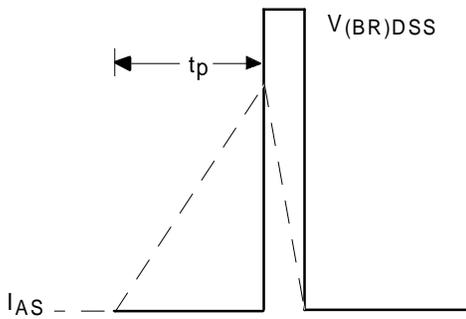
Fig 12b. Unclamped Inductive Waveforms

E_{AS}, Single Pulse Avalanche Energy (mJ)

	I_D
TOP	4.1A
	5.8A
BOTTOM	9.2A

Starting T_J, Junction Temperature ($^\circ$C)

Fig 12c. Maximum Avalanche Energy Vs. Drain Current

Fig 13a. Basic Gate Charge Waveform
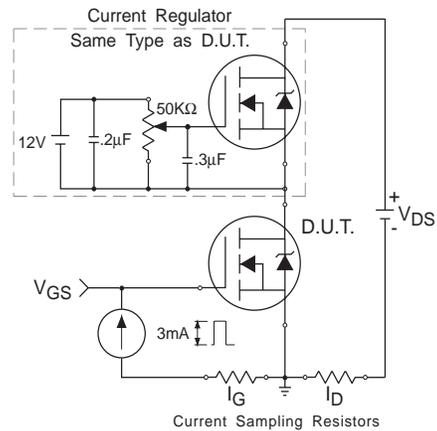
Fig 13b. Gate Charge Test Circuit

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Peak Diode Recovery dv/dt Test Circuit

D.U.T

③

Circuit Layout Considerations
- Low Stray Inductance
- Ground Plane
- Low Leakage Inductance Current Transformer

②

④

①

R_G

- dv/dt controlled by R_G
- Driver same type as D.U.T.
- I_{SD} controlled by Duty Factor "D"
- D.U.T. - Device Under Test

+ V_{DD} -

① Driver Gate Drive

P.W.

Period

$D = \dfrac{P.W.}{Period}$

$V_{GS}=10V$ *

② D.U.T. I_{SD} Waveform

Reverse Recovery Current

Body Diode Forward Current

di/dt

③ D.U.T. V_{DS} Waveform

Diode Recovery dv/dt

V_{DD}

Re-Applied Voltage

Body Diode Forward Drop

④ Inductor Curent

Ripple ≤ 5%

I_{SD}

* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFET® Power MOSFETs

IRFS9N60A

D²Pak Package Outline

10.54 (.415)
10.29 (.405)

1.40 (.055) MAX.

- A -

2

1.78 (.070)
1.27 (.050)

1   3

15.49 (.610)
14.73 (.580)

3X   1.40 (.055)
1.14 (.045)

3X   0.93 (.037)
0.69 (.027)

5.08 (.200)

⊕   0.25 (.010) Ⓜ B Ⓐ M

4.69 (.185)
4.20 (.165)

- B -

1.32 (.052)
1.22 (.048)

2.79 (.110)
2.29 (.090)

5.28 (.208)
4.78 (.188)

0.55 (.022)
0.46 (.018)

1.39 (.055)
1.14 (.045)

10.16 (.400)
REF.

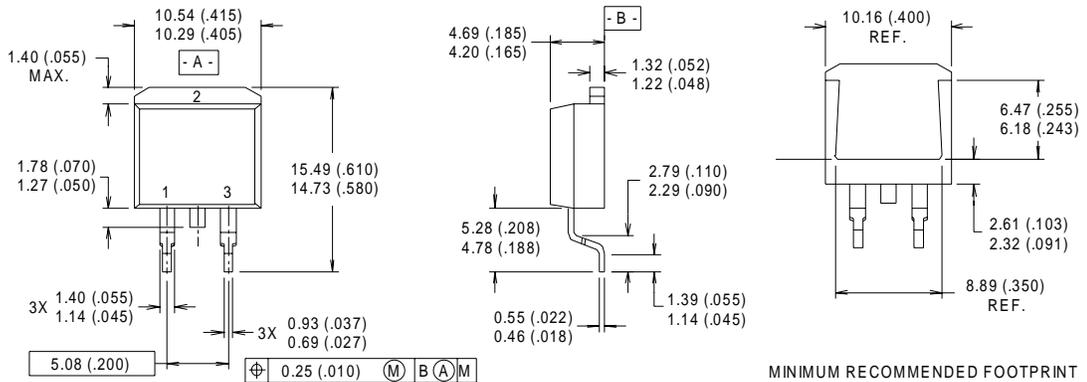6.47 (.255)
6.18 (.243)

2.61 (.103)
2.32 (.091)

8.89 (.350)
REF.

MINIMUM RECOMMENDED FOOTPRINT

11.43 (.450)

8.89 (.350)

17.78 (.700)

3.81 (.150)

2.08 (.082)
2X

2.54 (.100)
2X

NOTES:
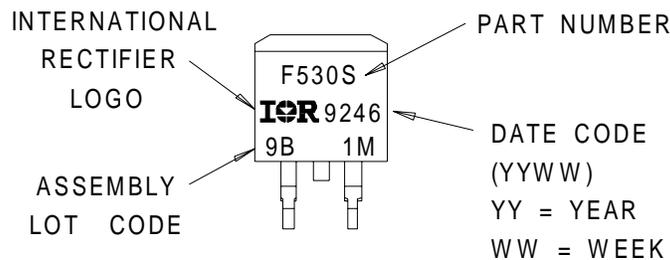1 DIMENSIONS AFTER SOLDER DIP.
2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
3 CONTROLLING DIMENSION : INCH.
4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.
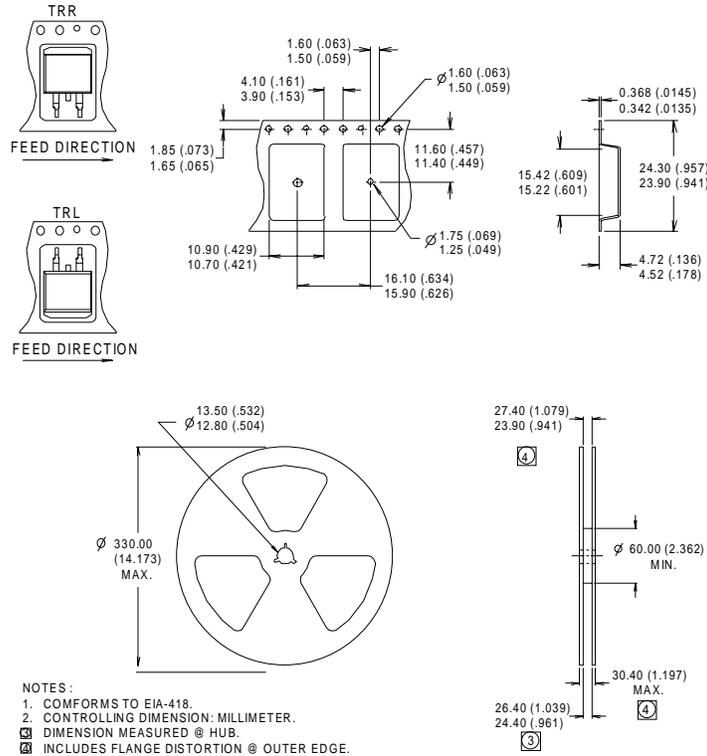
LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE

Part Marking Information
D²Pak

INTERNATIONAL
RECTIFIER
LOGO

PART NUMBER

F530S

IƏR 9246

9B   1M

DATE CODE
(YYWW)
YY = YEAR
WW = WEEK

ASSEMBLY
LOT CODE

8

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Tape & Reel Information
D²Pak

TRR

FEED DIRECTION

TRL

FEED DIRECTION

1.60 (.063)
1.50 (.059)

4.10 (.161)
3.90 (.153)

Ø 1.60 (.063)
1.50 (.059)

0.368 (.0145)
0.342 (.0135)

1.85 (.073)
1.65 (.065)

11.60 (.457)
11.40 (.449)

15.42 (.609)
15.22 (.601)

24.30 (.957)
23.90 (.941)

10.90 (.429)
10.70 (.421)

Ø 1.75 (.069)
1.25 (.049)

4.72 (.136)
4.52 (.178)

16.10 (.634)
15.90 (.626)

13.50 (.532)
Ø 12.80 (.504)

27.40 (1.079)
23.90 (.941)

④

Ø 330.00
(14.173)
MAX.

Ø 60.00 (2.362)
MIN.

30.40 (1.197)
MAX.

④

26.40 (1.039)
24.40 (.961)

③

NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
③ DIMENSION MEASURED @ HUB.
④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting T_J = 25°C, L = 6.8mH
R_G = 25Ω, I_{AS} = 9.2A. (See Figure 12)

③ $I_{SD} \leq$ 9.2A, di/dt $\leq$ 50A/μs, $V_{DD} \leq V_{(BR)DSS}$,
$T_J \leq$ 150°C

④ Pulse width $\leq$ 300μs; duty cycle $\leq$ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

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