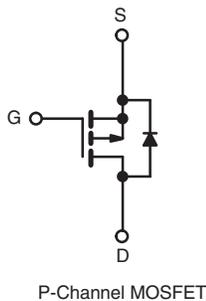
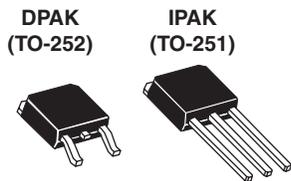


## Power MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V)	- 50
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = - 10$ V   0.28
$Q_g$ (Max.) (nC)	14
$Q_{gs}$ (nC)	6.5
$Q_{gd}$ (nC)	6.5
Configuration	Single



### FEATURES

- Surface Mountable (Order As IRFR9020/SiHFR9020)
- Straight Lead Option (Order As IRFU9020/SiHFU9020)
- Repetitive Avalanche Ratings
- Dynamic  $dV/dt$  Rating
- Simple Drive Requirements
- Ease of Paralleling
- Lead (Pb)-free Available



### DESCRIPTION

The Power MOSFET technology is the key to Vishay's advanced line of Power MOSFET transistors. The efficient geometry and unique processing of this latest "State of the Art" design achieves: very low on-state resistance combined with high transconductance; superior reverse energy and diode recovery  $dV/dt$ .

The Power MOSFET transistors also feature all of the well established advantages of MOSFET'S such as voltage control, very fast switching, ease of paralleling and temperature stability of the electrical parameters.

Surface mount packages enhance circuit performance by reducing stray inductances and capacitance. The TO-252 surface mount package brings the advantages of Power MOSFET's to high volume applications where PC Board surface mounting is desirable. The surface mount option IRFR9020/SiHFR9020 is provided on 16mm tape. The straight lead option IRFR9020/SiHFR9020 of the device is called the IPAK (TO-251).

They are well suited for applications where limited heat dissipation is required such as, computers and peripherals, telecommunication equipment, DC/DC converters, and a wide range of consumer products.

ORDERING INFORMATION				
Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)
Lead (Pb)-free	IRFR9020PbF	IRFR9020TRPbF <sup>a</sup>	IRFR9020TRLpbf <sup>a</sup>	IRFU9020PbF
	SiHFR9020-E3	SiHFR9020T-E3 <sup>a</sup>	SiHFR9020TL-E3 <sup>a</sup>	SiHFU9020-E3
SnPb	IRFR9020	IRFR9020TR <sup>a</sup>	IRFR9020TRL <sup>a</sup>	IRFU9020
	SiHFR9020	SiHFR9020T <sup>a</sup>	SiHFR9020TL <sup>a</sup>	SiHFU9020

#### Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ , unless otherwise noted				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	$V_{DS}$	- 50	V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$		
Continuous Drain Current	$V_{GS}$ at - 10 V	$T_C = 25^\circ\text{C}$	- 9.9	A
		$T_C = 100^\circ\text{C}$	- 6.3	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	- 40		
Linear Derating Factor		0.33	W/ $^\circ\text{C}$	
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	440	mJ	
Repetitive Avalanche Current <sup>a</sup>	$I_{AR}$	- 9.9	A	
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	4.2	mJ	

\* Pb containing terminations are not RoHS compliant, exemptions may apply

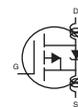
<b>ABSOLUTE MAXIMUM RATINGS</b> $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted				
PARAMETER		SYMBOL	LIMIT	UNIT
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	$P_D$	42	W
Peak Diode Recovery $dV/dt^c$		$dV/dt$	5.8	V/ns
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s		300 <sup>d</sup>	

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 14).
- $V_{DD} = -25\text{ V}$ , Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 5.1\text{ mH}$ ,  $R_G = 25\text{ }\Omega$ , Peak  $I_L = -9.9\text{ A}$
- $I_{SD} \leq -9.9\text{ A}$ ,  $dI/dt \leq -120\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq 40\text{ V}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- 0.063" (1.6 mm) from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).

<b>THERMAL RESISTANCE RATINGS</b>					
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	-	110	$^\circ\text{C}/\text{W}$
Case-to-Sink	$R_{thCS}$	-	1.7	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	-	3.0	

<b>SPECIFICATIONS</b> $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted								
PARAMETER	SYMBOL	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
<b>Static</b>								
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = -250\text{ }\mu\text{A}$			- 50	-	-	V
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = -250\text{ }\mu\text{A}$			- 2.0	-	- 4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$			-	-	$\pm 500$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = \text{max. rating}$ , $V_{GS} = 0\text{ V}$			-	-	250	$\mu\text{A}$
		$V_{DS} = 0.8 \times \text{max. rating}$ , $V_{GS} = 0\text{ V}$ , $T_J = 125\text{ }^\circ\text{C}$			-	-	1000	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}$	$I_D = 5.7\text{ A}^b$		-	0.20	0.28	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} \leq -50\text{ V}$ , $I_{DS} = -5.7\text{ A}$			2.3	3.5	-	S
<b>Dynamic</b>								
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = -25\text{ V}$ , $f = 1.0\text{ MHz}$ , see fig. 9			-	490	-	pF
Output Capacitance	$C_{oss}$				-	320	-	
Reverse Transfer Capacitance	$C_{rss}$				-	70	-	
Total Gate Charge	$Q_g$	$V_{GS} = -10\text{ V}$	$I_D = -9.7\text{ A}$ , $V_{DS} = 0.8 \times \text{max. rating}$ , see fig. 16 (Independent operating temperature)		-	9.4	14	nC
Gate-Source Charge	$Q_{gs}$				-	4.3	6.5	
Gate-Drain Charge	$Q_{gd}$				-	4.3	6.5	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -25\text{ V}$ , $I_D = -9.7\text{ A}$ , $R_G = 18\text{ }\Omega$ , $R_D = 2.4\text{ }\Omega$ , see fig. 15 (Independent operating temperature)			-	8.2	12	ns
Rise Time	$t_r$				-	57	66	
Turn-Off Delay Time	$t_{d(off)}$				-	12	18	
Fall Time	$t_f$				-	25	38	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact.			-	4.5	-	nH
Internal Source Inductance	$L_S$				-	7.5	-	





SPECIFICATIONS $T_J = 25^\circ\text{C}$ , unless otherwise noted						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p-n junction diode 	-	-	- 9.9	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	- 40	
Body Diode Voltage	$V_{SD}$	$T_J = 25^\circ\text{C}$ , $I_S = -9.9\text{ A}$ , $V_{GS} = 0\text{ V}^b$	-	-	- 6.3	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25^\circ\text{C}$ , $I_F = -9.7\text{ A}$ , $dI/dt = 100\text{ A}/\mu\text{s}^b$	56	110	280	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		0.17	0.34	0.85	nC
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )				

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 14).
- b. Pulse width  $\leq 300\ \mu\text{s}$ ; duty cycle  $\leq 2\%$ .

**TYPICAL CHARACTERISTICS**  $25^\circ\text{C}$ , unless otherwise noted

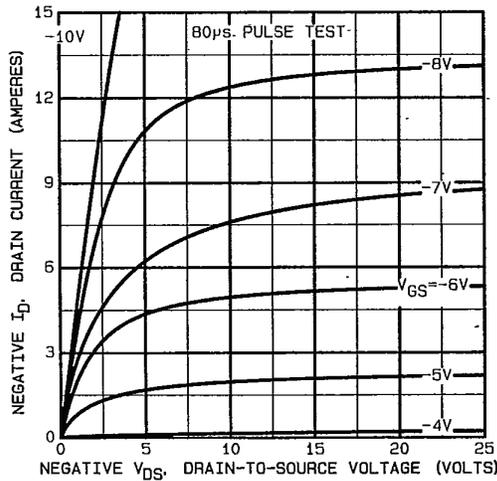


Fig. 1 - Typical Output Characteristics

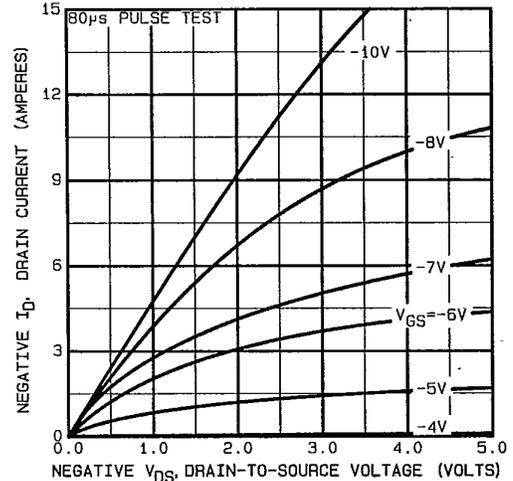


Fig. 3 - Typical Saturation Characteristics

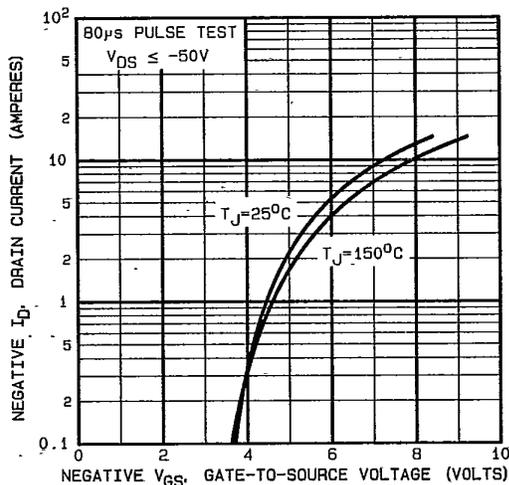


Fig. 2 - Typical Transfer Characteristics

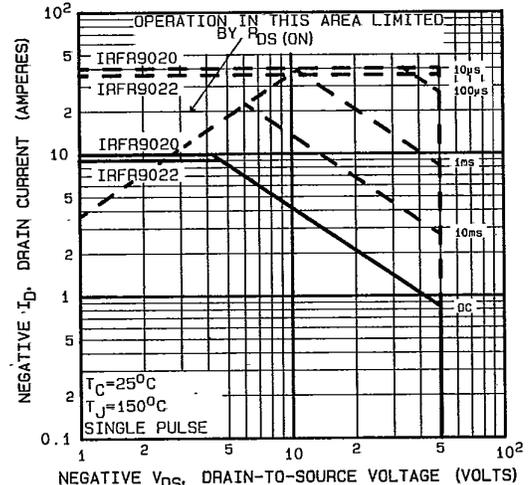


Fig. 4 - Maximum Safe Operating Area

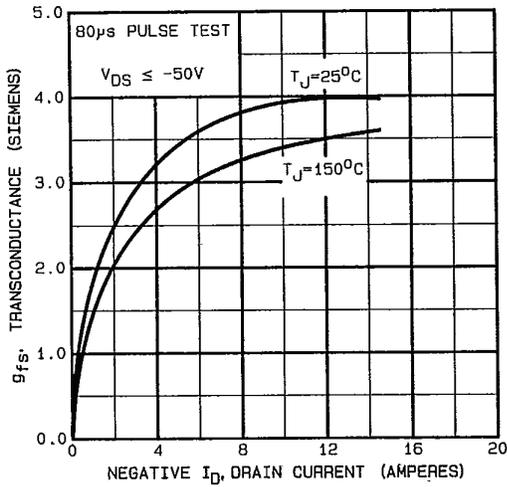


Fig. 5 - Typical Transconductance vs. Drain Current

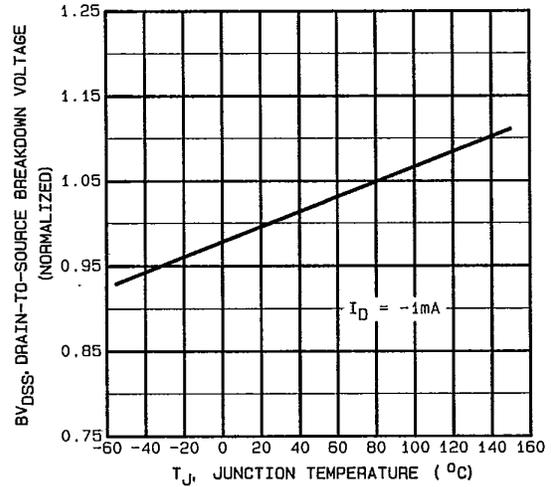


Fig. 7 - Breakdown Voltage vs. Temperature

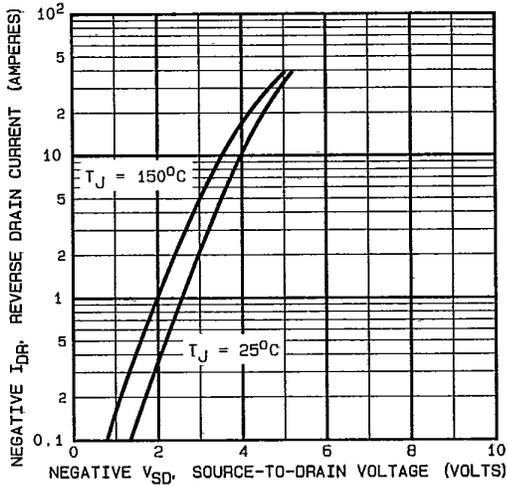


Fig. 6 - Typical Source-Drain Diode Forward Voltage

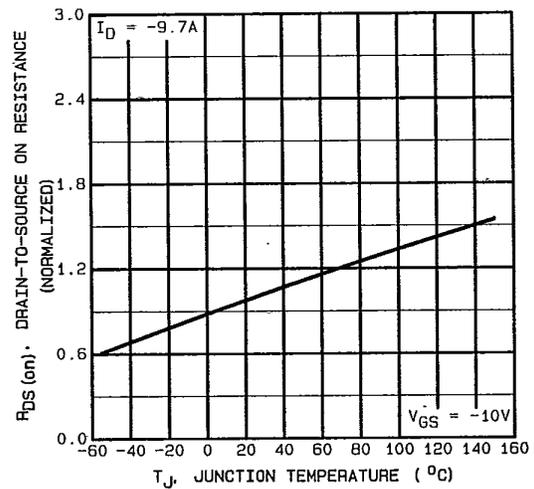


Fig. 8 - Normalized On-Resistance vs. Temperature

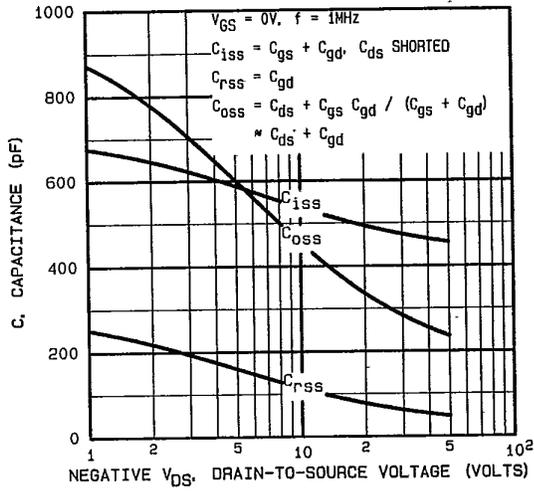


Fig. 9 - Typical Capacitance vs. Drain-to-Source Voltage

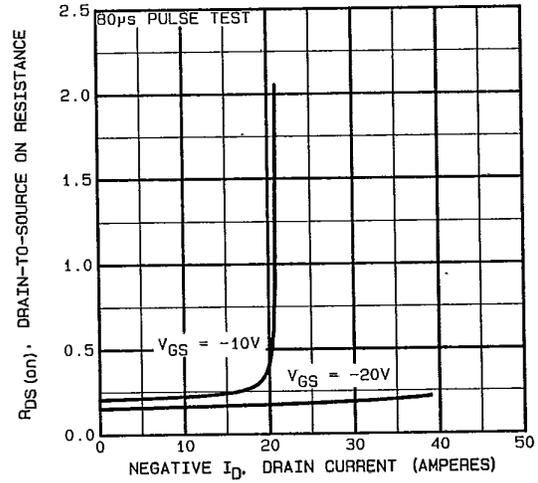


Fig. 11 - Typical On-Resistance vs. Drain Current

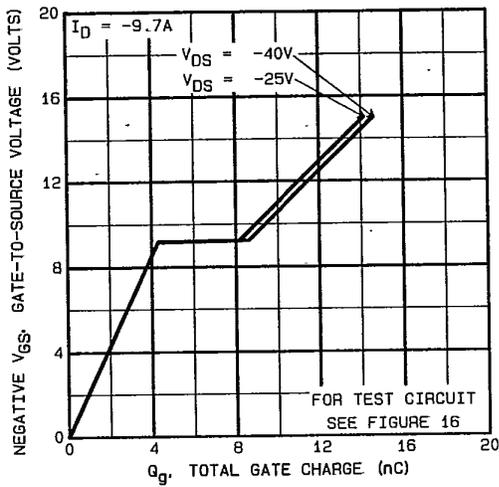


Fig. 10 - Typical Gate Charge vs. Gate-to-Source Voltage

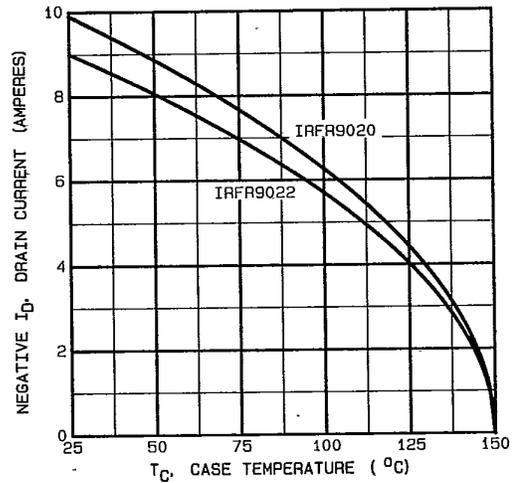


Fig. 12 - Maximum Drain Current vs. Case Temperature

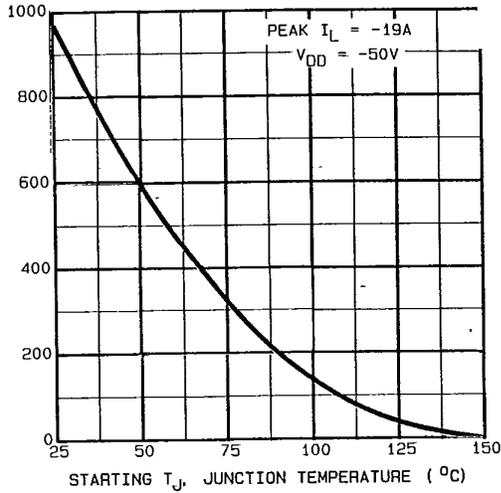


Fig. 13a - Maximum Avalanche vs. Starting Junction Temperature

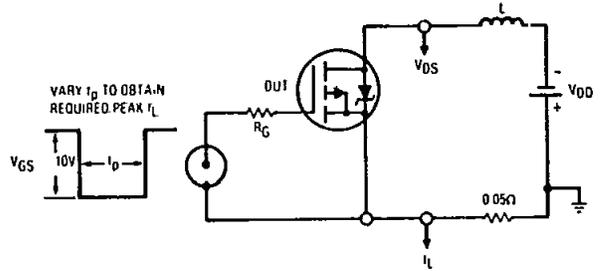


Fig. 13b - Unclamped Inductive Test Circuit

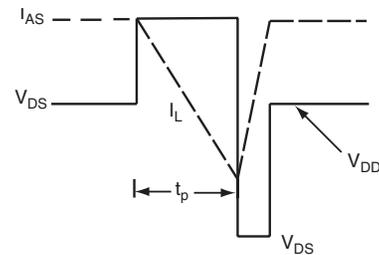


Fig. 13c - Unclamped Inductive Waveforms

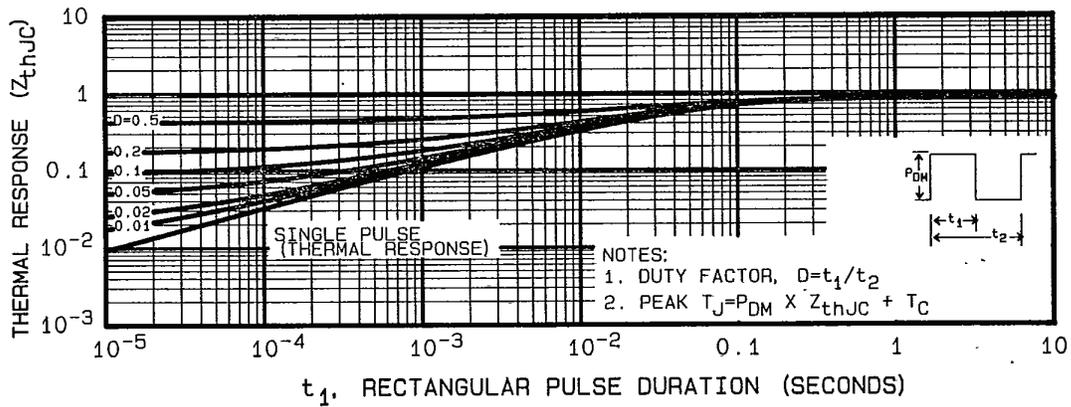


Fig. 14 - Maximum Effective Transient Thermal Impedance, Junction-to-Case vs. Pulse Duration

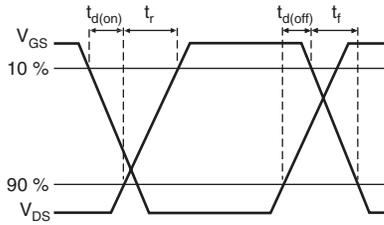


Fig. 15a - Switching Time Waveforms

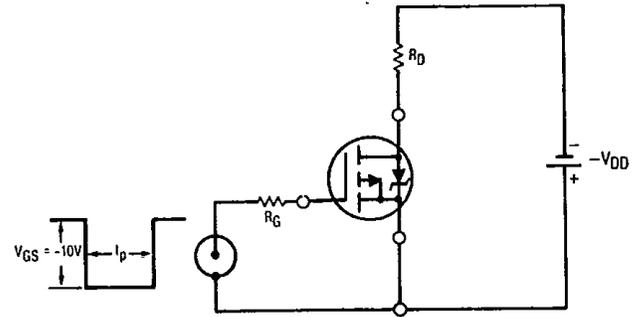


Fig. 15b - Switching Time Test Circuit

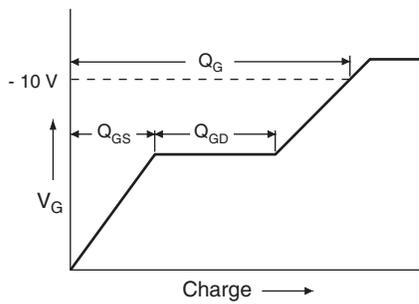


Fig. 16a - Basic Gate Charge Waveform

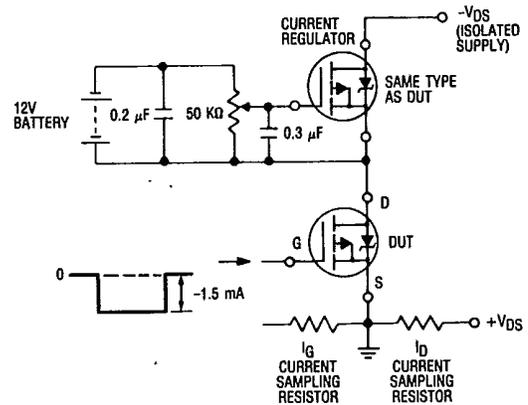
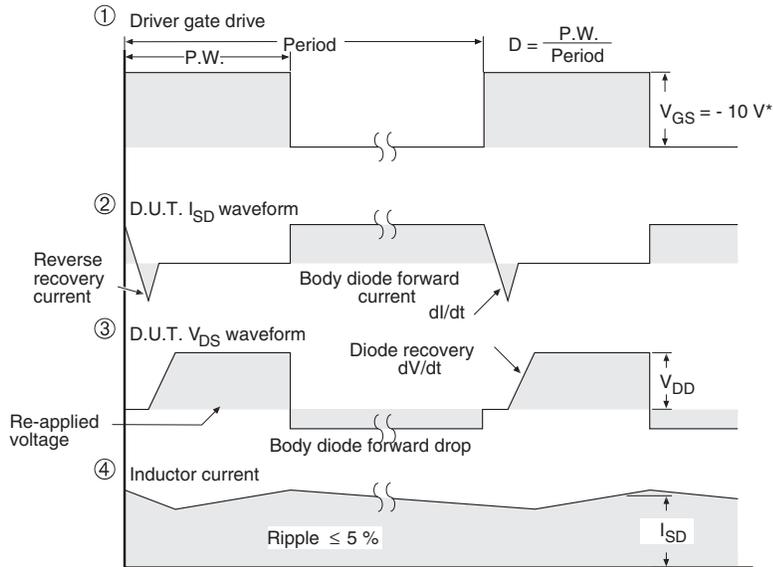
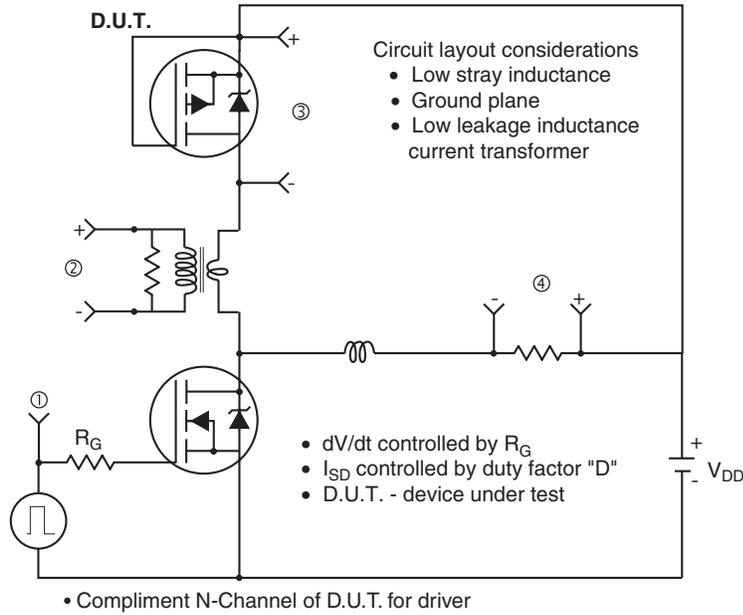


Fig. 16b - Gate Charge Test Circuit

## Peak Diode Recovery dV/dt Test Circuit



\*  $V_{GS} = -5 V$  for logic level and  $-3 V$  drive devices

**Fig. 17 - For P-Channel**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?90350>.



## Disclaimer

All product specifications and data are subject to change without notice.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained herein or in any other disclosure relating to any product.

Vishay disclaims any and all liability arising out of the use or application of any product described herein or of any information provided herein to the maximum extent permitted by law. The product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein, which apply to these products.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications unless otherwise expressly indicated. Customers using or selling Vishay products not expressly indicated for use in such applications do so entirely at their own risk and agree to fully indemnify Vishay for any damages arising or resulting from such use or sale. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

Product names and markings noted herein may be trademarks of their respective owners.