

Power MOSFET

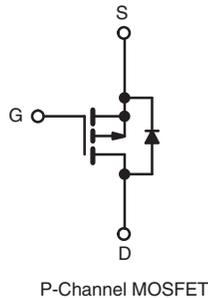
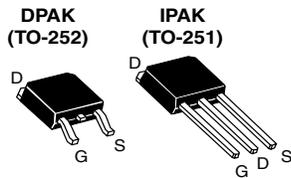
PRODUCT SUMMARY		
V_{DS} (V)	- 400	
$R_{DS(on)}$ (Ω)	$V_{GS} = - 10$ V	7.0
Q_g (Max.) (nC)	13	
Q_{gs} (nC)	3.2	
Q_{gd} (nC)	5.0	
Configuration	Single	

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- P-Channel
- Surface Mount (IRFR9310/SiHFR9310)
- Straight Lead (IRFU9310/SiHFU9310)
- Advanced Process Technology
- Fast Switching
- Fully Avalanche Rated
- Compliant to RoHS Directive 2002/95/EC



RoHS*
COMPLIANT
HALOGEN
FREE
Available



DESCRIPTION

Third generation Power MOSFETs from Vishay utilize advanced processing techniques to achieve low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The DPAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU/SiHFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 W are possible in typical surface mount applications.

ORDERING INFORMATION					
Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)
Lead (Pb)-free and Halogen-free	SiHFR9310-GE3	SiHFR9310TRL-GE3	SiHFR9310TR-GE3	SiHFR9310TRR-GE3	SiHFU9310-GE3
Lead (Pb)-free	IRFR9310PbF	IRFR9310TRLPbF ^a	IRFR9310TRPbF ^a	IRFR9310TRRPbF ^a	IRFU9310PbF
	SiHFR9310-E3	SiHFR9310TL-E3 ^a	SiHFR9310T-E3 ^a	SiHFR9310TR-E3 ^a	SiHFU9310-E3
SnPb	IRFR9310	IRFR9310TRL ^a	IRFR9310TR ^a	-	IRFU9310
	SiHFR9310	SiHFR9310TL ^a	SiHFR9310T ^a	-	SiHFU9310

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted				
PARAMETER	SYMBOL		LIMIT	UNIT
Drain-Source Voltage	V_{DS}		- 400	V
Gate-Source Voltage	V_{GS}		± 20	
Continuous Drain Current	V_{GS} at - 10 V		$T_C = 25$ °C	- 1.8
			$T_C = 100$ °C	- 1.1
Pulsed Drain Current ^a			- 7.2	A
Linear Derating Factor			0.40	W/°C
Single Pulse Avalanche Energy ^b			92	mJ
Repetitive Avalanche Current ^a			- 1.8	A
Repetitive Avalanche Energy ^a			5.0	mJ
Maximum Power Dissipation	$T_C = 25$ °C		50	W
Peak Diode Recovery dV/dt ^c			- 24	V/ns
Operating Junction and Storage Temperature Range			- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s		300 ^d	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting $T_J = 25$ °C, $L = 57$ mH, $R_g = 25$ Ω , $I_{AS} = - 1.8$ A (see fig. 12).
- $I_{SD} \leq - 1.1$ A, $dI/dt \leq 450$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS						
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient	R_{thJA}	-	-	110	°C/W	
Maximum Junction-to-Ambient (PCB Mount) ^a	R_{thJA}	-	-	50		
Maximum Junction-to-Case (Drain)	R_{thJC}	-	-	2.5		

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$		-400	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = -1\text{ mA}$		-	-0.41	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$		-2.0	-	-4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -400\text{ V}, V_{GS} = 0\text{ V}$		-	-	-100	μA
		$V_{DS} = -320\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	-500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}$	$I_D = -1.1\text{ A}^b$	-	-	7.0	Ω
Forward Transconductance	g_{fs}	$V_{DS} = -50\text{ V}, I_D = -1.1\text{ A}$		0.91	-	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = -25\text{ V}, f = 1.0\text{ MHz}$, see fig. 5		-	270	-	pF
Output Capacitance	C_{oss}			-	50	-	
Reverse Transfer Capacitance	C_{rss}			-	8.0	-	
Total Gate Charge	Q_g	$V_{GS} = -10\text{ V}$	$I_D = -1.1\text{ A}, V_{DS} = -320\text{ V}$, see fig. 6 and 13 ^b	-	-	13	nC
Gate-Source Charge	Q_{gs}			-	-	3.2	
Gate-Drain Charge	Q_{gd}			-	-	5.0	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -200\text{ V}, I_D = -1.1\text{ A}, R_g = 21\text{ }\Omega, R_D = 180\text{ }\Omega$, see fig. 10 ^b		-	11	-	ns
Rise Time	t_r			-	10	-	
Turn-Off Delay Time	$t_{d(off)}$			-	25	-	
Fall Time	t_f			-	24	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact ^c		-	4.5	-	nH
Internal Source Inductance	L_S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p-n junction diode		-	-	-1.9	A
Pulsed Diode Forward Current ^a	I_{SM}			-	-	-7.6	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = -1.1\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	-4.0	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = -1.1\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$		-	170	260	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	640	960	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- This is applied for IPAK, L_S of DPAK is measured between lead and center of die contact.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

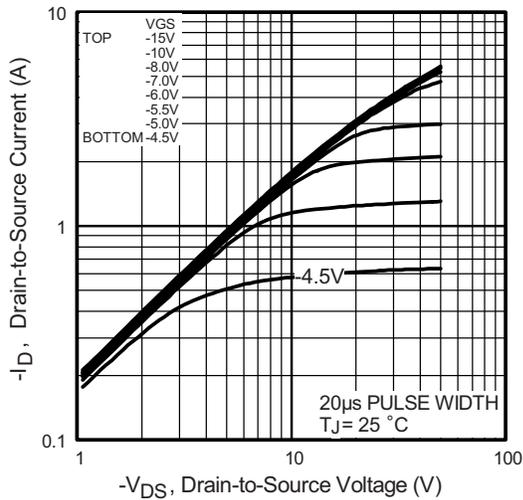


Fig. 1 - Typical Output Characteristics

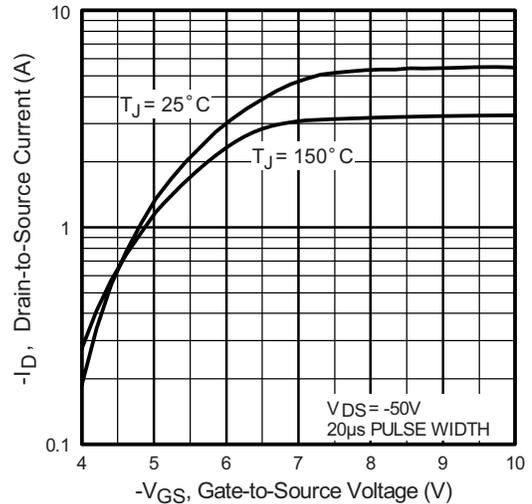


Fig. 3 - Typical Transfer Characteristics

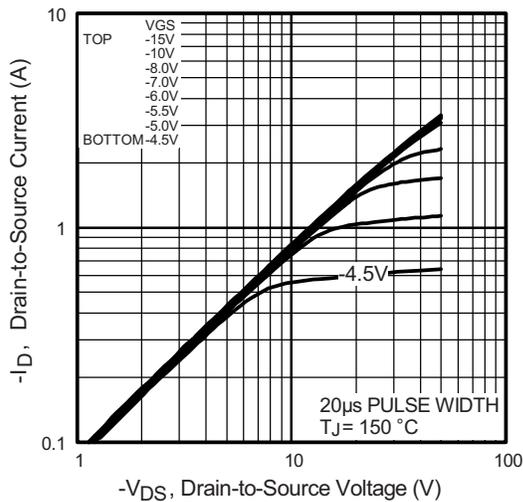


Fig. 2 - Typical Output Characteristics

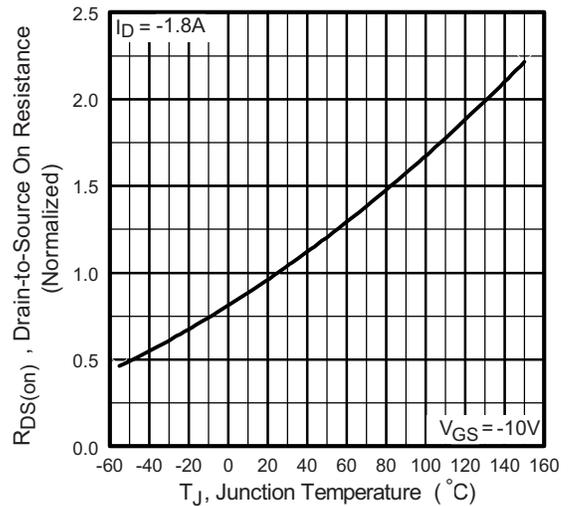


Fig. 4 - Normalized On-Resistance vs. Temperature

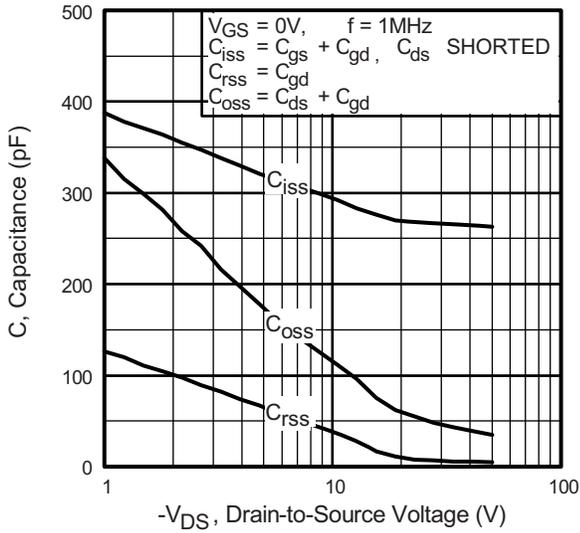


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

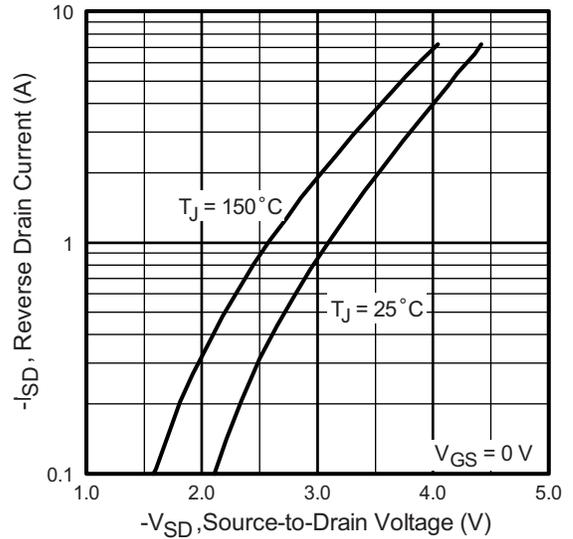


Fig. 7 - Typical Source-Drain Diode Forward Voltage

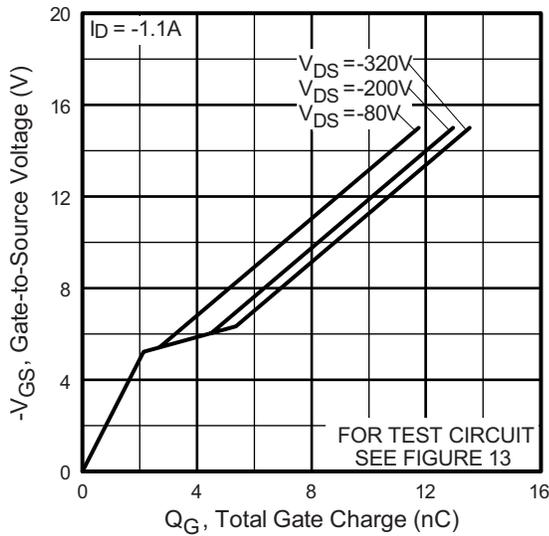


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

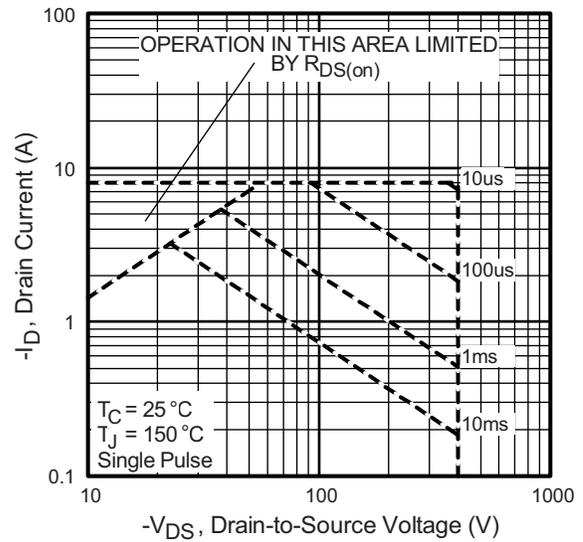


Fig. 8 - Maximum Safe Operating Area

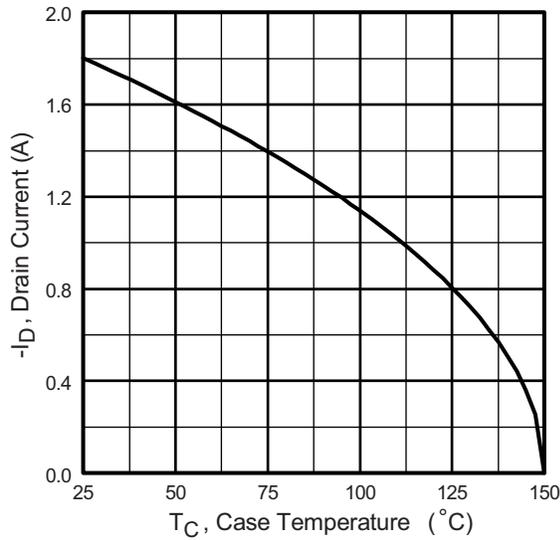


Fig. 9 - Maximum Drain Current vs. Case Temperature

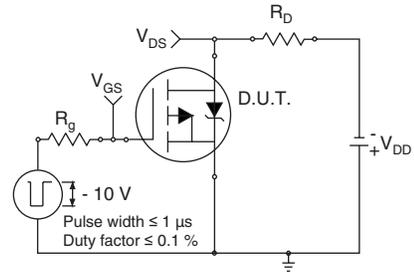


Fig. 10a - Switching Time Test Circuit

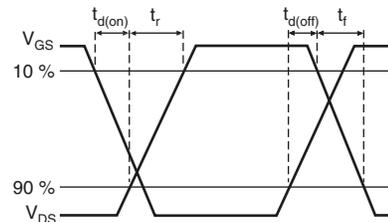


Fig. 10b - Switching Time Waveforms

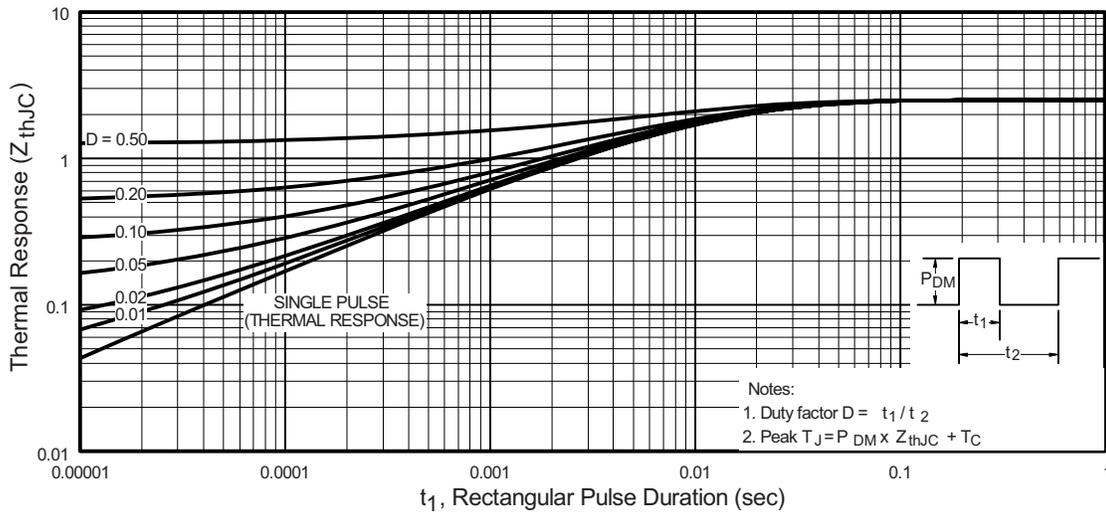


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

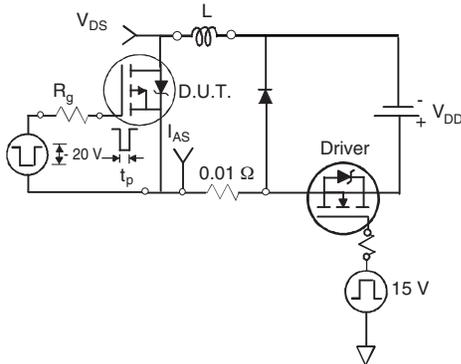


Fig. 12a - Unclamped Inductive Test Circuit

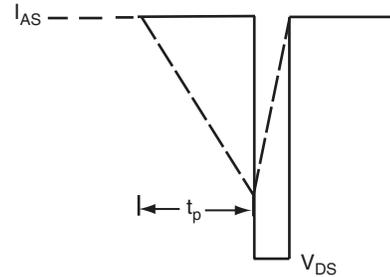


Fig. 12b - Unclamped Inductive Waveforms

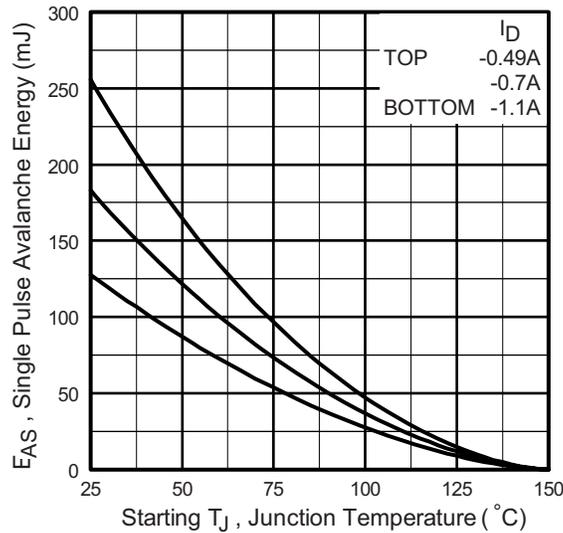


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

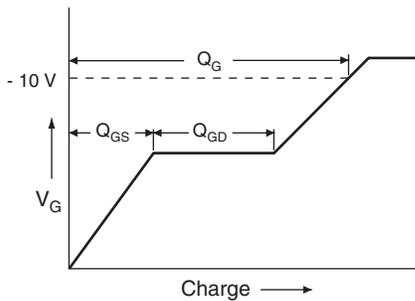


Fig. 13a - Basic Gate Charge Waveform

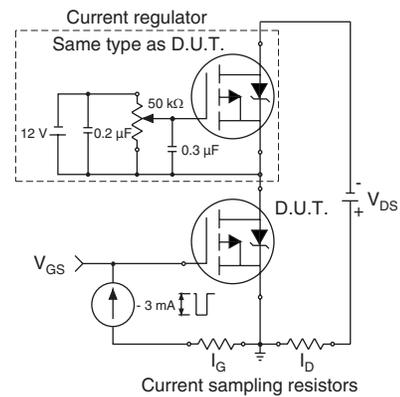


Fig. 13b - Gate Charge Test Circuit

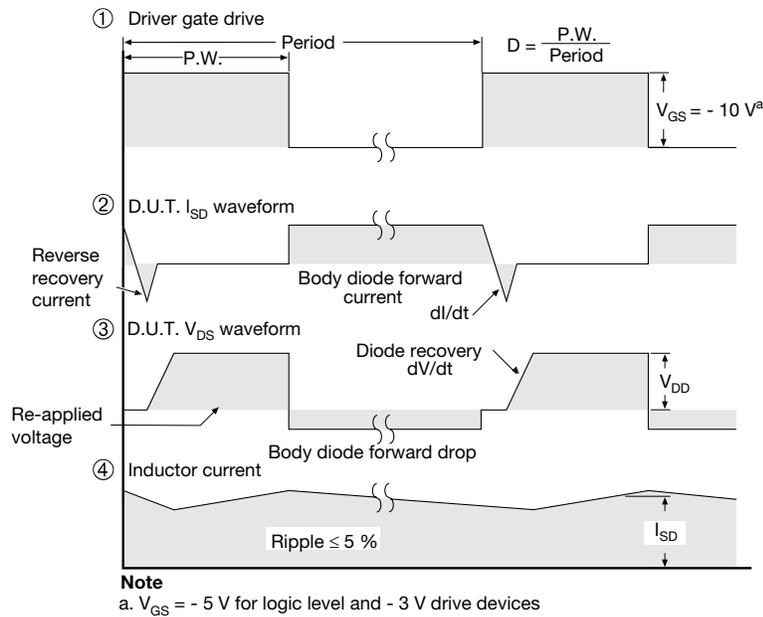
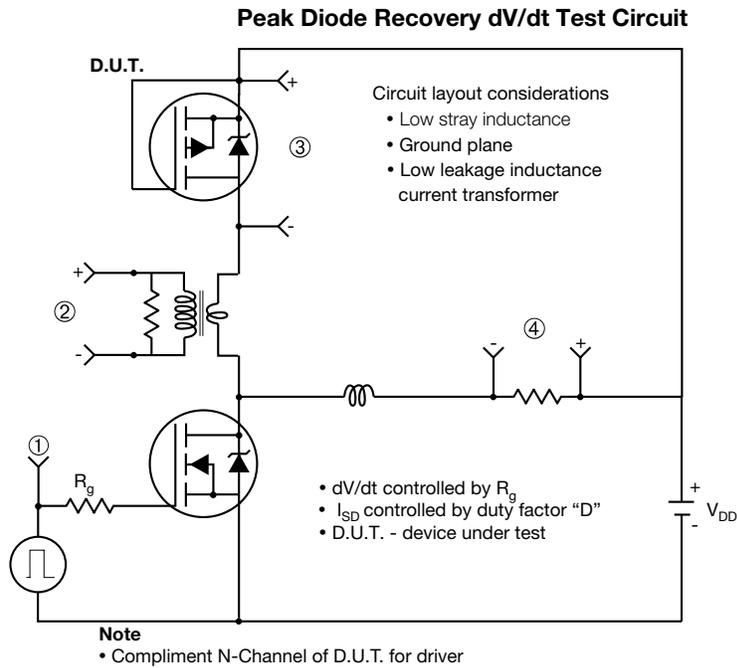


Fig. 14 - For P-Channel

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