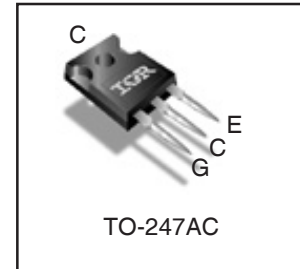
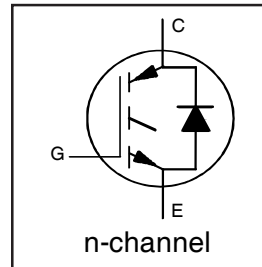


**PDP TRENCH IGBT** **IRGP4055DPbF**

**Features**

- Advanced Trench IGBT Technology
- Optimized for Sustain and Energy Recovery circuits in PDP applications
- Low  $V_{CE(on)}$  and Energy per Pulse ( $E_{PULSE}^{TM}$ ) for improved panel efficiency
- High repetitive peak current capability
- Lead Free package

Key Parameters		
$V_{CE\ min}$	300	V
$V_{CE(on)}\ typ.\ @\ 110A$	1.70	V
$I_{RP}\ max\ @\ T_C = 25^\circ C$ ①	270	A
$T_J\ max$	150	°C



G	C	E
Gate	Collector	Emitter

**Description**

This IGBT is specifically designed for applications in Plasma Display Panels. This device utilizes advanced trench IGBT technology to achieve low  $V_{CE(on)}$  and low  $E_{PULSE}^{TM}$  rating per silicon area which improve panel efficiency. Additional features are 150°C operating junction temperature and high repetitive peak current capability. These features combine to make this IGBT a highly efficient, robust and reliable device for PDP applications.

**Absolute Maximum Ratings**

	Parameter	Max.	Units
$V_{GE}$	Gate-to-Emitter Voltage	±30	V
$I_C @ T_C = 25^\circ C$	Continuous Collector Current, $V_{GE} @ 15V$	110	A
$I_C @ T_C = 100^\circ C$	Continuous Collector, $V_{GE} @ 15V$	60	
$I_{RP} @ T_C = 25^\circ C$	Repetitive Peak Current ①	270	
$P_D @ T_C = 25^\circ C$	Power Dissipation	255	W
$P_D @ T_C = 100^\circ C$	Power Dissipation	102	
	Linear Derating Factor	2.04	W/°C
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-40 to + 150	°C
	Soldering Temperature for 10 seconds	300	
	Mounting Torque, 6-32 or M3 Screw	10lb·in (1.1N·m)	

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$ (IGBT)	Thermal Resistance Junction-to-Case-(each IGBT) ②	—	0.48	°C/W
$R_{\theta JC}$ (Diode)	Thermal Resistance Junction-to-Case-(each Diode)	1.45	2.5	
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink (flat, greased surface)	0.20	—	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (typical socket mount)	—	70	
	Weight	2.0 (0.07)	—	

## Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV <sub>CES</sub>	Collector-to-Emitter Breakdown Voltage	300	—	—	V	V <sub>GE</sub> = 0V, I <sub>CE</sub> = 1 mA
ΔBV <sub>CES</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.23	—	V/°C	Reference to 25°C, I <sub>CE</sub> = 1 mA
V <sub>CE(on)</sub>	Static Collector-to-Emitter Voltage	—	1.10	1.30	V	V <sub>GE</sub> = 15V, I <sub>CE</sub> = 35A ③
		—	1.70	2.10		V <sub>GE</sub> = 15V, I <sub>CE</sub> = 110A ③
		—	2.35	—		V <sub>GE</sub> = 15V, I <sub>CE</sub> = 200A ③
		—	1.95	—		V <sub>GE</sub> = 15V, I <sub>CE</sub> = 110A, T <sub>J</sub> = 150°C
V <sub>GE(th)</sub>	Gate Threshold Voltage	2.6	—	5.0	V	V <sub>CE</sub> = V <sub>GE</sub> , I <sub>CE</sub> = 1 mA
ΔV <sub>GE(th)</sub> /ΔT <sub>J</sub>	Gate Threshold Voltage Coefficient	—	-11	—	mV/°C	
I <sub>CES</sub>	Collector-to-Emitter Leakage Current	—	2.0	25	μA	V <sub>CE</sub> = 300V, V <sub>GE</sub> = 0V
		—	100	—		V <sub>CE</sub> = 300V, V <sub>GE</sub> = 0V, T <sub>J</sub> = 150°C
I <sub>GES</sub>	Gate-to-Emitter Forward Leakage	—	—	100	nA	V <sub>GE</sub> = 30V
	Gate-to-Emitter Reverse Leakage	—	—	-100		V <sub>GE</sub> = -30V
g <sub>fe</sub>	Forward Transconductance	—	38	—	S	V <sub>CE</sub> = 25V, I <sub>CE</sub> = 35A
Q <sub>g</sub>	Total Gate Charge	—	132	—	nC	V <sub>CE</sub> = 200V, I <sub>C</sub> = 35A, V <sub>GE</sub> = 15V ③
Q <sub>gc</sub>	Gate-to-Collector Charge	—	42	—		
t <sub>d(on)</sub>	Turn-On delay time	—	44	57		
t <sub>r</sub>	Rise time	—	39	55	ns	I <sub>C</sub> = 35A, V <sub>CC</sub> = 180V R <sub>G</sub> = 10Ω, L = 250μH, L <sub>S</sub> = 150nH T <sub>J</sub> = 25°C
t <sub>d(off)</sub>	Turn-Off delay time	—	245	308		
t <sub>f</sub>	Fall time	—	152	198		
t <sub>d(on)</sub>	Turn-On delay time	—	42	—		
t <sub>r</sub>	Rise time	—	40	—	ns	I <sub>C</sub> = 35A, V <sub>CC</sub> = 180V R <sub>G</sub> = 10Ω, L = 250μH, L <sub>S</sub> = 150nH T <sub>J</sub> = 150°C
t <sub>d(off)</sub>	Turn-Off delay time	—	362	—		
t <sub>f</sub>	Fall time	—	309	—		
t <sub>st</sub>	Shoot Through Blocking Time	100	—	—		
E <sub>PULSE</sub>	Energy per Pulse	—	705	—	μJ	L = 220nH, C = 0.40μF, V <sub>GE</sub> = 15V V <sub>CC</sub> = 240V, R <sub>G</sub> = 5.1Ω, T <sub>J</sub> = 25°C
		—	915	—		L = 220nH, C = 0.40μF, V <sub>GE</sub> = 15V V <sub>CC</sub> = 240V, R <sub>G</sub> = 5.1Ω, T <sub>J</sub> = 100°C
		—	—	—		
C <sub>iss</sub>	Input Capacitance	—	4280	—	pF	V <sub>GE</sub> = 0V V <sub>CE</sub> = 30V f = 1.0MHz, See Fig.13
C <sub>oss</sub>	Output Capacitance	—	200	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	125	—		
L <sub>C</sub>	Internal Collector Inductance	—	5.0	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L <sub>E</sub>	Internal Emitter Inductance	—	13	—		

## Diode Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>F(AV)</sub>	Average Forward Current	—	—	8.0	A	T <sub>C</sub> = 155°C
I <sub>FSM</sub>	Non Repetitive Peak Surge Current	—	—	100	A	T <sub>J</sub> = 155°C, PW = 6.0ms half sine wave
V <sub>F</sub>	Forward Voltage	—	1.0	1.25	V	I <sub>F</sub> = 8A
		—	0.83	1.0		I <sub>F</sub> = 8A, T <sub>J</sub> = 125°C
t <sub>rr</sub>	Diode Reverse Recovery Time	—	—	35	ns	I <sub>F</sub> = 1.0A, di/dt = -50A/μs, V <sub>R</sub> = 30V
		—	27	—		T <sub>J</sub> = 25°C I <sub>F</sub> = 8.0A, V <sub>R</sub> = 200V,
		—	40	—		T <sub>J</sub> = 125°C di/dt = 200A/μs
Q <sub>rr</sub>	Diode Reverse Recovery Charge	—	30	—	nC	T <sub>J</sub> = 25°C I <sub>F</sub> = 8.0A, V <sub>R</sub> = 200V,
		—	106	—		T <sub>J</sub> = 125°C di/dt = 200A/μs
I <sub>rr</sub>	Peak Reverse Recovery Current	—	2.2	—	A	T <sub>J</sub> = 25°C I <sub>F</sub> = 8.0A, V <sub>R</sub> = 200V,
		—	5.3	—		T <sub>J</sub> = 125°C di/dt = 200A/μs

### Notes:

- ① Half sine wave with duty cycle = 0.25, ton=1μsec.  
② R<sub>θ</sub> is measured at T<sub>J</sub> of approximately 90°C.

- ③ Pulse width ≤ 400μs; duty cycle ≤ 2%.

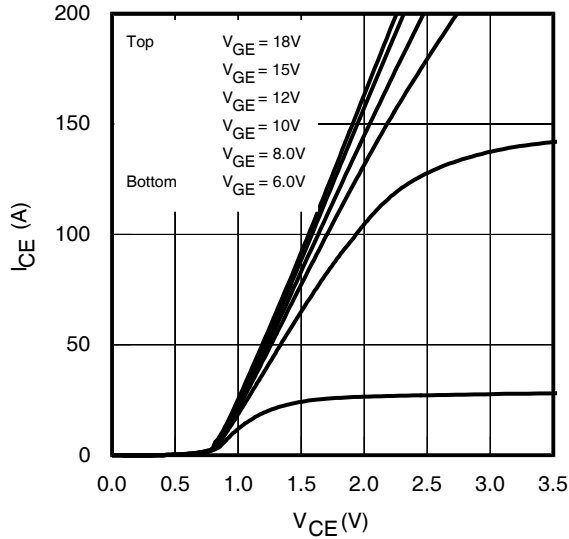


Fig 1. Typical Output Characteristics @ 25°C

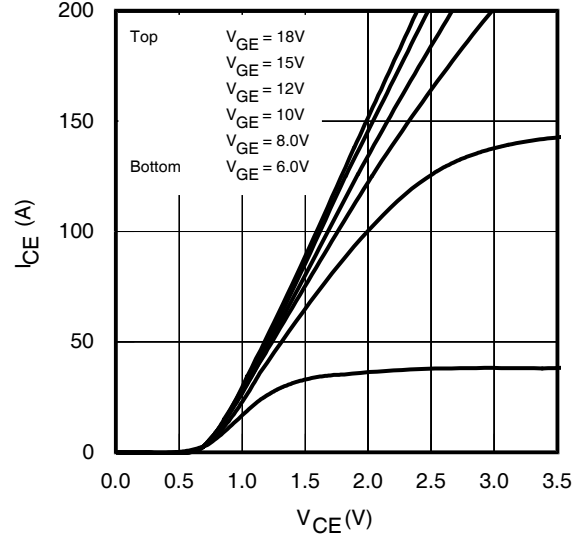


Fig 2. Typical Output Characteristics @ 75°C

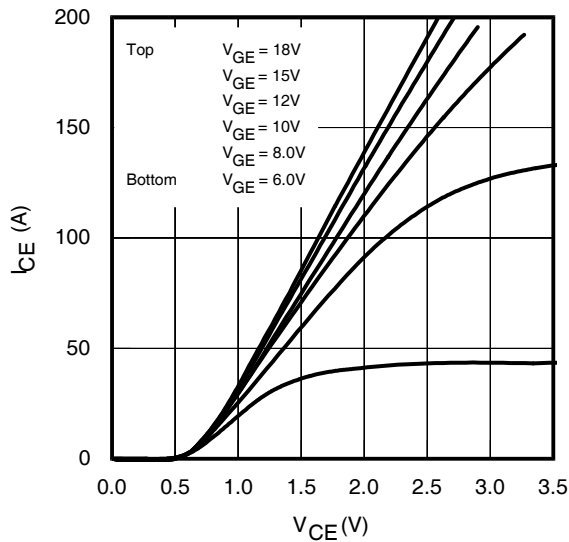


Fig 3. Typical Output Characteristics @ 125°C

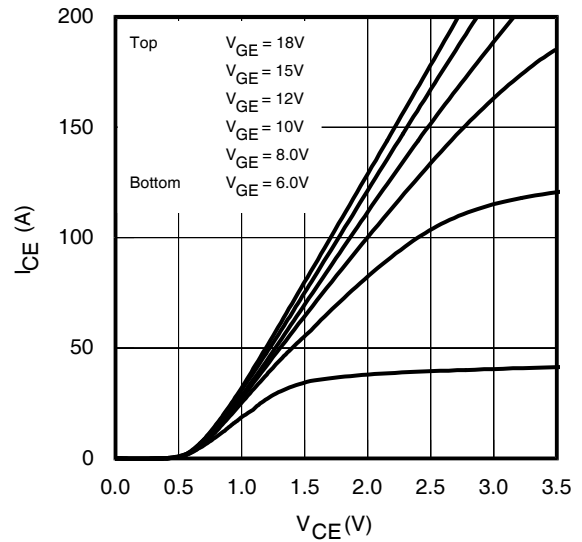


Fig 4. Typical Output Characteristics @ 150°C

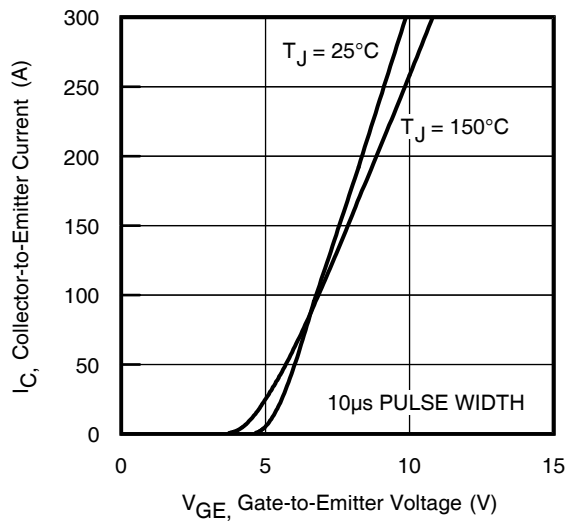


Fig 5. Typical Transfer Characteristics

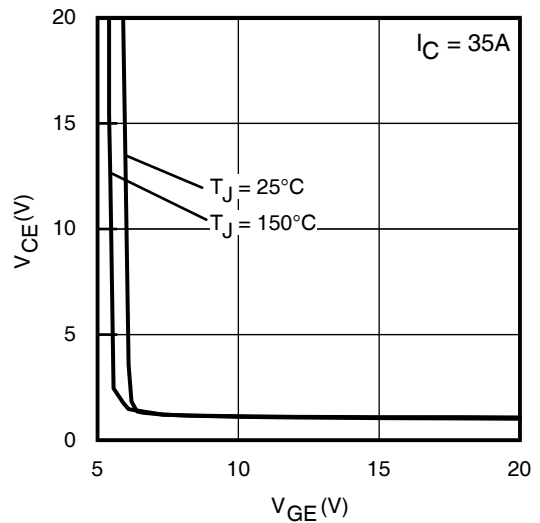


Fig 6.  $V_{CE(ON)}$  vs. Gate Voltage

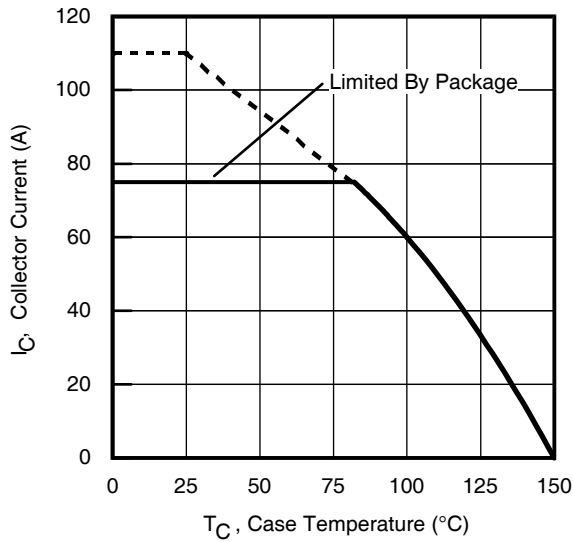


Fig 7. Maximum Collector Current vs. Case Temperature

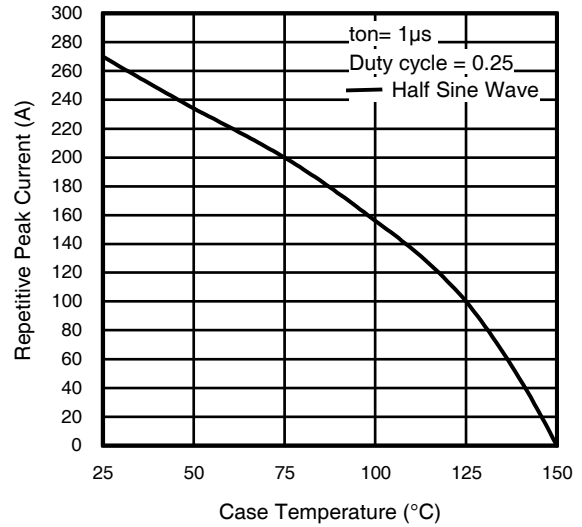


Fig 8. Typical Repetitive Peak Current vs. Case Temperature

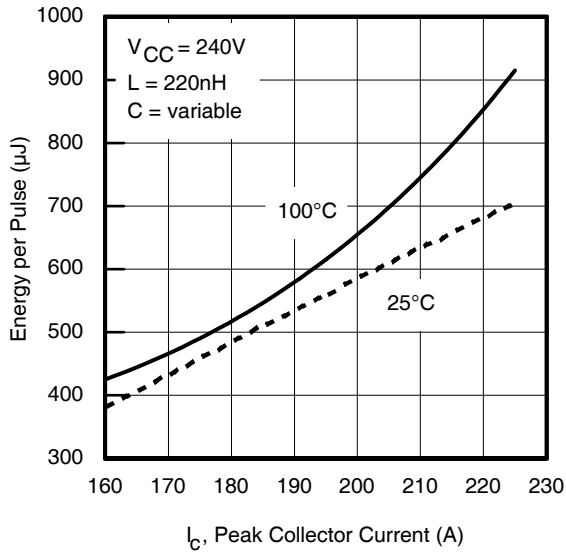


Fig 9. Typical  $E_{PULSE}$  vs. Collector Current

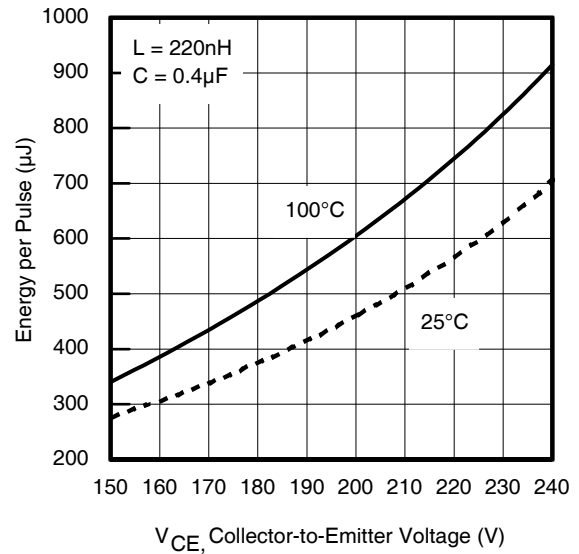


Fig 10. Typical  $E_{PULSE}$  vs. Collector-to-Emitter Voltage

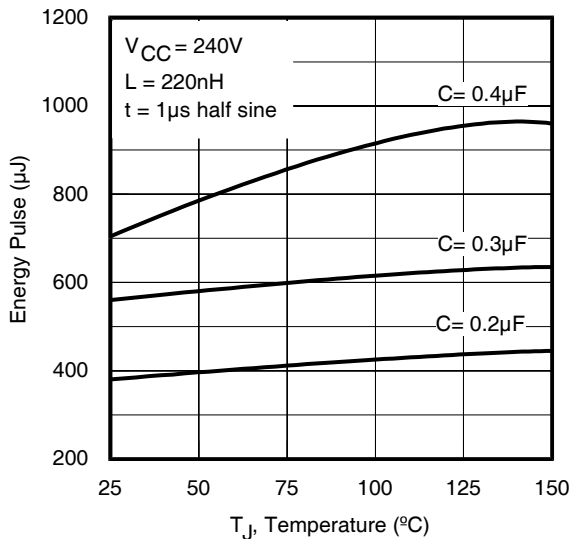


Fig 11.  $E_{PULSE}$  vs. Temperature

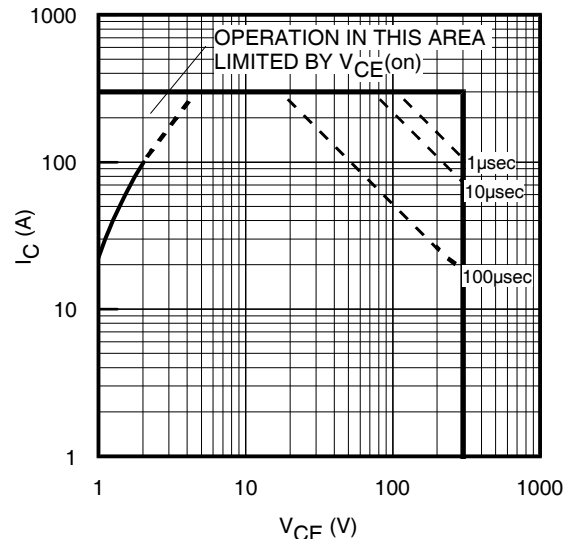


Fig 12. Forward Bias Safe Operating Area

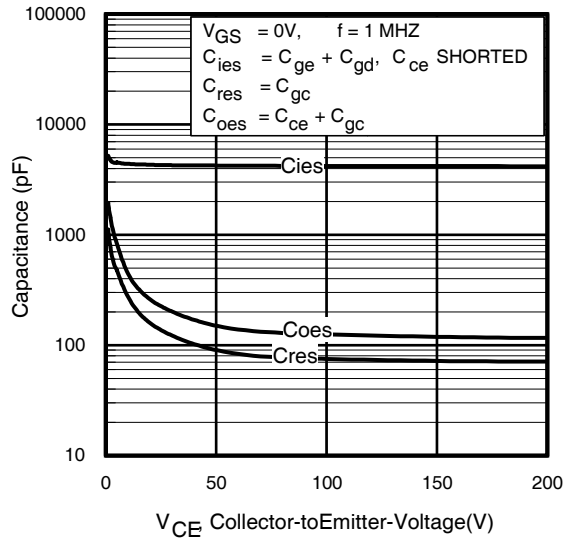


Fig 13. Typical Capacitance vs. Collector-to-Emitter Voltage

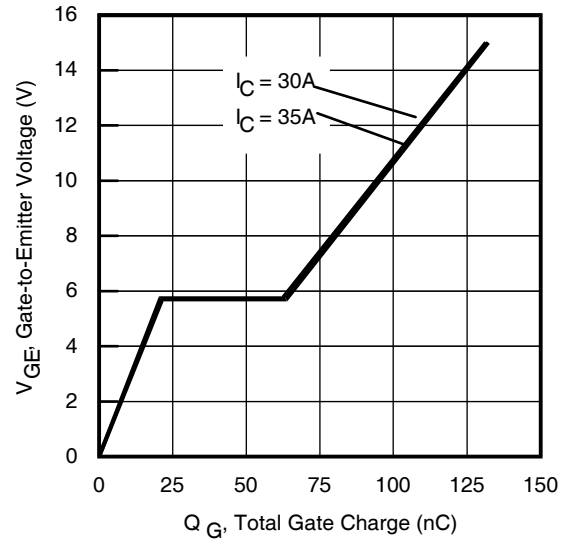


Fig 14. Typical Gate Charge vs. Gate-to-Emitter Voltage

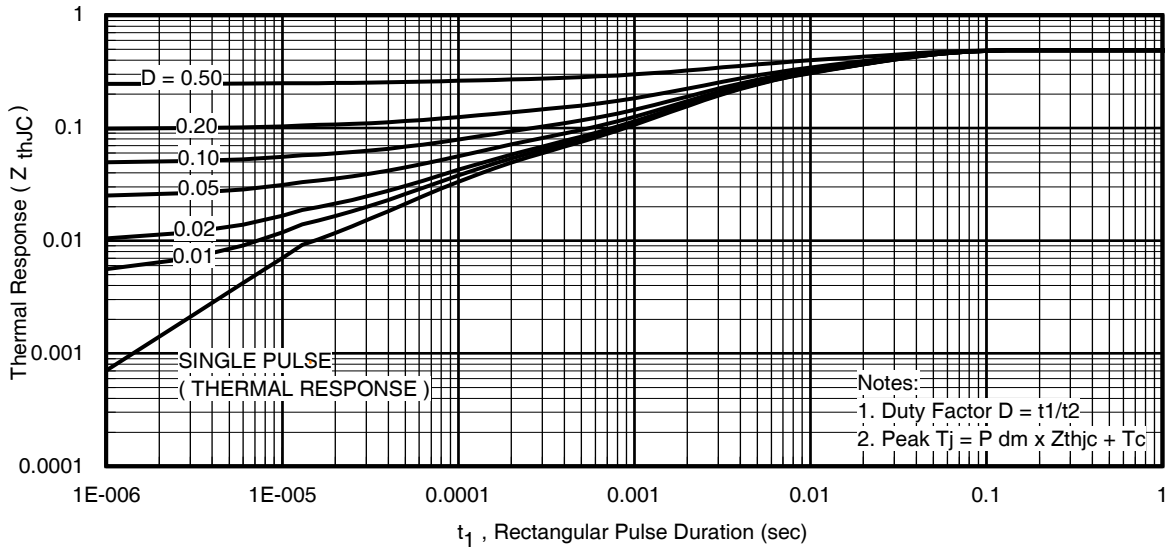


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Case (IGBT)

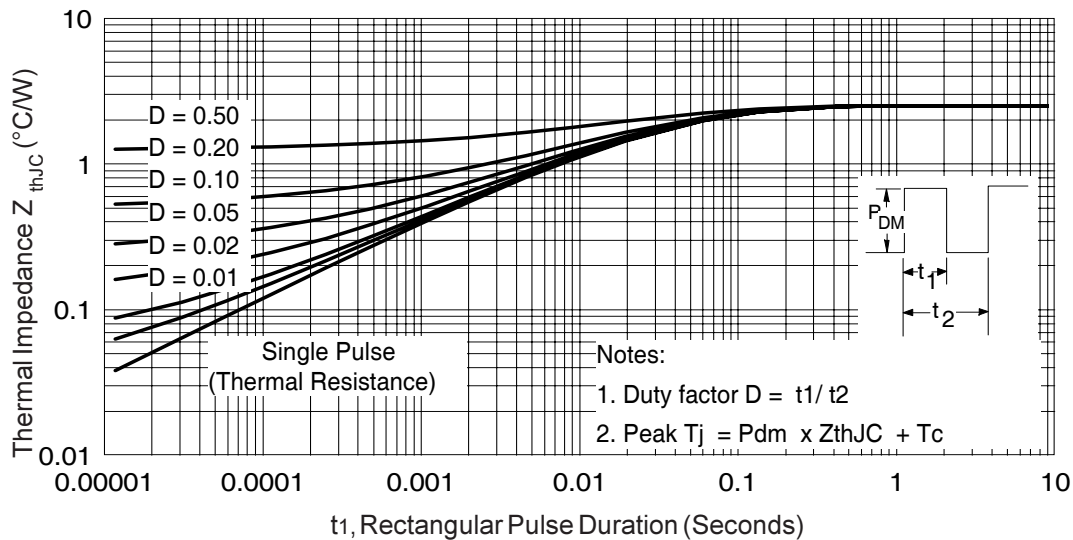


Fig 16. Maximum Effective Transient Thermal Impedance, Junction-to-Case (Diode)

# IRGP4055DPbF

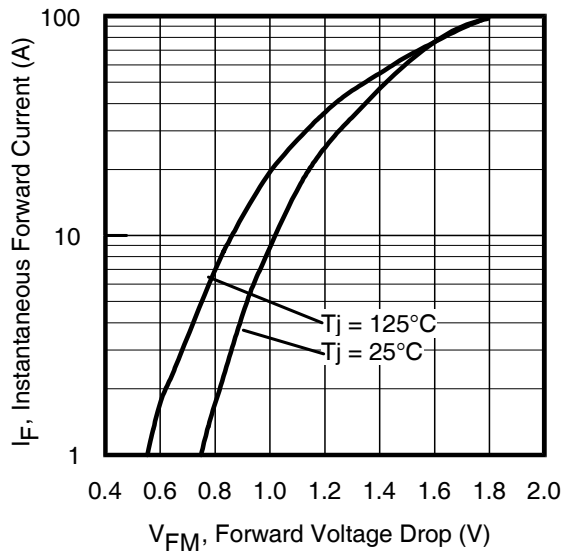


Fig. 17 - Typical Forward Voltage Drop Characteristics

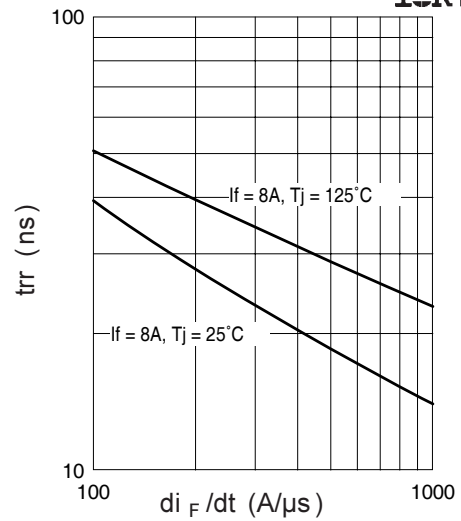


Fig. 18. Typical Reverse Recovery vs.  $di_F/dt$

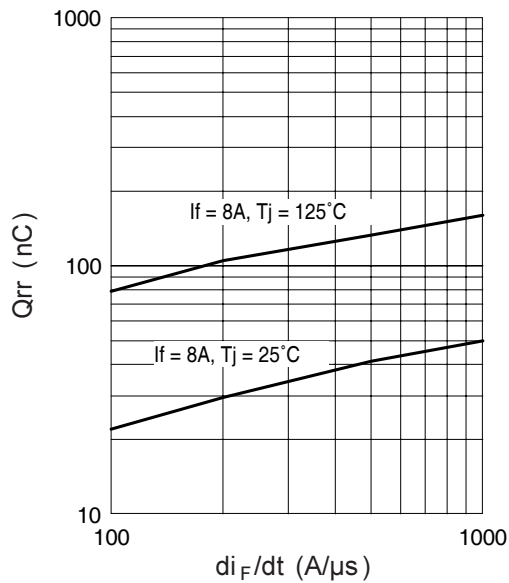


Fig. 19 - Typical Stored Charge vs.  $di_F/dt$

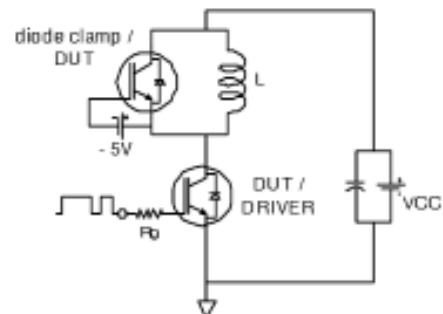


Fig. 20 - Switching Loss Circuit

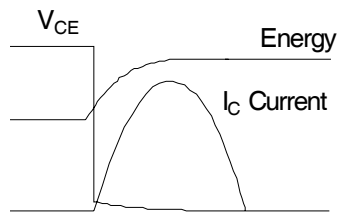


Fig 21b.  $t_{st}$  Test Waveforms

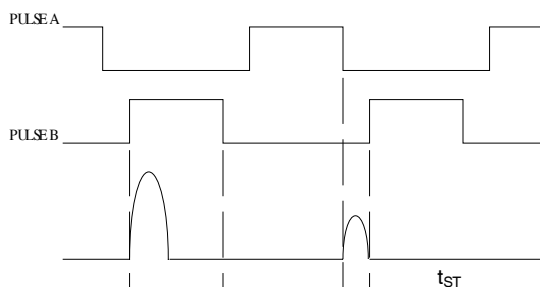


Fig 21c.  $E_{PULSE}$  Test Waveforms

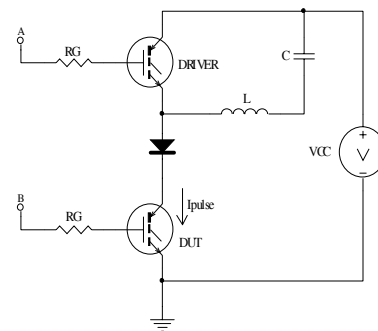


Fig 21a.  $t_{st}$  and  $E_{PULSE}$  Test Circuit

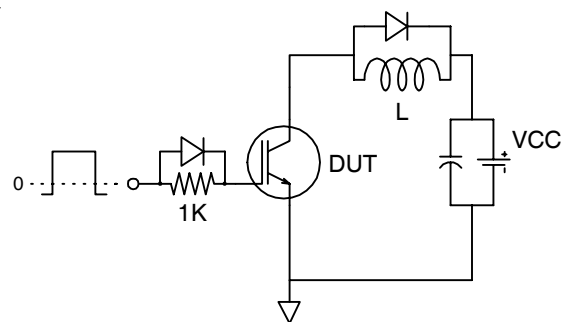
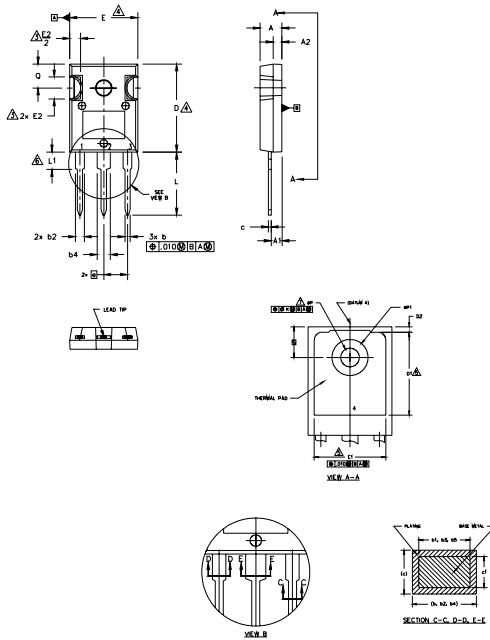


Fig. 22 - Gate Charge Circuit (turn-off)

## TO-247AC Package Outline Dimensions are shown in millimeters (inches)



- NOTES:
1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
  2. DIMENSIONS ARE SHOWN IN INCHES.
  3. CONTOUR OF SLOT OPTIONAL.
  4. DIMENSION D & E DO NOT INCLUDE WELD FLASH. WELD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
  5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
  6. LEAD FINISH UNCONTROLLED IN L1.
  7.  $\phi P$  TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
  8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC.

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.055	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	-	13.08	-	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	-	13.46	-	
E2	.178	.216	4.52	5.49	
e	.215 BSC		3.46 BSC		
e1	.010		0.25		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
$\phi P$	.140	.144	3.56	3.66	
$\phi P1$	-	.291	-	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

**LEAD ASSIGNMENTS**

- HEXFET**
- 1.- GATE
  - 2.- DRAIN
  - 3.- SOURCE
  - 4.- DRAIN

**IGBTs, CoPACK**

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

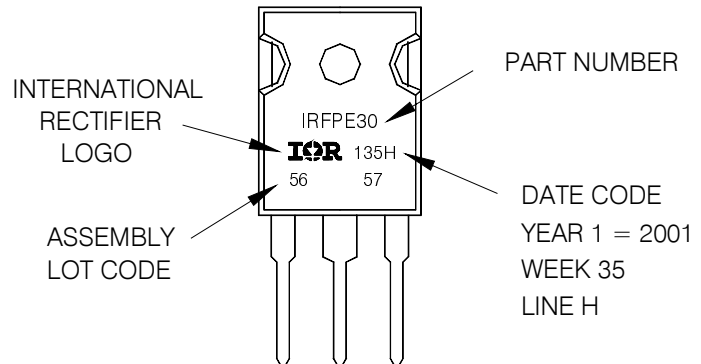
**DIODES**

- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE

## TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30  
WITH ASSEMBLY  
LOT CODE 5657  
ASSEMBLED ON WW 35, 2001  
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position  
indicates "Lead-Free"



**TO-247AC package is not recommended for Surface Mount Application.**

The specifications set forth in this data sheet are the sole and exclusive specifications applicable to the identified product, and no specifications or features are implied whether by industry custom, sampling or otherwise. We qualify our products in accordance with our internal practices and procedures, which by their nature do not include qualification to all possible or even all widely used applications. Without limitation, we have not qualified our product for medical use or applications involving hi-reliability applications. Customers are encouraged to and responsible for qualifying product to their own use and their own application environments, especially where particular features are critical to operational performance or safety. Please contact your IR representative if you have specific design or use requirements or for further information.

Data and specifications subject to change without notice. This product has been designed for the Industrial market. Qualification Standards can be found on IR's Web site.

Note: For the most current drawings please refer to the IR website at:  
<http://www.irf.com/package/>