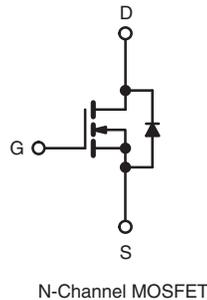
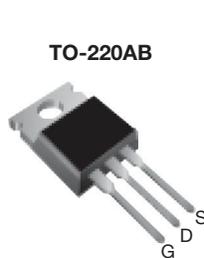


## Power MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	100	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 5.0$ V	0.077
$Q_g$ (Max.) (nC)	64	
$Q_{gs}$ (nC)	9.4	
$Q_{gd}$ (nC)	27	
Configuration	Single	



### FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Logic-Level Gate Drive
- $R_{DS(on)}$  Specified at  $V_{GS} = 4$  V and 5 V
- 175 °C Operating Temperature
- Fast Switching
- Ease of Paralleling
- Compliant to RoHS Directive 2002/95/EC



**RoHS\***  
COMPLIANT

### DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRL540PbF SiHL540-E3
SnPb	IRL540 SiHL540

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	$V_{DS}$	100	V	
Gate-Source Voltage	$V_{GS}$	$\pm 10$		
Continuous Drain Current	$V_{GS}$ at 5.0 V	$T_C = 25$ °C	28	A
		$T_C = 100$ °C		
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	110		
Linear Derating Factor		1.0	W/°C	
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	440	mJ	
Avalanche Current <sup>a</sup>	$I_{AR}$	28	A	
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	15	mJ	
Maximum Power Dissipation	$T_C = 25$ °C	$P_D$	150	W
Peak Diode Recovery dV/dt <sup>c</sup>		dV/dt	5.5	V/ns
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature)	for 10 s		300 <sup>d</sup>	
Mounting Torque	6-32 or M3 screw		10	lbf · in
			1.1	N · m

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25$  V, starting  $T_J = 25$  °C,  $L = 841$   $\mu$ H,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 28$  A (see fig. 12c).
- $I_{SD} \leq 28$  A,  $di/dt \leq 170$  A/ $\mu$ s,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 175$  °C.
- 1.6 mm from case.

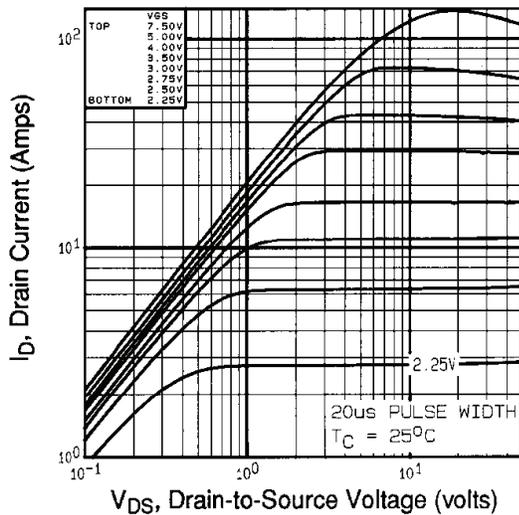
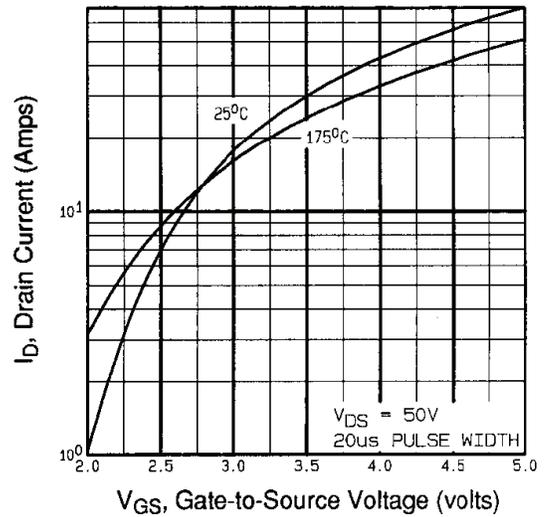
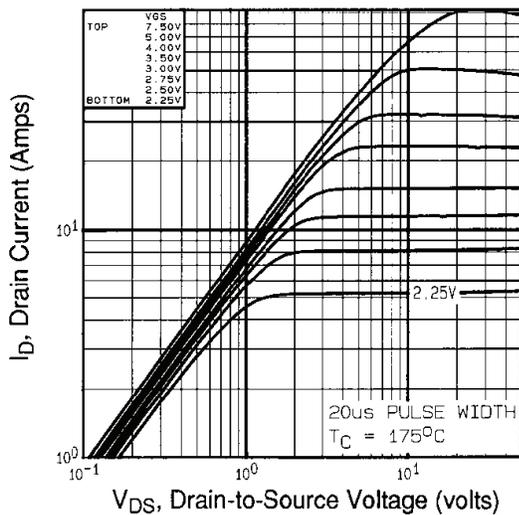
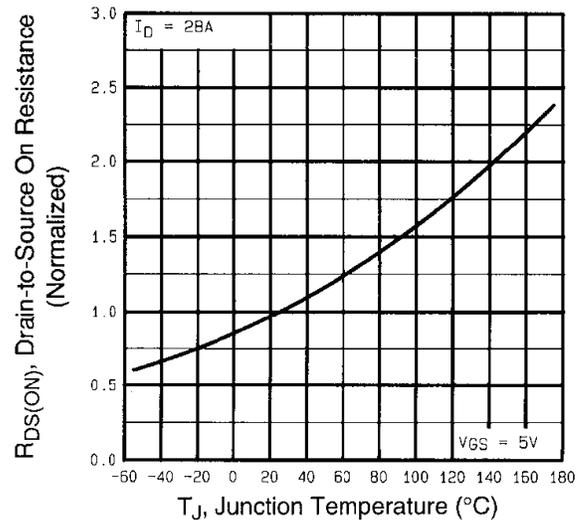
\* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	°C/W
Case-to-Sink, Flat, Greasd Surface	$R_{thCS}$	0.50	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	1.0	

SPECIFICATIONS ( $T_J = 25\text{ °C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	100	-	-	V	
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ °C}$ , $I_D = 1\text{ mA}$	-	0.12	-	V/°C	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.0	-	2.0	V	
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 10\text{ V}$	-	-	$\pm 100$	nA	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$	-	-	25	$\mu\text{A}$	
		$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ °C}$	-	-	250		
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 5.0\text{ V}$	-	-	0.077	$\Omega$	
		$V_{GS} = 4.0\text{ V}$	-	-	0.11		
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 17\text{ A}$	12	-	-	S	
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V},$ $V_{DS} = 25\text{ V},$ $f = 1.0\text{ MHz},$ see fig. 5	-	2200	-	pF	
Output Capacitance	$C_{oss}$		-	560	-		
Reverse Transfer Capacitance	$C_{rss}$		-	140	-		
Total Gate Charge	$Q_g$	$V_{GS} = 5.0\text{ V}$	$I_D = 28\text{ A}, V_{DS} = 80\text{ V},$ see fig. 6 and 13 <sup>b</sup>	-	-	64	nC
Gate-Source Charge	$Q_{gs}$			-	-	9.4	
Gate-Drain Charge	$Q_{gd}$			-	-	27	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50\text{ V}, I_D = 28\text{ A},$ $R_g = 9.0\text{ }\Omega, R_D = 1.7\text{ }\Omega,$ see fig. 10 <sup>b</sup>	-	8.5	-	ns	
Rise Time	$t_r$		-	170	-		
Turn-Off Delay Time	$t_{d(off)}$		-	35	-		
Fall Time	$t_f$		-	80	-		
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact	-	4.5	-	nH	
Internal Source Inductance	$L_S$		-	7.5	-		
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode	-	-	28	A	
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	110		
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ °C}, I_S = 28\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	2.5	V	
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ °C}, I_F = 28\text{ A},$ $di/dt = 100\text{ A}/\mu\text{s}^b$	-	200	260	ns	
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	1.7	2.90	$\mu\text{C}$	
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^\circ\text{C}$** 

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 2 - Typical Output Characteristics,  $T_C = 175\text{ }^\circ\text{C}$** 

**Fig. 4 - Normalized On-Resistance vs. Temperature**

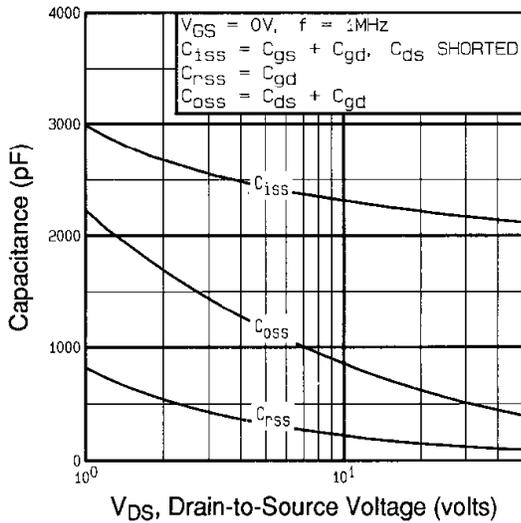


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

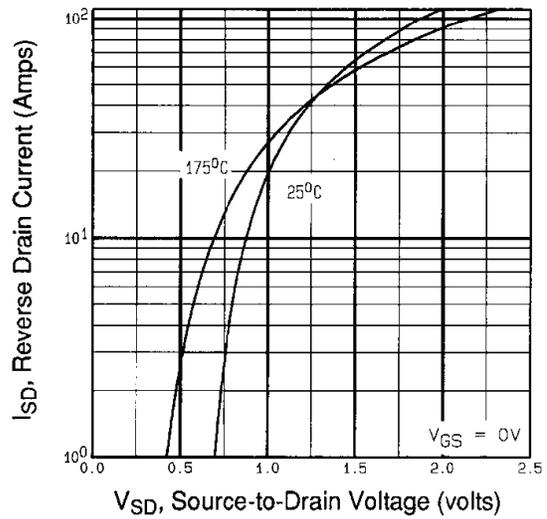


Fig. 7 - Typical Source-Drain Diode Forward Voltage

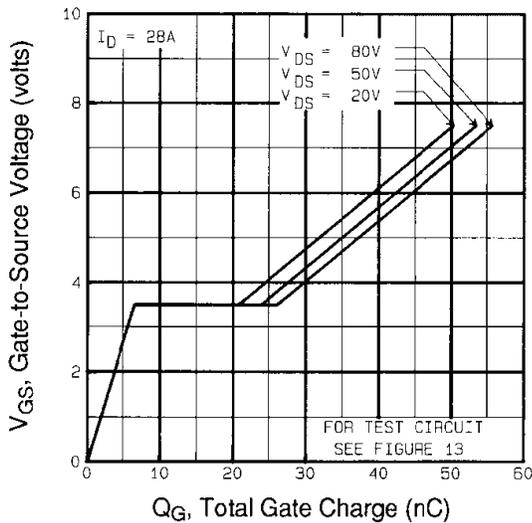


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

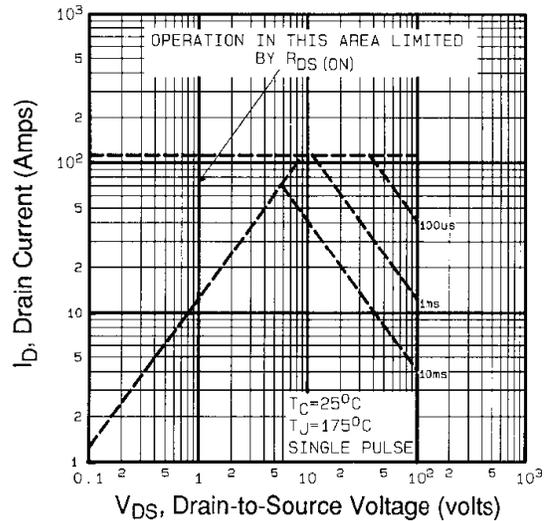


Fig. 8 - Maximum Safe Operating Area

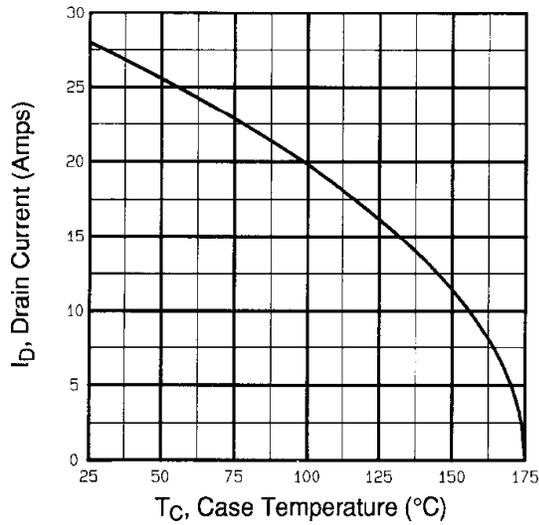


Fig. 9 - Maximum Safe Operating Area

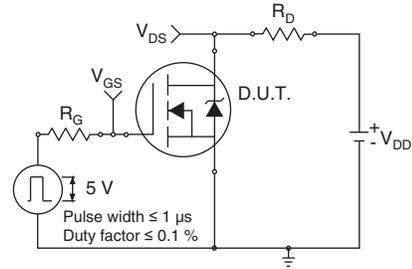


Fig. 10a - Switching Time Test Circuit

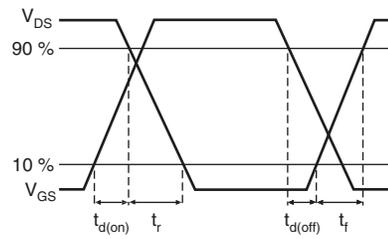


Fig. 10b - Switching Time Waveforms

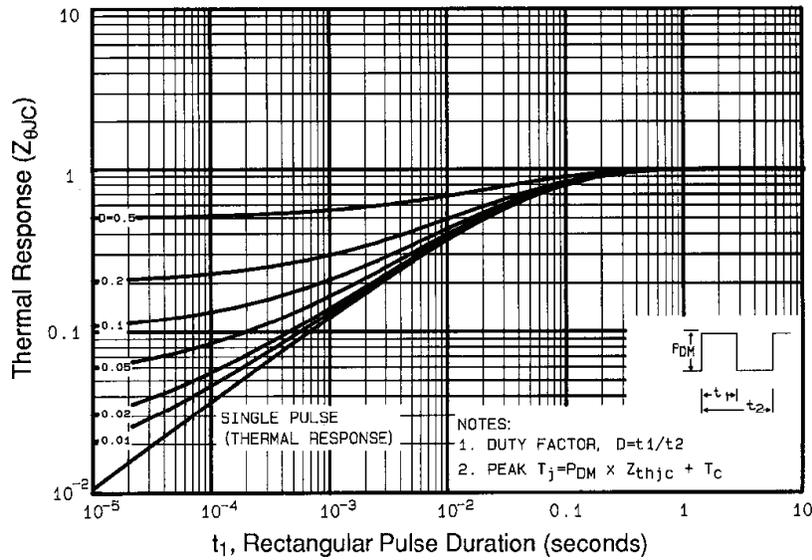


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

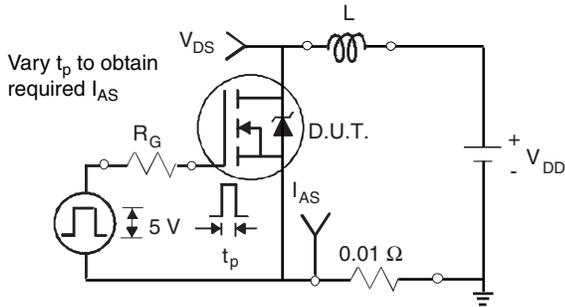


Fig. 12a - Unclamped Inductive Test Circuit

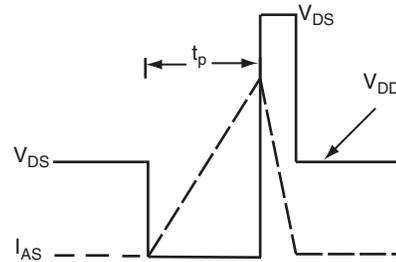


Fig. 12b - Unclamped Inductive Waveforms

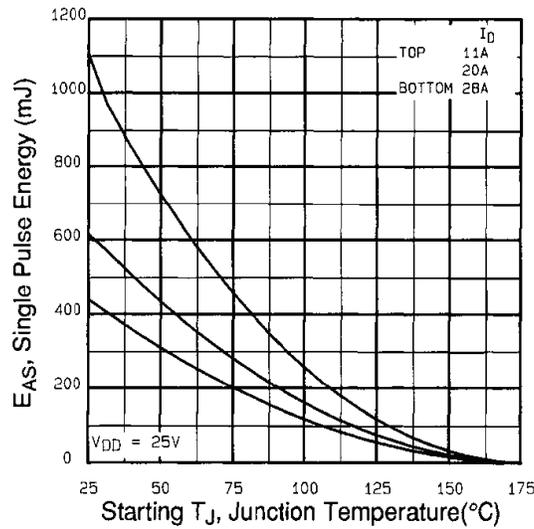


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

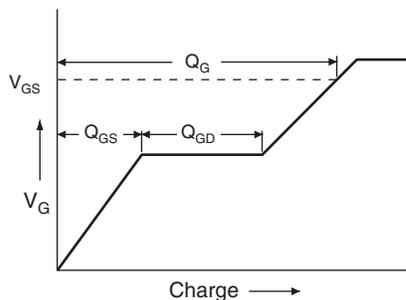


Fig. 13a - Basic Gate Charge Waveform

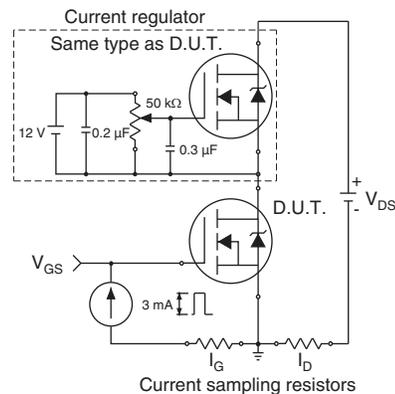
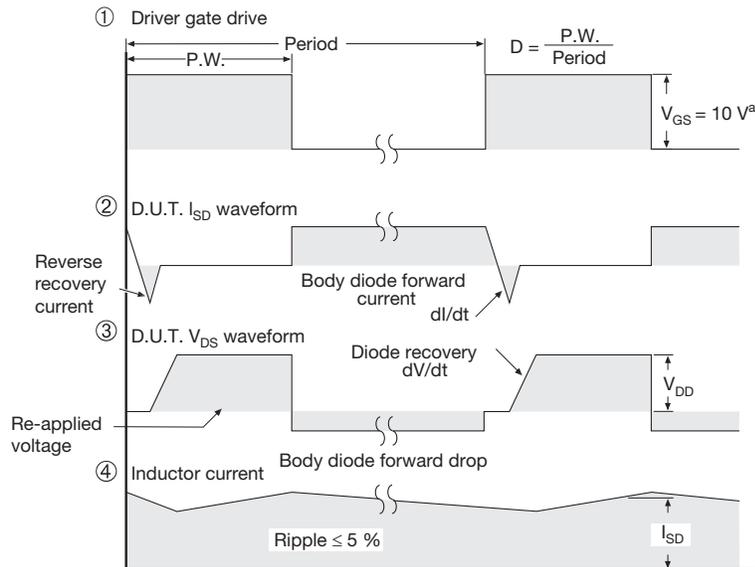
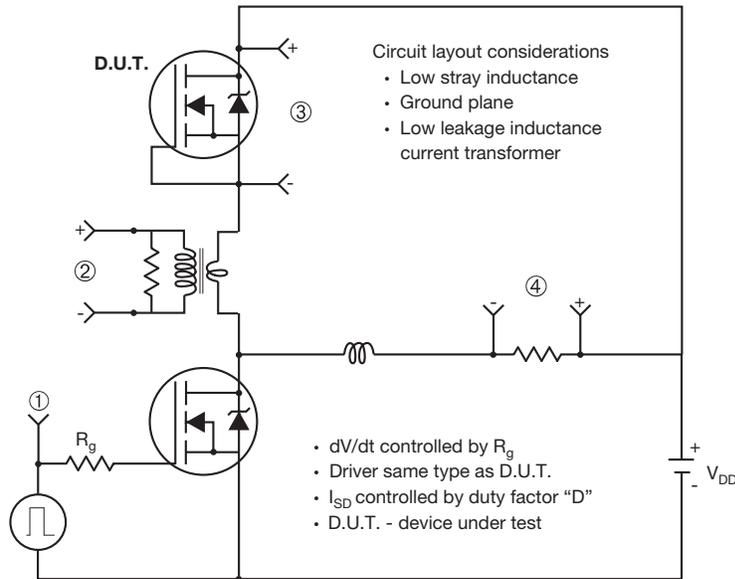


Fig. 13b - Gate Charge Test Circuit

### Peak Diode Recovery dV/dt Test Circuit



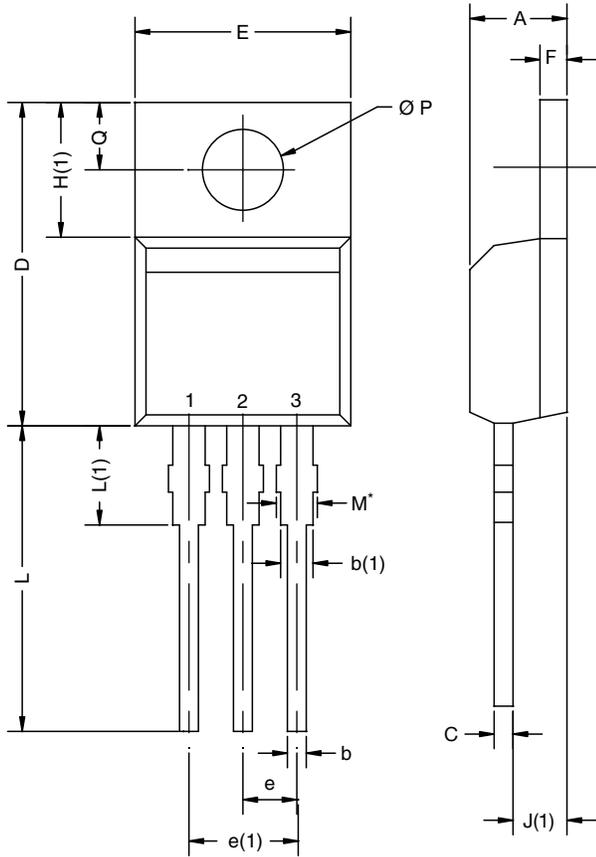
**Note**  
a.  $V_{GS} = 5\text{ V}$  for logic level devices

**Fig. 14 - For N-Channel**

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# TO-220AB



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
c	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
E	10.04	10.51	0.395	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
Ø P	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118

ECN: T13-0724-Rev. O, 14-Oct-13  
DWG: 5471

**Note**

\* M = 1.32 mm to 1.62 mm (dimension including protrusion)  
Heatsink hole for HVM



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