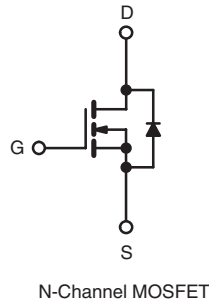
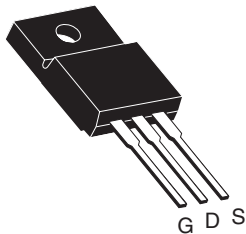


Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	100	
$R_{DS(on)}$ (Ω)	$V_{GS} = 5\text{ V}$	0.27
Q_g (Max.) (nC)	12	
Q_{gs} (nC)	3.0	
Q_{gd} (nC)	7.1	
Configuration	Single	

TO-220 FULLPAK



FEATURES

- Isolated Package
- High Voltage Isolation = 2.5 kV_{RMS} (t = 60 s; f = 60 Hz)
- Sink to Lead Creepage Distance = 4.8 mm
- Logic-Level Gate Drive
- $R_{DS(on)}$ Specified at $V_{GS} = 4\text{ V}$ and 5 V
- Fast Switching
- Ease of Paralleling
- Lead (Pb)-free Available



RoHS*
COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 FULLPAK eliminates the need for additional insulating hardware in commercial-industrial applications. The molding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The FULLPAK is mounted to a heatsink using a single clip or by a single screw fixing.

ORDERING INFORMATION

Package	TO-220 FULLPAK
Lead (Pb)-free	IRLI520GPbF
	SiHLI520G-E3
SnPb	IRLI520G
	SiHLI520G

ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V _{DS}	100	V
Gate-Source Voltage			V _{GS}	± 10	
Continuous Drain Current	V _{GS} at 5 V	T _C = 25 °C	I _D	7.2	A
		T _C = 100 °C		5.1	
Pulsed Drain Current ^a			I _{DM}	29	
Linear Derating Factor				0.24	W/°C
Single Pulse Avalanche Energy ^b			E _{AS}	170	mJ
Repetitive Avalanche Current ^a			I _{AR}	7.2	A
Repetitive Avalanche Energy ^a			E _{AR}	3.7	mJ
Maximum Power Dissipation	T _C = 25 °C		P _D	37	W
Peak Diode Recovery dV/dt ^c			dV/dt	5.5	V/ns
Operating Junction and Storage Temperature Range			T _J , T _{stg}	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300 ^d	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes

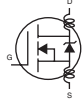
- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25\text{ V}$, starting $T_J = 25\text{ }^{\circ}\text{C}$, $L = 4.9\text{ mH}$, $R_G = 25\text{ }\Omega$, $I_{AS} = 7.2\text{ A}$ (see fig. 12).
- $I_{SD} \leq 9.2\text{ A}$, $dI/dt \leq 110\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 175\text{ }^{\circ}\text{C}$.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

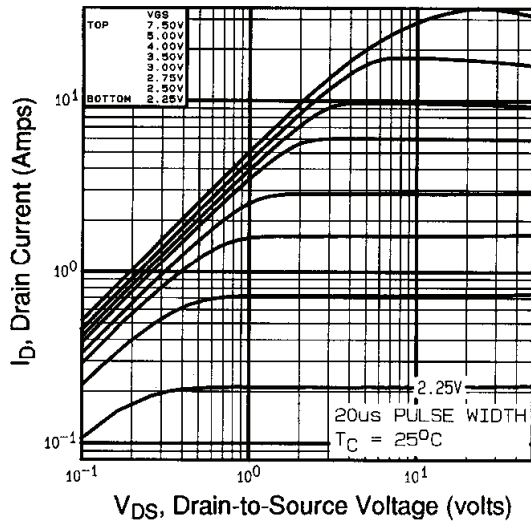
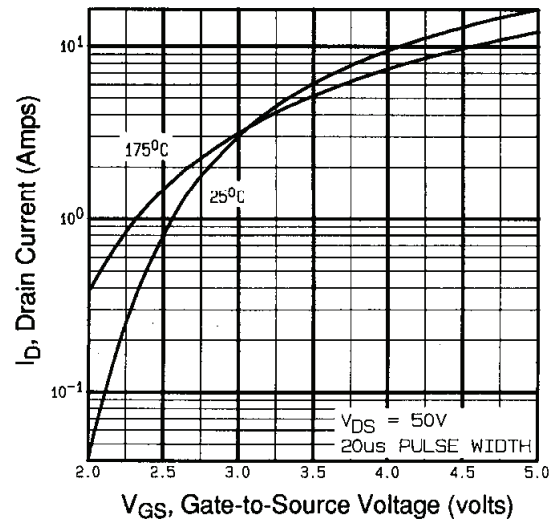
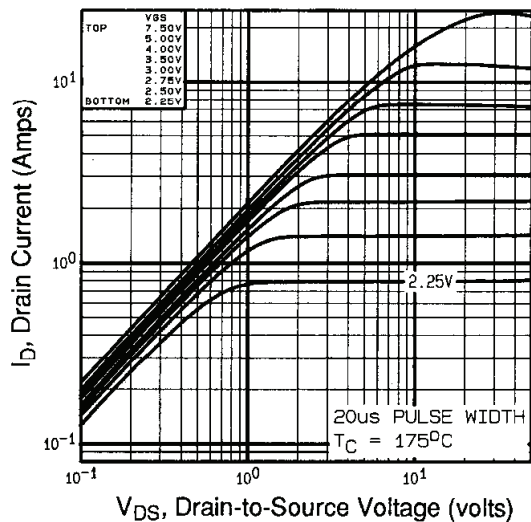
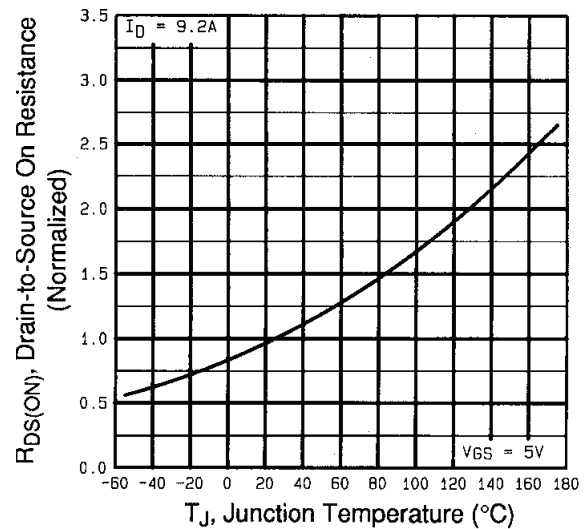
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	65	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	4.1	

SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		100	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.12	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		1.0	-	2.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 10 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V		-	-	25	μA
		V _{DS} = 80 V, V _{GS} = 0 V, T _J = 150 °C		-	-	250	
Drain-Source On-State Resistance	R _{DS (on)}	V _{GS} = 5 V	I _D = 4.3 A ^b	-	-	0.27	Ω
		V _{GS} = 4 V	I _D = 3.6 A ^b	-	-	0.38	
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 4.3 A ^b		3.3	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	490	-	pF
Output Capacitance	C _{oss}			-	150	-	
Reverse Transfer Capacitance	C _{rss}			-	30	-	
Drain to Sink Capacitance	C	f = 1.0 MHz		-	12	-	
Total Gate Charge	Q _g	V _{GS} = 5 V	I _D = 9.2 A, V _{DS} = 80 V, see fig. 6 and 13 ^b	-	-	12	nC
Gate-Source Charge	Q _{gs}			-	-	3.0	
Gate-Drain Charge	Q _{gd}			-	-	7.1	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 50 V, I _D = 9.2 A, R _G = 9 Ω, R _D = 5.2 Ω, see fig. 10 ^b		-	9.8	-	ns
Rise Time	t _r			-	64	-	
Turn-Off Delay Time	t _{d(off)}			-	21	-	
Fall Time	t _f			-	27	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal Source Inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	7.2	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	29	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 7.2 A, V _{GS} = 0 V ^b		-	-	2.5	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 9.2 A, dI/dt = 100 A/μs ^b		-	130	190	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	0.83	1.0	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Fig. 3 - Typical Output Characteristics, $T_C = 25^\circ\text{C}$

Fig. 5 - Typical Transfer Characteristics

Fig. 4 - Typical Output Characteristics, $T_C = 175^\circ\text{C}$

Fig. 6 - Normalized On-Resistance vs. Temperature

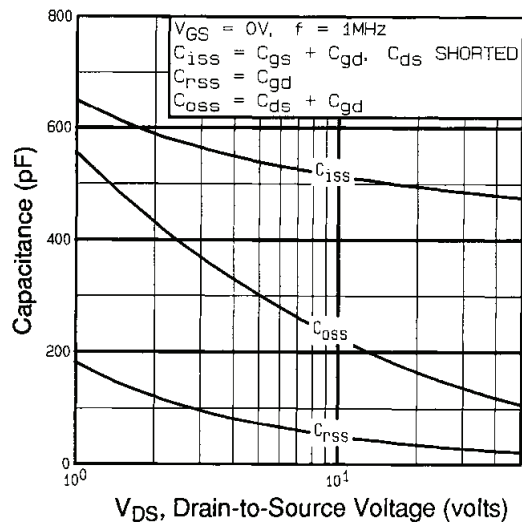


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

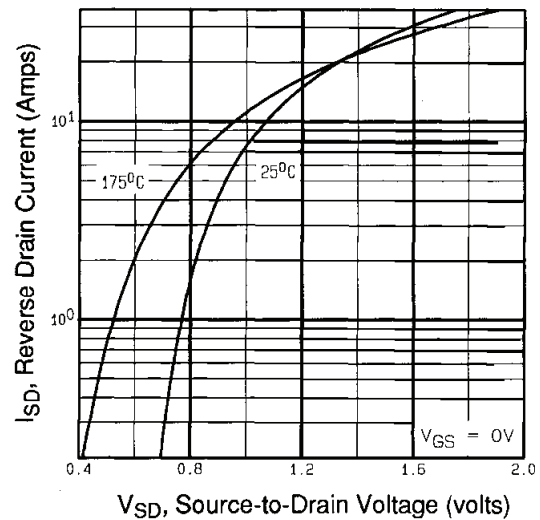


Fig. 7 - Typical Source-Drain Diode Forward Voltage

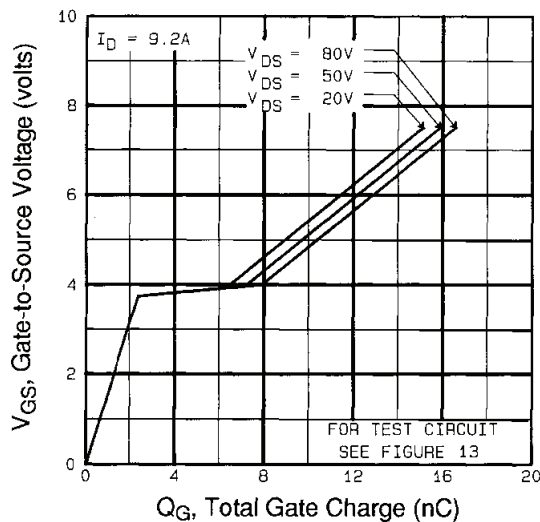


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

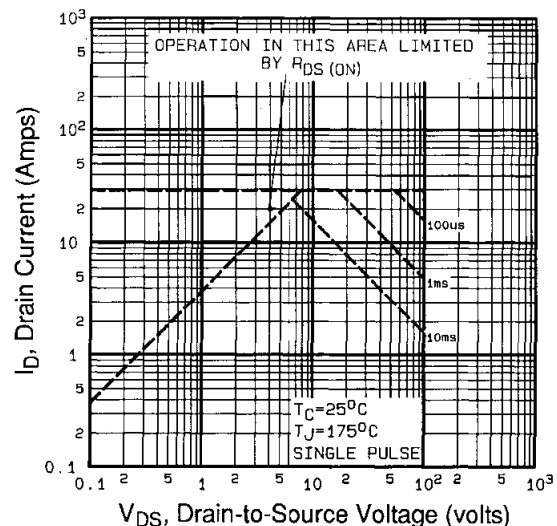


Fig. 8 - Maximum Safe Operating Area

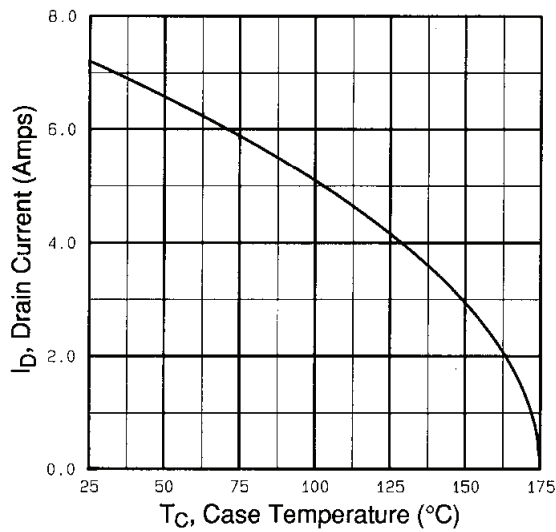


Fig. 9 - Maximum Drain Current vs. Case Temperature

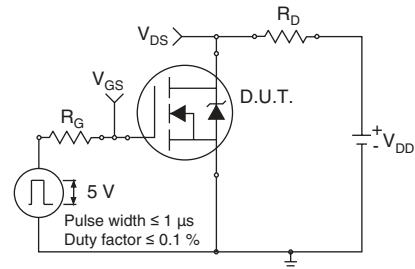


Fig. 10a - Switching Time Test Circuit

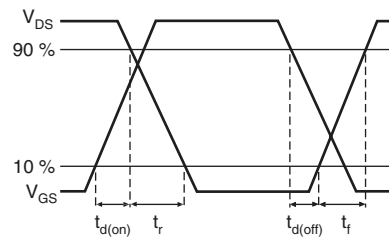


Fig. 10b - Switching Time Waveforms

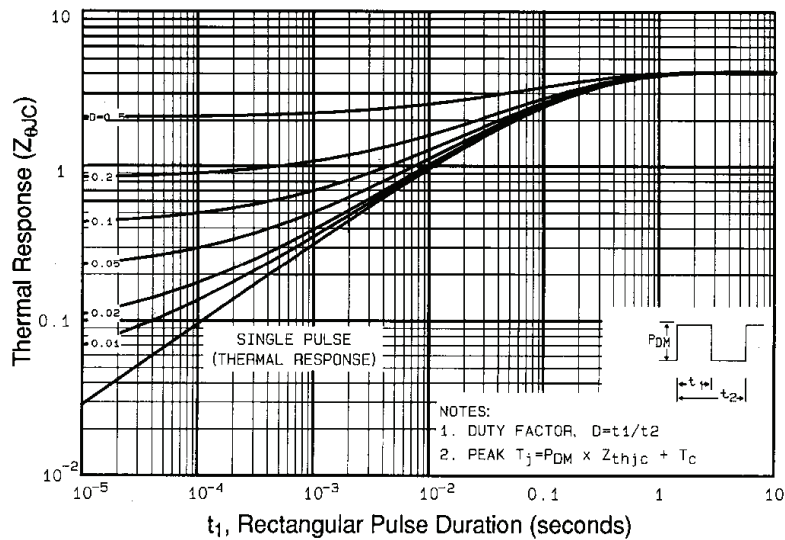


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

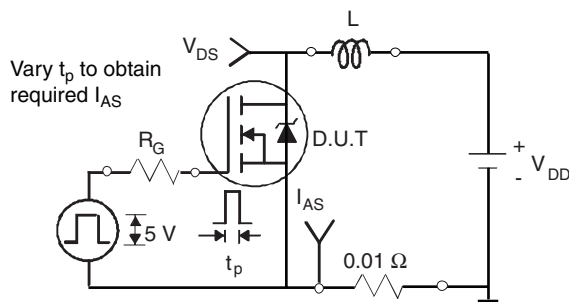


Fig. 12a - Unclamped Inductive Test Circuit

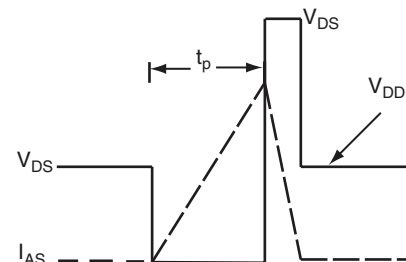


Fig. 12b - Unclamped Inductive Waveforms

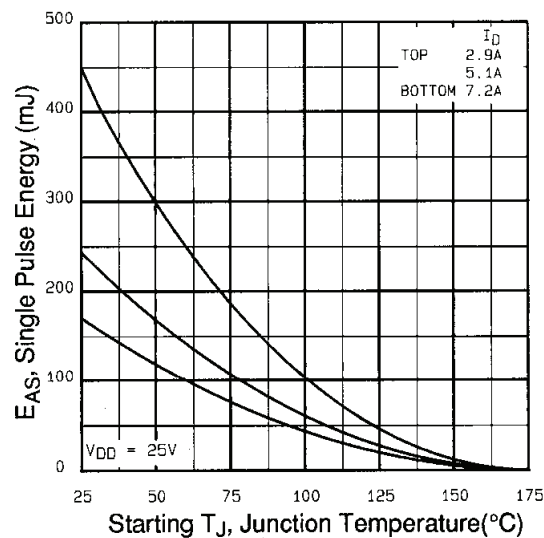


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

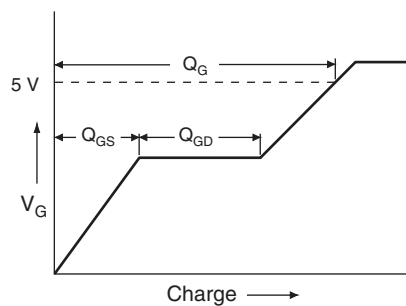


Fig. 13a - Basic Gate Charge Waveform

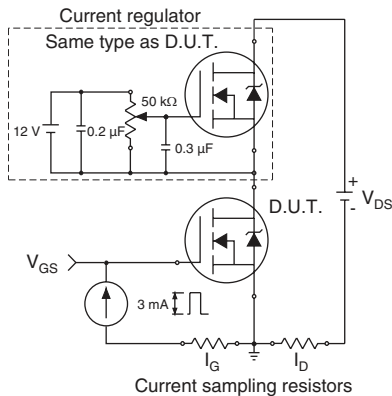


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

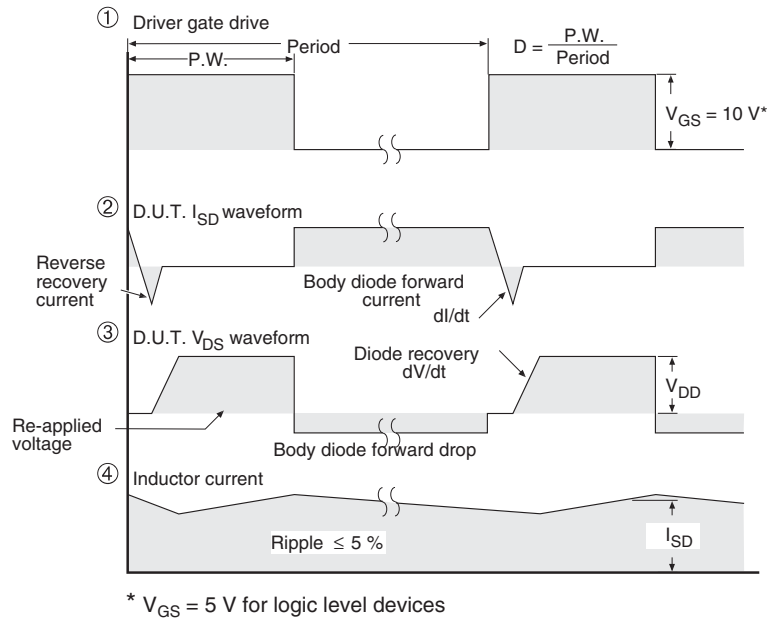
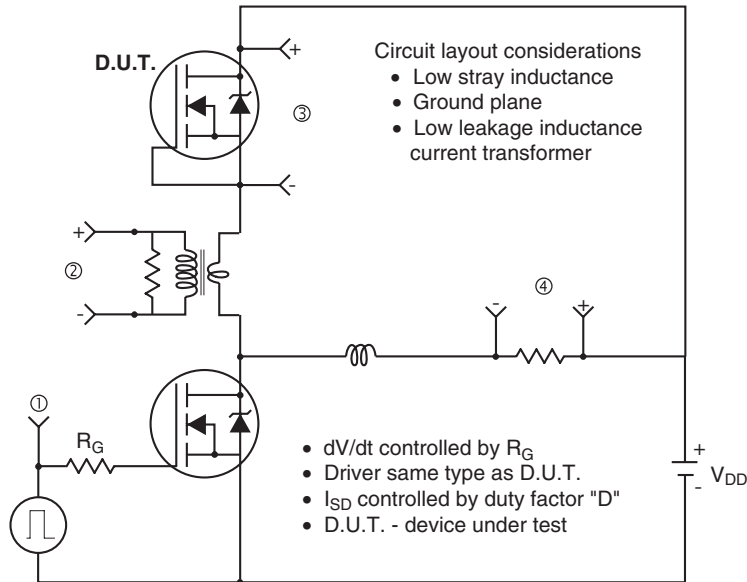


Fig.14 - For N-Channel

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