

FEATURES

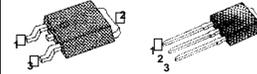
- ◆ Avalanche Rugged Technology
- ◆ Rugged Gate Oxide Technology
- ◆ Lower Input Capacitance
- ◆ Improved Gate Charge
- ◆ Extended Safe Operating Area
- ◆ Lower Leakage Current: 10µA (Max.) @ $V_{DS} = 100V$
- ◆ Lower $R_{DS(ON)}$: 0.336Ω (Typ.)

$$BV_{DSS} = 100 V$$

$$R_{DS(on)} = 0.44\Omega$$

$$I_D = 4.7 A$$

D-PAK **I-PAK**



1. Gate 2. Drain 3. Source

Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
V_{DSS}	Drain-to-Source Voltage	100	V
I_D	Continuous Drain Current ($T_C=25^\circ C$)	4.7	A
	Continuous Drain Current ($T_C=100^\circ C$)	3	
I_{DM}	Drain Current-Pulsed (1)	16	A
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulsed Avalanche Energy (2)	58	mJ
I_{AR}	Avalanche Current (1)	4.7	A
E_{AR}	Repetitive Avalanche Energy (1)	2.2	mJ
dv/dt	Peak Diode Recovery dv/dt (3)	6.5	V/ns
P_D	Total Power Dissipation ($T_A=25^\circ C$) *	2.5	W
	Total Power Dissipation ($T_C=25^\circ C$)	22	W
	Linear Derating Factor	0.18	W/ $^\circ C$
T_J, T_{STG}	Operating Junction and Storage Temperature Range	- 55 to +150	$^\circ C$
T_L	Maximum Lead Temp. for Soldering Purposes, 1/8. from case for 5-seconds	300	

Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	5.6	$^\circ C/W$
$R_{\theta JA}$	Junction-to-Ambient *	--	50	
$R_{\theta JA}$	Junction-to-Ambient	--	110	

* When mounted on the minimum pad size recommended (PCB Mount).

Rev. B

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Electrical Characteristics (T_C=25°C unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV _{DSS}	Drain-Source Breakdown Voltage	100	--	--	V	V _{GS} =0V, I _D =250μA
ΔBV/ΔT _J	Breakdown Voltage Temp. Coeff.	--	0.1	--	V/°C	I _D =250μA See Fig 7
V _{GS(th)}	Gate Threshold Voltage	1.0	--	2.0	V	V _{DS} =5V, I _D =250μA
I _{GSS}	Gate-Source Leakage, Forward	--	--	100	nA	V _{GS} =20V
	Gate-Source Leakage, Reverse	--	--	-100		V _{GS} =-20V
I _{DSS}	Drain-to-Source Leakage Current	--	--	10	μA	V _{DS} =100V
		--	--	100		V _{DS} =80V, T _C =125°C
R _{DS(on)}	Static Drain-Source On-State Resistance	--	--	0.44	Ω	V _{GS} =5V, I _D =2.35A (4)
g _{fs}	Forward Transconductance	--	3.2	--	Ū	V _{DS} =40V, I _D =2.35A (4)
C _{iss}	Input Capacitance	--	180	235	pF	V _{GS} =0V, V _{DS} =25V, f=1MHz See Fig 5
C _{oss}	Output Capacitance	--	50	65		
C _{rss}	Reverse Transfer Capacitance	--	20	25		
t _{d(on)}	Turn-On Delay Time	--	8	25	ns	V _{DD} =50V, I _D =5.6A, R _G =12Ω See Fig 13 (4) (5)
t _r	Rise Time	--	10	30		
t _{d(off)}	Turn-Off Delay Time	--	17	45		
t _f	Fall Time	--	8	25		
Q _g	Total Gate Charge	--	5.5	8	nC	V _{DS} =80V, V _{GS} =5V, I _D =5.6A See Fig 6 & Fig 12 (4) (5)
Q _{gs}	Gate-Source Charge	--	0.9	--		
Q _{gd}	Gate-Drain (. Miller.) Charge	--	3.5	--		

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
I _S	Continuous Source Current	--	--	4.7	A	Integral reverse pn-diode in the MOSFET
I _{SM}	Pulsed-Source Current (1)	--	--	16		
V _{SD}	Diode Forward Voltage (4)	--	--	1.5	V	T _J =25°C, I _S =4.7A, V _{GS} =0V
t _{rr}	Reverse Recovery Time	--	85	--	ns	T _J =25°C, I _F =5.6A
Q _{rr}	Reverse Recovery Charge	--	0.23	--	μC	di _F /dt=100A/μs (4)

Notes;

- (1) Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
- (2) L=4mH, I_{AS}=4.7A, V_{DD}=25V, R_G=27Ω, Starting T_J=25°C
- (3) I_{SD} ≤ 5.6A, di/dt ≤ 250A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J=25°C
- (4) Pulse Test: Pulse Width = 250μs, Duty Cycle ≤ 2%
- (5) Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

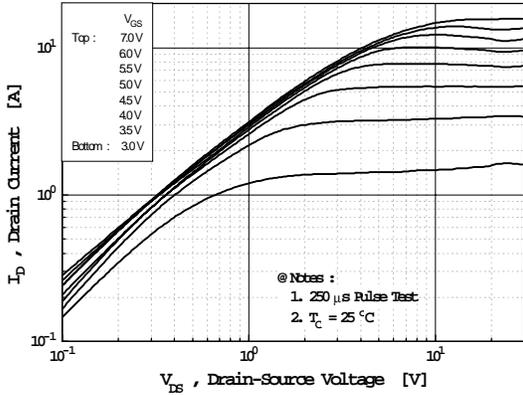


Fig 2. Transfer Characteristics

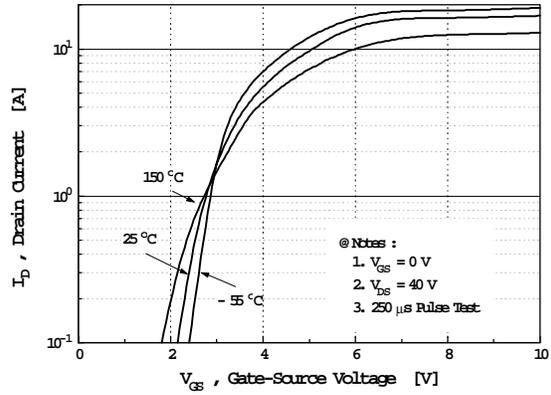


Fig 3. On-Resistance vs. Drain Current

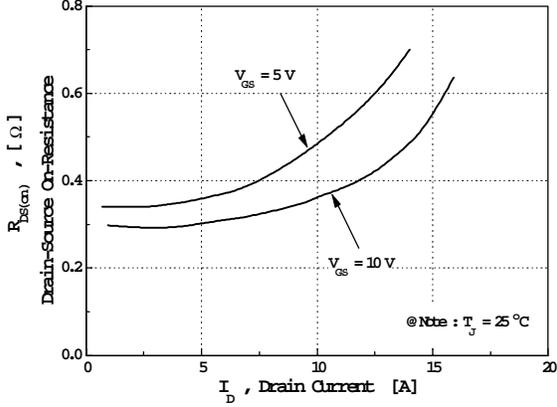


Fig 4. Source-Drain Diode Forward Voltage

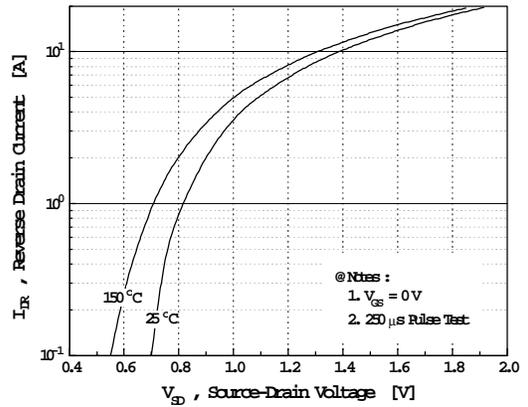


Fig 5. Capacitance vs. Drain-Source Voltage

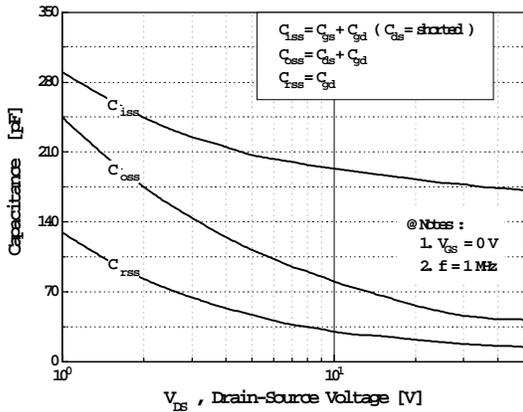


Fig 6. Gate Charge vs. Gate-Source Voltage

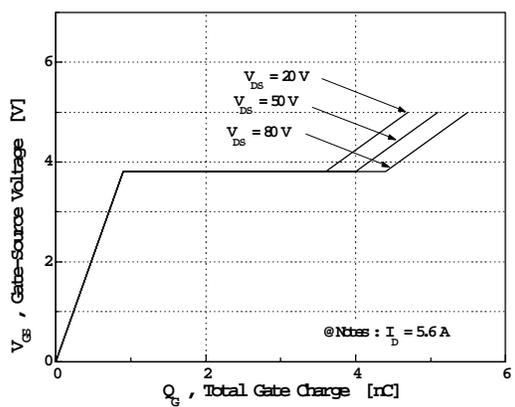


Fig 7. Breakdown Voltage vs. Temperature

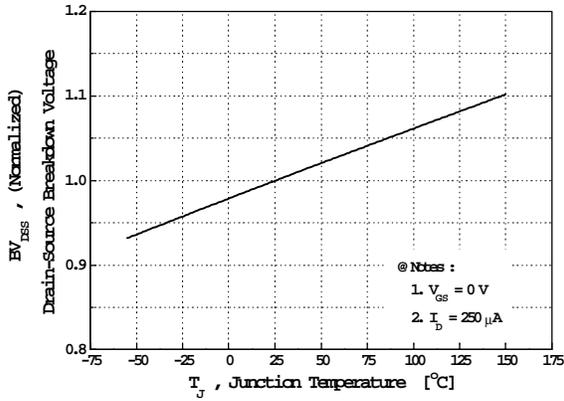


Fig 8. On-Resistance vs. Temperature

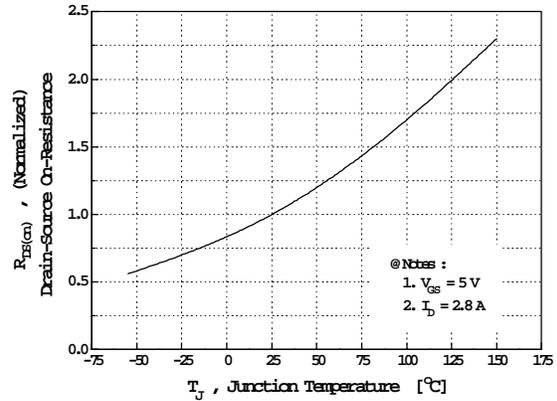


Fig 9. Max. Safe Operating Area

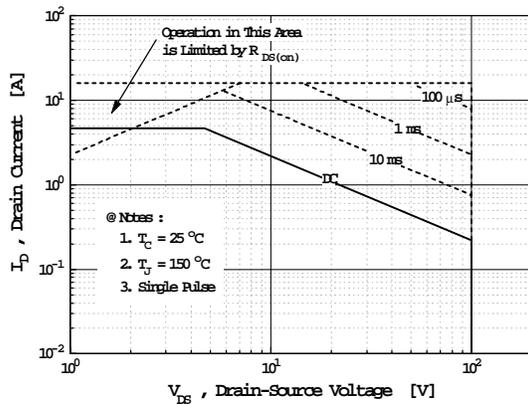


Fig 10. Max. Drain Current vs. Case Temperature

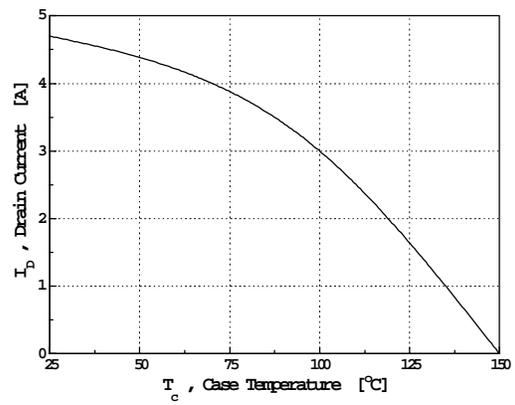


Fig 11. Thermal Response

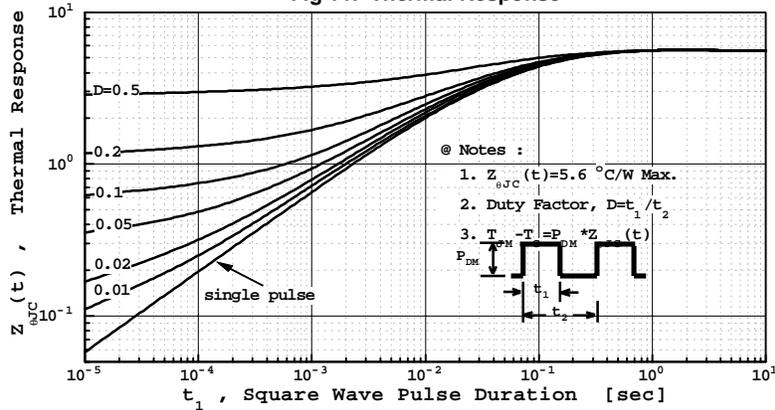


Fig 12. Gate Charge Test Circuit & Waveform

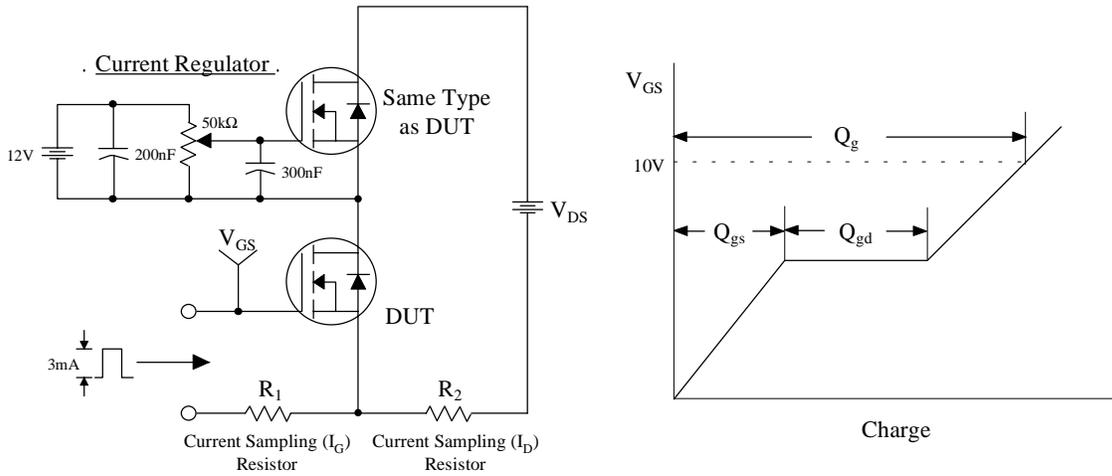


Fig 13. Resistive Switching Test Circuit & Waveforms

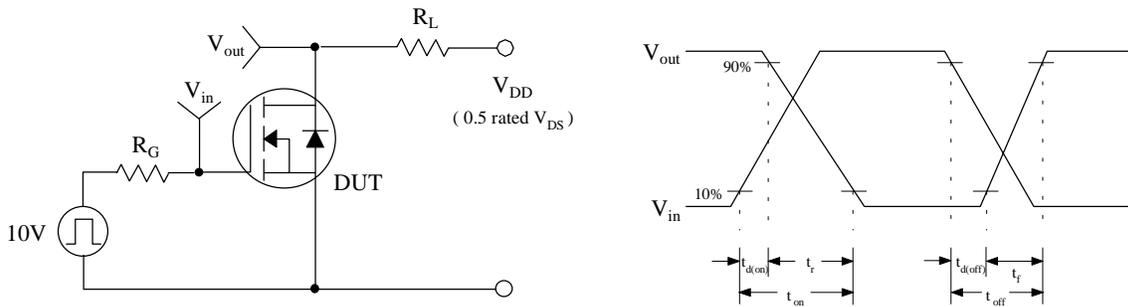


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

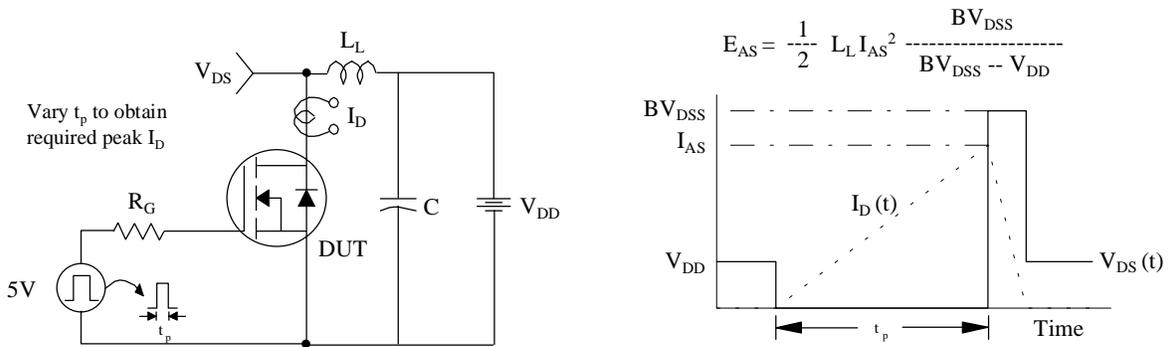
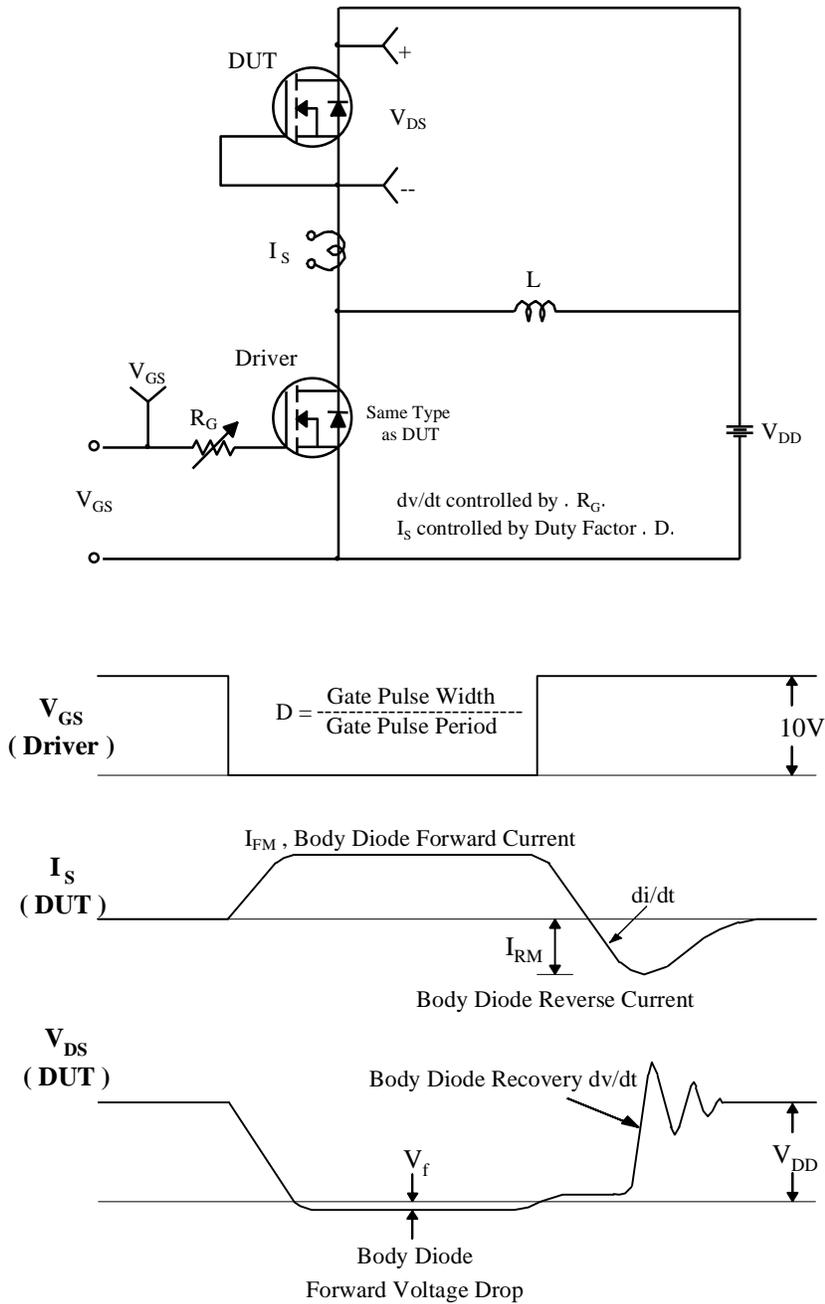


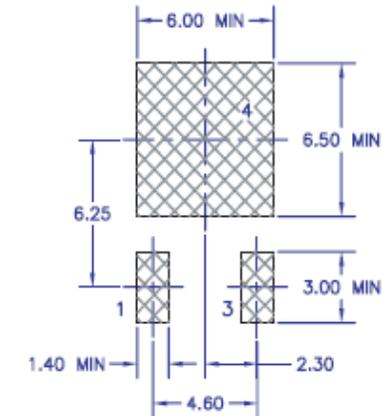
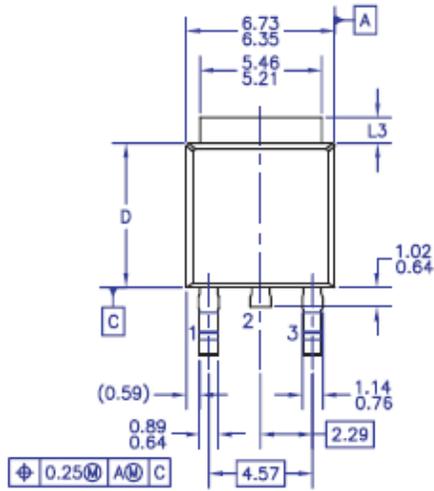
Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



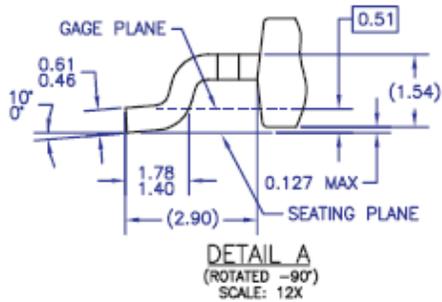
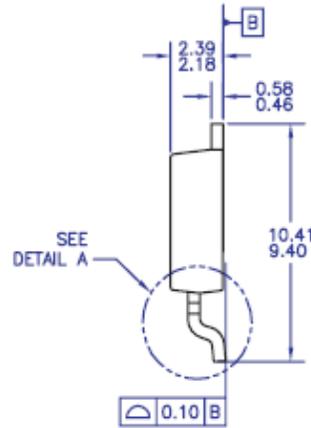
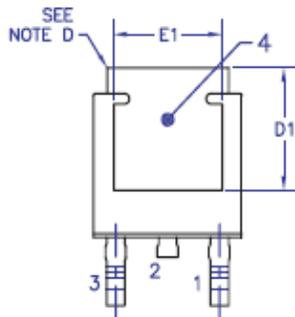
DPAK Package Dimensions



D - PAK



LAND PATTERN RECOMMENDATION



Dimensions in Millimeters

September 1999, Rev B

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