

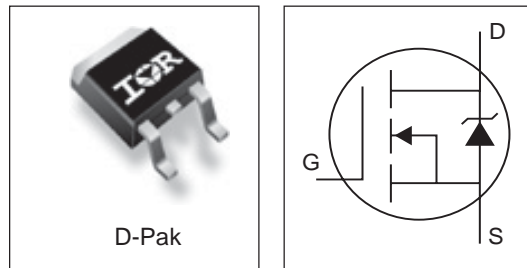
- N-Channel Application-Specific MOSFETs
- Ideal for CPU Core DC-DC Converters
- Low Conduction Losses
- Low Switching Losses
- Minimizes Parallel MOSFETs for high current applications
- 100% R_g Tested

Description

This new device employs advanced HEXFET Power MOSFET technology to achieve an unprecedented balance of on-resistance and gate charge. The reduced conduction and switching losses make it ideal for high efficiency DC-DC converters that power the latest generation of microprocessors.

The IRLR8103V has been optimized for all parameters that are critical in synchronous buck converters including R_{DS(on)}, gate charge and Cdv/dt-induced turn-on immunity. The IRLR8103V offers an extremely low combination of Q_{sw} & R_{DS(on)} for reduced losses in both control and synchronous FET applications.

The package is designed for vapor phase, infra-red, convection, or wave soldering techniques. Power dissipation of greater than 2W is possible in a typical PCB mount application.



DEVICE CHARACTERISTICS ⑤

	IRLR8103V
R _{DS(on)}	7.9 mΩ
Q _G	27 nC
Q _{SW}	12 nC
Q _{OSS}	29nC

Absolute Maximum Ratings

Parameter		Symbol	IRLR8103V	Units
Drain-Source Voltage		V _{DS}	30	V
Gate-Source Voltage		V _{GS}	±20	
Continuous Drain or Source Current (V _{GS} > 10V)	TC = 25°C	I _D	91	A
	TC = 90°C		63	
Pulsed Drain Current ①		I _{DM}	363	
Power Dissipation ③	TC = 25°C	P _D	115	W
	TC = 90°C		60	
Junction & Storage Temperature Range		T _J , T _{STG}	-55 to 150	°C
Continuous Source Current (Body Diode)		I _S	91	A
Pulsed Source Current ①		I _{SM}	363	

Thermal Resistance

Parameter	Symbol	Typ.	Max.	Units
Maximum Junction-to-Ambient ③⑥	R _{θJA}	—	50	°C/W
Maximum Junction-to-Case ⑥	R _{θJC}	—	1.09	

Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Drain-to-Source Breakdown Voltage	V_{DSS}	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
Static Drain-Source On-Resistance	$R_{DS(on)}$	—	6.9	9.0	m Ω	$V_{GS} = 10V, I_D = 15A$ ②
		—	7.9	10.5		$V_{GS} = 4.5V, I_D = 15A$ ②
Gate Threshold Voltage	$V_{GS(th)}$	1.0	—	3.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
Drain-to-Source Leakage Current	I_{DSS}	—	—	50	μA	$V_{DS} = 30V, V_{GS} = 0V$
		—	—	20	μA	$V_{DS} = 24V, V_{GS} = 0$
		—	—	100		$V_{DS} = 24V, V_{GS} = 0, T_J = 100^\circ C$
Gate-Source Leakage Current	I_{GSS}	—	—	± 100	nA	$V_{GS} = \pm 20V$
Total Gate Charge, Control FET	Q_G	—	27	—	nC	$V_{GS} = 5V, I_D = 15A, V_{DS} = 16V$
Total Gate Charge, Synch FET	Q_G	—	23	—		$V_{GS} = 5V, V_{DS} < 100mV$
Pre-Vth Gate-Source Charge	Q_{GS1}	—	4.7	—		$V_{DS} = 16V, I_D = 15A$
Post-Vth Gate-Source Charge	Q_{GS2}	—	2.0	—		
Gate to Drain Charge	Q_{GD}	—	9.7	—		
Switch Charge ($Q_{gs2} + Q_{gd}$)	Q_{SW}	—	12	—		
Output Charge	Q_{OSS}	—	29	—		
Gate Resistance	R_G	0.8	—	3.1		Ω
Turn-On Delay Time	$t_{d(on)}$	—	10	—	ns	$V_{DD} = 16V$
Rise Time	t_r	—	9	—		$I_D = 15A$
Turn-Off Delay Time	$t_{d(off)}$	—	24	—		$V_{GS} = 5.0V$
Fall Time	t_f	—	18	—		Clamped Inductive Load
Input Capacitance	C_{iss}	—	2672	—	pF	$V_{GS} = 16V, V_{GS} = 0$
Output Capacitance	C_{oss}	—	1064	—		
Reverse Transfer Capacitance	C_{rss}	—	109	—		

Source-Drain Rating & Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Diode Forward Voltage	V_{SD}	—	0.9	1.3	V	$I_S = 15A$ ②, $V_{GS} = 0V$
Reverse Recovery Charge ④	Q_{rr}	—	103	—	nC	$di/dt \sim 700A/\mu s$ $V_{DS} = 16V, V_{GS} = 0V, I_F = 15A$
Reverse Recovery Charge (with Parallel Schottky) ④	$Q_{rr(s)}$	—	96	—	nC	$di/dt = 700A/\mu s$, (with 10BQ040) $V_{DS} = 16V, V_{GS} = 0V, I_F = 15A$

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Pulse width $\leq 400 \mu s$; duty cycle $\leq 2\%$.
- ③ When mounted on 1 inch square copper board, $t < 10$ sec.
- ④ Typ = measured - Q_{oss}
- ⑤ Typical values of $R_{DS(on)}$ measured at $V_{GS} = 4.5V$, Q_G , Q_{SW} and Q_{OSS} measured at $V_{GS} = 5.0V$, $I_F = 15A$.
- ⑥ R_θ is measured at T_J approximately $90^\circ C$

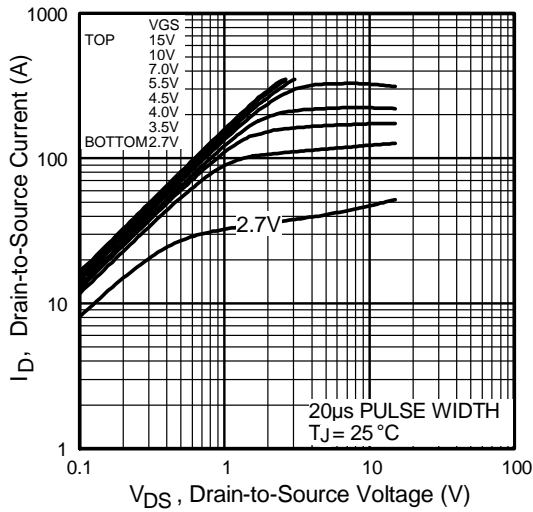


Fig 1. Typical Output Characteristics

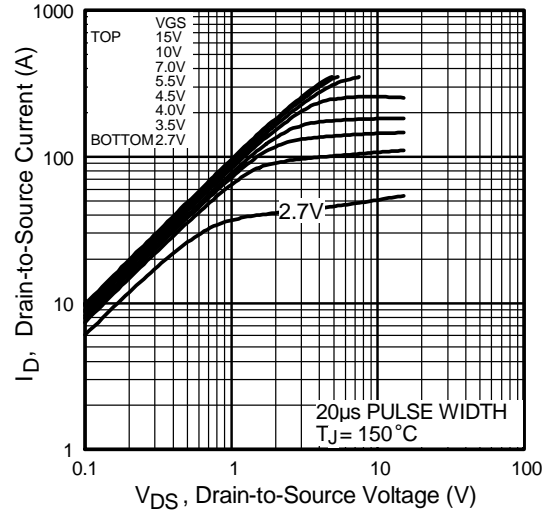


Fig 2. Typical Output Characteristics

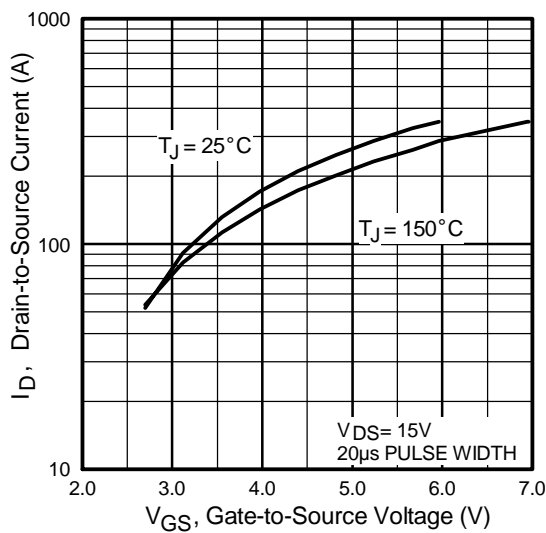


Fig 3. Typical Transfer Characteristics

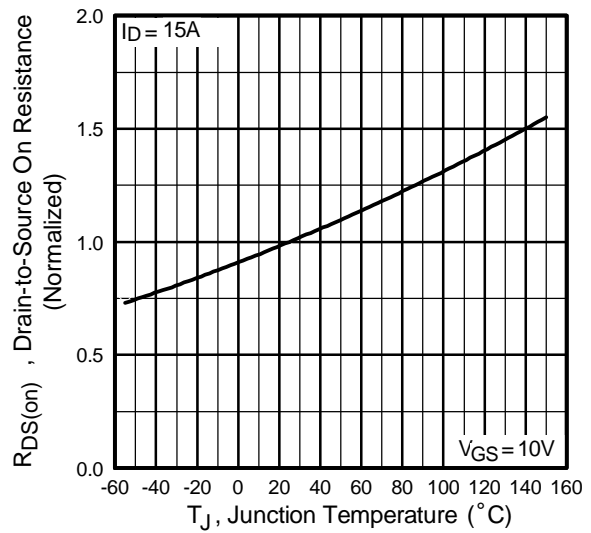


Fig 4. Normalized On-Resistance Vs. Temperature

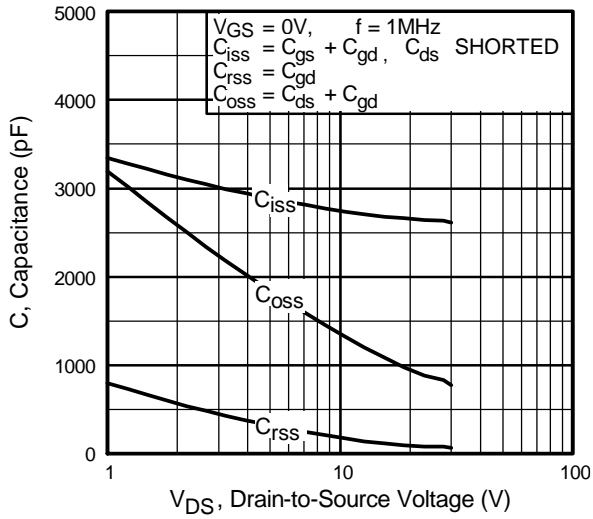


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

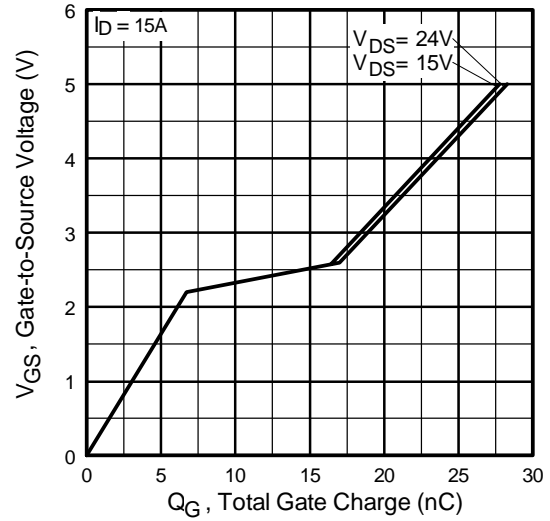


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

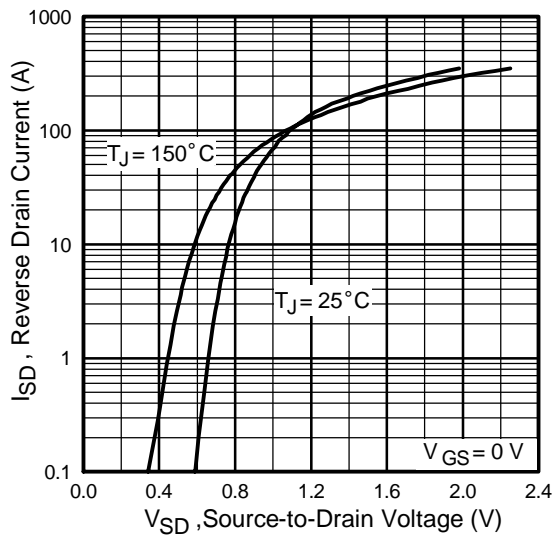


Fig 7. Typical Source-Drain Diode Forward Voltage

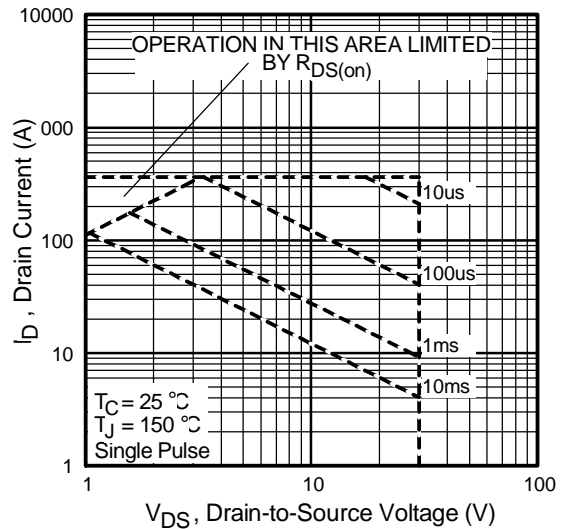


Fig 8. Maximum Safe Operating Area

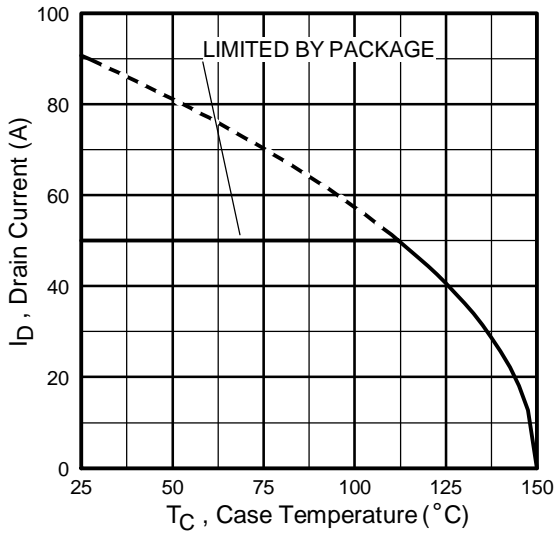


Fig 9. Maximum Drain Current Vs. Case Temperature

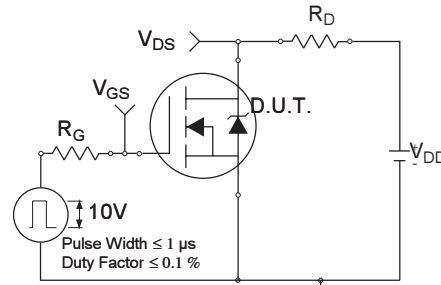


Fig 10a. Switching Time Test Circuit

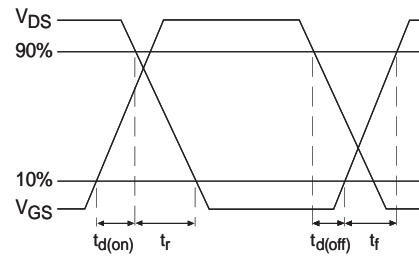


Fig 10b. Switching Time Waveforms

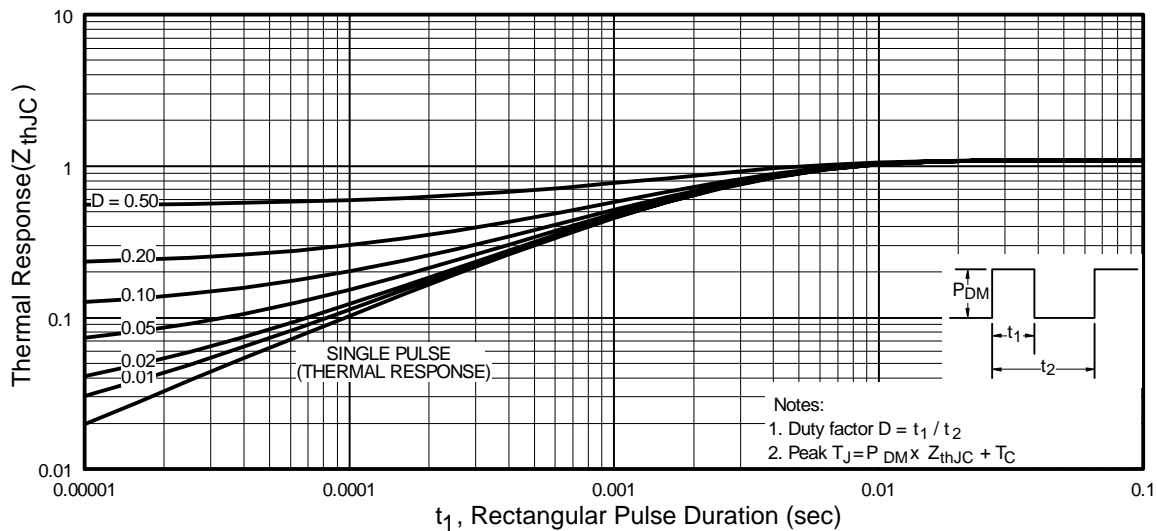


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

IRLR8103V

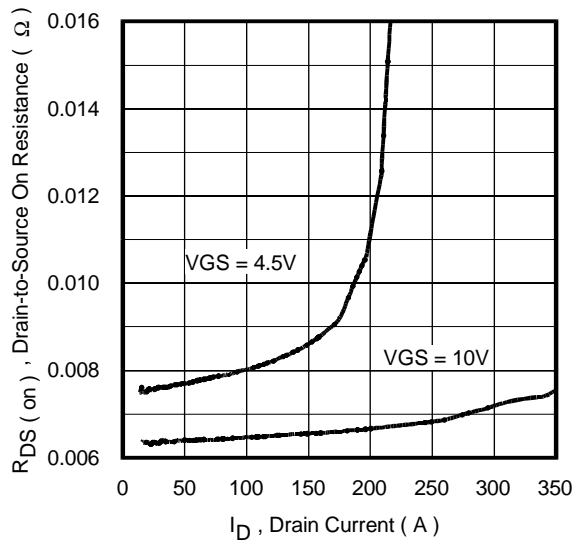


Fig 12. On-Resistance Vs. Drain Current

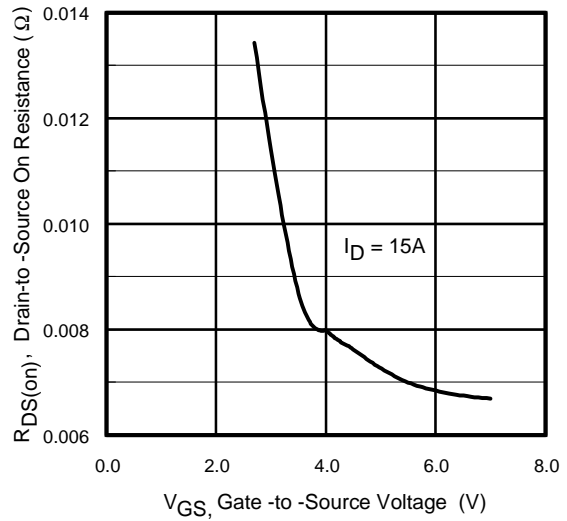


Fig 13. On-Resistance Vs. Gate Voltage

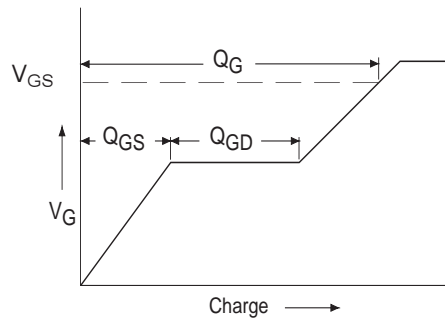
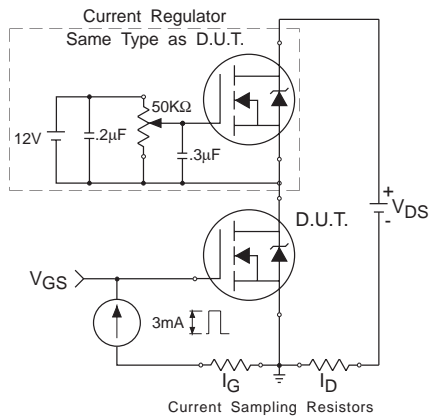
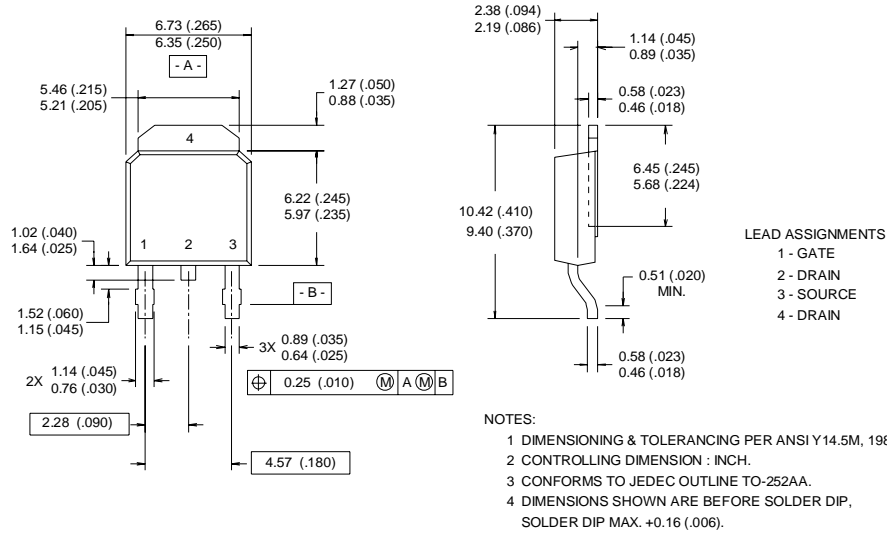


Fig 14a&b. Basic Gate Charge Test Circuit and Waveform

D-Pak (TO-252AA) Package Outline

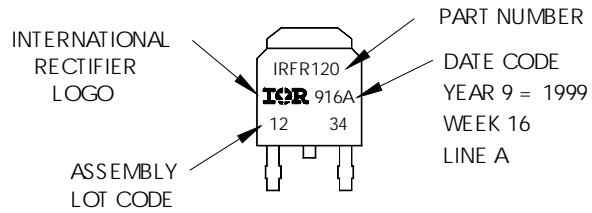
Dimensions are shown in millimeters (inches)



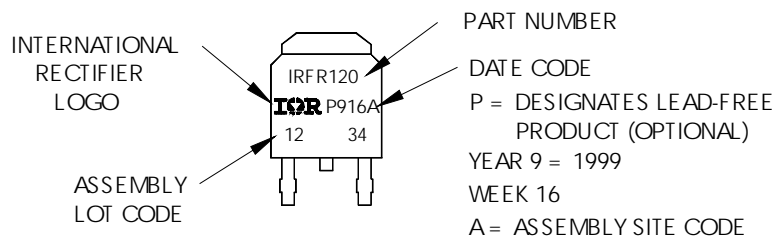
D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
 WITH ASSEMBLY
 LOT CODE 1234
 ASSEMBLED ON WW 16, 1999
 IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line
 position indicates "Lead-Free"



OR

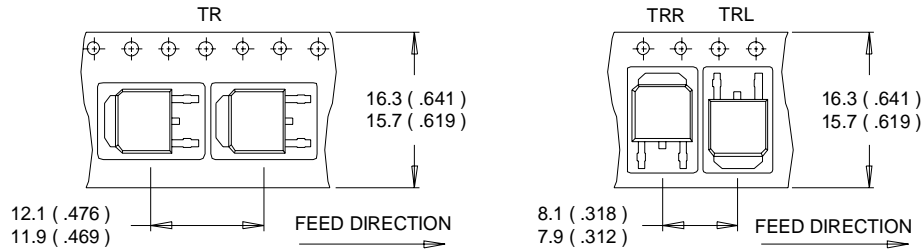


IRLR8103V

International
IR Rectifier

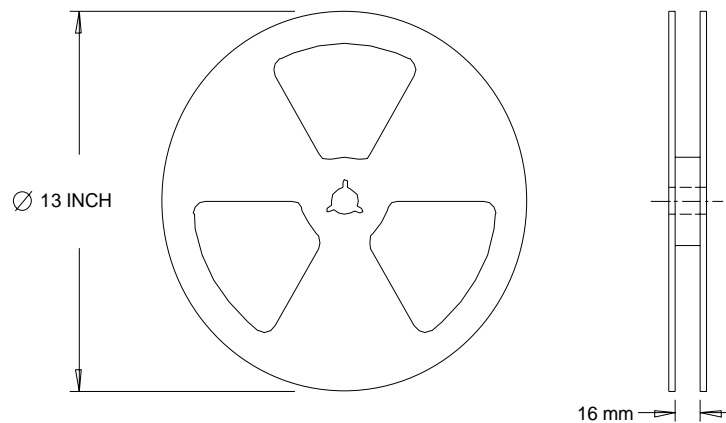
D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IR Rectifier

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Visit us at www.irf.com for sales contact information. 10/04

www.irf.com

Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>