International **IƆR** Rectifier

IRMCK311

Dual Channel Sensorless Motor Control IC for Appliances

Features

- **MCE^{TM} (Motion Control Engine) - Hardware based computation engine for high efficiency sinusoidal sensorless control of permanent magnet AC motor**
- **Integrated Power Factor Correction control**
- **Supports both interior and surface permanent magnet motors**
- **Built-in hardware peripheral for single shunt current feedback reconstruction**
- **No external current or voltage sensing operational amplifier required**
- **Dual channel three/two-phase Space Vector PWM**
- **Three-channel analog output (PWM)**
- **Embedded 8-bit high speed microcontroller (8051) for flexible I/O and man-machine control**
- **JTAG programming port for emulation/debugger**
- **Two serial communication interface (UART)**
- **I^{2}C/SPI serial interface**
- **Watchdog timer with independent analog clock**
- **Three general purpose timers/counters**
- **Two special timers: periodic timer, capture timer**
- **Internal 'One-Time Programmable' (OTP) memory and internal RAM for final production usage**
- **Pin compatible with IRMCF311 RAM version**
- **1.8V/3.3V CMOS**

Product Summary

Maximum crystal frequency	60 MHz
Maximum internal clock (SYSCLK) frequency	128 MHz
Maximum 8051 clock frequency	33 MHz
Sensorless control computation time	11 µsec typ
MCE^{TM} computation data range	16 bit signed
8051 OTP Program memory	56K bytes
MCE program and Data RAM	8K bytes
GateKill latency (digital filtered)	2 µsec
PWM carrier frequency counter	16 bits/ SYSCLK
A/D input channels	6
A/D converter resolution	12 bits
A/D converter conversion speed	2 µsec
8051 instruction execution speed	2 SYSCLK
Analog output (PWM) resolution	8 bits
UART baud rate (typ)	57.6K bps
Number of I/O (max)	14
Package (lead-free)	QFP64
Operating temperature	-40°C ~ 85°C

Description

IRMCK311 is a high performance OTP based motion control IC designed primarily for appliance applications. IRMCK311 is designed to achieve low cost and high performance control solutions for advanced inverterized appliance motor control. IRMCK311 contains two computation engines. One is Motion Control Engine (MCE^{TM}) for sensorless control of permanent magnet motors; the other is an 8-bit high-speed microcontroller (8051). Both computation engines are integrated into one monolithic chip. The MCE^{TM} contains a collection of control elements such as Proportional plus Integral, Vector rotator, Angle estimator, Multiply/Divide, Low loss SVPWM, Single Shunt IFB. The user can program a motion control algorithm by connecting these control elements using a graphic compiler. Key components of the sensorless control algorithms, such as the Angle Estimator, are provided as complete pre-defined control blocks implemented in hardware. A unique analog/digital circuit and algorithm to fully support single shunt current reconstruction is also provided. The 8051 microcontroller performs 2-cycle instruction execution (16MIPS at 33MHz). The MCE and 8051 microcontroller are connected via dual port RAM to process signal monitoring and command input. An advanced graphic compiler for the MCE^{TM} is seamlessly integrated into the MATLAB/Simulink environment, while third party JTAG based emulator tools are supported for 8051 developments. IRMCK311 comes with a small QFP64 pin lead-free package.

Rev 1.0

TABLE OF CONTENTS

TABLE OF FIGURES

TABLE OF TABLES

1 Overview

IRMCK311 is a new International Rectifier integrated circuit device primarily designed as a one-chip solution for complete inverter controlled appliance dual motor control applications. Unlike a traditional microcontroller or DSP, the IRMCK311 provides a built-in closed loop sensorless control algorithm using the unique Motion Control Engine (MCE^{TM}) for permanent magnet motors. The MCE^{TM} consists of a collection of control elements, motion peripherals, a dedicated motion control sequencer and dual port RAM to map internal signal nodes. IRMCK311 also employs a unique single shunt current reconstruction circuit to eliminate additional analog/digital circuitry and enables a direct shunt resistor interface to the IC. The sensorless control is the same for both motors with a single shunt current sensing capability. Motion control programming is achieved using a dedicated graphical compiler integrated into the MATLAB/Simulink^{TM} development environment. Sequencing, user interface, host communication, and upper layer control tasks can be implemented in the 8051 high-speed 8-bit microcontroller. The 8051 microcontroller is equipped with a JTAG port to facilitate emulation and debugging tools. Figure 1 shows a typical application schematic using IRMCK311.

IRMCK311 is intended for volume production purpose and contains 64K bytes of OTP (One Time Programming) ROM, which can be programmed through a JTAG port. For a development purpose use, IRMCF311 contains a 48k byte of RAM in place of program OTP to facilitate an application development work. Both IRMCF311 and IRMCK311 come in the same 64-pin QFP package with identical pin configuration to facilitate PC board layout and transition to mass production
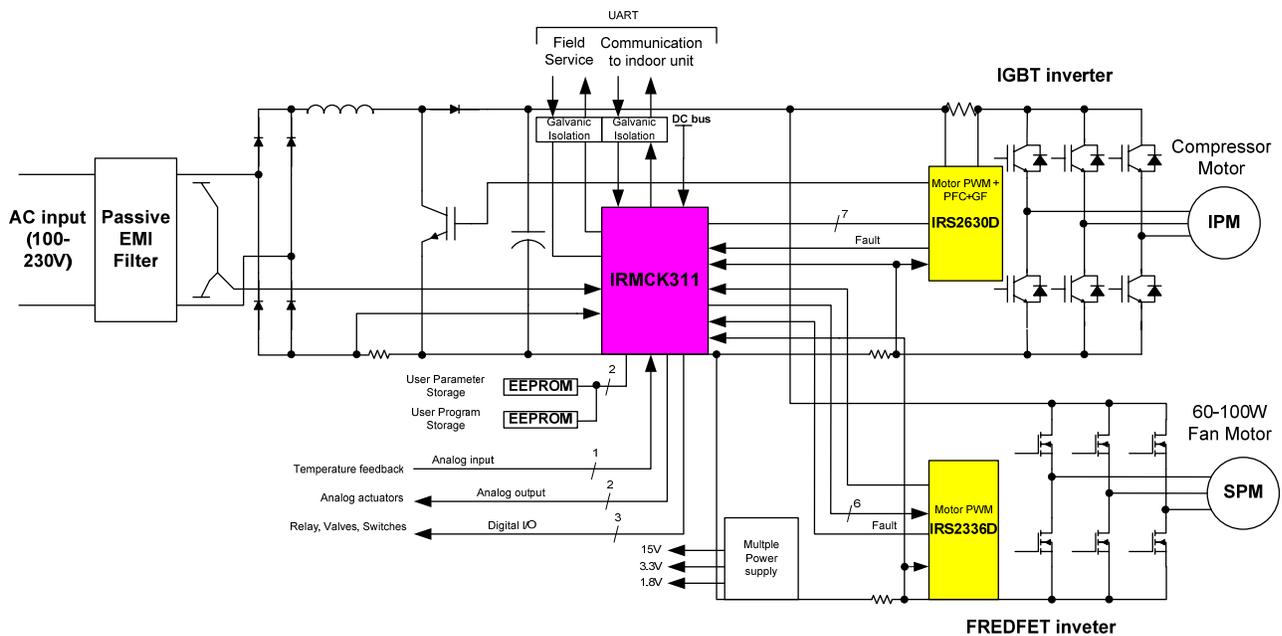
Figure 1.   Typical Application Block Diagram Using IRMCK311

2 IRMCK311 Block Diagram and Main Functions

IRMCK311 block diagram is shown in Figure 2.
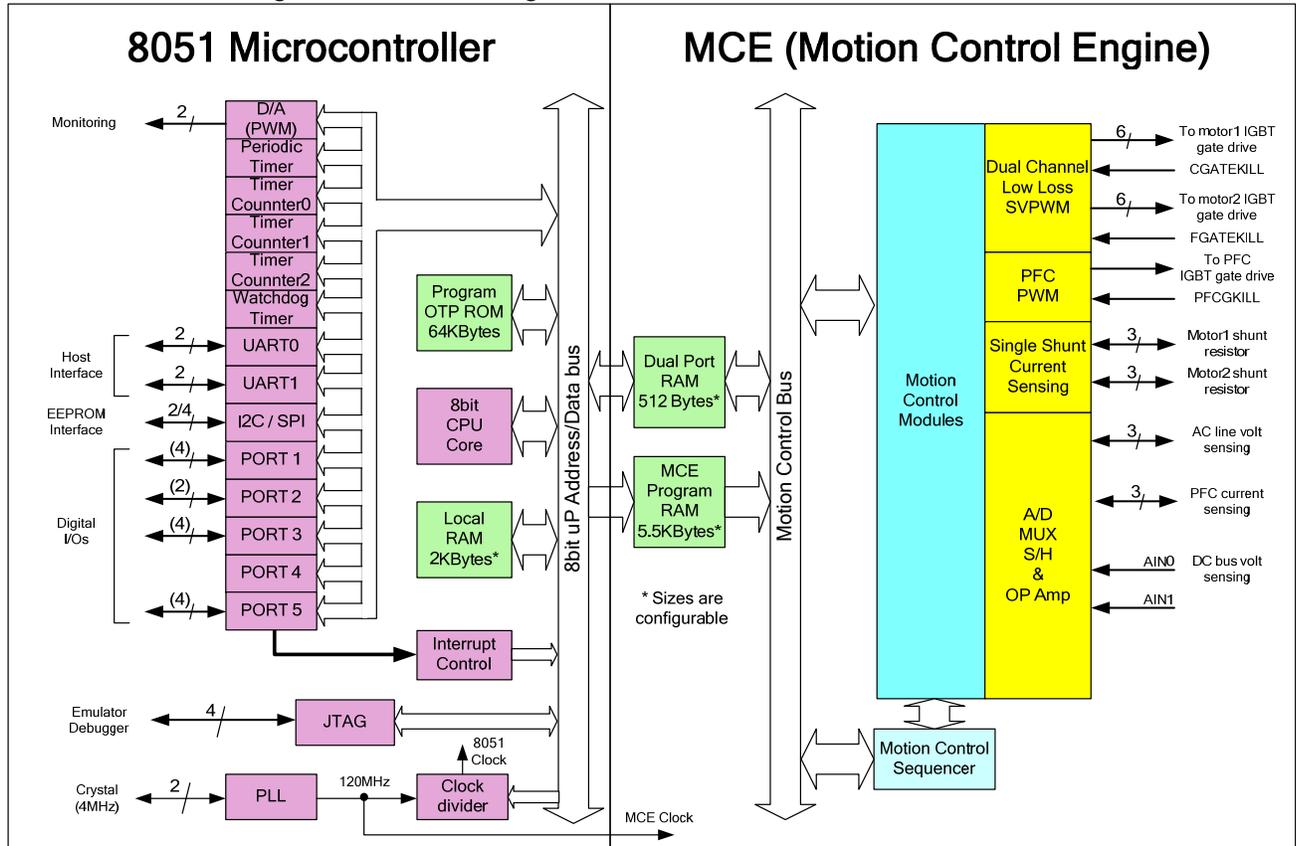
Figure 2.   IRMCK311 Internal Block Diagram

IRMCK311 contains the following functions for sensorless AC motor control applications:

- Motion Control Engine (MCE^{TM})
    - Proportional plus Integral block
    - Low pass filter
    - Differentiator and lag (high pass filter)
    - Ramp
    - Limit
    - Angle estimate (sensorless control)
    - Inverse Clark transformation
    - Vector rotator
    - Bit latch
    - Peak detect
    - Transition

- o Multiply-divide (signed and unsigned)
- o Divide (signed and unsigned)
- o Adder
- o Subtractor
- o Comparator
- o Counter
- o Accumulator
- o Switch
- o Shift
- o ATAN (arc tangent)
- o Function block (any curve fitting, nonlinear function)
- o 16-bit wide Logic operations (AND, OR, XOR, NOT, NEGATE)
- o MCE^{TM} program and data memory (6K byte). [Note 1]
- o MCE^{TM} control sequencer

- • 8051 microcontroller
  - o Three 16-bit timer/counters
  - o 16-bit periodic timer
  - o 16-bit analog watchdog timer
  - o 16-bit capture timer
  - o Up to 36 discrete I/Os
  - o Eleven-channel 12-bit A/D
    - ▪ Five buffered channels (0 – 1.2V input)
    - ▪ One unbuffered channel (0 – 1.2V input)
  - o JTAG port (4 pins)
  - o Up to three channels of analog output (8-bit PWM)
  - o Two UART
  - o I^{2}C/SPI port
  - o 64K byte [Note 1] program One-Time Programmable memory
  - o 2K byte data RAM. [Note 2]

    Note 1: Total size of OTP memory is 64K byte, however MCE program occupies maximum 8K byte which will be loaded into internal RAM at a powerup/boot process. Therefore only 56K byte OTP memory area is usable for 8051 microcontroller.
    Note 2: Total size of RAM is 8K byte including MCE program, MCE data, and 8051 data. Different sizes can be allocated depending on applications.

3 Pinout

Figure 3.   IRMCK311 Pin Configuration

4 Input/Output of IRMCK311

All I/O signals of IRMCK311 are shown in Figure 4. All I/O pins are 3.3V logic interface except A/D interface pins.

Figure 4.   Input/Output of IRMCK311

4.1 8051 Peripheral Interface Group

UART Interface

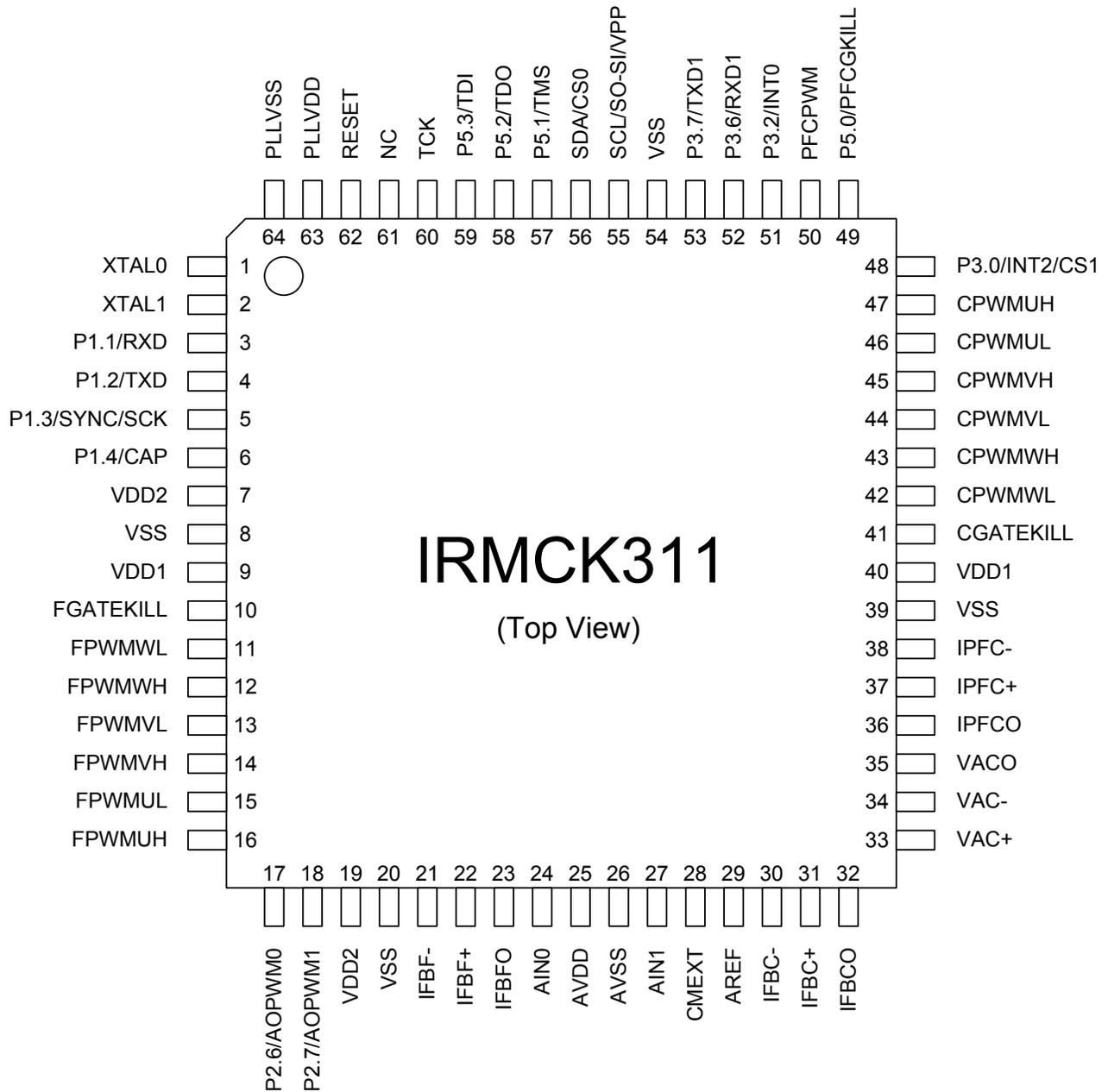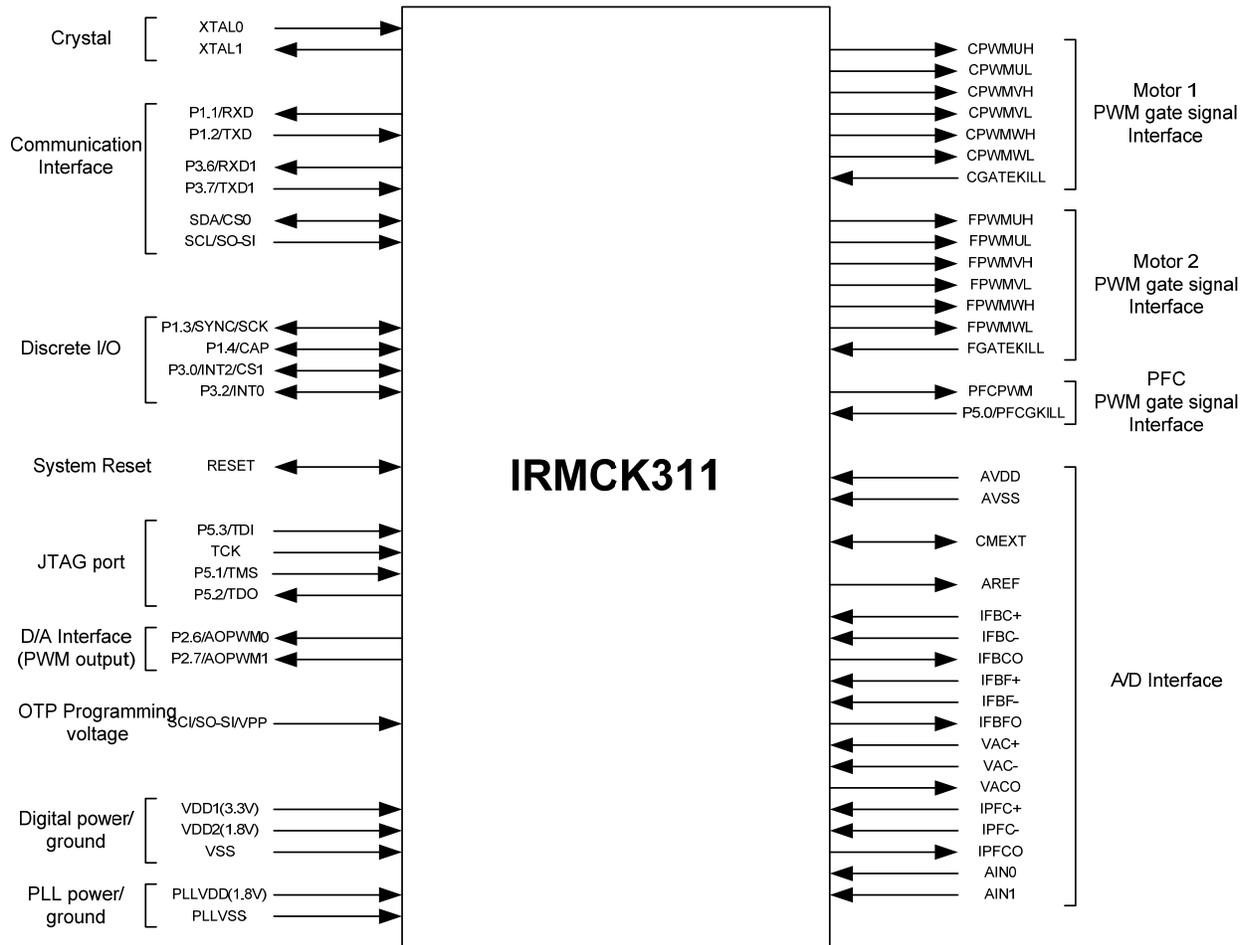|	
P1.1/RXD	Input, Receive data to IRMCK311, can be configured as P1.1
P1.2/TXD	Output, Transmit data from IRMCK311, can be configured as P1.2
P3.6/RXD1	Input, 2nd channel Receive data to IRMCK311, can be configured as P3.6
P3.7/TXD1	Output, 2nd channel Transmit data from IRMCK311, can be configured as P3.7

Discrete I/O Interface

P1.3/SYNC/SCK	Input/output port 1.3, can be configured as SYNC output or SPI clock
P1.4/CAP	Input/output port 1.4, can be configured as Capture Timer input
P3.0/INT2/CS1	Input/output port 3.0, can be configured as external interrupt 2 or SPI chip select 1
P3.2/INT0	Input/output port 3.2, can be configured as external interrupt 0

Analog Output Interface

P2.6/AOPWM0	Input/output, can be configured as 8-bit PWM output 0 with programmable carrier frequency
P2.7/AOPWM1	Input/output, can be configured as 8-bit PWM output 1 with programmable carrier frequency

Crystal Interface

XTAL0	Input, connected to crystal
XTAL1	Output, connected to crystal

Reset Interface

RESET	Inout, system reset, needs to be pulled up to VDD1 but doesn't require external RC time constant

I^{2}C/SPI Interface

SCL/SO-SI/VPP	Output, I^{2}C clock output, SPI SO-SI
SDA/CS0	Input/output, I^{2}C Data line, Chip Select 0 of SPI
P3.0/INT2/CS1	Input/output port 3.0, can be configured as external interrupt 2 or SPI chip select 1
P1.3/SYNC/SCK	Input/output port 1.3, can be configured as SYNC output or SPI clock

4.2 Motion Peripheral Interface Group

PWM

CPWMUH	Output, motor 1 PWM phase U high side gate signal
CPWMUL	Output, motor 1 PWM phase U low side gate signal
CPWMVH	Output, motor 1 PWM phase V high side gate signal
CPWMVL	Output, motor 1 PWM phase V low side gate signal
CPWMWH	Output, motor 1 PWM phase W high side gate signal
CPWMWL	Output, motor 1 PWM phase W low side gate signal
FPWMUH	Output, motor 2 PWM phase U high side gate signal
FPWMUL	Output, motor 2 PWM phase U low side gate signal

FPWMVH	Output, motor 2 PWM phase V high side gate signal
FPWMVL	Output, motor 2 PWM phase V low side gate signal
FPWMWH	Output, motor 2 PWM phase W high side gate signal
FPWMWL	Output, motor 2 PWM phase W low side gate signal
PFCPWM	Output, PFC PWM

Fault

CGATEKILL	Input, upon assertion, this negates all six PWM signals for motor 1, programmable logic sense
P5.0/PFCGKILL	Input, upon assertion, this negates PFCPWM signal, programmable logic sense, can be configured as discrete I/O in which case CGATEKILL negates PFCPWM
FGATEKILL	Input, upon assertion, this negates all six PWM signals for motor 2, programmable logic sense

4.3 Analog Interface Group

AVDD	Analog power (1.8V)
AVSS	Analog power return
AREF	Buffered 0.6V output
CMEXT	Unbuffered 0.6V, input to the AREF buffer, capacitor needs to be connected.
IFBC+	Input, Operational amplifier positive input for shunt resistor current sensing of motor 1
IFBC-	Input, Operational amplifier negative input for shunt resistor current sensing of motor 1
IFBCO	Output, Operational amplifier output for shunt resistor current sensing of motor 1
IFBF+	Input, Operational amplifier positive input for shunt resistor current sensing of motor 2
IFBF-	Input, Operational amplifier negative input for shunt resistor current sensing of motor 2
IFBFO	Output, Operational amplifier output for shunt resistor current sensing of motor 2
IPFC+	Input, Operational amplifier positive input for PFC current sensing
IPFC-	Input, Operational amplifier negative input for PFC current sensing
IPFO	Output, Operational amplifier output for PFC current sensing
VAC+	Input, Operational amplifier positive input for PFC AC voltage sensing
VAC-	Input, Operational amplifier negative input for PFC AC voltage sensing
VACO	Output, Operational amplifier output for PFC AC voltage sensing
VDC+	Input, Operational amplifier positive input for DC bus voltage sensing
VDC-	Input, Operational amplifier negative input for DC bus voltage sensing
AIN0/VDCO	Input/Output, Analog input channel 0 or Operational amplifier output for DC bus voltage sensing
AIN1	Input, Analog input channel 1 (0-1.2V), needs to be pulled down to AVSS if unused

4.4 Power Interface Group

| VDD1 | Digital power for I/O (3.3V) |
| VDD2 | Digital power for core logic (1.8V) |

VSS   Digital common
PLLVDD   PLL power (1.8V)
PLLVSS   PLL ground return
SCL/SO-SI/VPP   OTP programming supply. Can be left open in OTP read mode (normal)

4.5   Test Interface

P5.3/TDI   Input, JTAG test data input
P5.1/TMS   Input, JTAG test mode select
TCK   Input, JTAG test clock
P5.2/TDO   Output, JTAG test data output

5 Application Connections

Typical application connection is shown in Figure 5. All components necessary to implement a complete sensorless drive control algorithm are shown connected to IRMCK311.
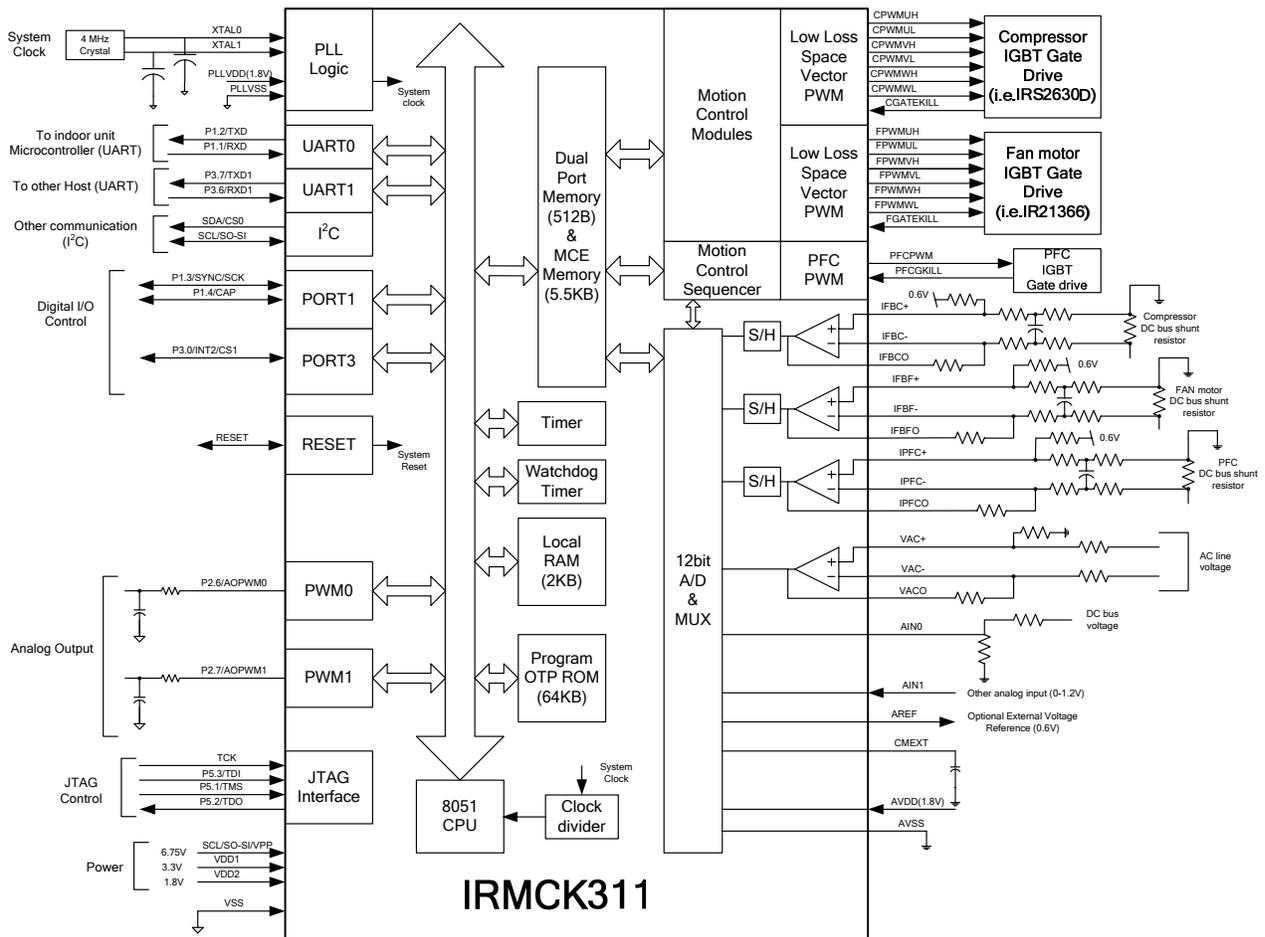

Figure 5.   Application Connection of IRMCK311

International **I2R** Rectifier

6 DC Characteristics

6.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Condition
V_{DD1}	Supply Voltage	-0.3 V	-	3.6 V	Respect to VSS
V_{DD2}	Supply Voltage	-0.3 V	-	1.98 V	Respect to VSS
V_{PP}	OTP Programming Voltage	-0.3V	-	7.0V	Respect to VSS
V_{IA}	Analog Input Voltage	-0.3 V	-	1.98 V	Respect to AVSS
V_{ID}	Digital Input Voltage	-0.3 V	-	3.65 V	Respect to VSS
T_A	Ambient Temperature	-40 °C	-	85 °C	
T_S	Storage Temperature	-65 °C	-	150 °C	

Table 1.   Absolute Maximum Ratings

Caution: Stresses beyond those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and function of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

6.2 System Clock Frequency and Power Consumption

Symbol	Parameter	Min	Typ	Max	Unit
SYSCLK	System Clock	32	-	128	**MHz**
8051CLK	8051 Clock	-	-	32	**MHz**

Table 2.   System Clock Frequency
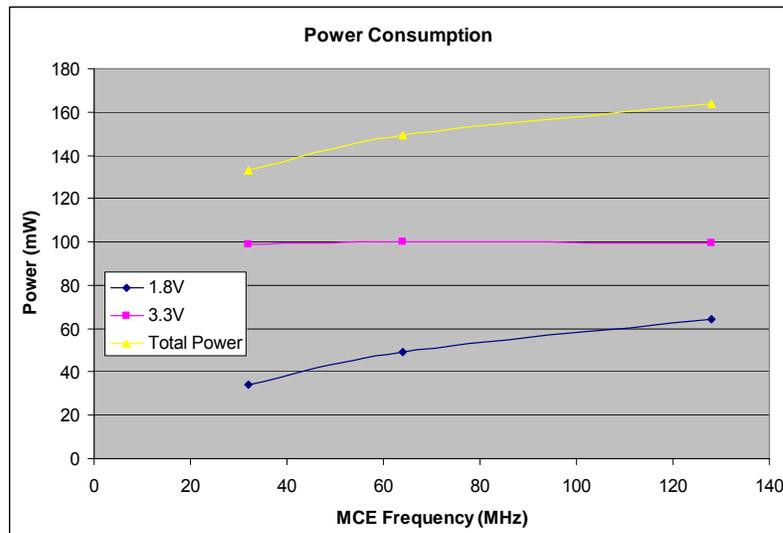
Figure 6.   Clock Frequency vs. Power Consumption

6.3 Digital I/O DC Characteristics

Symbol	Parameter	Min	Typ	Max	Condition
V_{DD1}	Supply Voltage	3.0 V	3.3 V	3.6 V	Recommended
V_{DD2}	Supply Voltage	1.62 V	1.8 V	1.98 V	Recommended
V_{PP}	OTP Programming voltage	6.50V	6.75V	7.0V	Recommended
V_{IL}	Input Low Voltage	-0.3 V	-	0.8 V	Recommended
V_{IH}	Input High Voltage	2.0 V		3.6 V	Recommended
C_{IN}	Input capacitance	-	3.6 pF	-	(1)
I_L	Input leakage current		±10 nA	±1 µA	V_O = 3.3 V or 0 V
I_{OL1}[2]	Low level output current	8.9 mA	13.2 mA	15.2 mA	V_{OL} = 0.4 V (1)
I_{OH1}[2]	High level output current	12.4 mA	24.8 mA	38 mA	V_{OH} = 2.4 V (1)
I_{OL2}[3]	Low level output current	17.9 mA	26.3 mA	33.4 mA	V_{OL} = 0.4 V (1)
I_{OH2}[3]	High level output current	24.6 mA	49.5 mA	81 mA	V_{OH} = 2.4 V (1)

Table 3. Digital I/O DC Characteristics

Note:
  (1) Data guaranteed by design.
  (2) Applied to SCL/SO-SI, SDA/CS0 pins.
  (3) Applied to P1.1/RXD, P1.2/TXD, P1.3/SYNC/SCK, P1.4/CAP, P2.6/AOPWM0, P2.7/AOPWM1, P3.0/INT2/CS1, P3.2/INT0, P3.6/RXD1, P3.7/TXD1, P5.0/PFCGKILL, P5.1/TMS, P5.2/TDO, P5.3/TDI, CGATEKILL, FGATEKILL, CPWMUL, CPWMUH, CPWMVL, CPWMVH, CPWMWL, CPWMWH, FPWMUL, FPWMUH, FPWMVL, FPWMVH, FPWMWL, FPWMWH, and PFCPWM pins.

6.4 PLL and Oscillator DC Characteristics

Symbol	Parameter	Min	Typ	Max	Condition
V_{PLLVDD}	Supply Voltage	1.62 V	1.8 V	1.92 V	Recommended
$V_{IL\ OSC}$	Oscillator Input Low Voltage	V_{PLLVSS}	-	0.2* V_{PLLVDD}	V_{PLLVDD} = 1.8 V (1)
$V_{IH\ OSC}$	Oscillator Input High Voltage	0.8* V_{PLLVDD}		V_{PLLVDD}	V_{PLLVDD} = 1.8 V (1)

Table 4. PLL DC Characteristics

Note:
  (1) Data guaranteed by design.

6.5 Analog I/O DC Characteristics

- OP amps for current sensing (IFBC+, IFBC-, IFBCO, IFBF+, IFBF-, IFBFO, IPFC+, IPFC-, IPFCO)

C_{AREF} = 1nF, C_{MEXT}= 100nF. Unless specified, Ta = 25°C.

Symbol	Parameter	Min	Typ	Max	Condition
V_{AVDD}	Supply Voltage	1.71 V	1.8 V	1.89 V	Recommended
V_{OFFSET}	Input Offset Voltage	-	-	26 mV	V_{AVDD} = 1.8 V
V_I	Input Voltage Range	0 V		1.2 V	Recommended
V_{OUTSW}	OP amp output operating range	50 mV [1]	-	1.2 V	V_{AVDD} = 1.8 V
C_{IN}	Input capacitance	-	3.6 pF	-	[1]
R_{FDBK}	OP amp feedback resistor	5 kΩ	-	20 kΩ	Requested between op amp output and negative input
OP_{GAINCL}	Operating Close loop Gain	80 db	-	-	[1]
CMRR	Common Mode Rejection Ratio	-	80 db	-	[1]
I_{SRC}	Op amp output source current	-	1 mA	-	V_{OUT} = 0.6 V [1]
I_{SNK}	Op amp output sink current	-	100 µA	-	V_{OUT} = 0.6 V [1]

Table 5. Analog I/O DC Characteristics

Note: (1) Data guaranteed by design.

6.6 Under Voltage Lockout DC Characteristics

- Based on AVDD (1.8V)

Unless specified, Ta = 25°C.

Symbol	Parameter	Min	Typ	Max	Condition
UV_{CC+}	UVcc positive going Threshold[1]	1.53 V	1.66 V	1.71 V	V_{DD1} = 3.3 V
UV_{CC-}	UVcc negative going Threshold	1.52 V	1.62 V	1.71 V	V_{DD1} = 3.3 V
$UV_{CC}H$	UVcc Hysteresys	-	40 mV	-	

Table 6.   UVcc DC Characteristics

Note:
   1) Data guaranteed by design.

6.7 AREF Characteristics

C_{AREF} = 1nF, C_{MEXT}= 100nF. Unless specified, Ta = 25°C.

Symbol	Parameter	Min	Typ	Max	Condition
V_{AREF}	AREF Output Voltage	495 mV	600 mV	700 mV	V_{AVDD} = 1.8 V
ΔV_o	Load regulation (V_{DC}-0.6)	-	1 mV	-	[1]
PSRR	Power Supply Rejection Ratio	-	75 db	-	[1]

Table 7.   AREF DC Characteristics

Note:
   (1) Data guaranteed by design.

Rev 1.0

7 AC Characteristics

7.1   PLL AC Characteristics

Symbol	Parameter	Min	Typ	Max	Condition
F_{CLKIN}	Crystal input frequency	3.2 MHz	4 MHz	60 MHz	(1) (see figure below)
F_{PLL}	Internal clock frequency	32 MHz	50 MHz	128 MHz	(1)
F_{LWPW}	Sleep mode output frequency	$F_{CLKIN} \div 256$	-	-	(1)
J_S	Short time jitter	-	200 psec	-	(1)
D	Duty cycle	-	50 %	-	(1)
T_{LOCK}	PLL lock time	-	-	500 µsec	(1)

Table 8.   PLL AC Characteristics

Note:
   (1) Data guaranteed by design.

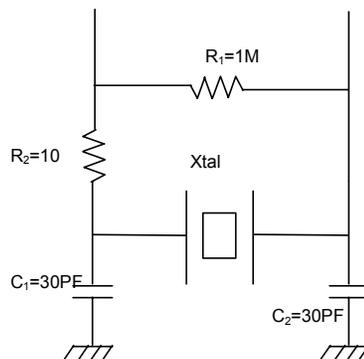**Figure 7   Crystal oscillator circuit**

7.2 Analog to Digital Converter AC Characteristics

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Condition
T_{CONV}	Conversion time	-	-	2.05 μsec	[1]
T_{HOLD}	Sample/Hold maximum hold time	-	-	10 μsec	Voltage droop ≤ 15 LSB (see figure below)

Table 9.   A/D Converter AC Characteristics

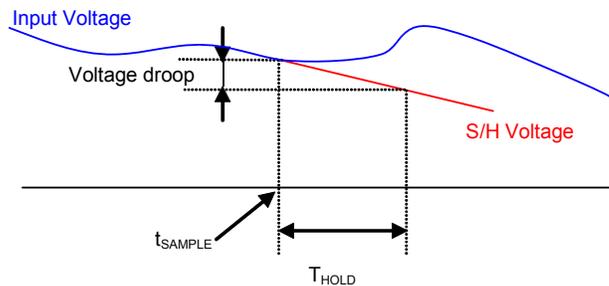Note:
(1) Data guaranteed by design.

Figure 8   Voltage droop of sample and hold

7.3 Op Amp AC Characteristics
- OP amps for current sensing (IFBC+, IFBC-, IFBCO, IFBF+, IFBF-, IFBFO, IPFC+, IPFC-, IPFCO)

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Condition
OP_{SR}	OP amp slew rate	-	10 V/μsec	-	V_{AVDD} = 1.8 V, CL = 33 pF [1]
OP_{IMP}	OP input impedance	-	10^8 Ω	-	[1]
T_{SET}	Settling time	-	400 ns	-	V_{AVDD} = 1.8 V, CL = 33 pF [1]

Table 10.   Current Sensing OP Amp AC Characteristics

Note:
(1) Data guaranteed by design.
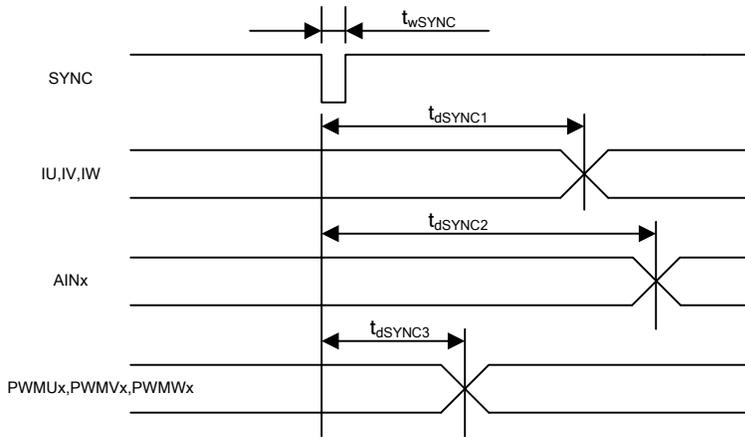
7.4   SYNC to SVPWM and A/D Conversion AC Timing

Figure 9   SYNC to SVPWM and A/D conversion AC Timing

Unless specified, Ta = 25°C.

Symbol	Parameter	Min	Typ	Max	Unit
t_{wSYNC}	SYNC pulse width	-	32	-	SYSCLK
t_{dSYNC1}	SYNC to current feedback conversion time	-	-	100	SYSCLK
t_{dSYNC2}	SYNC to AIN0-6 analog input conversion time	-	-	200	SYSCLK (1)
t_{dSYNC3}	SYNC to PWM output delay time	-	-	2	SYSCLK

Table 11.   SYNC AC Characteristics

Note:
    (1) AIN1 through AIN6 channels are converted once every 6 SYNC events
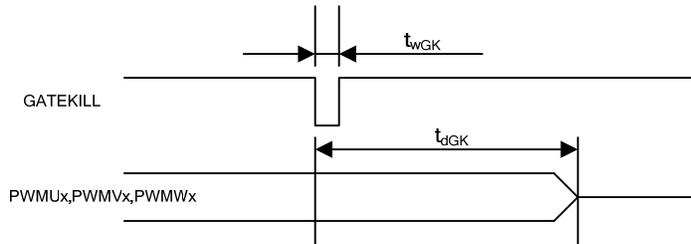
7.5   GATEKILL to SVPWM AC Timing

Figure 10 GATEKILL to SVPWM AC Timing

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
t_{wGK}	GATEKILL pulse width	32	-	-	SYSCLK
t_{dGK}	GATEKILL to PWM output delay	-	-	100	SYSCLK

Table 12.   GATEKILL to SVPWM AC Timing

7.6   Interrupt AC Timing
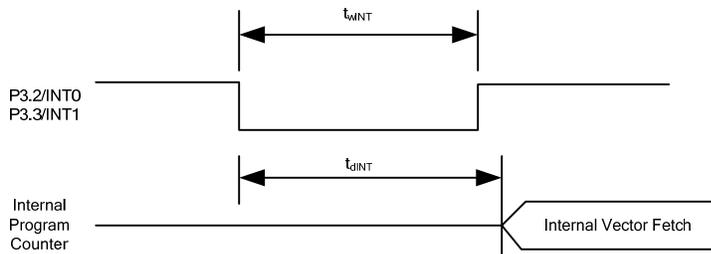
Figure 11   Interrupt AC Timing

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
t_{wINT}	INT0, INT1 Interrupt Assertion Time	4	-	-	SYSCLK
t_{dINT}	INT0, INT1 latency	-	-	4	SYSCLK

Table 13.   Interrupt AC Timing

7.7 I^{2}C AC Timing
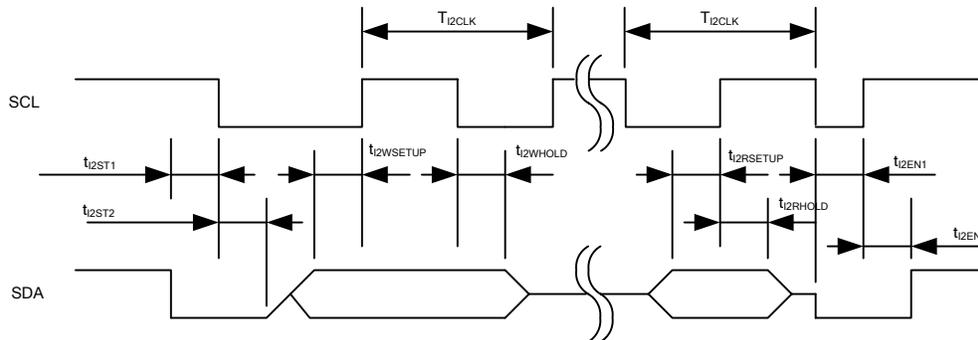
Figure 12   I^{2}C AC Timing

Unless specified, Ta = 25°C.

Symbol	Parameter	Min	Typ	Max	Unit
T$_{I2CLK}$	I^{2}C clock period	10	-	8192	SYSCLK
t$_{I2ST1}$	I^{2}C SDA start time	0.25	-	-	T$_{I2CLK}$
t$_{I2ST2}$	I^{2}C SCL start time	0.25	-	-	T$_{I2CLK}$
t$_{I2WSETUP}$	I^{2}C write setup time	0.25	-	-	T$_{I2CLK}$
t$_{I2WHOLD}$	I^{2}C write hold time	0.25	-	-	T$_{I2CLK}$
t$_{I2RSETUP}$	I^{2}C read setup time	I^{2}C filter time[1]	-	-	SYSCLK
t$_{I2RHOLD}$	I^{2}C read hold time	1	-	-	SYSCLK

Table 14.   I^{2}C AC Timing

Note:
  (1) I^{2}C read setup time is determined by the programmable filter time applied to I^{2}C communication.
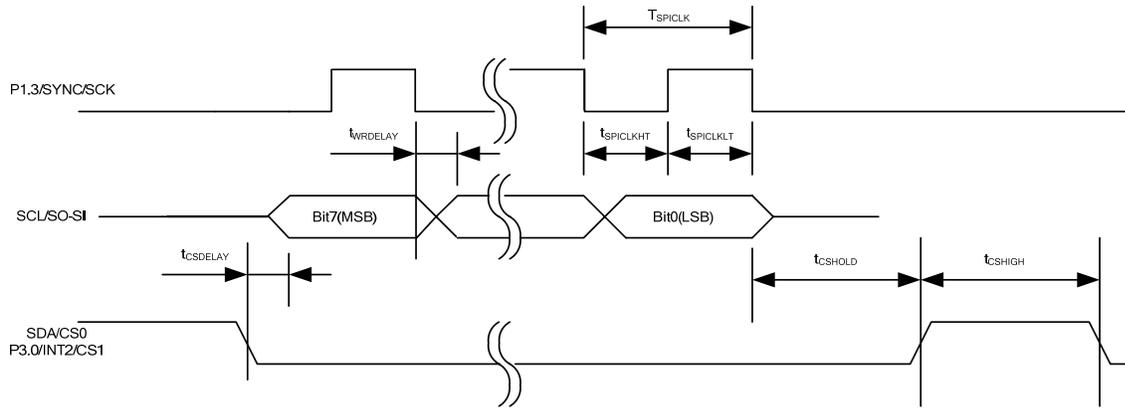
7.8 SPI AC Timing

7.8.1 SPI Write AC timing

Figure 13   SPI AC Timing

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
T_{SPICLK}	SPI clock period	4	-	-	SYSCLK
$t_{SPICLKHT}$	SPI clock high time	-	1/2	-	T_{SPICLK}
$t_{SPICLKLT}$	SPI clock low time	-	1/2	-	T_{SPICLK}
$t_{CSDELAY}$	CS to data delay time	-	-	10	nsec
$t_{WRDELAY}$	CLK falling edge to data delay time	-	-	10	nsec
t_{CSHIGH}	CS high time between two consecutive byte transfer	1	-	-	T_{SPICLK}
t_{CSHOLD}	CS hold time	-	1	-	T_{SPICLK}

Table 15.   SPI Write AC Timing

7.8.2 SPI Read AC Timing
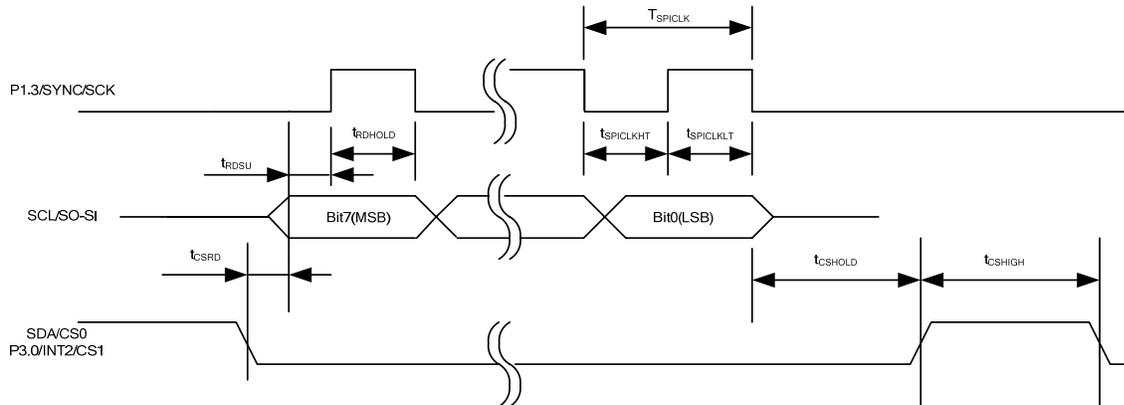
Figure 14   SPI Read AC Timing

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
T_{SPICLK}	SPI clock period	4	-	-	SYSCLK
$t_{SPICLKHT}$	SPI clock high time	-	1/2	-	T_{SPICLK}
$t_{SPICLKLT}$	SPI clock low time	-	1/2	-	T_{SPICLK}
t_{CSRD}	CS to data delay time	-	-	10	nsec
t_{RDSU}	SPI read data setup time	10	-	-	nsec
t_{RDHOLD}	SPI read data hold time	10	-	-	nsec
t_{CSHIGH}	CS high time between two consecutive byte transfer	1	-	-	T_{SPICLK}
t_{CSHOLD}	CS hold time	-	1	-	T_{SPICLK}

Table 16.   SPI Read AC Timing

7.9 UART AC Timing
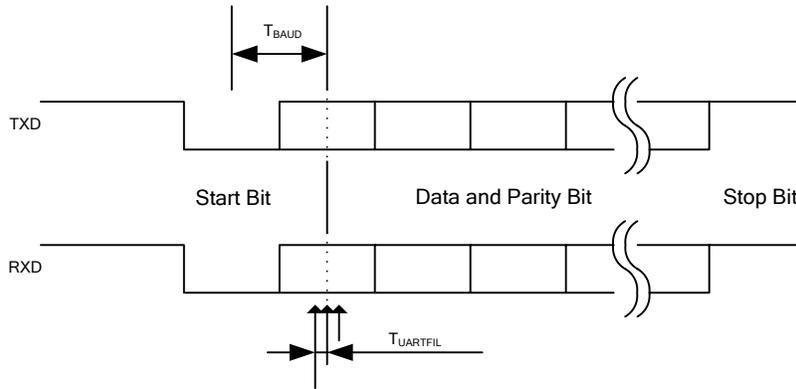
Figure 15   UART AC Timing

Unless specified, Ta = 25°C.

Symbol	Parameter	Min	Typ	Max	Unit
T_{BAUD}	Baud Rate Period	-	57600	-	bit/sec
$T_{UARTFIL}$	UART sampling filter period [1]	-	1/16	-	T_{BAUD}

Table 17.   UART AC Timing

Note:
(1) Each bit including start and stop bit is sampled three times at center of a bit at an interval of 1/16 T_{BAUD}. If three sampled values do not agree, then UART noise error is generated.
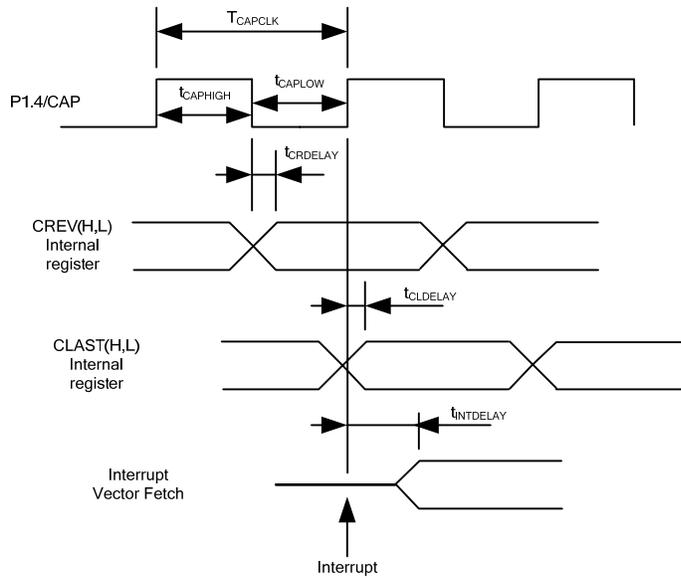
7.10 CAPTURE Input AC Timing

Figure 16   CAPTURE Input AC Timing

Unless specified, Ta = 25°C.

Symbol	Parameter	Min	Typ	Max	Unit
T_{CAPCLK}	CAPTURE input period	8	-	-	SYSCLK
$t_{CAPHIGH}$	CAPTURE input high time	4	-	-	SYSCLK
t_{CAPLOW}	CAPTURE input low time	4	-	-	SYSCLK
$t_{CRDELAY}$	CAPTURE falling edge to capture register latch time	-	-	4	SYSCLK
$t_{CLDELAY}$	CAPTURE rising edge to capture register latch time	-	-	4	SYSCLK
$t_{INTDELAY}$	CAPTURE input interrupt latency time	-	-	4	SYSCLK

Table 18.   CAPTURE AC Timing

7.11 JTAG AC Timing
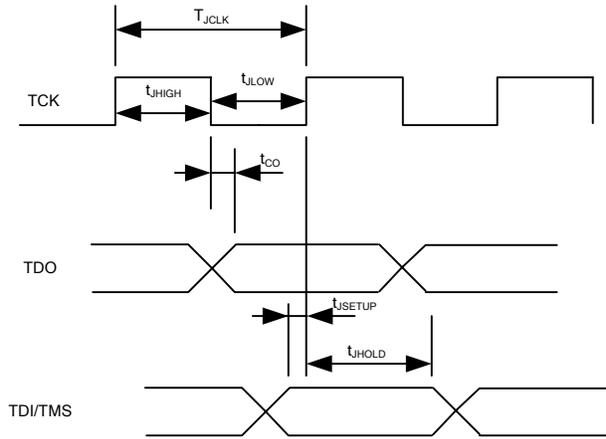
Figure 17   JTAG AC Timing

Unless specified, Ta = 25˚C.

Symbol	Parameter	Min	Typ	Max	Unit
T_{JCLK}	TCK Period	-	-	50	MHz
t_{JHIGH}	TCK High Period	10	-	-	nsec
t_{JLOW}	TCK Low Period	10	-	-	nsec
t_{CO}	TCK to TDO propagation delay time	0	-	5	nsec
t_{JSETUP}	TDI/TMS setup time	4	-	-	nsec
t_{JHOLD}	TDI/TMS hold time	0	-	-	nsec

Table 19.   JTAG AC Timing

7.12 OTP Programming Timing
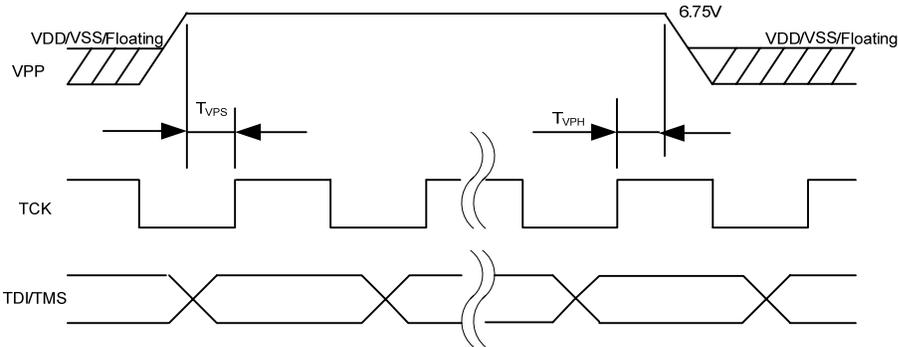
Figure 18   OTP Programming Timing

Unless specified, Ta = 25°C.

Symbol	Parameter	Min	Typ	Max	Unit
T_{VPS}	VPP Setup Time	10	-	-	nsec
T_{VPH}	VPP Hold Time	15	-	-	nsec

Table 20.   OTP Programming Timing

8 I/O Structure

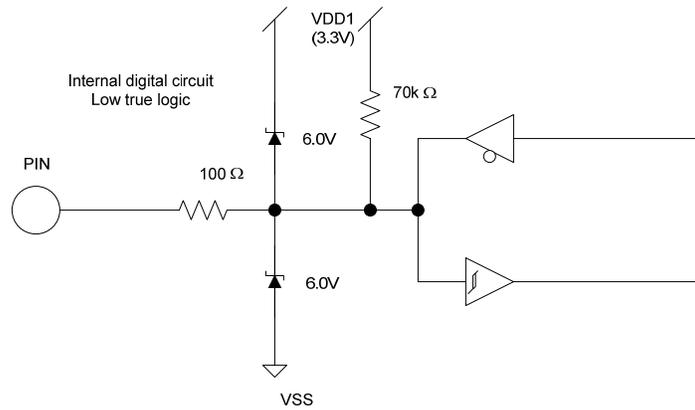The following figure shows the motor PWM and digital I/O structure except the motor PWM output

Figure 19 All digital I/O except motor PWM output
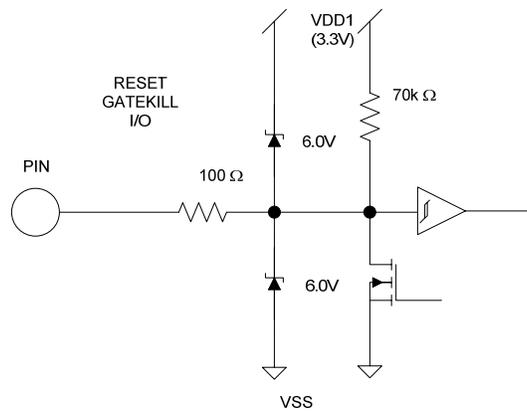
The following figure shows RESET and GATEKILL I/O structure.

Figure 20 RESET, GATEKILL I/O

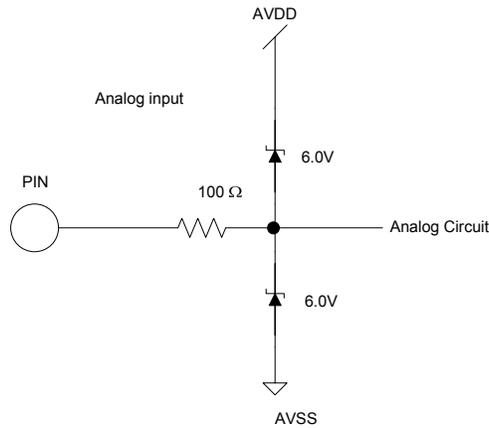The following figure shows the analog input structure.

Figure 21 Analog input

The following figure shows all analog operational amplifier output pins and AREF pin I/O structure.
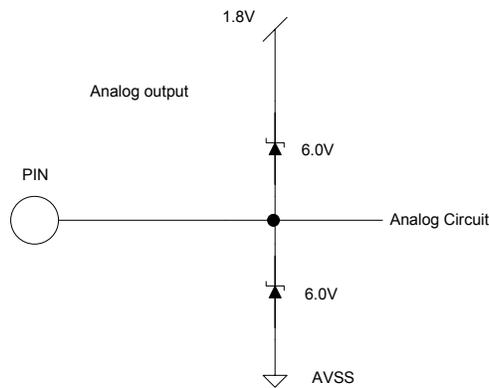

Figure 22   Analog operational amplifier output and AREF I/O structure
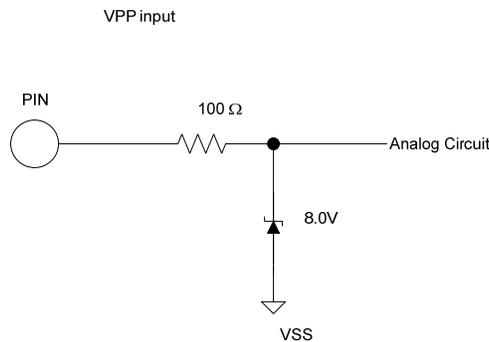
The following figure shows the VPP pin I/O structure

VPP input

Figure 23 VPP programming pin I/O structure

The following figure shows the VSS, AVSS and PLLVSS pin structure
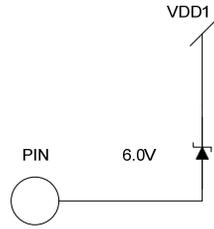
VDD1

PIN   6.0V

Figure 24 VSS, AVSS and PLLVSS pin structure

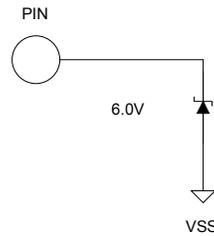The following figure shows the VDD1, VDD2, AVDD and PLLVDD pin structure

PIN

6.0V

VSS

Figure 25 VDD1, VDD2, AVDD and PLLVDD pin structure

The following figure shows the XTAL0 and XTAL1 pins structure

VDD1

6.0V

PIN

6.0V

VSS

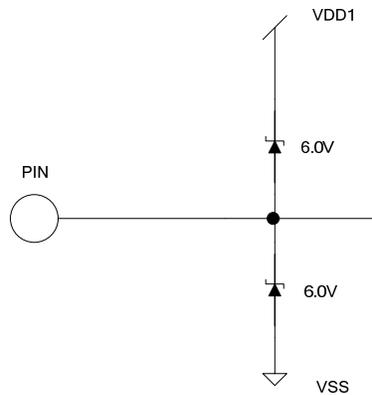**Figure 26   XTAL0/XTAL1 pins structure**

International IQR Rectifier

9 Pin List

Pin Number	Pin Name	Internal IC Pull-up /Pull-down	Pin Type	Description
1	XTAL0		I	Crystal input
2	XTAL1		O	Crystal output
3	P1.1/RXD		I/O	Discrete programmable I/O or UART receive input
4	P1.2/TXD		I/O	Discrete programmable I/O or UART transmit output
5	P1.3/SYNC/ SCK		I/O	Discrete programmable I/O or SYNC output or SPI clock
6	P1.4/CAP		I/O	Discrete programmable I/O or Capture Timer input
7	VDD2		P	1.8V digital power
8	VSS		P	Digital common
9	VDD1		P	3.3V digital power
10	FGATEKILL		I	Fan PWM shutdown input, 2-µsec digital filter, configurable either high or low true.
11	FPWMWL	70 kΩ Pull up	O	Fan PWM gate drive for phase W low side, configurable either high or low true
12	FPWMWH	70 kΩ Pull up	O	Fan PWM gate drive for phase W high side, configurable either high or low true
13	FPWMVL	70 kΩ Pull up	O	Fan PWM gate drive for phase V low side, configurable either high or low true
14	FPWMVH	70 kΩ Pull up	O	Fan PWM gate drive for phase V high side, configurable either high or low true
15	FPWMUL	70 kΩ Pull up	O	Fan PWM gate drive for phase U low side, configurable either high or low true
16	FPWMUH	70 kΩ Pull up	O	Fan PWM gate drive for phase U high side, configurable either high or low true
17	P2.6/ AOPWM0		I/O	Discrete programmable I/O or analog output 0 (PWM)
18	P2.7/ AOPWM1			Discrete programmable I/O or analog output 1 (PWM)
19	VDD2		P	1.8V digital power
20	VSS		P	Digital common
21	IFBF-		I	Fan single shunt current sensing OP amp input (-)
22	IFBF+		I	Fan single shunt current sensing OP amp input (+)
23	IFBFO		O	Fan single shunt current sensing OP amp output
24	AIN0		I	Analog input channel 0, 0-1.2V range, needs to be pulled down to AVSS if unused
25	AVDD		P	1.8V analog power
26	AVSS		P	Analog common
27	AIN1		I	Analog input channel 1, 0-1.2V range, needs to be pulled down to AVSS if unused
28	AREF		O	Analog reference voltage output (0.6V)
29	CMEXT		O	Unbuffered analog reference voltage output (0.6V)

Pin Number	Pin Name	Internal IC Pull-up /Pull-down	Pin Type	Description
30	IFBC-		I	Compressor single shunt current sensing OP amp input (-)
31	IFBC+		I	Compressor single shunt current sensing OP amp input (+)
32	IFBCO		O	Compressor single shunt current sensing OP amp output
33	VAC-		I	AC input voltage sensing OP amp input (-)
34	VAC+		I	AC input voltage sensing OP amp input (+)
35	VACO		O	AC input voltage sensing OP amp output
36	IPFCO		O	PFC shunt current sensing OP amp output
37	IPFC+		I	PFC shunt current sensing OP amp input (+)
38	IPFC-		I	PFC shunt current sensing OP amp input (-)
39	VSS		P	Digital common
40	VDD1		P	3.3V digital power
41	CGATEKILL		I	Compressor PWM shutdown input, 2-µsec digital filter, configurable either high or low true.
42	CPWMWL	70 kΩ Pull up	O	Compressor PWM gate drive for phase W low side, configurable either high or low true
43	CPWMWH	70 kΩ Pull up	O	Compressor PWM gate drive for phase W high side, configurable either high or low true
44	CPWMVL	70 kΩ Pull up	O	Compressor PWM gate drive for phase V low side, configurable either high or low true
45	CPWMVH	70 kΩ Pull up	O	Compressor PWM gate drive for phase V high side, configurable either high or low true
46	CPWMUL	70 kΩ Pull up	O	Compressor PWM gate drive for phase U low side, configurable either high or low true
47	CPWMUH	70 kΩ Pull up	O	Compressor PWM gate drive for phase U high side, configurable either high or low true
48	P3.0/INT2		I/O	Discrete programmable I/O or INT2 digital input
49	P5.0/ PFCGKILL		I	Discrete programmable I/O or PFC PWM shutdown input, 2-µsec digital filter, configurable either high or low true.
50	PFCPWM	70 kΩ Pull up	O	PFC PWM gate drive, configurable either high or low true
51	P3.2/INT0		I/O	Discrete programmable I/O or INT0 input
52	P3.6/RXD1		I/O	Discrete programmable I/O or 2nd UART receive input
53	P3.7/TXD1		I/O	Discrete programmable I/O or 2nd UART transmit output
54	VSS		P	Digital common
55	SCL/SO-SI/VPP		I/O P	I²C clock output or SPI data or OTP programming voltage
56	SDA/CS0		I/O	I²C data or SPI chip select 0
57	P5.1/TMS		I/O	Discrete programmable I/O or JTAG test mode select

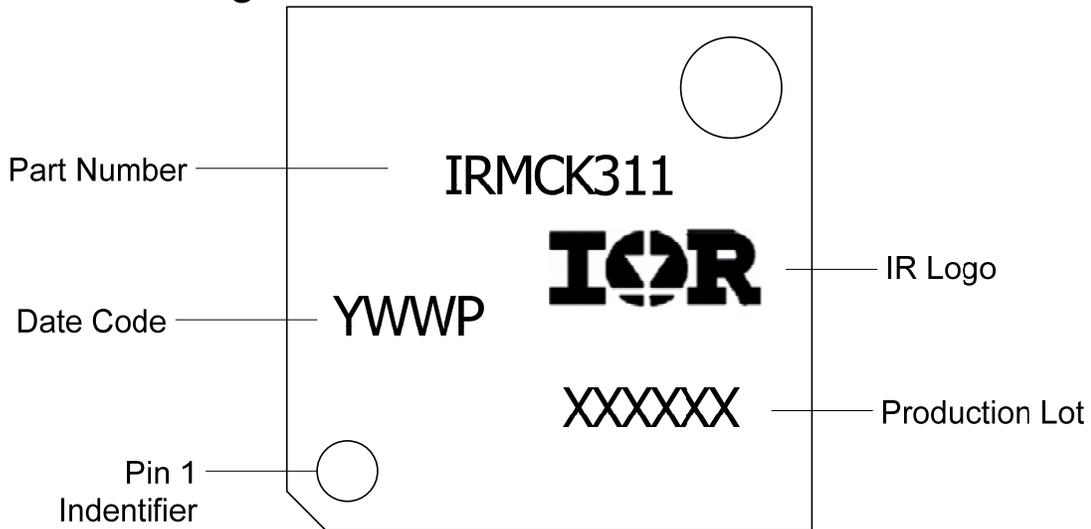| Pin Number	Pin Name	Internal IC Pull-up /Pull-down	Pin Type	Description
58	P5.2/TDO		I/O	Discrete programmable I/O or JTAG port test data output
59	P5.3/TDI		I/O	Discrete programmable I/O or JTAG test data input
60	TCK		I	JTAG test clock
61	N.C.		-	No connection
62	RESET		I/O	Reset , low true, Schmitt trigger input
63	PLLVDD		P	1.8 V PLL power
64	PLLVSS		P	PLL ground

Table 21.   Pin List

10 Package Dimensions
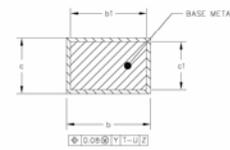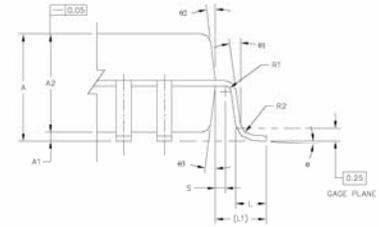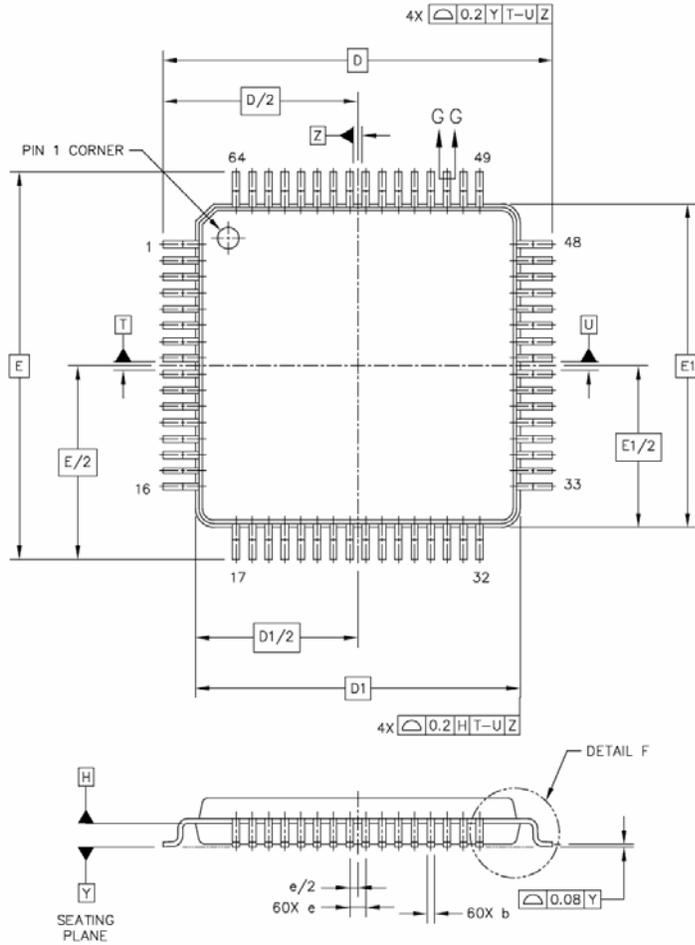
NOTES:

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D1 AND E1 ARE MAXIMUN PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm AND 0.5mm PITCH PACKAGES.

DIM	MIN	MAX	DIM	MIN	MAX	DIM	MIN	MAX
A	— — —	1.6	L1	1 REF				
A1	0.05	0.15	R1	0.1	0.2			
A2	1.35	1.45	R2	0.1	0.2			
b	0.17	0.27	S	0.2 REF				
b1	0.17	0.23	θ	0°	7°			
c	0.09	0.2	θ1	0°	— — —			
c1	0.09	0.16	θ2	12° REF				
D	12 BSC		θ3	12° REF				
D1	10 BSC							
e	0.5 BSC							
E	12 BSC							
E1	10 BSC							
L	0.45	0.75						

11 Part Marking Information

Part Number —————— IRMCK311

Date Code —————— YWWP

IR Logo

XXXXXX —— Production Lot

Pin 1
Indentifier

12 Ordering Information

Lead-Free Part in 64-lead QFP
Moisture sensitivity rating – MSL3

Part number	Order quantities
IRMCK311TY	1600 parts on trays (160 parts per tray) in dry pack

International **IQR** Rectifier