# **Errata Sheet**

# IC ID:

IRMCK312 IRMCK311 IRMCK343 IRMCK341 IRMCK371

## **Revision History:**

10/10/08 – Initial Release

### Case no. 1

## Symptom:

Analog Op Amp for current sensing has oscillatory behavior when configured with proper feedback resistors.

# Source of problem:

Impedance of internal layout for supplies.

#### Workaround:

Put a 47pF capacitor on between the op amp output and ground to eliminate the oscillation. A smaller value may work in some cases but the severity of the oscillation problem varies across production lots.

## Case no. 2

### Symptom:

The execution of the following particular consecutive 8051 instructions, which access the external RAM, does not perform correctly: the contents of RAM may be different than expected.

MOVX @DPTR,A MOVX A,@DPTR

The following is an example of application code written in C which can result in this problem:

```
Tx_data[0]=value
Tx_data[1]=Tx_data[0]
```

Where, TX\_data[] is a array variable to store UART transmit data. The uVision C compiler, with level 3 optimization, produces the following assembly code:

```
18:
            txd_data[0]=rxd_data[0]|0x80;
C:0x0660 90F945 MOV
                       DPTR,#rxd data(0xF945)
                      A,@DPTR
C:0x0663
        E0
              MOVX
C:0x0664 4480 ORL
                     A, #P0(0x80)
C:0x0666 90F94A MOV
                       DPTR,#txd_data(0xF94A)
C:0x0669 F0
              MOVX
                      @DPTR.A
  19:
            txd_data[1]=txd_data[0];
               MOVX A,@DPTR
C:0x066A E0
C:0x066B A3
               INC
                     DPTR
              MOVX
C:0x066C F0
                       @DPTR,A
```

Here we can see that the highlighted consecutive instructions match the problem definition.

# Source of problem:

When a RAM location (pointed to by DPTR above) is written (MOVX @DPTR,A), the data is not ready to be read back (MOVX A,@DPTR) in the next instruction cycle. This delay is due to the separate clock domains of the MCE and 8051 processors during memory access.

#### Workaround:

- 1) Insert a NOP instruction between the consecutive instructions, MOVX @DPTR,A and MOVX A,@DPTR to generate correct operation. Details on how to place assembly code in a C program can be found at: <a href="http://www.keil.com/support/man/docs/c51/c51\_asm.htm">http://www.keil.com/support/man/docs/c51/c51\_asm.htm</a>
  If the user wants that the C compiler to take care of this problem, then he/she may need to choose a different optimization level at a compilation.
- 2) Avoid C programming code which immediately accesses a data variable or array component right after it has been written.