Boost PFC and SMPS Control IC

Features

- Critical-conduction mode PFC control (CrCM)
- High PF and ultra-low THD
- Wide line and load range
- Regulated DC output voltage
- No secondary winding required
- Cycle-by-cycle over-current protection
- Output over-voltage protection
- Ultra-low start-up current
- 20.8V internal zener clamp on VCC
- Excellent ESD and latch immunity
- RoHS compliant
- 5-pin SOT-23 package

Applications

- Off-line power supply
- Electronic ballast
- LED power supply

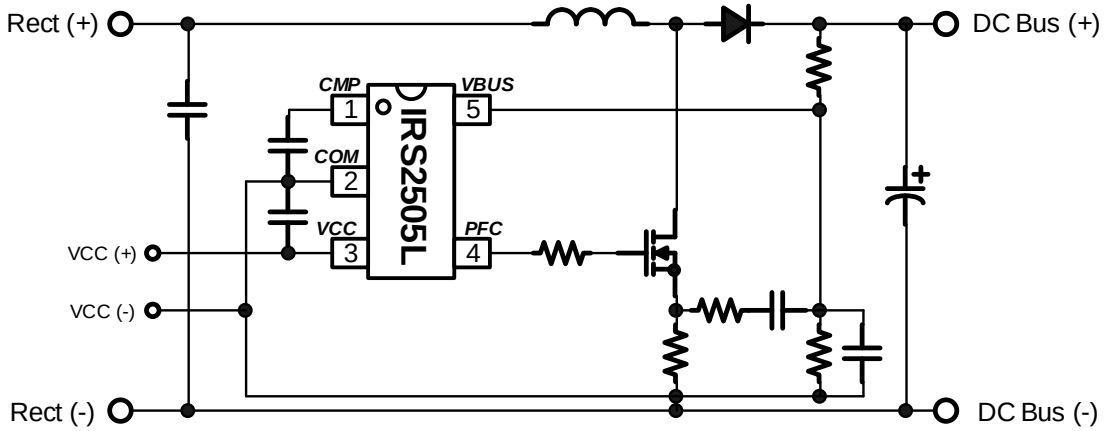
Description

The IRS2505L is a control IC for PFC boost converters operating in critical-conduction mode. The IC incorporates a voltage feedback loop for output voltage regulation combined with smart zero crossing detection to control the gate drive output without the need for a secondary inductor winding. DC output over-voltage protection and cycle-by-cycle over-current protection are also included. Multi-functional inputs enable the IRS2505L to perform all functions with only 5 pins.

Package Options

5 Lead SOT23

Application Diagram



Ordering Information

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRS2505LPBF	5L-SOT-23	Tape and Reel	3000	IRS2505LTRPBF

Qualification Information†

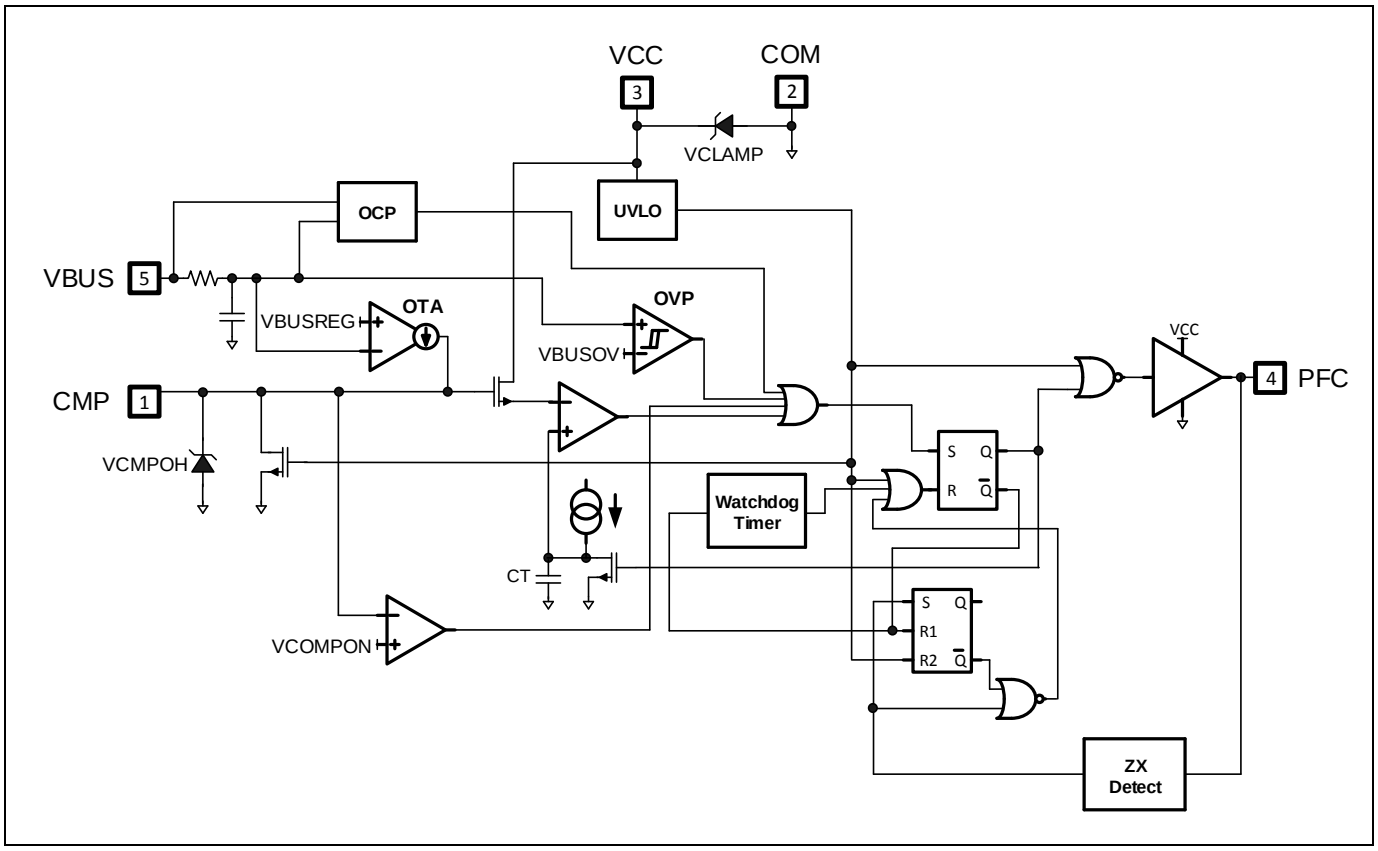
Qualification Level		Industrial†† (per JEDEC JESD 47E)	
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture Sensitivity Level		SOT-23	MSL1††† (per IPC/JEDEC J-STD-020C)
ESD	Machine Model	Class B (per JEDEC standard EIA/JESD22-A115-A)	
	Human Body Model	Class 2 (per EIA/JEDEC standard JESD22-A114-B)	
IC Latch-Up Test		Class I, Level A (per JESD78A)	
RoHS Compliant		Yes	

† Qualification standards can be found at the Infineon web site http://www.infineon.com

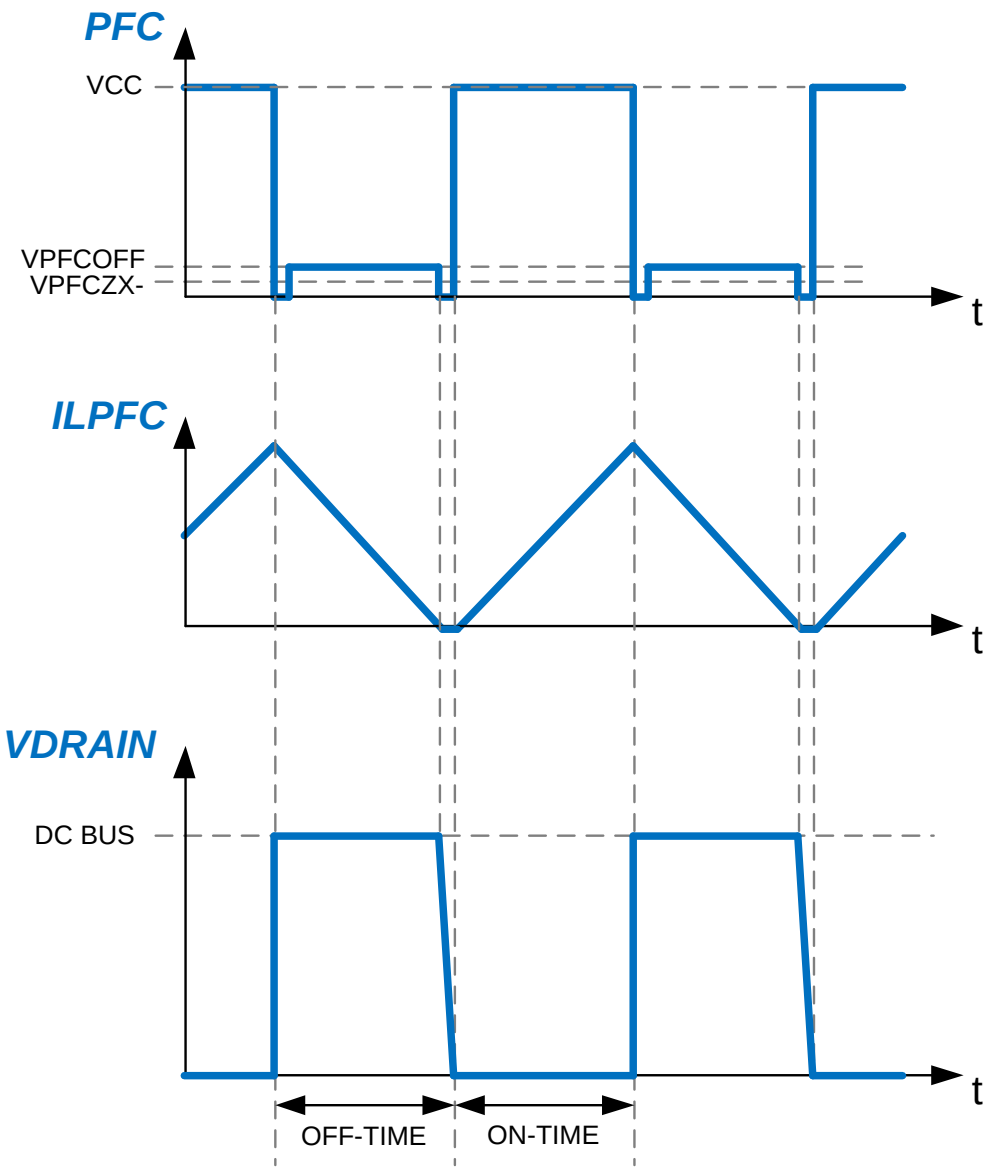
†† Higher qualification ratings may be available should the user have such requirements. Please contact your Infineon sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your Infineon sales representative for further information.

Functional Block Diagram



Timing Diagram



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any pin. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
VPFC	PFC pin voltage		-0.3	VCC + 0.3	V
VBUS	VBUS pin voltage		-0.3	VCC + 0.3	
ICC	VCC pin supply current†		---	25	mA
ICMP	CMP pin current††		---	1	
PD	Package power dissipation @ Ta ≤ +25 ºC	SOT-23 5L	---	0.5	W
Rθja	Thermal resistance, junction to ambient	SOT-23 5L	---	191	ºC/W
Tj	Junction temperature		-55	150	ºC
Ts	Storage temperature		-55	150	
TL	Lead temperature (soldering, 10 seconds)		---	300	

† This IC contains a voltage clamp structure between the chip VCC and COM which has a nominal breakdown voltage of 20.8V. This supply pin should not be driven by a DC, low impedance power source greater than the VCLAMP specified in the Electrical Characteristics section.

†† This IC contains a voltage clamp structure between the CMP and COM which has a nominal breakdown voltage of 10.2V. This pin should not be driven by a DC, low impedance power source greater than the VZCMP specified in the Electrical Characteristics section.

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.

Symbol	Definition	Min.	Max.	Units
VCC	Supply voltage	VCCUV+ + 0.5V	VCLAMP	V
ICC	Supply current	0	10	mA
VCMP	CMP pin voltage	0	VZCMP	V
Tj	Junction temperature	-40	125	ºC

Recommended Component Values

Symbol	Component	Value	Units
CCMP	Compensation capacitor value	0.68	µF
CVCC	VCC filter capacitor	0.1	µF
CVBUS	VBUS pin filter capacitor	1.0	nF

Electrical Characteristics

VCC=14V, CVCC=0.1uF, CCMP=0.68uF, CPFC=1nF, CVBUS=10nF, and Ta=25°C unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Supply Characteristics						
VCLAMP	VCC clamp voltage	19.8	20.8	21.8	V	ICC = 19 mA
VCCUV+	Rising VCC under-voltage threshold	10.0	11.1	12.0		
VCCUV-	Falling VCC under-voltage threshold	7.0	7.9	9.0		
VCCUVHYS	VCC UVLO hysteresis	2.9	3.2	3.5		
IQCCUV	Micro-power start-up VCC supply current	---	46.0	60.0	µA	VCC = VCCUV+ - 500mV rising
IQCC	No switching	---	1.2	1.6	mA	VCOMP=0V,GBD
ICC50kHz	VCC current @ 50kHz	---	1.6	2.1	mA	
PFC Characteristics						
tONMIN	Minimum PFC On-time	---	0.9	---	µs	
tONMAX	Maximum PFC On-time	51	68	86		
VBUSREG	VBUS Pin Regulation Voltage	4.02	4.1	4.18	V	
VBUSOV+	VBUS Pin OVP Threshold	4.30	4.50	4.70		
VBUSOV-	VBUS Pin OVP Fault Reset Threshold	4.13	4.26	4.48		
VBUSOC+	VBUS Pin Over-Current Threshold	0.45	0.53	0.62		VBUS = 3V
tOC	Over-Current Blanking Time	---	300	---	ns	
VPFCZX+	PFC Pin Zero-Crossing Arming Threshold	0.39	0.40	0.51	V	VPFC Rising, GBD
VPFCZX-	PFC Pin Zero-Crossing Detection Threshold	0.39	0.40	0.51		VPFC Falling, GBD
tOFFDLY	PFC Pin Off-Time Delay	---	0.5	---	µs	
tZXBLNK	PFC Pin Zero-Crossing Blank Time	---	0.5	---		
tWD	Watch Dog Timer Pulse Interval	100	140	180		
ICMP+	CMP Pin OTA IO+	25	33	40	µA	VBUS=3.5V,VCMP=0V
ICMP-	CMP Pin OTA IO-	-40	-33	-25		VBUS=4.5V,VCMP=5V
VCMPOH	OTA Output Voltage Swing (high state)	9.9	10.2	11.5	V	VBUS=3.5V
VCMPOL	OTA Output Voltage Swing (low state)	---	0	---		VBUS=4.5V
VCMPON	Minimum COMP Voltage for Switching	1.21	1.50	1.83		
VCMPFLT	OTA Output Voltage in Fault Mode	---	0	---		
VZCMP	CMP Pin Clamp Voltage	9.9	10.2	11.5		VBUS=3.5V

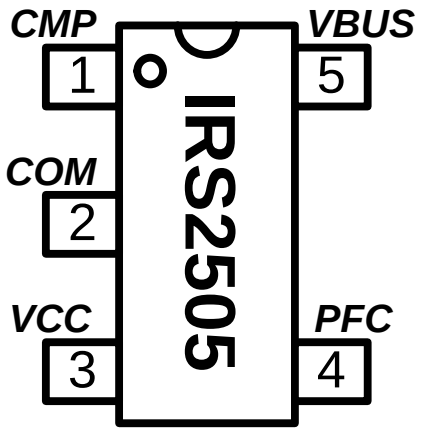
GBD : Guaranteed by design

Electrical Characteristics

VCC=14V, CVCC=0.1uF, CCMP=0.68uF, CPFC=1nF, CVBUS=10nF, and Ta=25°C unless otherwise specified.

Gate Driver Output Characteristics (PFC)						
VPFCON	Gate High Voltage	---	13.0	---	V	
VPFCOFFI	Gate Low Voltage during initial switch off period	---	---	0.1		
VPFCOFF	Gate Low Voltage (after initial switch off)	0.50	0.59	0.63		
tPD	Gate initial switch off pull down time	---	500	---	ns	
tr	Output rise time	---	135	220		Rising, 10% to 70%
tf	Output fall time	---	20	35		Falling, 80% to 20%
IO+	Output source current	---	50	---	mA	
IO-	Output sink current	---	450	---		

Pin Assignments and Definitions



Pin	Name	Description
1	***CMP***	PFC error amplifier compensation
2	***COM***	IC power and signal ground
3	***VCC***	Logic and gate drive supply voltage
4	***PFC***	PFC gate driver output and zero-crossing detection
5	***VBUS***	DC bus sensing input, OVP and OCP

Functional Description

The following topics are described in more detail below:

1) PFC Control Circuit
2) Multi-Function PFC Pin
3) On-Time Modulation
4) Over-Voltage Protection (OVP)
5) Over-Current Protection (OCP)

The IRS2505L is primarily intended for *but not limited to* pre-regulator PFC Boost converter front end stages in general power supplies and lighting applications such as LED power supplies, fluorescent and HID ballasts. The IRS2505L may also be used in other converter topologies such as Buck, Buck-Boost and Flyback, where its small size and functionality can offer simplicity and cost advantage. It can also be used in converters where PFC is not required.

1. PFC Control Circuit

The IRS2505 is a high frequency SMPS PWM controller designed for Boost PFC pre-regulators operating in critical-conduction mode (CrCM), also known as transition (TM) or boundary mode (BM). The PFC Boost converter provides a regulated high voltage DC output over a range of AC line input voltage and load, while at the same time shaping the input current so that it follows the sinusoidal profile of the voltage resulting in high power factor and low total harmonic distortion (THD).

Figure 1 shows the main elements of the PFC Boost converter; the input capacitor (CIN) is for high frequency bypass and does not provide smoothing at low frequency under steady state operation. When a load is connected at the output the rectified input voltage across CIN is full wave rectified. During the on-time of the PFC MOSFET (MPFC), the IRS2505 gate drive output (PFC) is high so the inductor (LPFC) current ramps up linearly to a peak current value. During the off-time the gate drive output is low and the inductor current linearly discharges back down to zero at which point MPFC is turned on again. The control loop response has to be slow compared to the line frequency so that the on time remains effectively constant over a single line half cycle; except for some gradual increase as the voltage approaches the zero crossings, which improves THD. The off time varies during the AC line half cycle being longest at the peak.

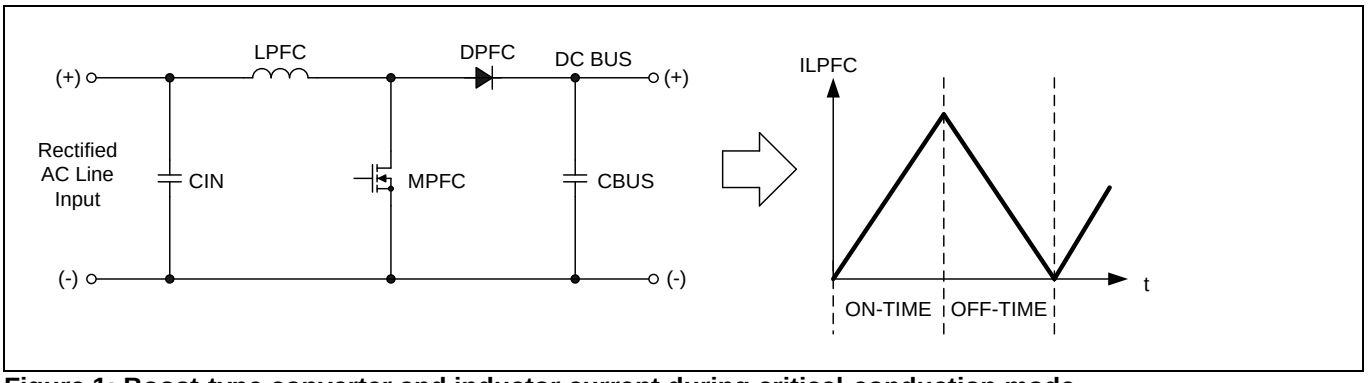


Figure 1: Boost-type converter and inductor current during critical-conduction mode.

The result is a triangular shaped inductor current that varies in frequency depending on the level of the instantaneous rectified AC line voltage shown in figure 2. The maximum switching frequency occurs at the zero-crossings of the rectified AC line voltage and the minimum at the peak of the rectified AC line voltage. The average inductor current is equal to half of the peak, which is equal to the instantaneous line input current after the high frequency elements have been filtered out.

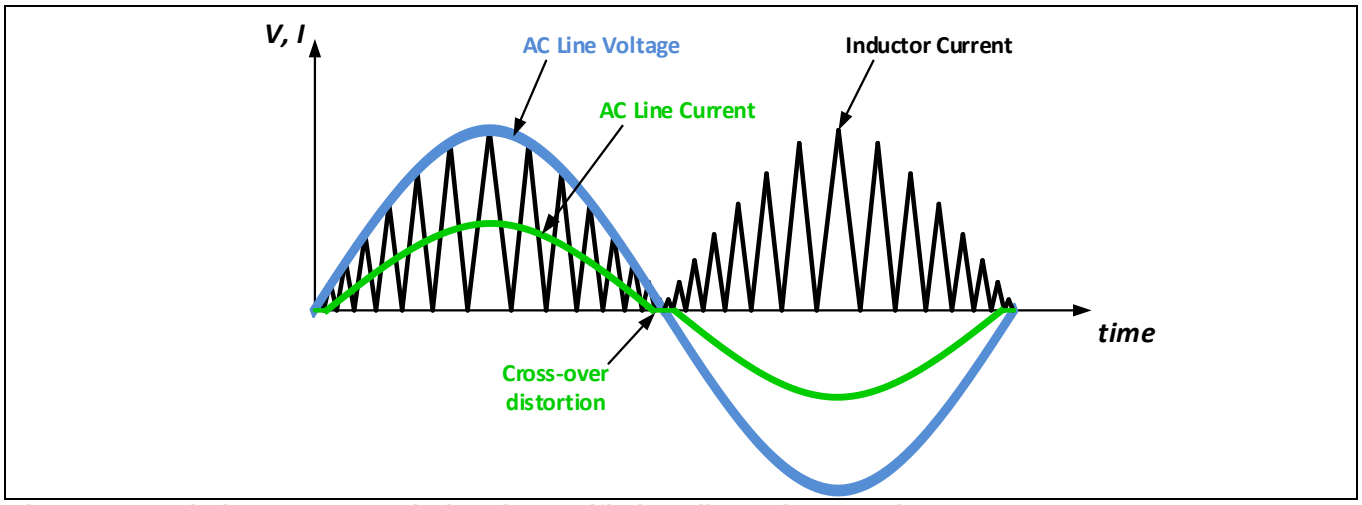


Figure 2: PFC inductor current during the rectified AC line voltage cycle.

The IRS2505 internal control circuit blocks shown in figure 3 include; the feedback error amplifier controlling on-time via timing capacitor (CT), zero-crossing (ZX) detection and off-time control, gate drive output, over-voltage protection (OVP) and over-current protection (OCP). The PFC pin is a multi-function input/output pin used for driving the external PFC MOSFET gate and also for sensing the PFC inductor current zero-crossing during the off-time. The VBUS pin is also a multi-function pin used for monitoring the DC bus voltage through an external divider network and also measuring the MOSFET (MPFC) source current. An internal OTA compares the voltage feedback with an accurate internal voltage reference (VBUSREG) to control the CMP pin voltage by charging and discharging the external compensation capacitor (CCMP). The voltage level at the CMP pin determines the on-time to control power transfer to the output. The MOSFET current is measured with a current-sensing resistor and then AC-coupled onto the VBUS pin through an external series resistor and capacitor.

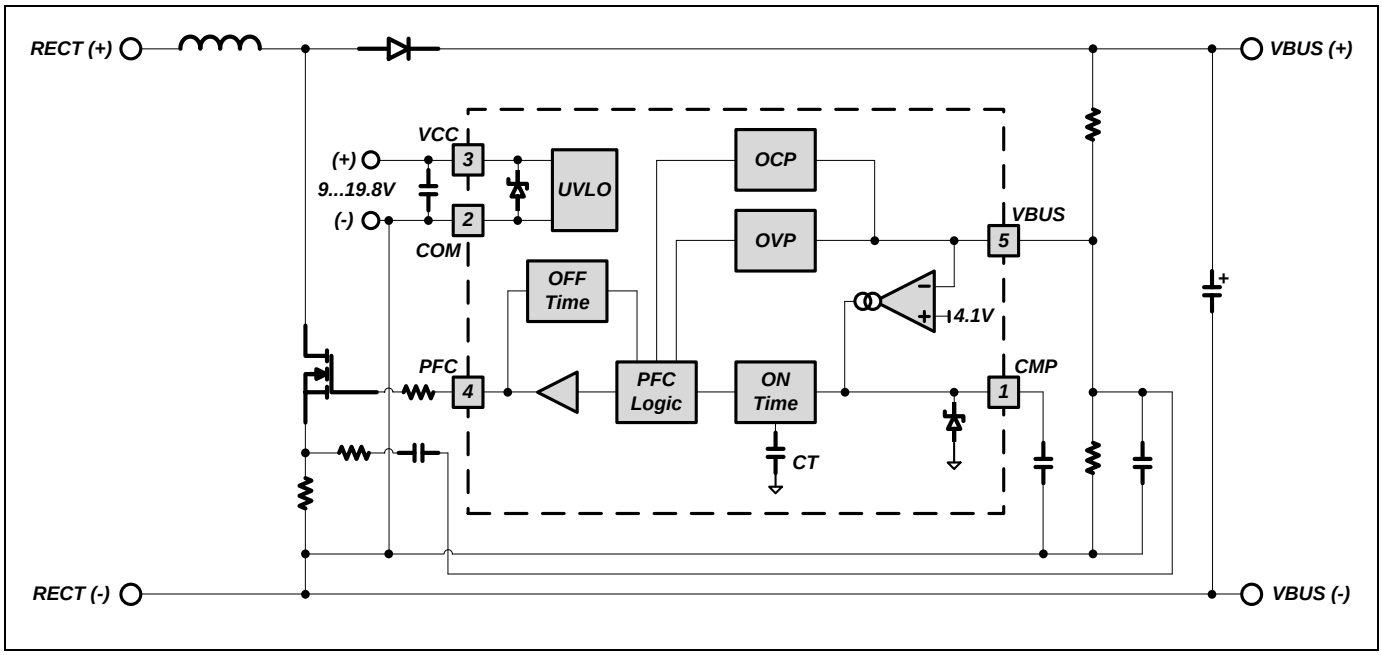


Figure 3: PFC control circuitry

2. PFC Multi-Function Pin

The multi-function PFC pin performs the following two functions:

1) PFC gate drive output.
2) PFC inductor current zero-crossing detection.

During each switching cycle illustrated in figure 4, at the beginning of each cycle the PFC pin gate drive output pulls the PFC pin voltage high to approximately VCC-1V and the external PFC MOSFET turns on; the on-time duration is set by the CMP pin voltage. The internal PFC control loop steers the CMP pin voltage to control the on-time such that if the DC bus voltage increases then the CMP pin voltage and on-time will decrease. This will decrease the peak inductor current each switching cycle transferring less energy and causing the DC bus voltage to decrease. If the DC bus voltage decreases, then the CMP pin voltage and on-time will increase having the opposite effect. This negative feedback control regulates the DC bus to a constant voltage over AC line voltage or output load variations. The speed of the control loop is determined by the internal OTA trans-conductance and compensation capacitor CCMP.

At the end of each on time period, the PFC pin gate drive circuit pulls the PFC pin to COM and the external PFC MOSFET turns off. After a short initial switch off delay (t_{PD}), the internal gate drive pull-down turns off and the PFC pin is then weakly pulled up and clamped at approximately one diode forward voltage drop (V_{PFCOFF}), which is well below the gate threshold of the MOSFET (MPFC) ensuring that it will not begin to switch on. During the off-time the PFC inductor current discharges through the boost diode into the DC output capacitor and load. When the inductor current falls to zero, the drain voltage falls from the level of the output voltage plus the output diode forward voltage and transitions negatively. During this transition current flows through the MOSFET parasitic gate to drain capacitance C_{GD} overcoming the internal weak pull up and causing the gate voltage to drop below the threshold V_{PFCZX-}. After remaining below this threshold for a period of $t_{ZXBLANK}$, the PFC gate drive will be turned on again to start the next switching cycle and so the sequence repeats. To ensure ZX detection, a minimum voltage headroom is needed between the peak line voltage at high line and the output voltage. This value depends on the MOSFET C_{GD}, a value of 60-70V is typical. To operate with a smaller headroom 500V minimum rated capacitor around 100pF may be added between drain and source.

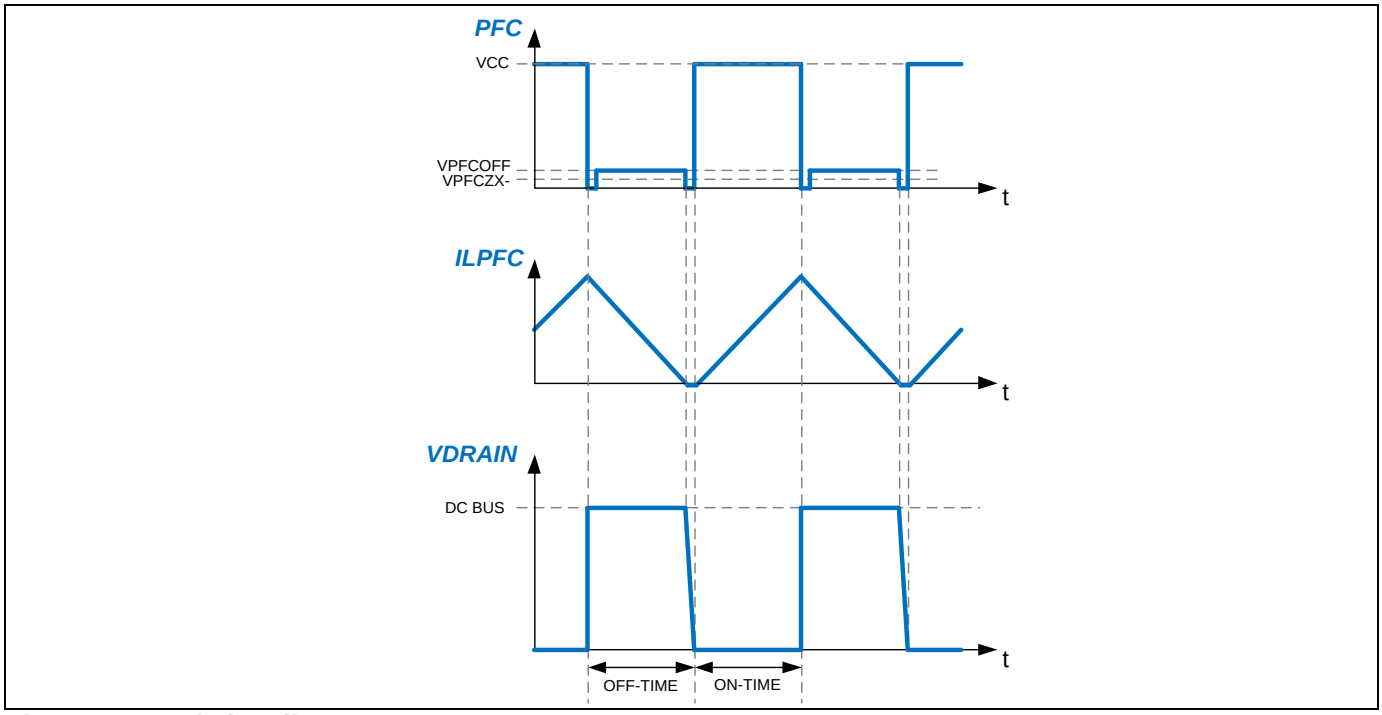


Figure 4: PFC timing diagram.

3. PFC On-Time Modulation

Fixed on-time over the entire half cycle of the line input voltage produces a peak inductor current that naturally follows the sinusoidal shape of the line input voltage. The filtered, averaged line input current is in phase with the line input voltage to provide high power factor. However some harmonic distortion of the current is still present mostly due to cross-over distortion occurring near the zero-crossings of the line input voltage as shown in figure 2. To achieve very low harmonics within the limits of international standards and to meet general market requirements, an additional on-time modulation function is included in the IRS2505L, which dynamically increases the on-time as the line input voltage nears the zero-crossings. As illustrated in figure 5, the peak LPFC current and therefore the smoothed line input current increase slightly higher near the zero-crossings of the line input voltage. This reduces the amount of cross-over distortion in the line input current and improves the shape of the current reducing the THD and harmonics to low levels.

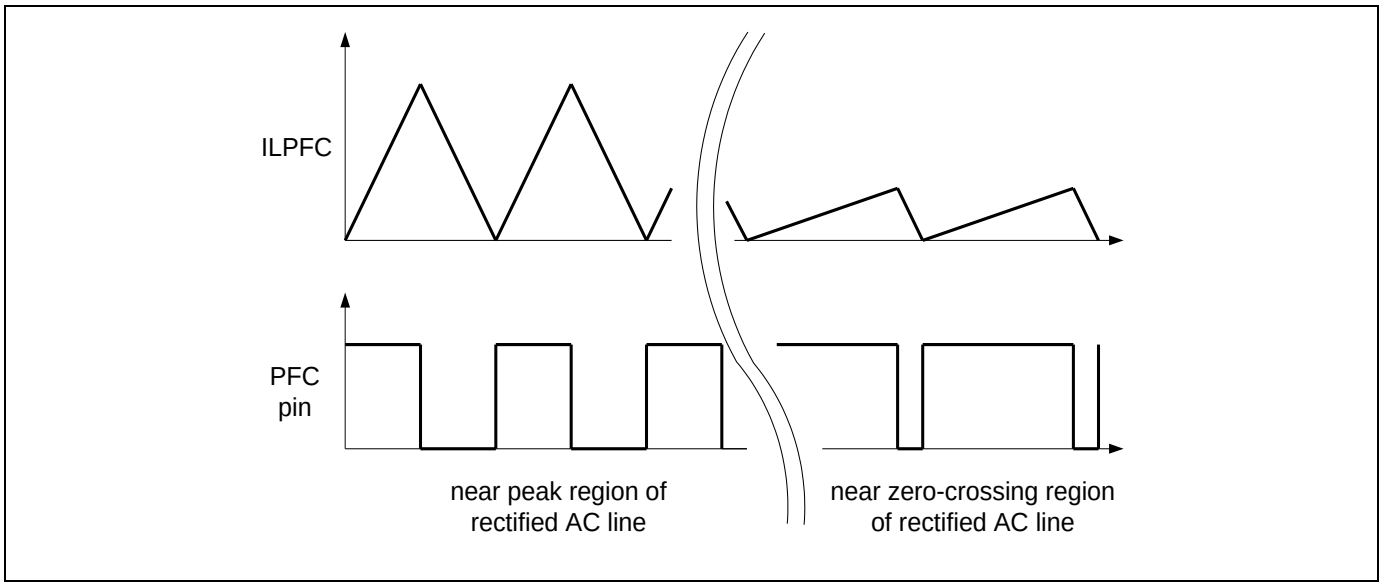


Figure 5: PFC on-time modulation.

4. DC Bus Over-Voltage Protection (OVP)

The VBUS pin includes output over-voltage protection (OVP). Should the VBUS pin feedback voltage exceed the internal over-voltage protection threshold (VBUSOV+) then the PFC gate drive will turn off until the VBUS pin voltage again falls below the over-voltage restart threshold (VBUSOV-) to resume normal operation.

5. Over-Current Protection (OCP)

As well as sensing the output voltage feedback, the VBUS input also includes a cycle-by-cycle, AC-coupled, over-current protection (OCP) function. The external network required to combine these two inputs is shown in figure 6. The high-frequency ramp shaped voltage produced across the current-sensing resistor (RCS) is coupled onto the VBUS feedback with an external series resistor (R1) and capacitor (C1) as shown in figure 7. An internal over-current protection circuit detects the difference between the peak and average of the combined signal so that if the triangular-shaped voltage peak at the VBUS input exceeds VBUSREG by VBUSOC+ the gate drive is immediately driven low. The capacitor CVBUS is added to make the current sense signal more triangular so that its peak value will be close to half its average.

The OCP function will safely limit the peak current in each switching cycle to prevent MOSFET damage during low AC line conditions, overload or during fast mains voltage interrupts. It should be remembered that in any Boost converter it is not possible to incorporate full output current control or short circuit protection by controlling the switching of MPFC. Shorting the output should be avoided as it will short the input and blow a fuse!

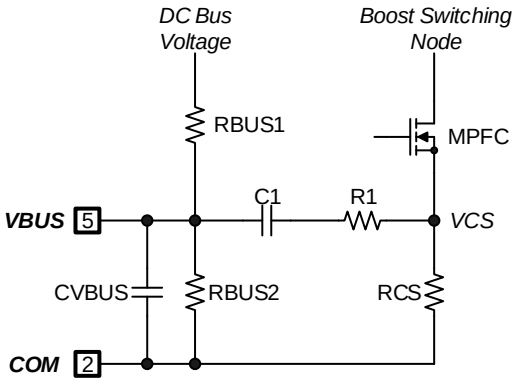


Figure 6: AC-coupled over-current protection circuit.

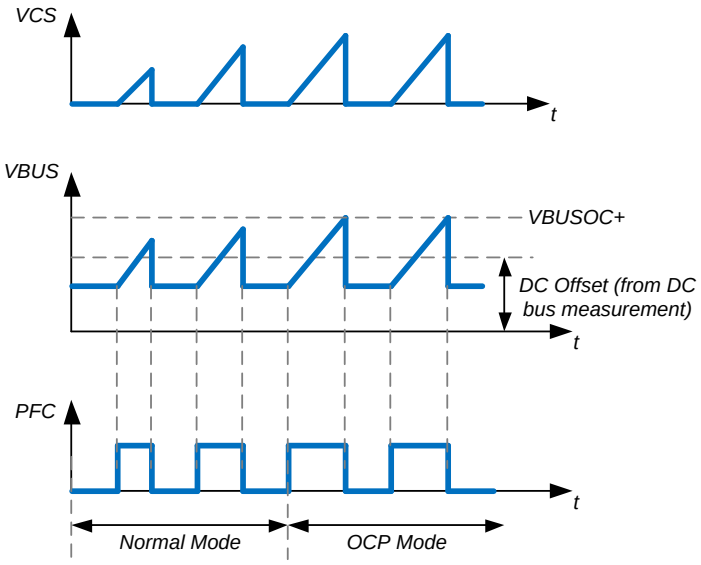
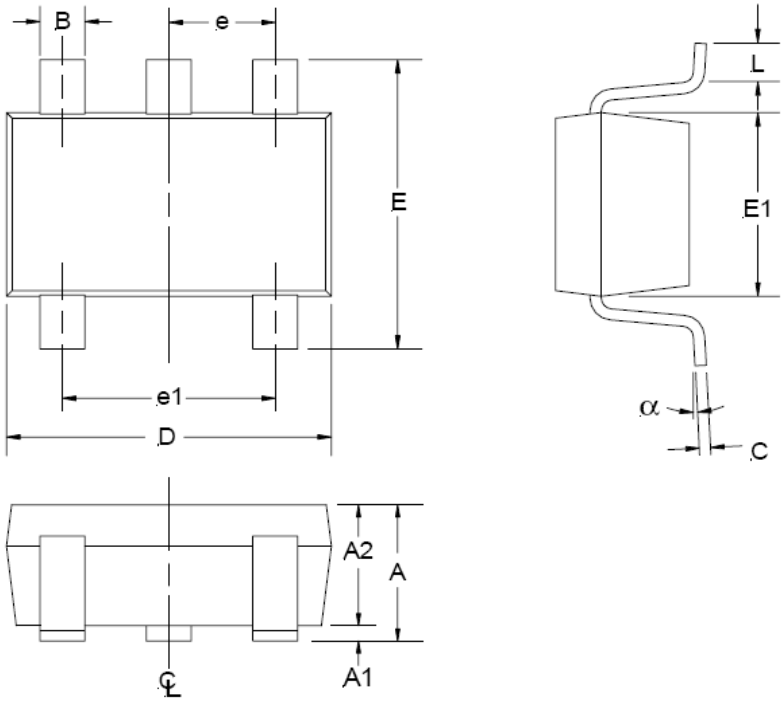


Figure 7: OCP circuit timing diagram.

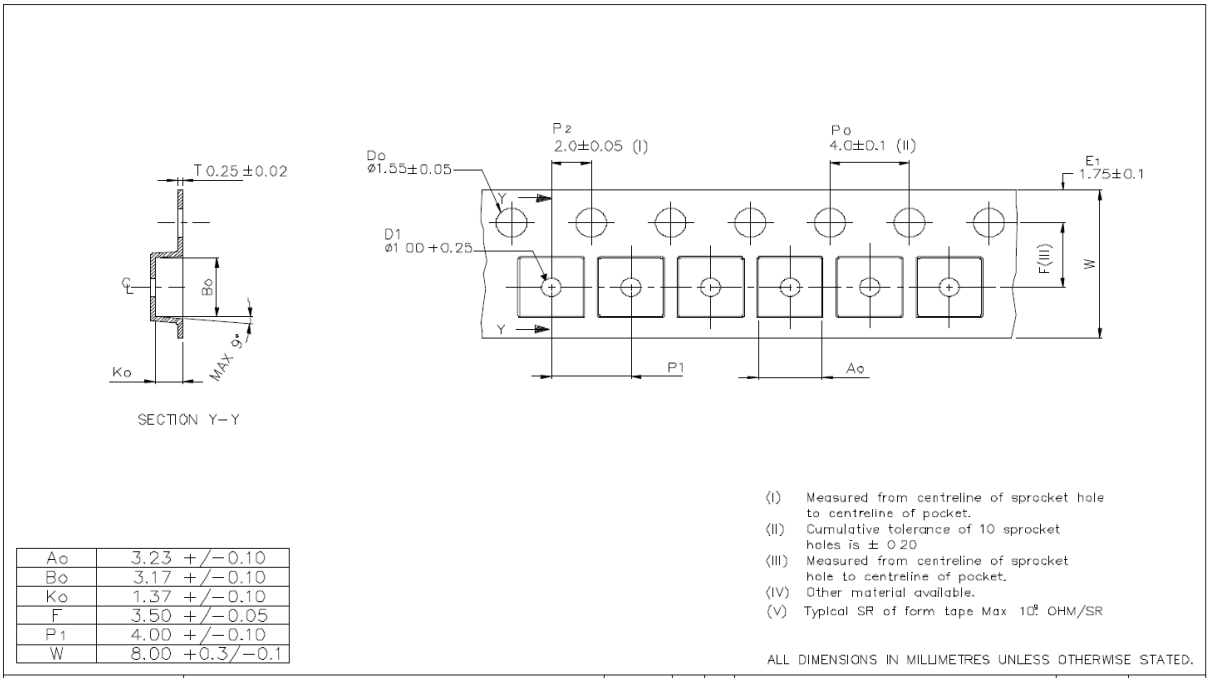
Package Details: 5 Lead SOT23



SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
B	0.25	0.50
C	0.09	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
e	0.95 REF	
e1	1.90 REF	
L	0.35	0.55
α	08	108

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

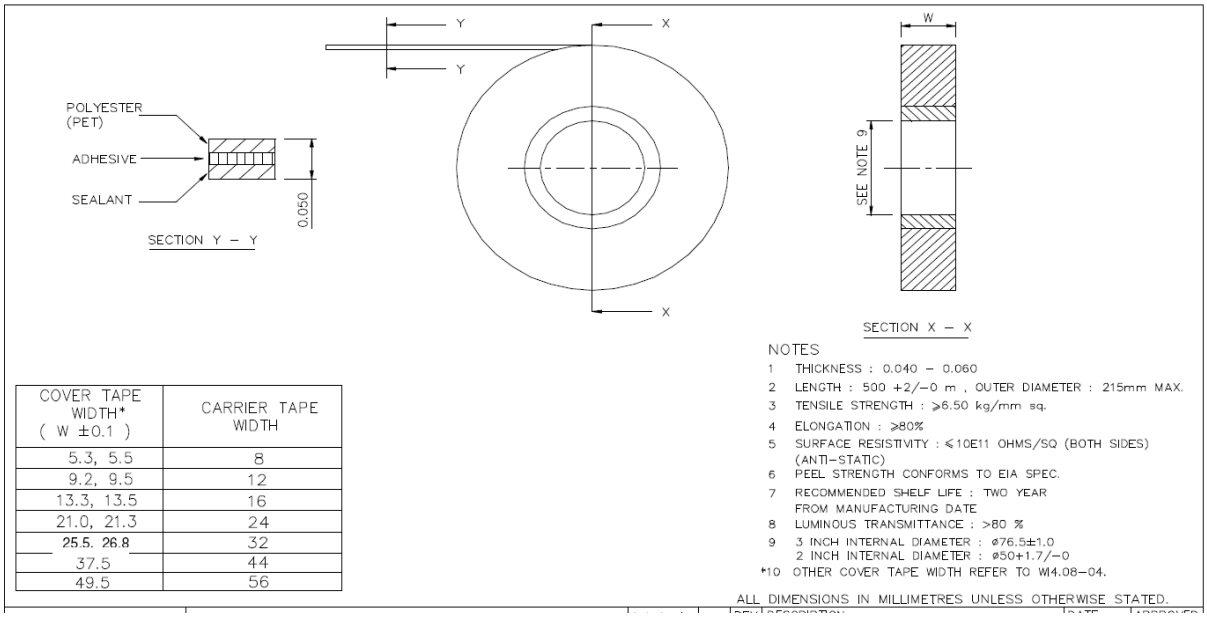
Tape and Reel Details: 5 Lead SOT23



Ao	3.23 +/−0.10
Bo	3.17 +/−0.10
Ko	1.37 +/−0.10
F	3.50 +/−0.05
P1	4.00 +/−0.10
W	8.00 +0.3/−0.1

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.
(V) Typical SR of form tape Max 10^9 OHM/SR

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

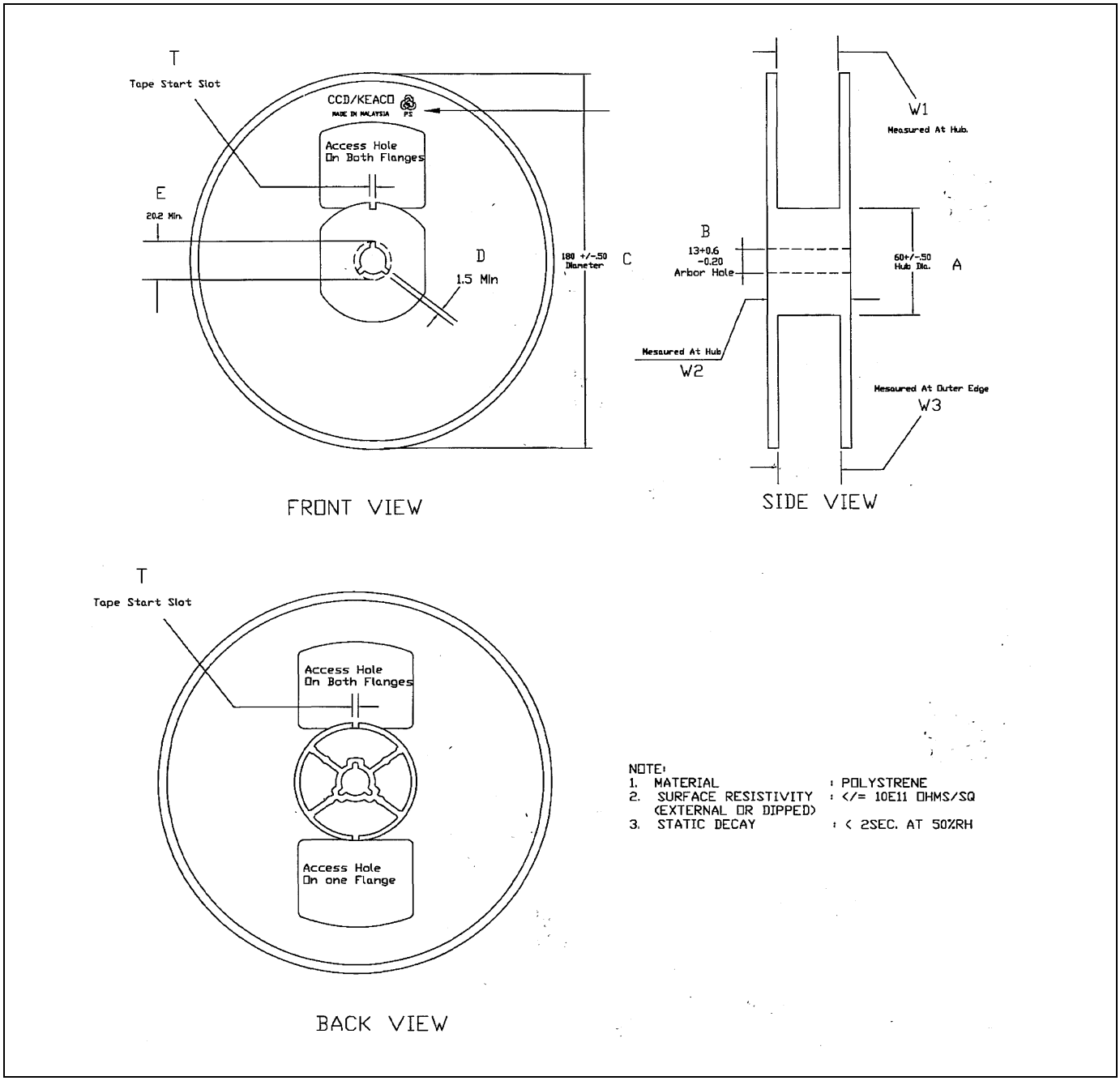


COVER TAPE WIDTH* (W ±0.1)	CARRIER TAPE WIDTH
5.3, 5.5	8
9.2, 9.5	12
13.3, 13.5	16
21.0, 21.3	24
25.5, 26.8	32
37.5	44
49.5	56

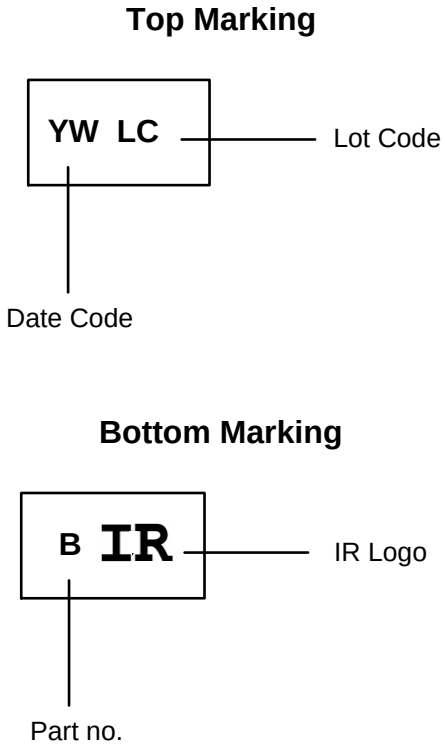
NOTES
1 THICKNESS : 0.040 – 0.060
2 LENGTH : 500 +2/−0 m , OUTER DIAMETER : 215mm MAX.
3 TENSILE STRENGTH : ≥6.50 kg/mm sq.
4 ELONGATION : ≥80%
5 SURFACE RESISTIVITY : ≤10E11 OHMS/SQ (BOTH SIDES) (ANTI–STATIC)
6 PEEL STRENGTH CONFORMS TO EIA SPEC.
7 RECOMMENDED SHELF LIFE : TWO YEAR FROM MANUFACTURING DATE
8 LUMINOUS TRANSMITTANCE : >80 %
9 3 INCH INTERNAL DIAMETER : ø76.5±1.0
2 INCH INTERNAL DIAMETER : ø50+1.7/−0
*10 OTHER COVER TAPE WIDTH REFER TO W4.08–04.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

Tape and Reel Details: 5 Lead SOT23



Part Marking Information: 5 Lead SOT23



Revision History

Major changes since the last revision

Date	Description of change
June 20, 2013	First Release
September 2, 2015	Updated block diagram and functional description. Added test limits for multiple parameters.
February 17, 2016	Added blanking time for cycle by cycle over-current protection

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